OPAx596 High-Voltage (85V), Low-Power (420µA), High-Slew Rate (100V/µs) Power Amplifier With MUX-Friendly Inputs

1 Features

- High slew rate: 100V/µs
- Low power consumption: 420µA
- Wide power-supply range:
  - ±4V to ±42.5V
  - 8V to 85V
- MUX-friendly inputs
- Input below the negative rail
- Rail-to-rail output
- Gain bandwidth: 3.75MHz
- Low noise: 12.8nV/√Hz
- Low input bias current: 5pA
- Low input offset voltage: ±1mV
- Output current drive: ±30mA
- Wide temperature range: –40°C to +125°C
- Industry-standard small packages:
  - D (8-pin SOIC)
  - DBV (5-pin SOT-23)
  - DGK (8-pin VSSOP)

2 Applications

- Semiconductor test
- LCD test
- Programmable dc power supply
- CT and PET scanner
- Source measurement unit (SMU)
- Optical module
- Lab and field Instrumentation

3 Description

The OPA596 and OPA2596 (OPAx596) are high-voltage (85V), high slew rate (100V/µs), micro-power (420µA), unity-gain stable operational amplifiers.

The OPAx596 enable the next generation of high-voltage systems, such as output load drivers in semiconductor test and digital power supplies by increasing the output voltage of the system though high-gain configurations. Low power consumption and industry-standard small packages allow the device to be used in high-density systems that are size constrained, while reducing the thermal management requirements for the system.

Through proprietary design techniques, the OPAx596 are capable of a very high slew rate with minimal power consumption to improve large-signal settling time and maximize the effective large-signal bandwidth. These devices also offers MUX-friendly inputs that enable large differential voltage (up to 85V) and help improve settling behavior when compared to traditional inputs in multiplexed applications.

The OPAx596 are available in industry-standard packages and operates across the temperature range of –40°C to +125°C.

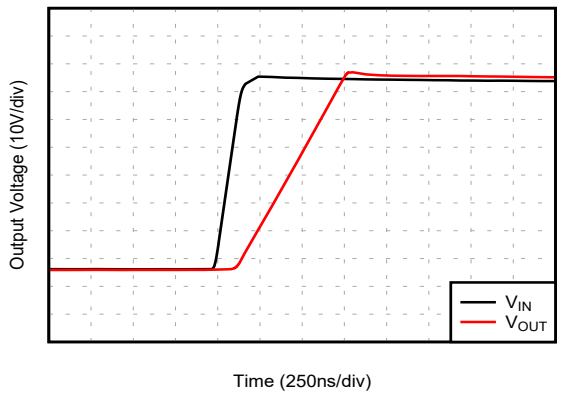
Device Information

PART NUMBER	CHANNELS	PACKAGE(1)
OPA596	Single	DBV (SOT-23, 5)
OPA2596	Dual	D (SOIC, 8)
		DGK (VSSOP, 8)

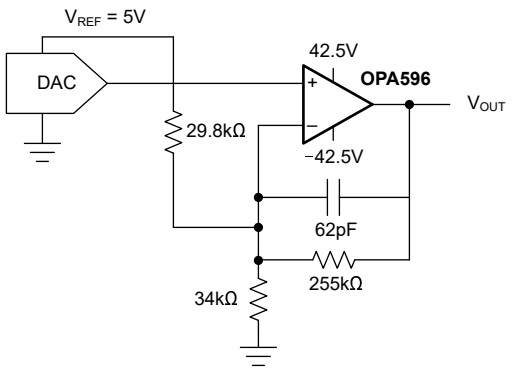
(1) For more information, see Section 10.

Related 85V Products

PART NUMBER	OUTPUT CURRENT	INPUT OFFSET
OPAx596	±30mA	1mV
OPAx593	±250mA	100µV



Large-Signal Step Response



DAC Output Buffer With Gain

Table of Contents

4 Pin Configuration and Functions

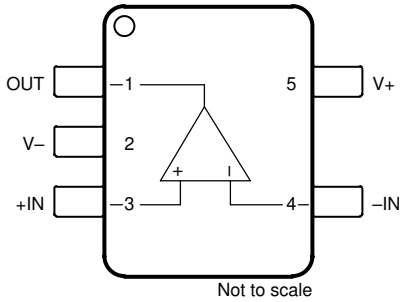


Figure 4-1. OPA596 DBV Package, 5-Pin SOT-23 (Top View)

Table 4-1. Pin Functions: OPA596

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN	3	Input	Noninverting input
–IN	4	Input	Inverting input
OUT	1	Output	Output
V+	5	Power	Positive (highest) power supply
V–	2	Power	Negative (lowest) power supply

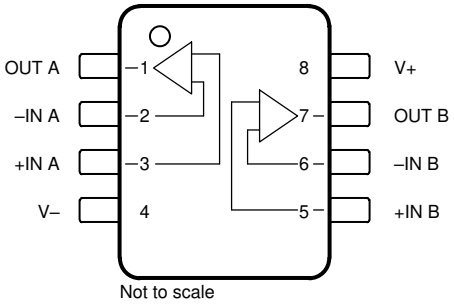


Figure 4-2. OPA2596 D Package, 8-Pin SOIC and DGK Package, 8-Pin VSSOP (Top View)

Table 4-2. Pin Functions: OPA2596

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
–IN A	2	Input	Inverting input, channel A
–IN B	6	Input	Inverting input, channel B
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
V+	8	Power	Positive (highest) power supply
V–	4	Power	Negative (lowest) power supply

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)			93	V
	Signal input pin voltage(2)	Common-mode	(V–) – 0.3	(V+) + 0.3	V
		Differential		(V+) – (V–)	
	Input current, all input pins(2)			±10	mA
I_{SC}	Output short circuit(3)			Continuous	
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails must be current-limited to 10mA or less.
(3) Short-circuit to ground.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage	Dual supply	±4		±42.5	V
		Single supply	8		85	
T_A	Ambient temperature		–40		125	°C

5.4 Thermal Information OPA596

THERMAL METRIC[1]		OPA596 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	99.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	42.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	64.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Thermal Information OPA2596

THERMAL METRIC[1]		OPA2596 D (SOIC) 8 PINS	OPA2596 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.3	143.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.2	50.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.0	78.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.8	3.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	58.1	77.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Electrical Characteristics

at V_S = 85V (±42.5V), T_A = 25°C, R_L = 10kΩ to mid-supply, and V_{CM} = V_{OUT} = mid-supply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±0.2	±1	mV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C(1)			±1	±6	µV/°C
PSRR	Power supply rejection ratio	8V ≤ V_S ≤ 85V			±1	±5	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current(1)				±5	±15	pA
		T_A = –40°C to +85°C				±50	
		T_A = –40°C to +125°C				±1	nA
I_{OS}	Input offset current(1)				±5	±15	pA
		T_A = –40°C to +85°C				±50	
		T_A = –40°C to +125°C				±1	nA
NOISE							
	Input voltage noise	f = 0.1Hz to 10Hz			1.4		μV_{PP}
e_n	Input voltage noise density	f = 100Hz			17.8		nV/√Hz
		f = 1kHz			12.9		
		f = 10kHz			12.8		
i_n	Current noise density	f = 1kHz			7		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage	Linear operation		(V–) – 0.1		(V+) – 3.5	V
CMRR	Common-mode rejection	(V–) ≤ V_{CM} ≤ (V+) – 3.5V		120	140		dB
			T_A = –40°C to +125°C(1)	120	140		
INPUT IMPEDANCE							
	Differential				100 || 2.5		MΩ || pF
	Common-mode				10 || 5.5		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 1V < V_O < (V+) – 1.5V, R_L = 10kΩ to mid-supply(1)		134	140		dB
			T_A = –40°C to +125°C	120	140		
		(V–) + 3V < V_O < (V+) – 3.5V, R_L = 2kΩ to mid-supply		116	126		
			OPA596 T_A = –40°C to +125°C(1)	116	126		
			OPA2596 T_A = –40°C to +125°C(1)	97	110		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	G = 1			2.25		MHz
		G = 10			3		
		G = 100			3.75		
SR	Slew rate	G = ±1, V_O = 70V step			100		V/µs
t_S	Settling time	To ±0.01%, G = 1, V_O = 70V step, C_L = 20pF			3		µs
	Overload recovery	G = –10			115		ns
THD+N	Total harmonic distortion + noise	G = +1, V_O = 70V_{PP}, f = 1kHz	R_L = 10kΩ		–102		dB
			R_L = 2kΩ		–95		

5.6 Electrical Characteristics (continued)

at V_S = 85V (±42.5V), T_A = 25°C, R_L = 10kΩ to mid-supply, and V_{CM} = V_{OUT} = mid-supply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V_O	Voltage output swing from rail(1)	No load			40	50	mV
		R_L = 10kΩ to mid-supply			420	500	
		R_L = 2kΩ to mid-supply			2	2.5	V
I_{SC}	Output current				±30		mA
C_{LOAD}	Capacitive load drive				1		nF
Z_O	Open-loop output impedance	f = 1MHz			550		Ω
POWER SUPPLY							
I_Q	Quiescent current	I_O = 0mA			420	490	µA
			T_A = –40°C to +125°C(1)			500	
TEMPERATURE							
	Overtemperature shutdown	Shutdown temperature, T_J			170		°C
		Thermal hysteresis			20		

(1) Specification established from device population bench system measurements across multiple lots.

5.7 Typical Characteristics

at T_A = 25°C, V_S = 85V, V_{CM} = V_{OUT} = mid-supply, and R_L = 10kΩ (unless otherwise noted)

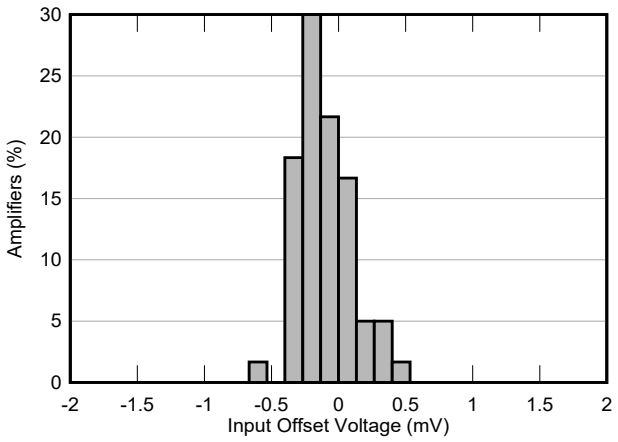


Figure 5-1. Offset Voltage Production Distribution at 25°C

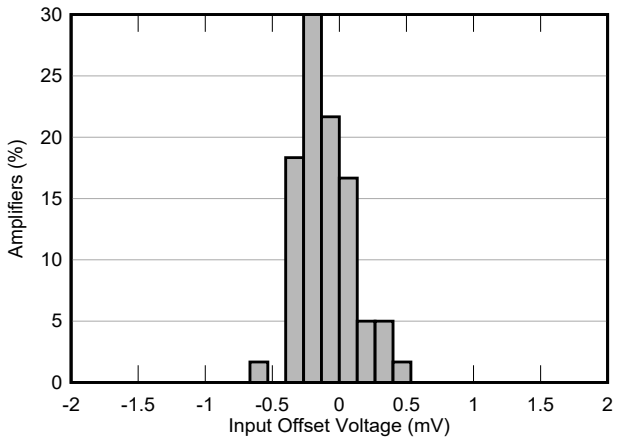


Figure 5-2. Offset Voltage Production Distribution at 125°C

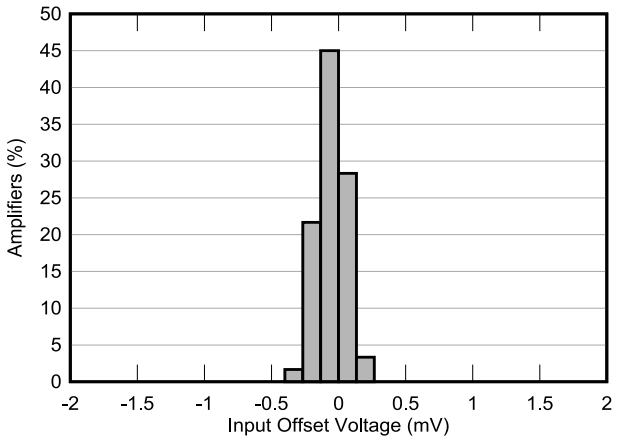


Figure 5-3. Offset Voltage Production Distribution at −40°C

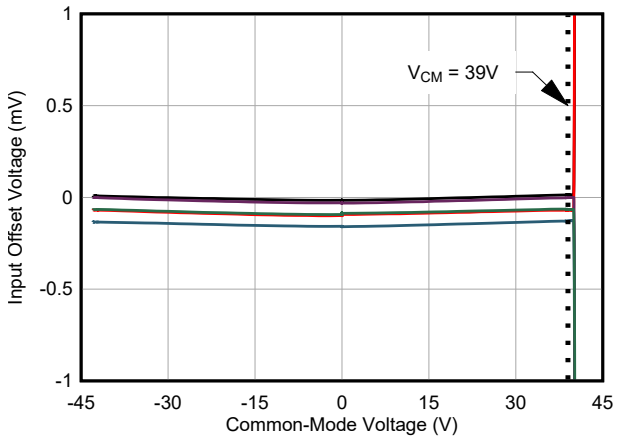


Figure 5-4. Input Offset Voltage vs Common-Mode Voltage

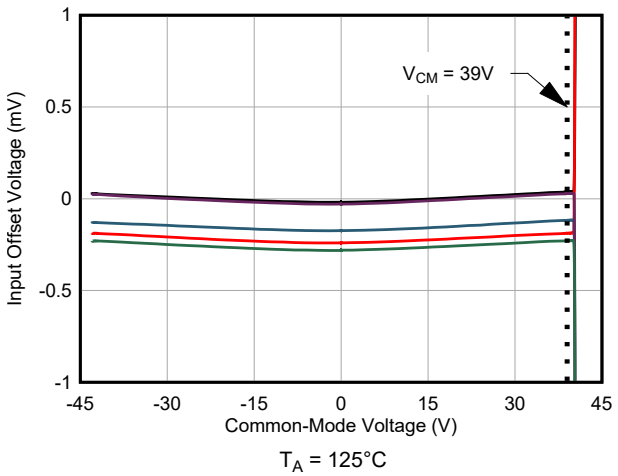


Figure 5-5. Input Offset Voltage vs Common-Mode Voltage

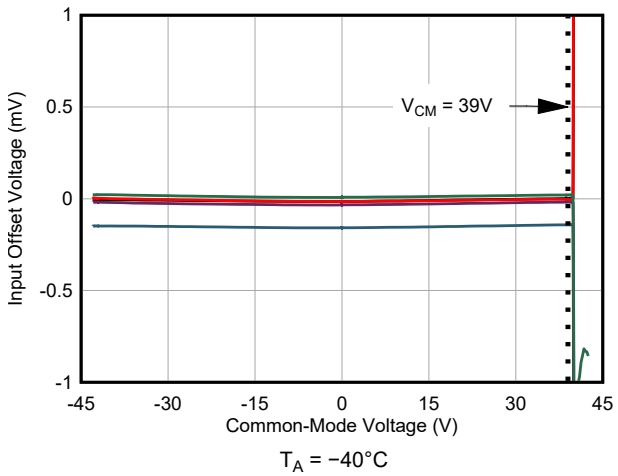


Figure 5-6. Input Offset Voltage vs Common-Mode Voltage

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 85V, V_{CM} = V_{OUT} = mid-supply, and R_L = 10kΩ (unless otherwise noted)

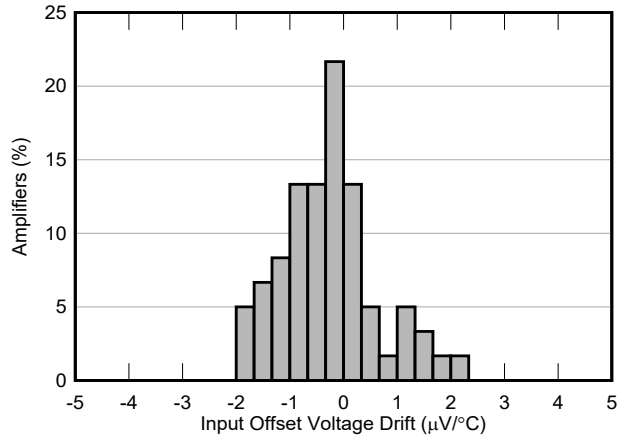


Figure 5-7. Offset Voltage Drift Distribution

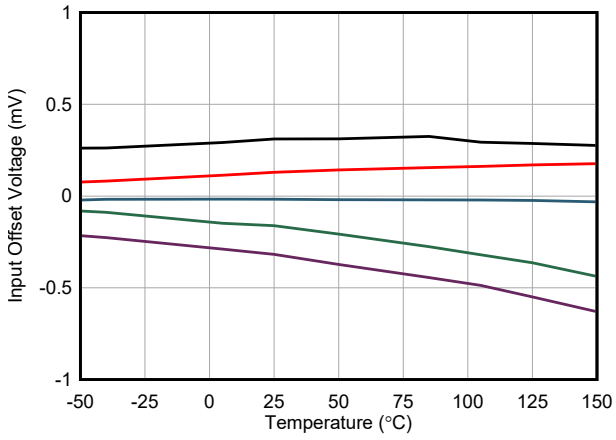


Figure 5-8. Input Offset Voltage vs Temperature

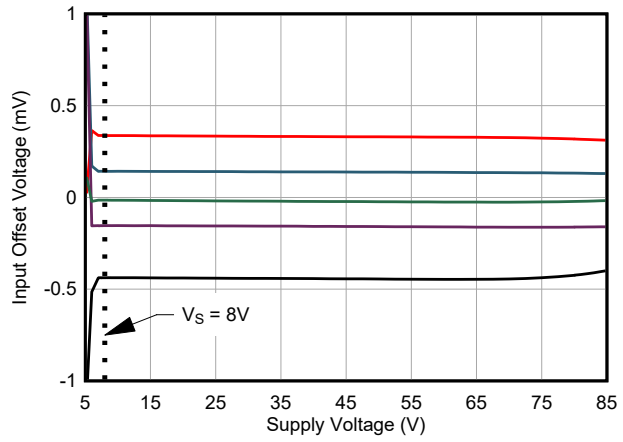


Figure 5-9. Offset Voltage vs Power Supply Voltage

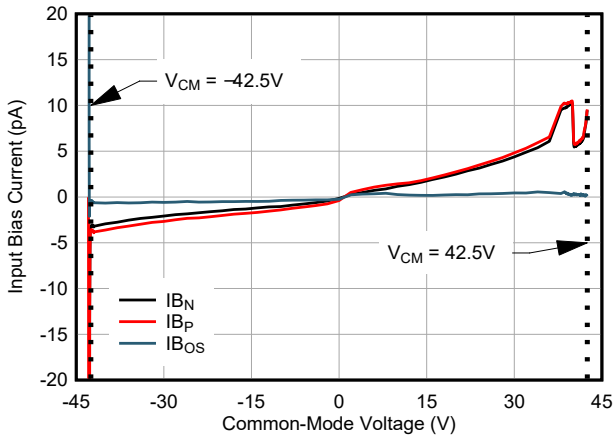


Figure 5-10. Input Bias vs Common-Mode Voltage

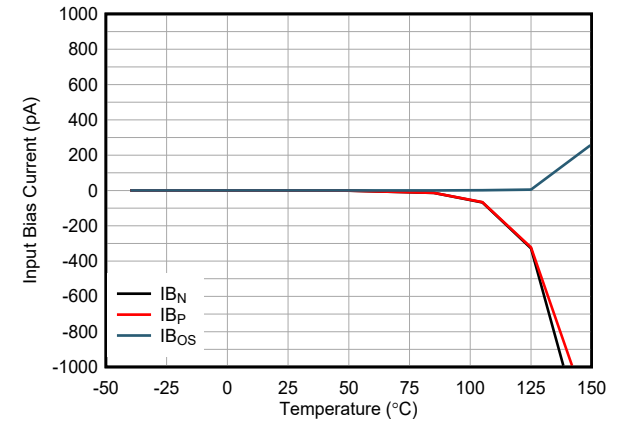


Figure 5-11. Input Bias and Input Offset Current vs Temperature

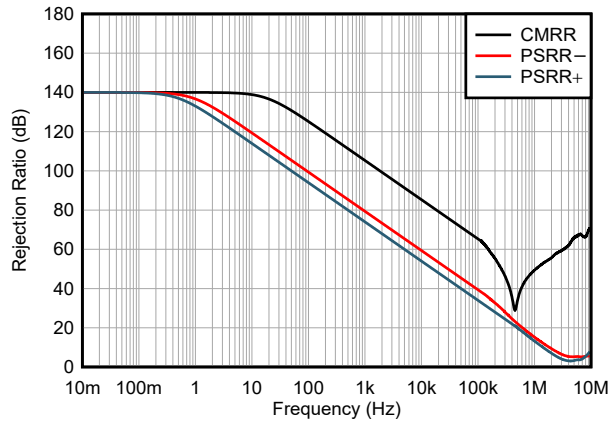


Figure 5-12. Power-Supply and Common-Mode Rejection Ratio vs Frequency

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 85V, V_{CM} = V_{OUT} = mid-supply, and R_L = 10kΩ (unless otherwise noted)

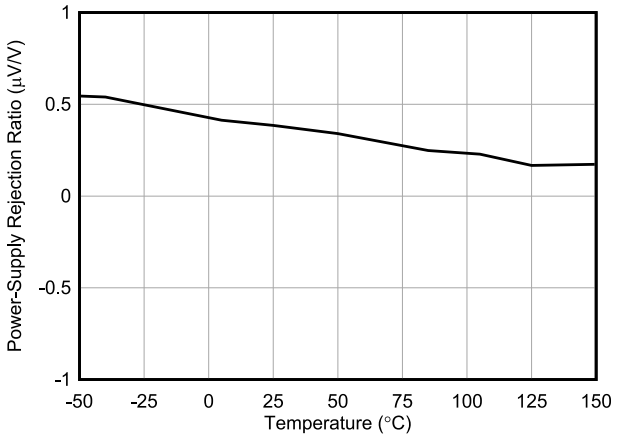


Figure 5-13. Power-Supply Rejection Ratio vs Temperature

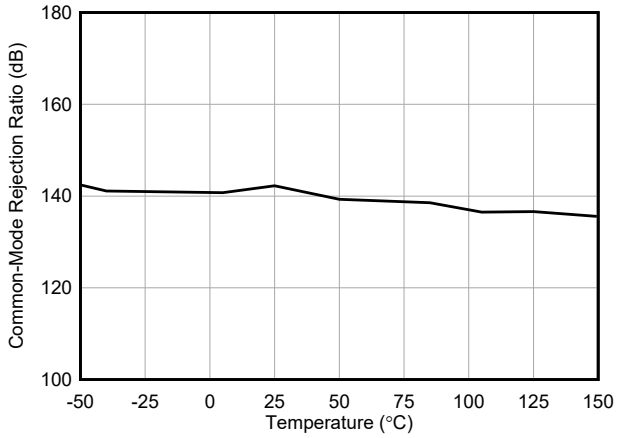


Figure 5-14. Common-Mode Rejection Ratio vs Temperature

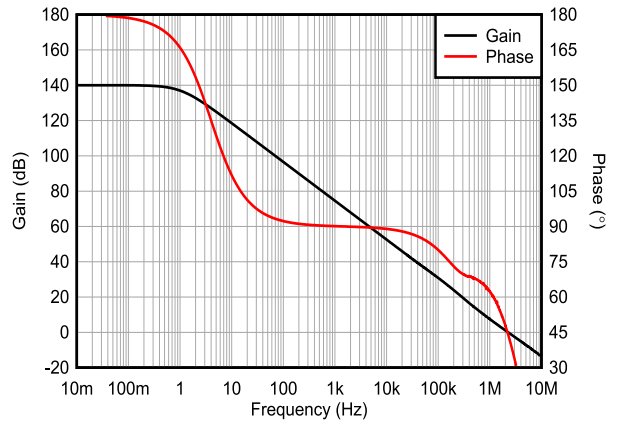


Figure 5-15. Open-Loop Gain and Phase vs Frequency

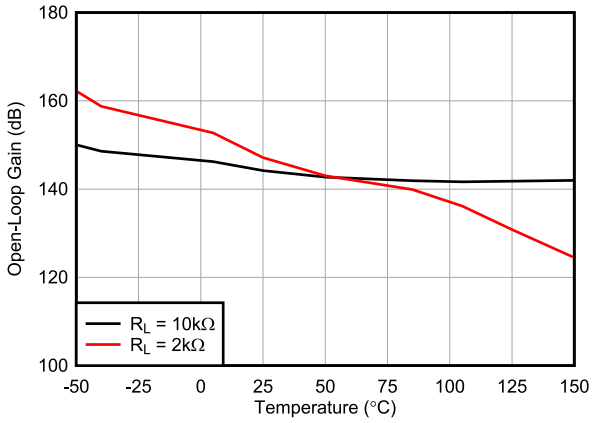


Figure 5-16. Open-Loop Gain vs Temperature

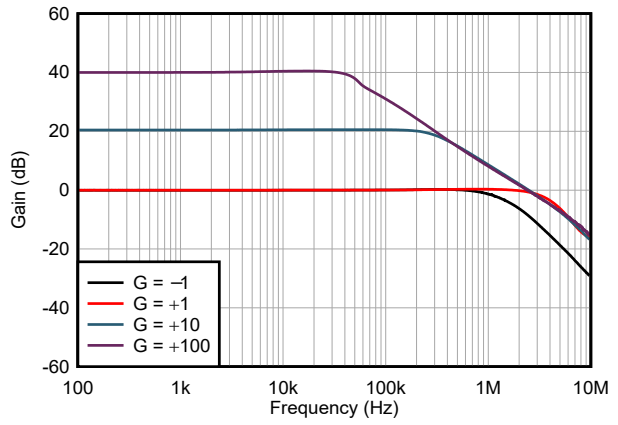


Figure 5-17. Closed-Loop Gain vs Frequency

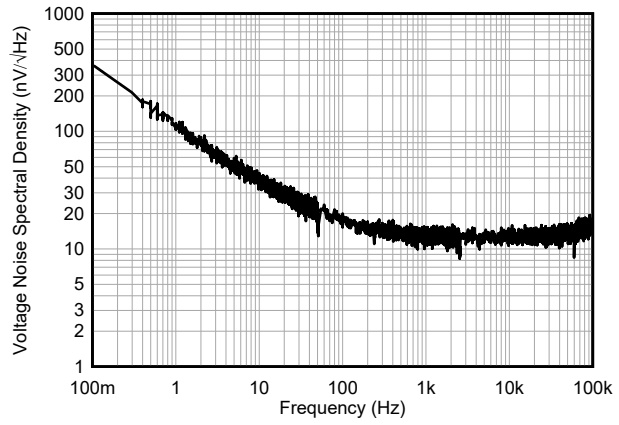


Figure 5-18. Voltage Noise Density vs Frequency

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 85V, V_{CM} = V_{OUT} = mid-supply, and R_L = 10kΩ (unless otherwise noted)

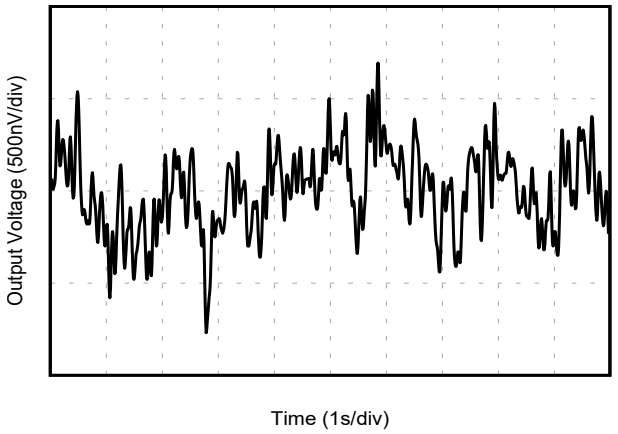


Figure 5-19. 0.1Hz to 10Hz Noise

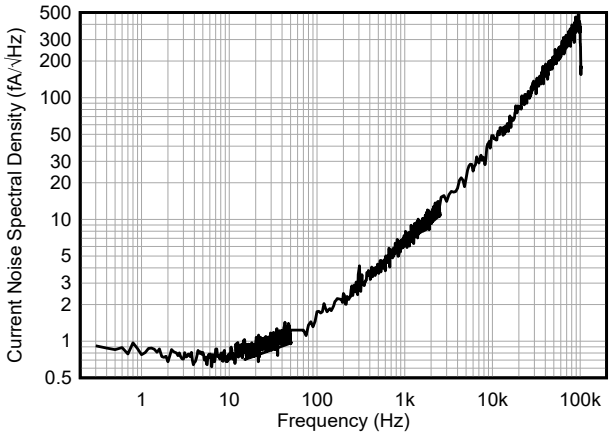


Figure 5-20. Current Noise Density vs Frequency

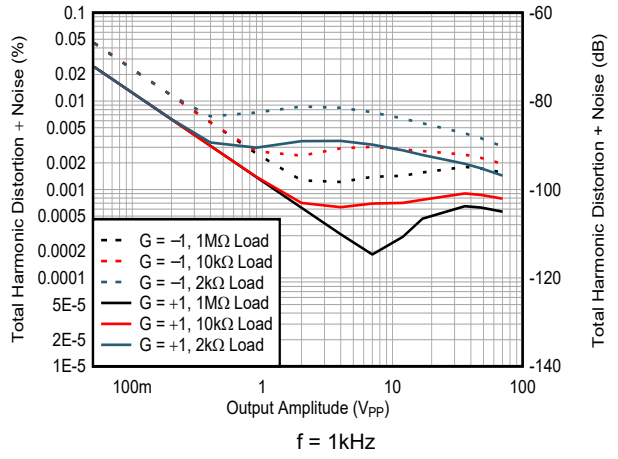


Figure 5-21. Total Harmonic Distortion + Noise Ratio vs Output Amplitude

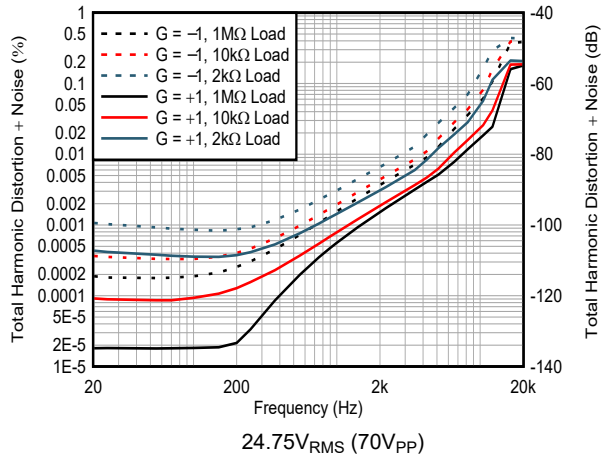


Figure 5-22. Total Harmonic Distortion + Noise Ratio vs Frequency

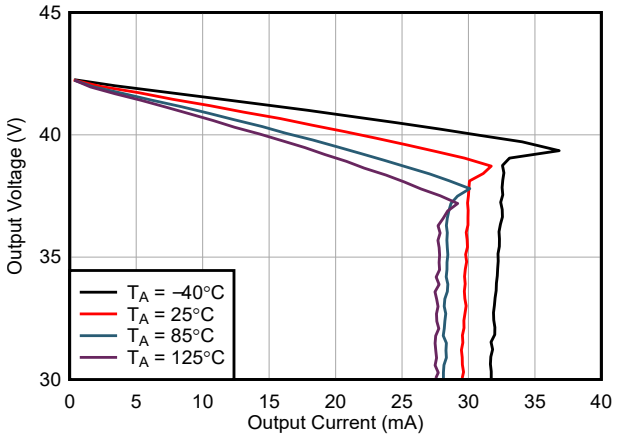


Figure 5-23. Output Voltage Swing vs Output Sourcing Current

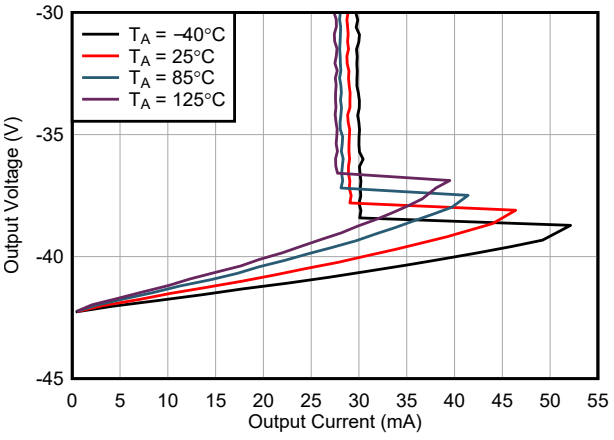


Figure 5-24. Output Voltage Swing vs Output Sinking Current

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 85V, V_{CM} = V_{OUT} = mid-supply, and R_L = 10kΩ (unless otherwise noted)

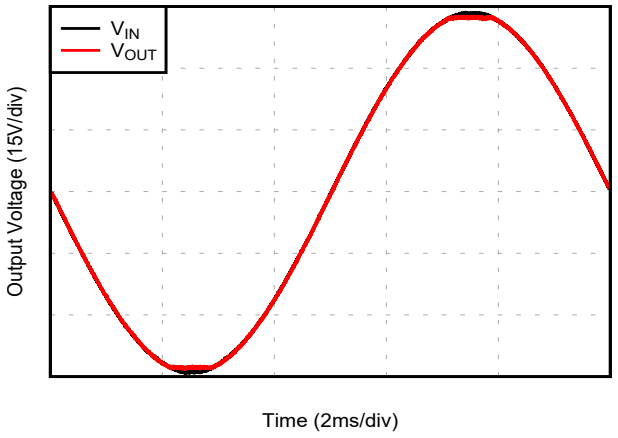


Figure 5-25. No Phase Reversal

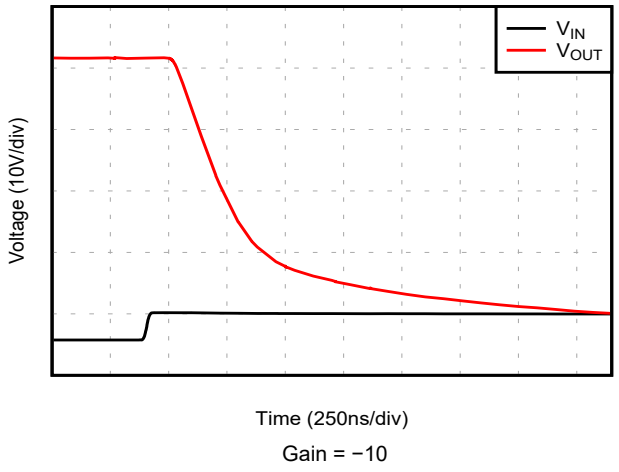


Figure 5-26. Positive Overload Recovery

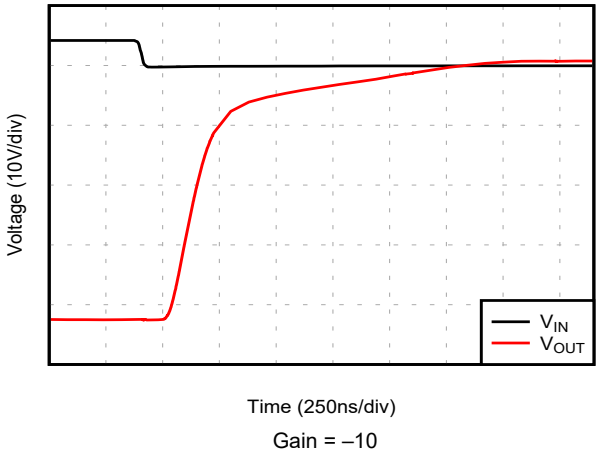


Figure 5-27. Negative Overload Recovery

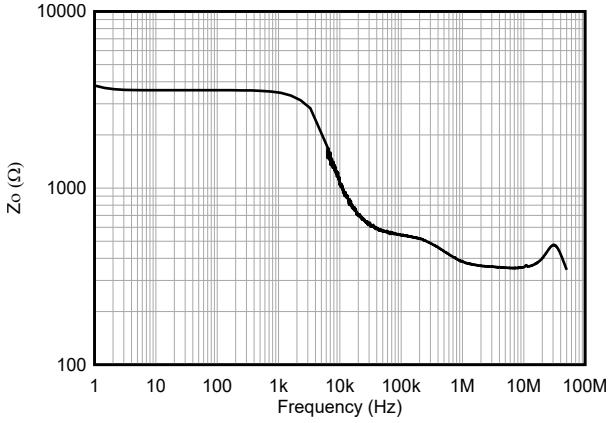


Figure 5-28. Open-Loop Output Impedance vs Frequency

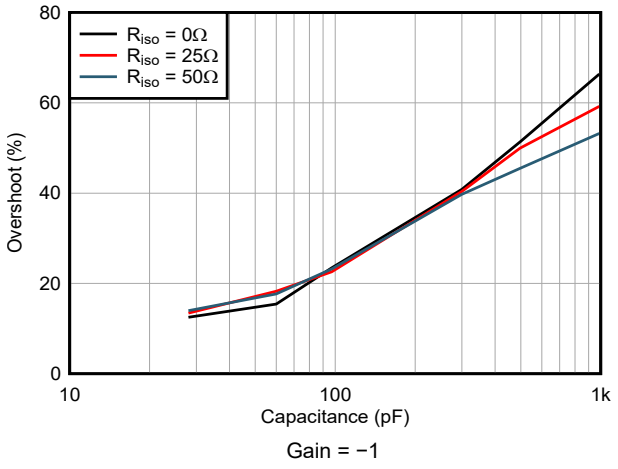


Figure 5-29. Small-Signal Overshoot vs Capacitive Load

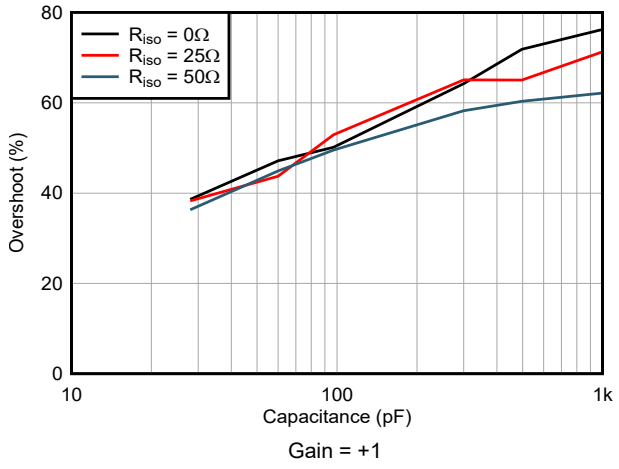


Figure 5-30. Small-Signal Overshoot vs Capacitive Load

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 85V, V_{CM} = V_{OUT} = mid-supply, and R_L = 10kΩ (unless otherwise noted)

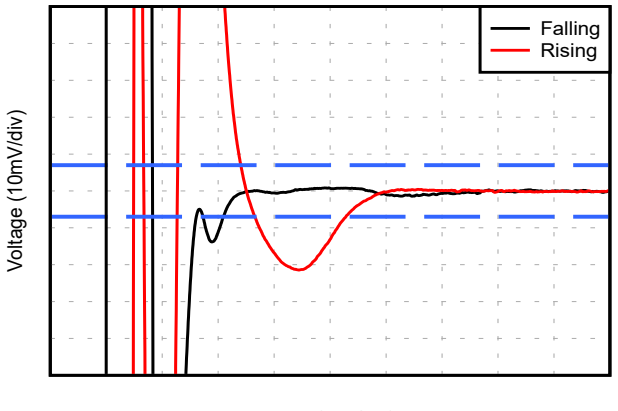


Figure 5-31. Settling Time

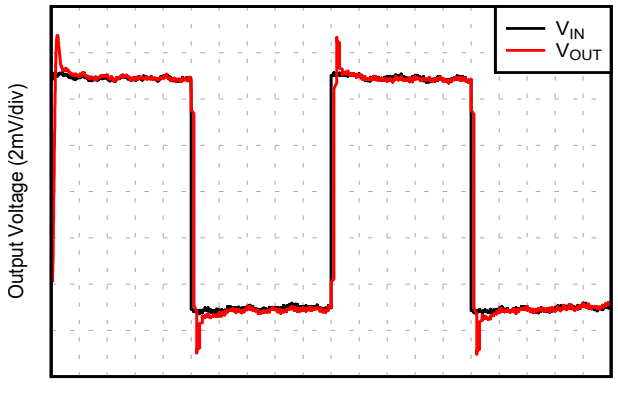


Figure 5-32. Small-Signal Step Response

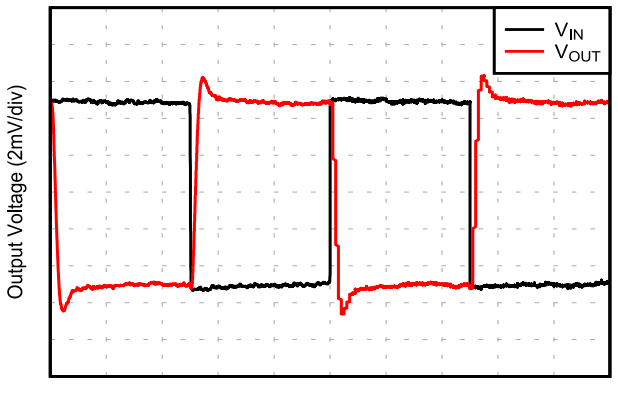


Figure 5-33. Small-Signal Step Response

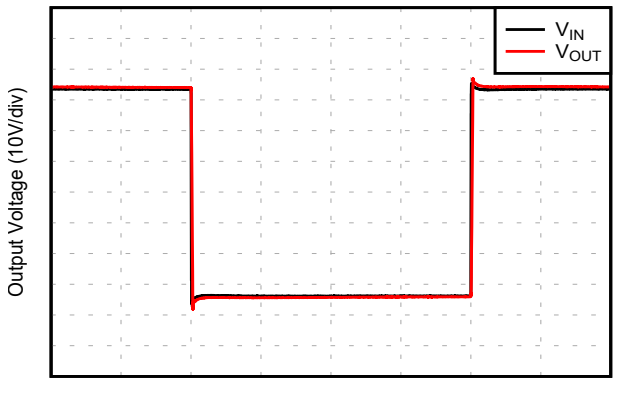


Figure 5-34. Large-Signal Step Response

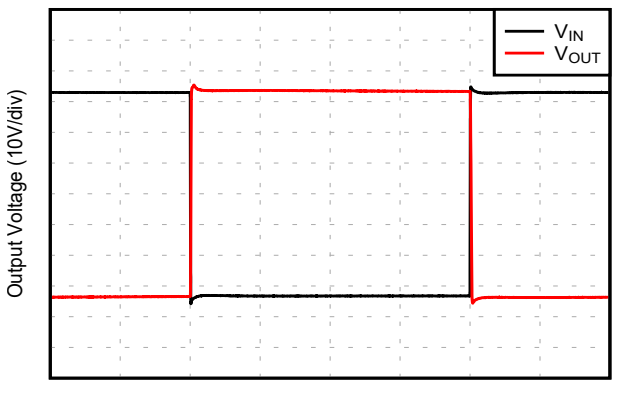


Figure 5-35. Large-Signal Step Response

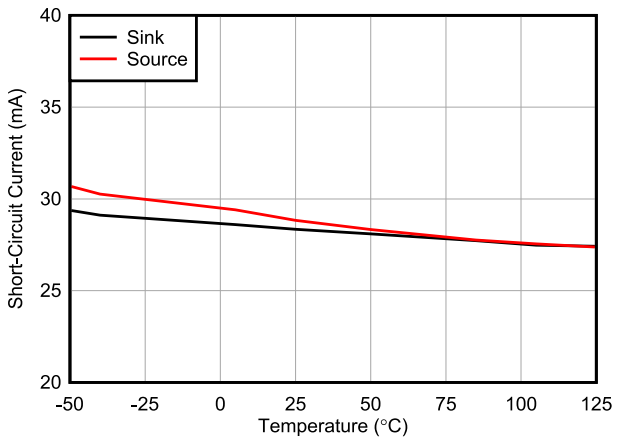


Figure 5-36. Short-Circuit Current vs Temperature

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 85V, V_{CM} = V_{OUT} = mid-supply, and R_L = 10kΩ (unless otherwise noted)

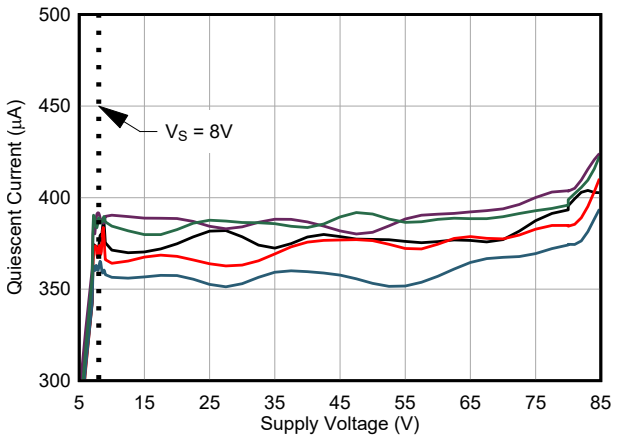


Figure 5-37. Quiescent Current vs Supply Voltage

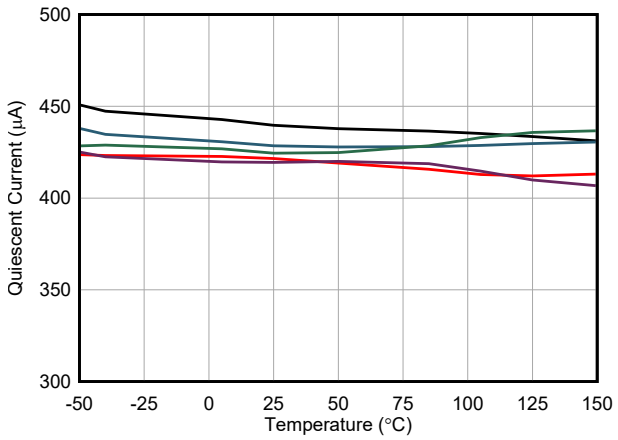


Figure 5-38. Quiescent Current vs Temperature

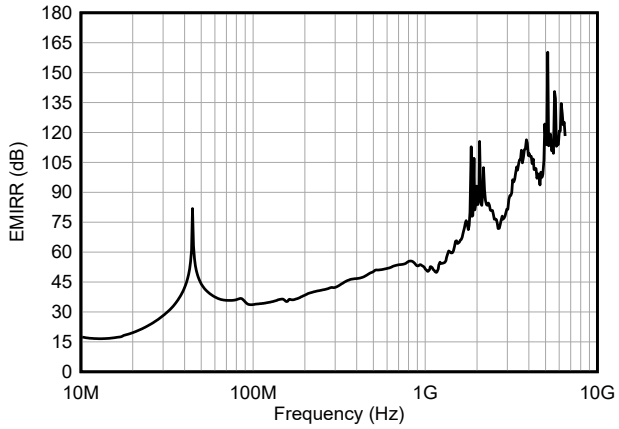


Figure 5-39. Electromagnetic Interference Rejection

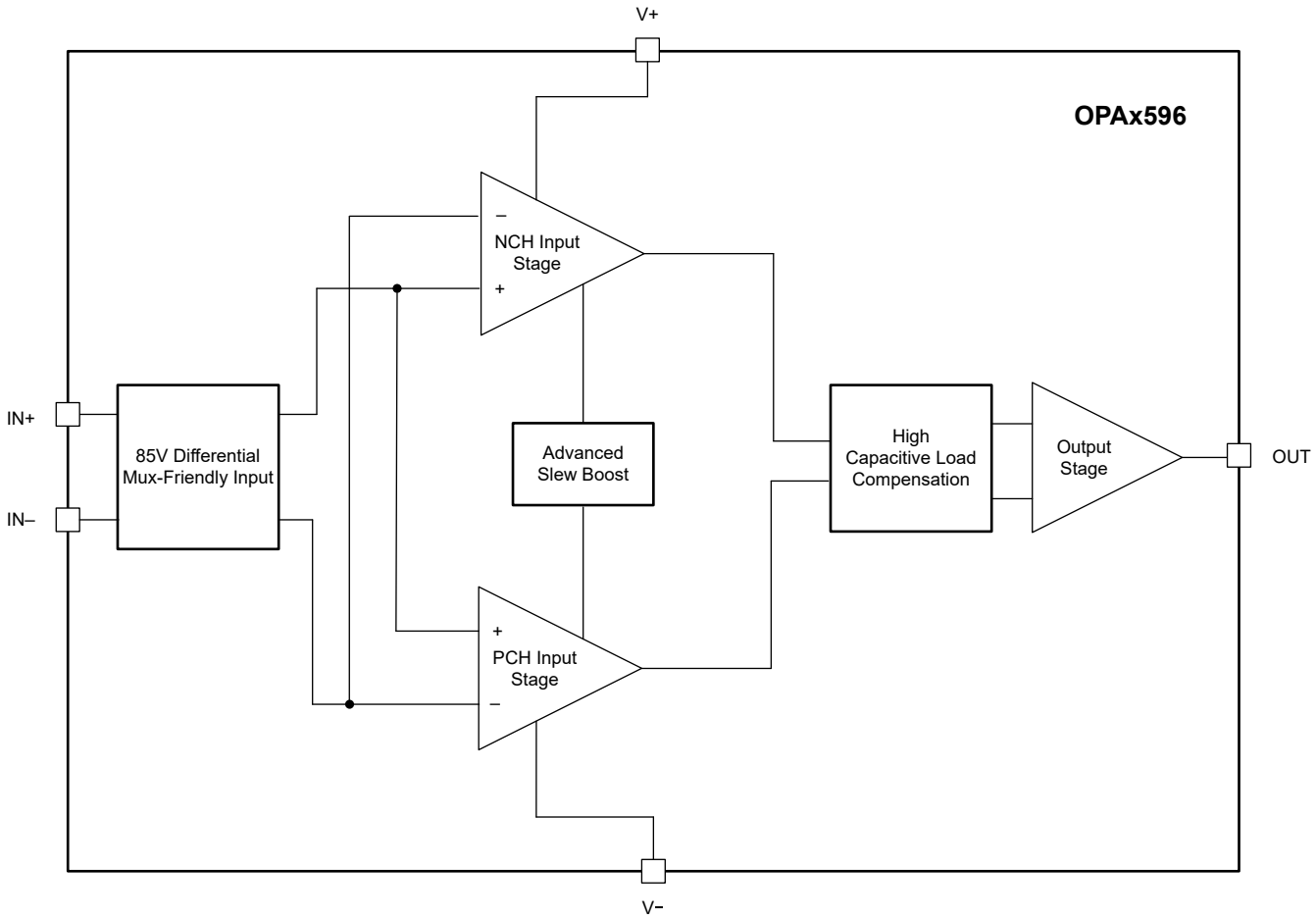
6 Detailed Description

6.1 Overview

The OPAx596 are low power (420µA), high-slew rate (100V/µs), 85V operational amplifiers (op amps). These op amps uses a proprietary design technique to achieve a very high slew capability with minimal power consumption. The OPAx596 is capable of driving ±30mA of output current and can swing to within 100mV of either power supply rail.

The amplifiers feature state-of-the-art CMOS technology and advanced design features that help achieve outstanding ac performance and enable small package options. The OPAx596 strengths also include 3.75MHz bandwidth, 12.8nV/√Hz noise spectral density, and low input bias current. These features make the OPAx596 an exceptional choice to gain or buffer the output of a digital-to-analog converter (DAC) in digitally programmable power supplies.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 MUX-Friendly Inputs

The OPAx596 use a unique input architecture to eliminate the need for input protection diodes but still provide robust input protection under transient conditions. The conventional input diode protection schemes in Figure 6-1are activated by fast transient step responses, and potentially introduce signal distortion and settling time delays because of alternate current paths; see also Figure 6-2. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes that cause an increase in input current and result in extended settling time.

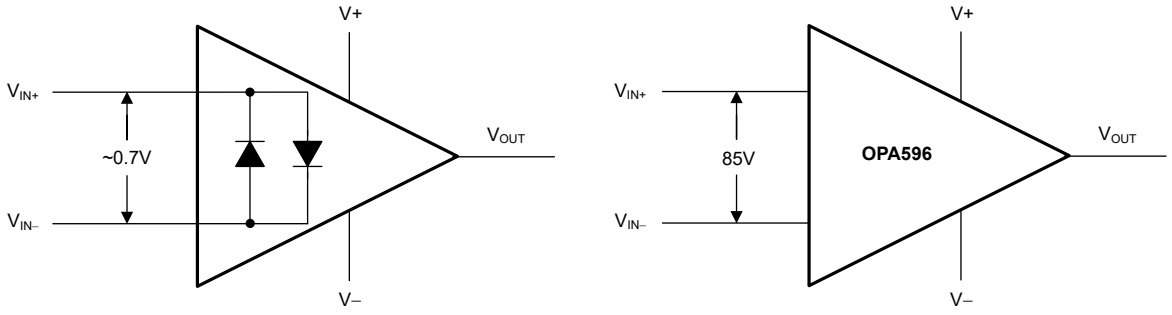


Figure 6-1. OPA596 Input Protection Does Not Limit Differential Input Capability

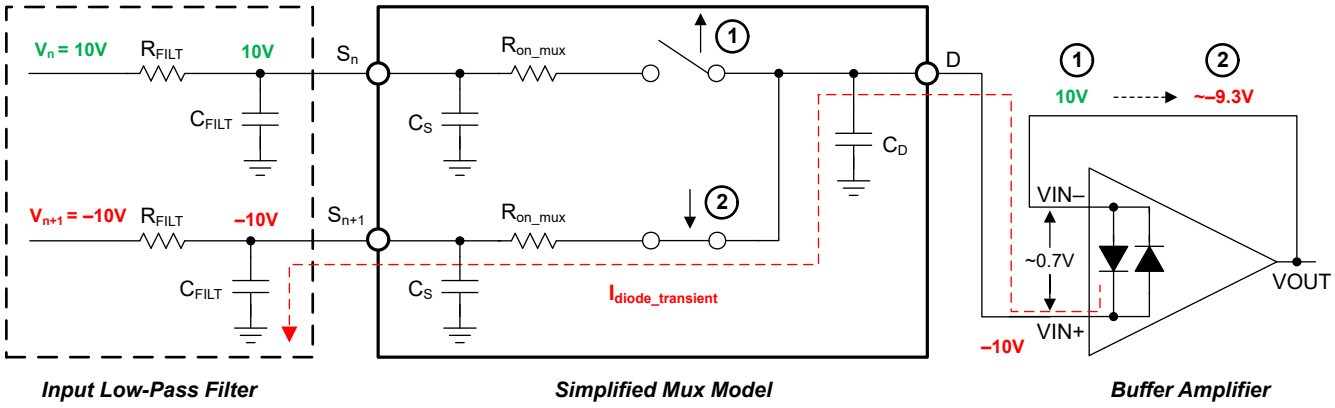


Figure 6-2. Back-to-Back Diodes Create Settling Issues

The OPAx596 feature a true high-impedance differential input capability for high-voltage applications. This patented input protection architecture does not introduce additional signal distortion or delayed settling time, making these devices an excellent choice for multichannel, high-switched, input applications. The OPAx596 tolerate a maximum differential swing (voltage between inverting and noninverting pins of the op amp) of up to 85V, making these devices a great choice for use as a comparator or in applications with fast-ramping or switched input signals.

6.3.2 Thermal Protection

The OPAx596 has a thermal protection feature that prevents damage from self heating. When the junction temperature (T_J) reaches approximately 170ºC, the op amp output stage disables. This thermal protection works by monitoring the temperature of the output stage and turning off the op amp output drive. Thermal protection forces the output to a high-impedance state. The OPAx596 is designed with approximately 20°C of thermal hysteresis and returns to normal operation when the output stage temperature becomes less than approximately 150°C.

This thermal protection is not designed to prevent this device from exceeding absolute maximum ratings, but rather from excessive thermal overload.

6.3.3 Advanced Slew Boost

Slew rate is the maximum rate of change of output voltage change with respect to time and is typically specified in units of volts per microsecond, V/µs. Op amps can enter a slew condition when a large, rapid moving signal is applied at the input. While slewing, the op amp enters an open loop condition and significant slew induced distortion can be seen on the output signal.

Equation 1 shows that the slew rate, SR, of an op amp is typically determined by the saturation current of the input stage, I_{TAIL}, and the compensation capacitor, C_C.

$$SR = \frac{I_{TAIL}}{C_C} \tag{1}$$

Slew rate typically scales with the quiescent current, I_Q, of the op amp. There are several ways that designers have overcome slew rate limitation. For example, lowering C_C, commonly known as decompensation, improves slew rate at the expense of stability. Decompensated op amps require a minimum gain and are not stable at unity gain. More commonly, modern op amps are equipped with slew boost technology that increases I_{SAT} to improve slew rate. Slew boost circuits can vary in implementation, but typically, expect about a four-fold improvement over comparable unboosted op amps.

The OPAx596 uses a proprietary design to achieve an unprecedented slew rate to I_Q ratio. The novel slew boost technology in OPAx596 provides a nearly 100 × slew rate improvement over comparable unboosted op amps. The op amp is unity gain stable and can be used configured as a buffer if desired.

Table 6-1 shows a comparison of slew rates and quiescent currents of different op amps.

Table 6-1. Op Amp Slew Rates and Quiescent Current

PART NUMBER	SLEW RATE	QUIESCENT CURRENT
OPAx596	100V/µs	420µA
OPAx188	0.8V/µs	425µA
OPAx202	0.35V/µs	580µA
OPAx192	20V/µs	1mA
OPA454	13V/µs	3.2mA

6.3.4 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time.

6.3.5 Full-Power Bandwidth Improved

The full-power bandwidth curve has been a staple in data sheets for decades. The full-power bandwidth of an op amp provides some indication about where designers can expect slew-induced distortion on a signal of a given amplitude and frequency. The full-power bandwidth curve is generated using Equation 2.

$$\text{FPBW} = \frac{\text{SR}}{2\pi V_{\text{OUT\_MAX}}} \tag{2}$$

Figure 6-3 shows the full-power bandwidth of the OPAx596. The curve is a good reference for designers that need to achieve high-voltage, high-frequency output swings with little concern for distortion performance. Unfortunately, the curve provides little indication of the true distortion at any given point on the curve. The full-power bandwidth curve is, after all, only a theoretical value and slew-induced distortion appears gradually as the output nears the maximum rate of change. Furthermore, slew-induced distortion is only one of several sources of op-amp distortion. Therefore, the curve is a decent starting point, but not a reliable source for distortion performance.

Figure 6-4 shows the full power bandwidth in terms of total harmonic distortion (THD) performance for the OPAx596. This curve provides a better indication of the level of distortion that a designer can expect for a signal of a given amplitude and frequency. For example, the OPAx596 can achieve approximately −100dB or better of THD at $70V_{PP}$ up to approximately 1kHz. As a second example, the OPAx596 can achieve approximately −130dB or better of THD at $10V_{PP}$ up to about 1kHz. As a result of limitations in measurement bandwidth, only 20kHz data are recorded.

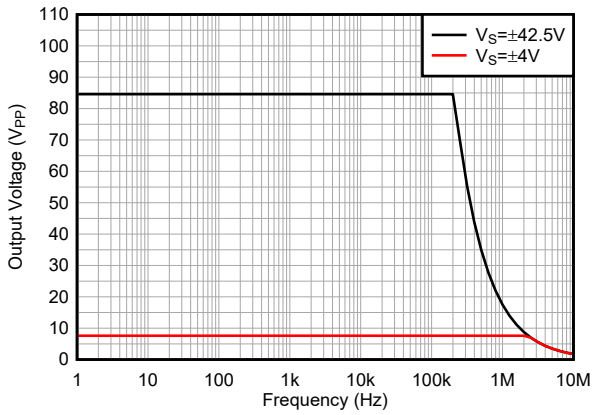


Figure 6-3. Full-Power Bandwidth

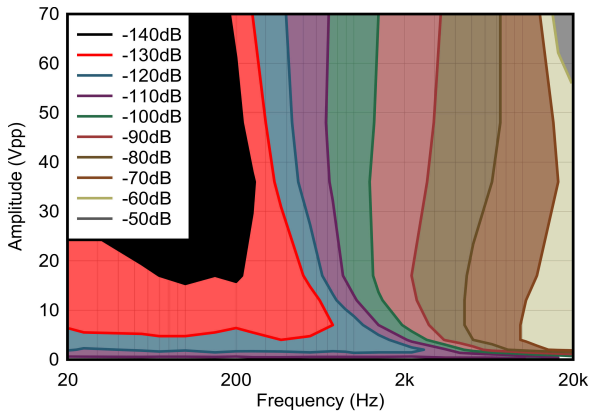


Figure 6-4. Full-Power Bandwidth Improved

6.4 Device Functional Modes

The OPAx596 has a single functional mode and is operational when the power-supply voltage is between 8V (±4V) and 85V (±42.5V).

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The OPAx596 are low power (420µA), high-slew rate (100V/µs), 85V power operational amplifiers (op amps). These op amps use a proprietary design technique to achieve a very high slewing capability while consuming minimal power. The low power consumption helps reduce heat generation on the board while the output swings near the supply rail. The high slew reduces slew related distortion at the output when dealing with large peak, high frequency signals.

7.2 Typical Applications

7.2.1 Bridge-Connected Piezoelectric Driver

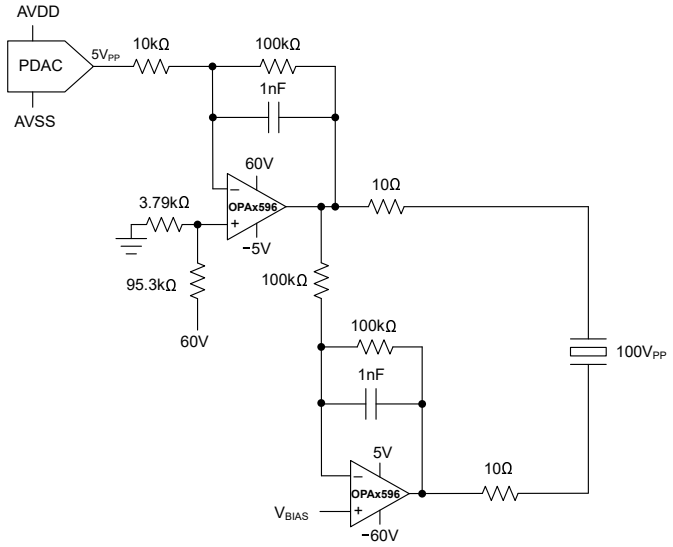


Figure 7-1. 100V_{PP} Piezoelectric Driver With Bridge Connected Load

7.2.1.1 Design Requirements

The OPAx596 is used to drive a piezoelectric actuator with a 100V operating range at a relatively low frequency of 100Hz. The large capacitance inherent to the piezoelectric actuator can cause undesired ringing of the driver amplifier. An inaccurate response of the actuator is possible due in part to amplifier instability. Adequate phase margin for a 500nF equivalent load and wide output swing capability is necessary for a robust driver circuit for the piezoelectric actuator presented here. Table 7-1 shows the design parameters.

Table 7-1. Design Parameters

PARAMETER	VALUE
Power supply voltage	65V
Piezoelectric actuator capacitance (1kHz)	500nF
Piezoelectric operating voltage range	0V to 100V
Operating frequency	100Hz
DAC output voltage	5V_{PP}

7.2.1.2 Detailed Design Procedure

Piezoelectric actuators offer many benefits over traditional solenoid counterparts. Piezoelectric actuators are more precise, power efficient, and smaller in general when compared to solenoid actuators. One challenge with piezoelectric actuators is that the piezoelectric actuators operate over a very wide voltage range. Driving voltages of more than 60V are not uncommon, and can easily reach hundreds of volts. The OPAx596 operate with a supply voltage of up to 85V.

In this design example, the OPAx596 are used to provide a $100V_{PP}$ signal to control a high-voltage piezoelectric actuator (see also Figure 7-1). The piezoelectric actuator can be modeled as a large capacitor when operated at less than the resonant frequency. The piezoelectric actuator is treated as a floating load driven by two op amps of the OPAx596. The outputs of the op amps are set to be 180° out-of-phase to essentially double the voltage seen by the actuator load. The signal voltage of the digital-to-analog converter is applied a −10V/V gain by the OPAx596. A simple voltage divider provides a dc reference to level shift the output to get a unipolar driving voltage. Figure 7-2 shows the output voltage of both amplifiers and the voltage seen by the piezoelectric load.

The large capacitive load seen by the amplifiers can lead to instability and proper compensation is required. A straight forward method to improve phase margin and stability is to add isolation resistors and compensation capacitors in the feedback. A small 10Ω R_{ISO} at the output of each of the OPAx596 and a 1nF compensation capacitor is effective. Keep the isolation resistors as small as possible to minimize the voltage drop across them. Choose the compensation capacitors according to the frequency of operation. For this example, 1nF capacitors leave enough bandwidth to accommodate a 100Hz signal. Use simulation tools, such as PSPICE or TINA-TI, to confirm stability.

Understanding the limitations of this circuit are important. As with any capacitive load, the impedance can significantly decrease at higher frequencies. This behavior greatly increases the current output capability requirements of the driver amplifier at high frequencies. If high frequency operation is required, consider other amplifiers with higher current drive capability. At 100Hz, the OPAx596 is capable of supplying the necessary current. Figure 7-3 shows the current output of the OPAx596 in this example.

7.2.1.3 Application Curves

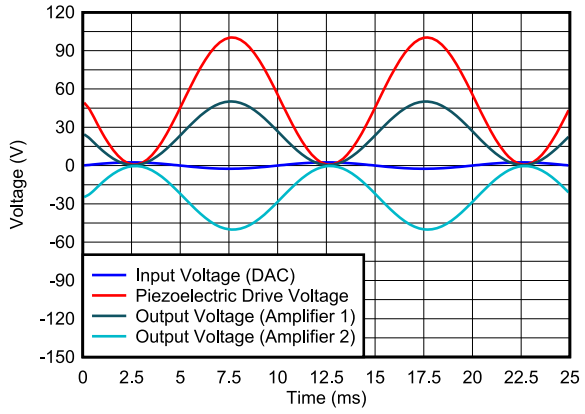


Figure 7-2. Piezoelectric Driver Output Voltage

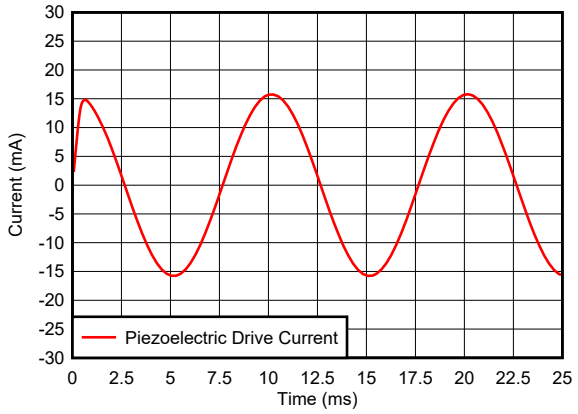
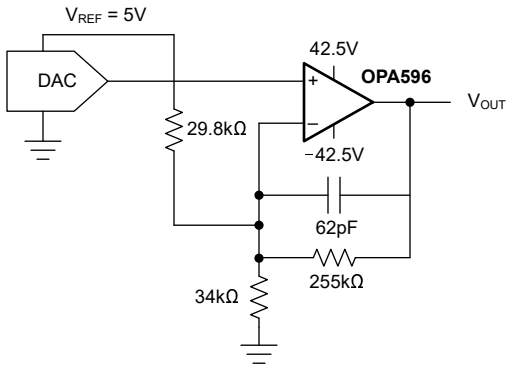


Figure 7-3. Piezoelectric Driver Output Current

7.2.2 DAC Output Gain and Buffer



7.2.2.1 Design Requirements

The OPAx596 is designed for use as an output driver stage with gain and provides a wide, bipolar supply voltage. Combined with the small size of the SOT23-5 package and the low power consumption, these features make this device a great choice for high-channel density systems, such as semiconductor test and manufacturing platforms where many channels are present. In this design example, the OPAx596 is configured for a gain of approximately 17V/V.

Table 7-2. Design Parameters

PARAMETER	VALUE
Supply voltage	−42.5V to +42.5V
Input voltage	0V to 5V
Output voltage	−42.5V to +42.5V
Gain	17V/V

7.2.2.2 Detailed Design Procedure

In this design example, the OPAx596 is configured as both a gain stage and output driver. The input signal to the amplifier is 0V to 5V, and the device is configured with a noninverting gain of 17V/V. The DAC reference voltage of 5V is used as a reference to enable a bipolar output swing. This configuration results in an output voltage of about −42.5V to +42.5V. This design example is common in many systems that use a DAC to provide the input signal and require a wide output signal with low output current requirements. The OPAx596 can swing to either rail while remaining within the thermally specified limits. Such systems include test and measurement platforms and power supplies.

7.2.3 Single-Supply Piezoelectric Driver

Some piezoelectric transducers can be referenced to ground as shown in Figure 7-4. The wide supply voltage of the OPAx596 enables designers to drive a high voltage transducer up to 85V, without having to use the more complicated bridge tied load configuration. The piezoelectric load presents a large capacitance at the output of the amplifier and proper compensation is required to avoid instability. Also consider the output current drive requirement. The current drive requirement is determined by the frequency of operation and the effective capacitance of the load. High frequency and large capacitance reduce the effective impedance of the load and thereby increase the current drive requirement. The OPAx596 are an excellent choice to drive piezoelectric loads at dc and low frequency.

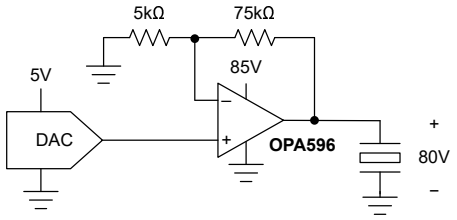


Figure 7-4. 80V Single-Supply Piezoelectric Driver

7.2.4 High-Side Current Sense

The OPAx596 enables high voltage current sense measurements. High-side voltage measurements of ±100V or more can be easily implemented using the OPAx596. The voltage capability is proportional to the gain of the sense circuit and the input common-mode range of the amplifier. Figure 7-5 shows the OPA596 configured for a ±500V high side current measurement and a gain of 2. A high precision amplifier is used as a gain stage to amplify the signal further.

Make the input resistors large enough to avoid any loading related errors. The low input bias current of the OPAx596 allows for the use of larger resistors when compared to other power amplifiers and is not a major contribution to the total error in this application. Special consideration of input bias current, thermal noise, and input common-mode range is warranted when choosing resistors for this design.

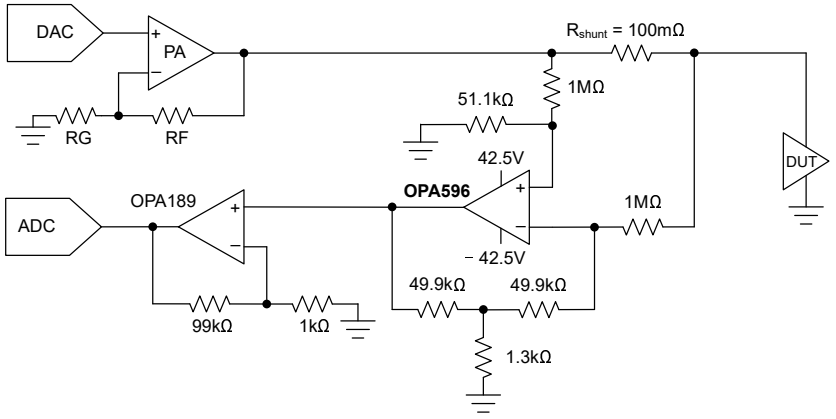


Figure 7-5. ±500V High-Side Current Sense

7.2.5 High-Voltage Instrumentation Amplifier

Differential measurements are common in a wide variety of applications. When high input impedance is needed in a differential measurement, an instrumentation amplifier can be employed. The challenge is that readily available, monolithic instrumentation amplifiers offer a limited input common-mode voltage range. Figure 7-6 shows a discrete instrumentation amplifier featuring the OPAx596. The circuit is valuable when a high impedance, differential measurement is required in the presence of very high common-mode.

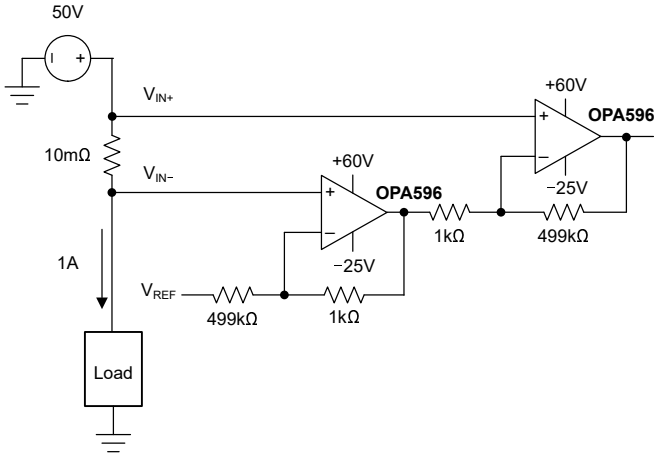


Figure 7-6. High-Voltage Instrumentation Amplifier

7.2.6 Composite Amplifier

The OPAx596 offers low input offset voltage and input offset drift. In some applications, however, even higher precision is required. Figure 7-7 shows how to greatly improve the dc precision of the OPAx596. The OPA186 is a 24V, zero-drift op amps offered at a competitive cost and can be paired with the OPAx596 in a composite amplifier configuration to create a high precision amplifier with high voltage output capability.

The first amplifier, OPA186, corrects the offset of the second amplifier, OPAx596. The gain of the composite amplifier is set by R_F and R_G, such that the gain is equal to R_F / R_G + 1. In this application, the overall gain of the circuit is 100V/V. Adding gain to the OPAx596 through R_1 and R_2 improves the overall bandwidth of the composite amplifier by reducing the gain burden on the OPA186. Increasing the gain too much on the second amplifier, however, reduces the closed loop bandwidth and can negatively affect phase margin. Special considerations for stability are warranted when building composite amplifiers.

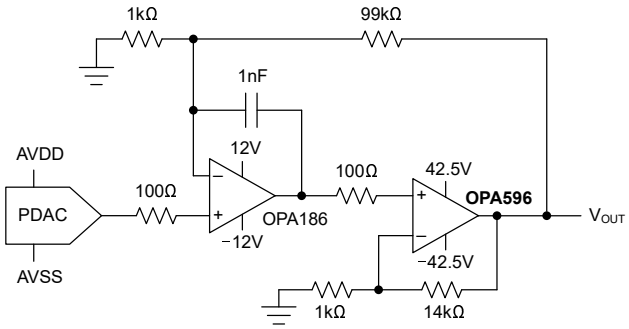


Figure 7-7. High-Precision, High-Voltage Output Composite Amplifier

7.3 Creepage and Clearance

When designing and building electrical systems with high voltage, two important concepts to consider are creepage and clearance. Creepage distance refers to the shortest path that an electric current can take along the surface of an insulating material, such as a printed circuit board (PCB) or a plastic enclosure. Clearance distance refers to the shortest distance between two conductive parts, such as wires, terminals, or components, through the air. Figure 7-8 illustrates creepage and clearance for a typical integrated circuit (IC).

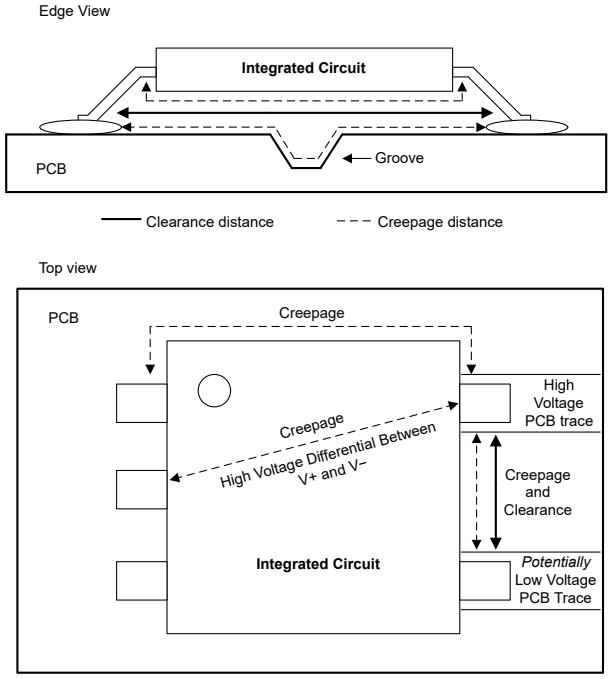


Figure 7-8. Creepage and Clearance in Integrated Circuits

Several standards exist with creepage and clearance guidance, but how the standards pertain to operational amplifiers and other integrated circuits is largely left to interpretation and internal requirements. The guidance distances are significantly affected by pollution degree, maximum voltage, and the underlying application. In the case of creepage, the comparative tracking index (CTI) rating of the insulating material is a major factor. Different design techniques exist to improve creepage and clearance if deemed necessary, including adding PBC grooves, conformal coating, and, or derating the operating voltage.

Texas Instruments offers modern packaging with small dimensions that are designed to minimize PCB area. However, the requirement to meet any creepage or clearance specifications depends on the designer's interpretation and implementation of any relevant IEC or system-level standards. For more information on this topic, visit the *Demystifying Clearance and Creepage Distance for High-Voltage End Equipment* document.

7.4 Power Supply Recommendations

The OPAx596 operates from power supplies up to ±42.5V (85V), and as little as ±4V (8V) with excellent performance. Most behavior remains unchanged throughout the full operating voltage range, but Section 5.7 shows parameters that vary with operating voltage. A power-supply bypass capacitor of at least 0.1µF is required for proper operation. Make sure that the capacitor voltage is rated for high voltage across the full operating temperature range. The OPAx596 can be powered with asymmetrical supplies to optimize power dissipation in applications that do not require an equal positive and negative output voltage swing.

7.5 Layout

7.5.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including the following guidelines:

- Noise can propagate into analog circuitry through the power pins of the op amp and the circuit as a whole. Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground. Place the capacitors as close to the device as possible. A single bypass capacitor from V+ to ground is sufficient for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

7.5.1.1 Thermal Considerations

Through normal operation, the op amps can self-heat. Self-heating is a natural increase in the die junction temperature that occurs in every amplifier. This self-heating is a result of several factors, including quiescent power consumption, package thermal resistance, PCB layout, and device operating conditions.

Operate the OPAx596 within the rated junction temperature, T_J, range to avoid thermal shutdown. Use the Equation 3 to determine the estimated T_J

$$T_J = P_D \times R_{\theta JA} + T_A \tag{3}$$

In a quiescent state, P_D is given by the product of the power supply and the quiescent current of the op amp. Equation 4 shows the calculation of T_J for the OPAx596 assuming an 85V power supply is used and an operating temperature of 25°C.

$$T_J = (85V \times 490\mu A) \times 165.4°\frac{C}{W} + 25°C \tag{4}$$

$$T_J = 31.89°C \tag{5}$$

The low power consumption of the OPAx596 causes minimal self-heating even in a small SOT23-5 package as given by Equation 5. In a loaded condition, P_D is equal to addition of the quiescent power, P_{DQ} and the power dissipated by the output stage, P_{DL}. The worst-case condition is given when the output voltage is equal to ½ of either supply rail (assuming symmetrical supplies, V+ and V-). In a worst-case condition, P_{DL} is given by Equation 6.

$$P_{DL} = \frac{(V+)^2}{4 \times R_L} \tag{6}$$

For example, assume the OPAx596 is powered with bipolar ±42.5V power supplies and drives a 5kΩ load, R_L, to ground. The maximum increase in T_J is expected to be about 22°C as given by Equation 7. In this example, to keep the op amp within the *Absolute Maximum Ratings*, operate in T_A well under 128°C to account for different factors. The calculation for a 5kΩ load is depicted visually in Figure 7-9.

$$\Delta T_J = (41.7\text{mW} + 90.3\text{mW}) \times 165.4\frac{^\circ\text{C}}{\text{W}} \quad (7)$$

For high-voltage amplifiers such as the OPAx596, the junction temperature can easily be tens of degrees higher than the ambient temperature in a quiescent (unloaded) condition. As shown by Equation 3, the junction temperature depends on the thermal properties of the package, as expressed by the junction-to-ambient thermal resistance ($R_{\Theta JA}$). If the device then begins to drive a heavy load, the junction temperature can rise and trip the thermal-shutdown circuit. Figure 7-9 shows the maximum output voltage versus ambient temperature to avoid exceeding the *Absolute Maximum Ratings* in both loaded and unloaded conditions for the SOT23-5 package version of the OPA596. The curve assumes a typical quiescent current and does not account for any temperature variation of quiescent current.

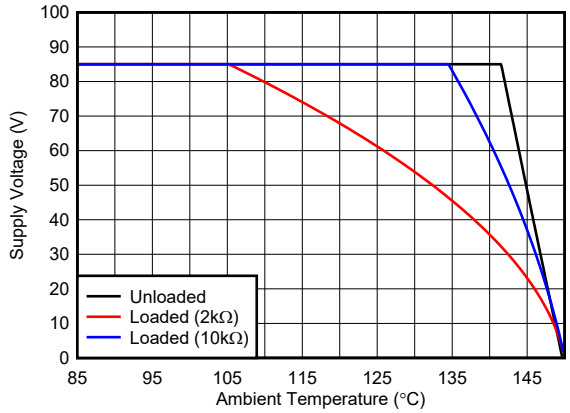


Figure 7-9. OPA596 (SOT23-5) Thermal Safe Operating Area

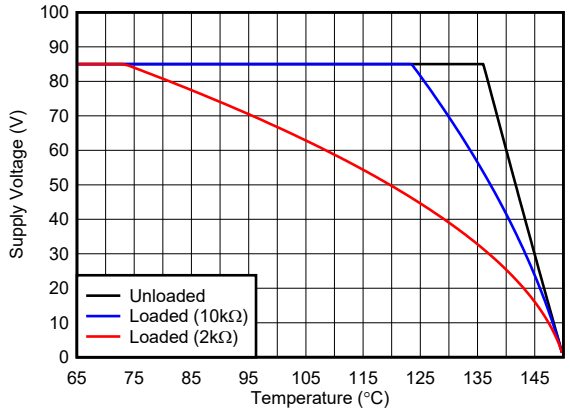


Figure 7-10. OPA2596 (VSSOP-8) Thermal Safe Operating Area

7.5.2 Layout Example

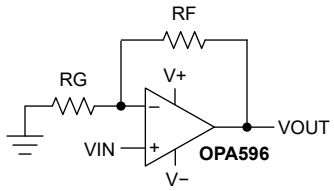


Figure 7-11. Schematic Representation of Noninverting Configuration

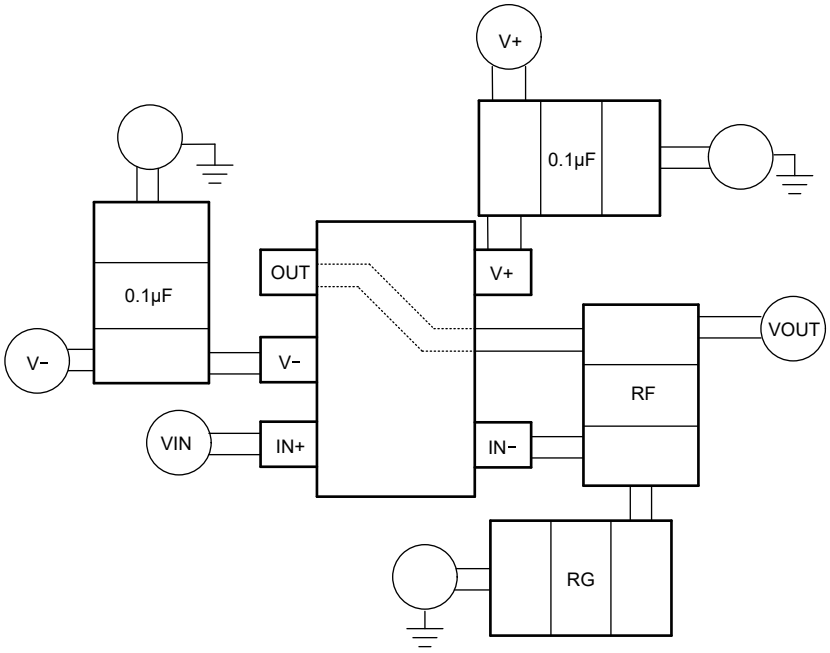


Figure 7-12. Board Layout for Noninverting Configuration of the SOT23-5 Package

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December 2025) to Revision C (December 2025)	Page
• Changed OP2596 D (SOIC, 8) package from preview to production data	1

Changes from Revision A (February 2025) to Revision B (December 2025)	Page
• Changed OP2596 DGK (VSSOP, 8) package from preview to production data	1
• Added note 1 to *Electrical Characteristics*	6
• Updated voltage output swing from rail TYP values	6
• Changed voltage output swing from rail (R_L = 10kΩ) MAX from 435mV to 500mV	6
• Changed voltage output swing from rail (R_L = 2k) MAX from 2.05V to 2.5V	6

Changes from Revision * (June 2024) to Revision A (February 2025)	Page
• Changed data sheet status from advanced information (preview) to production mix (active and preview)	1
• Added OP2596 preview D (SOIC, 8) package to the *Device Information* table	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2596DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3SAS
OPA2596DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2596D
OPA596DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	O596
OPA596DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	O596
OPA596DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	O596
OPA596DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	O596

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

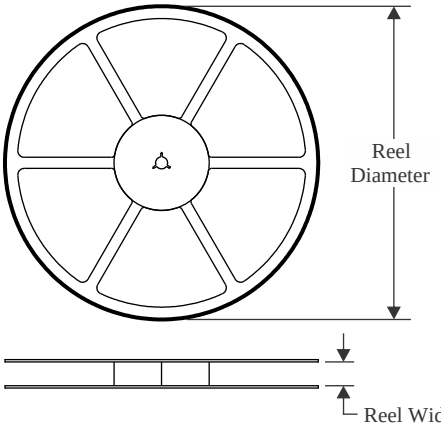
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

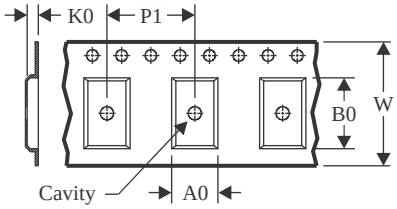
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

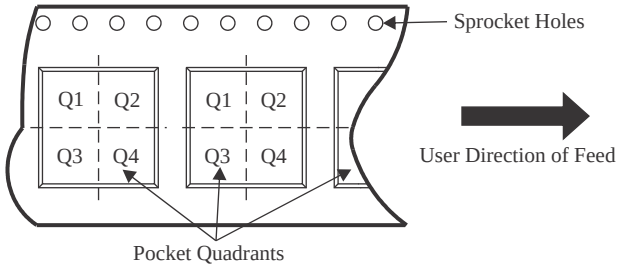


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

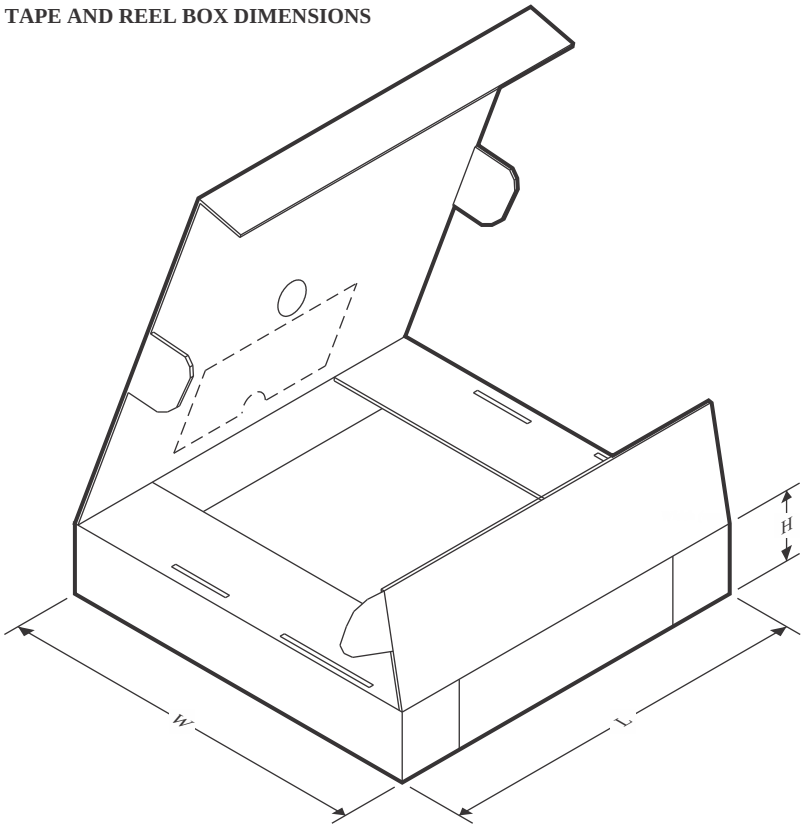
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2596DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2596DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA596DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA596DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

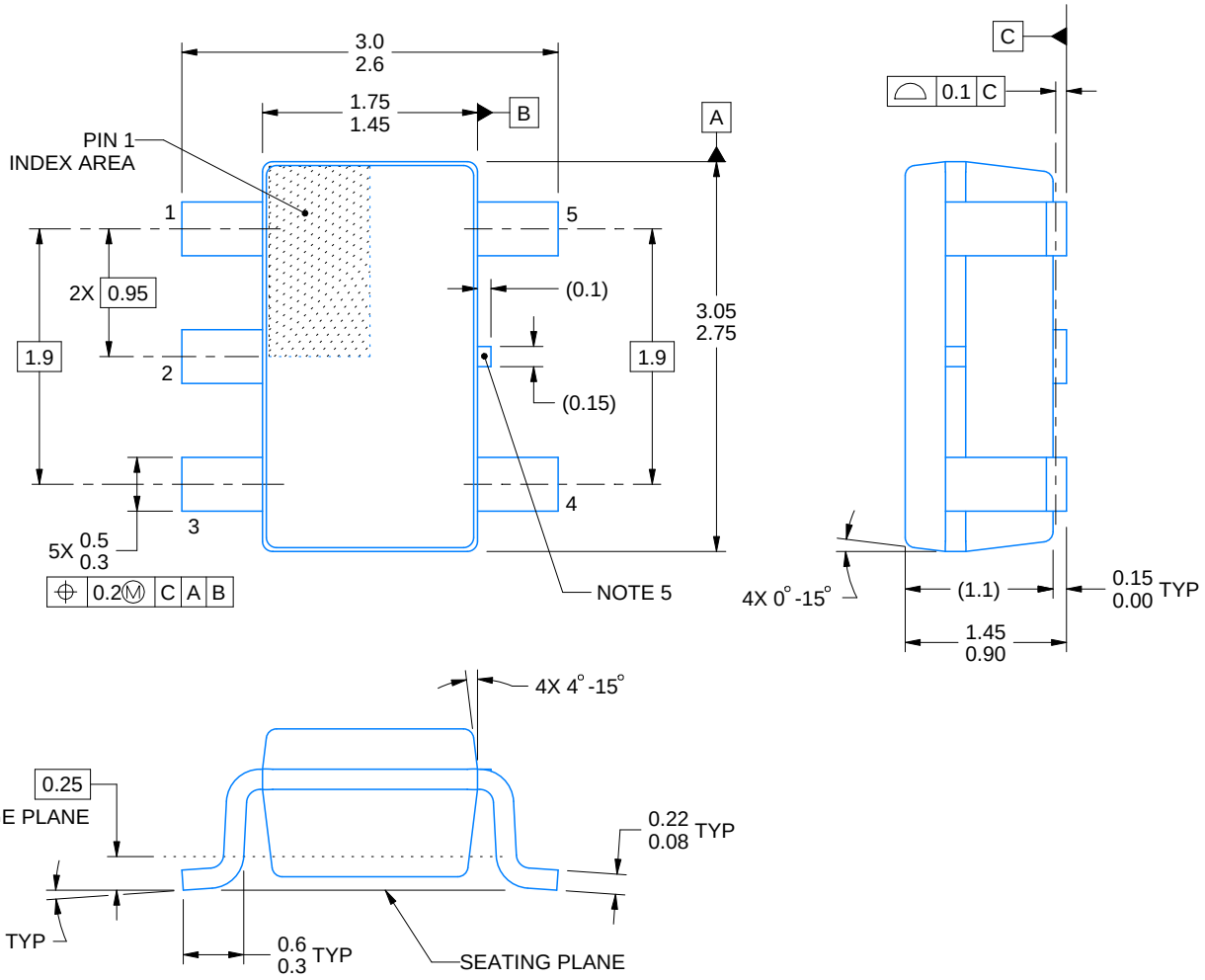
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2596DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2596DR	SOIC	D	8	2500	353.0	353.0	32.0
OPA596DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
OPA596DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

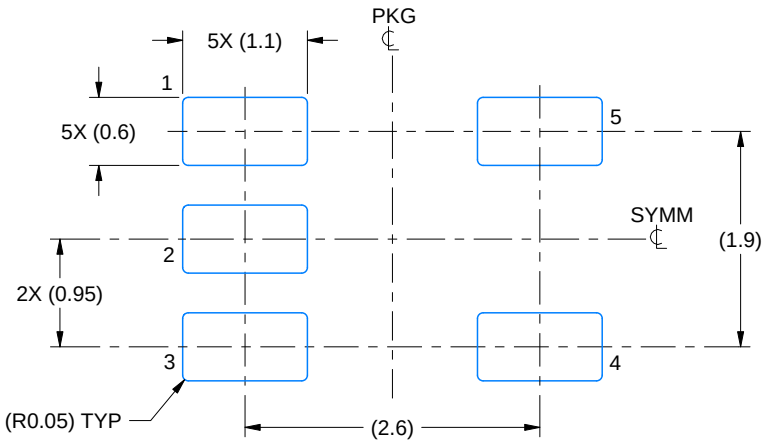
SMALL OUTLINE TRANSISTOR



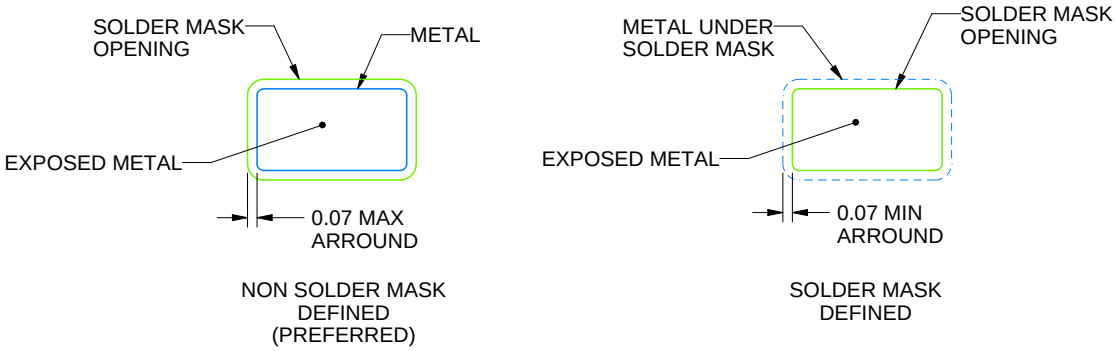
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

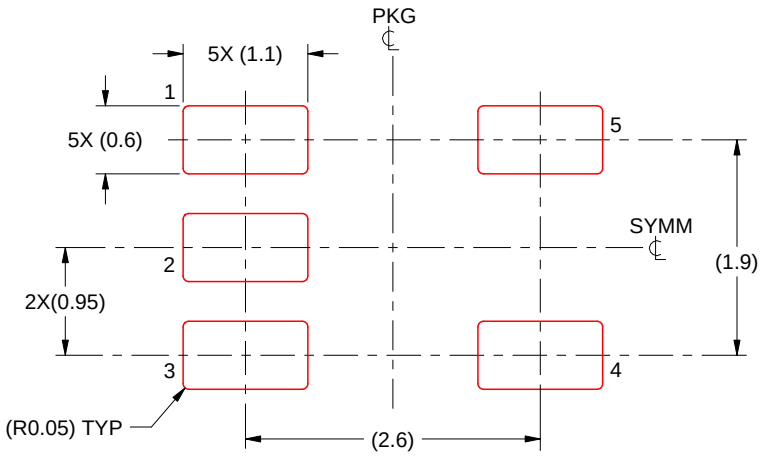


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

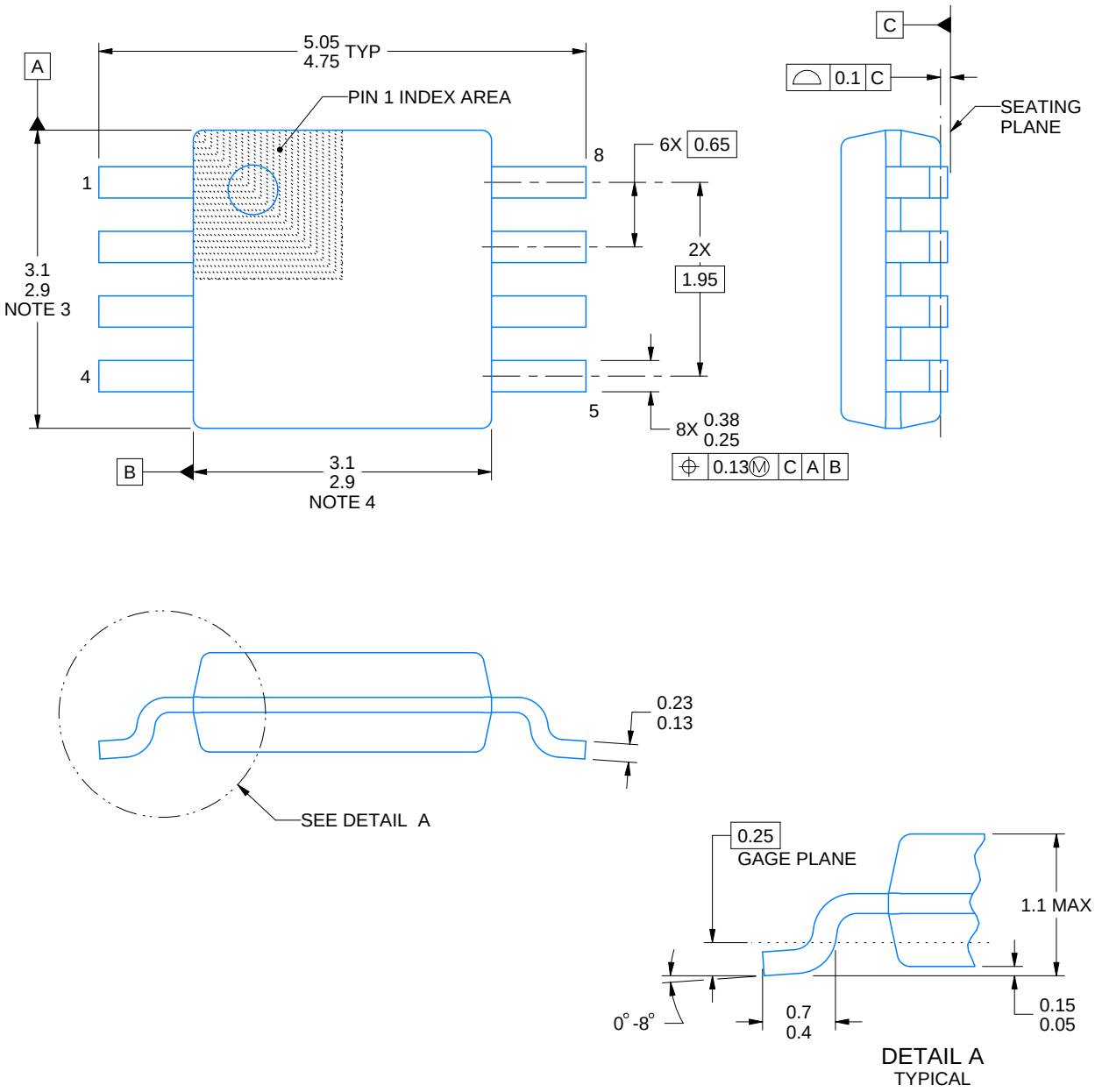
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

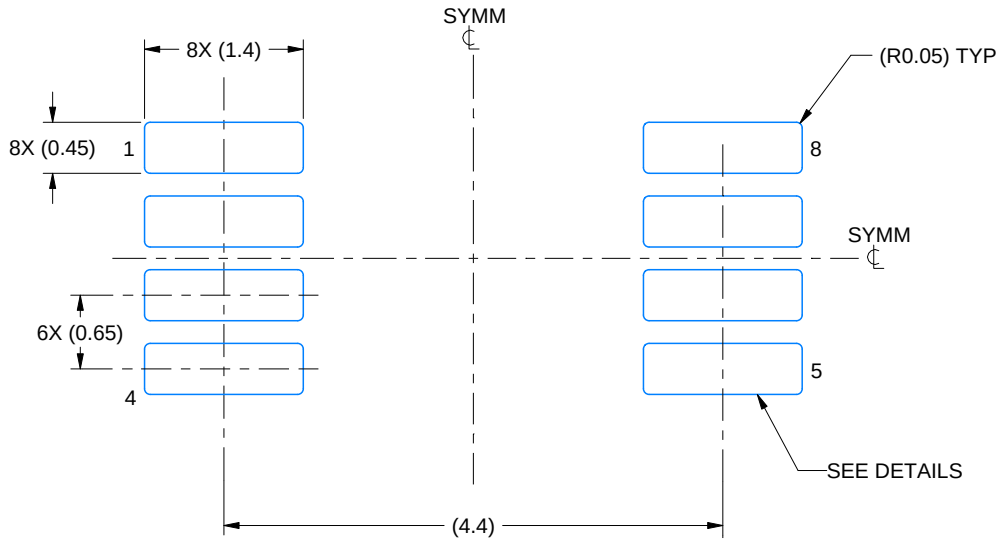
SMALL OUTLINE PACKAGE



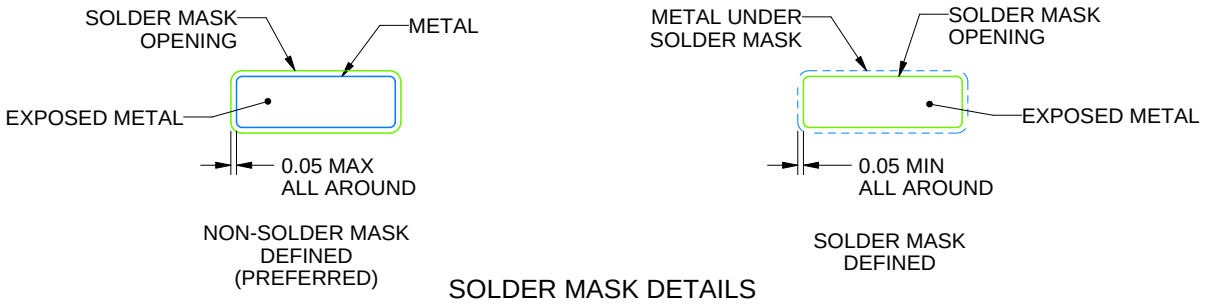
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

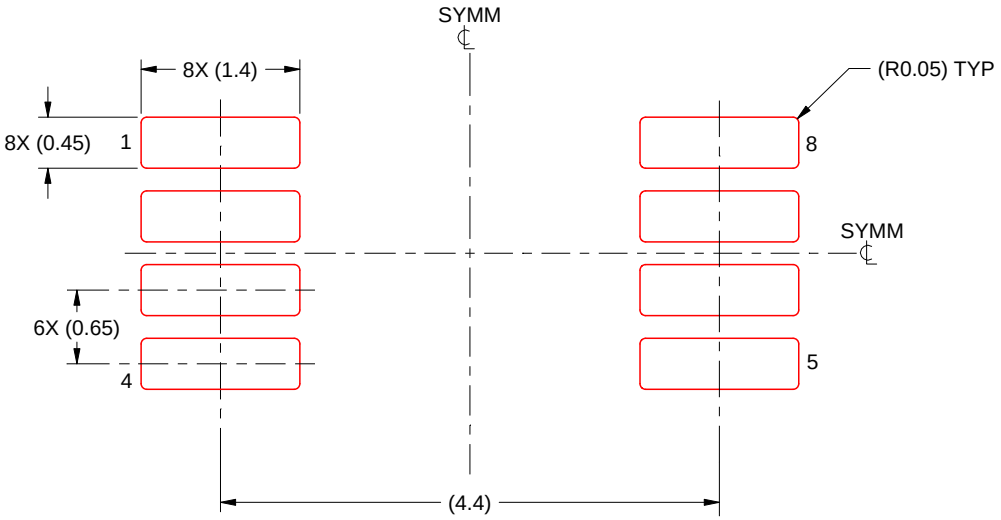


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

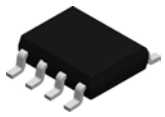


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

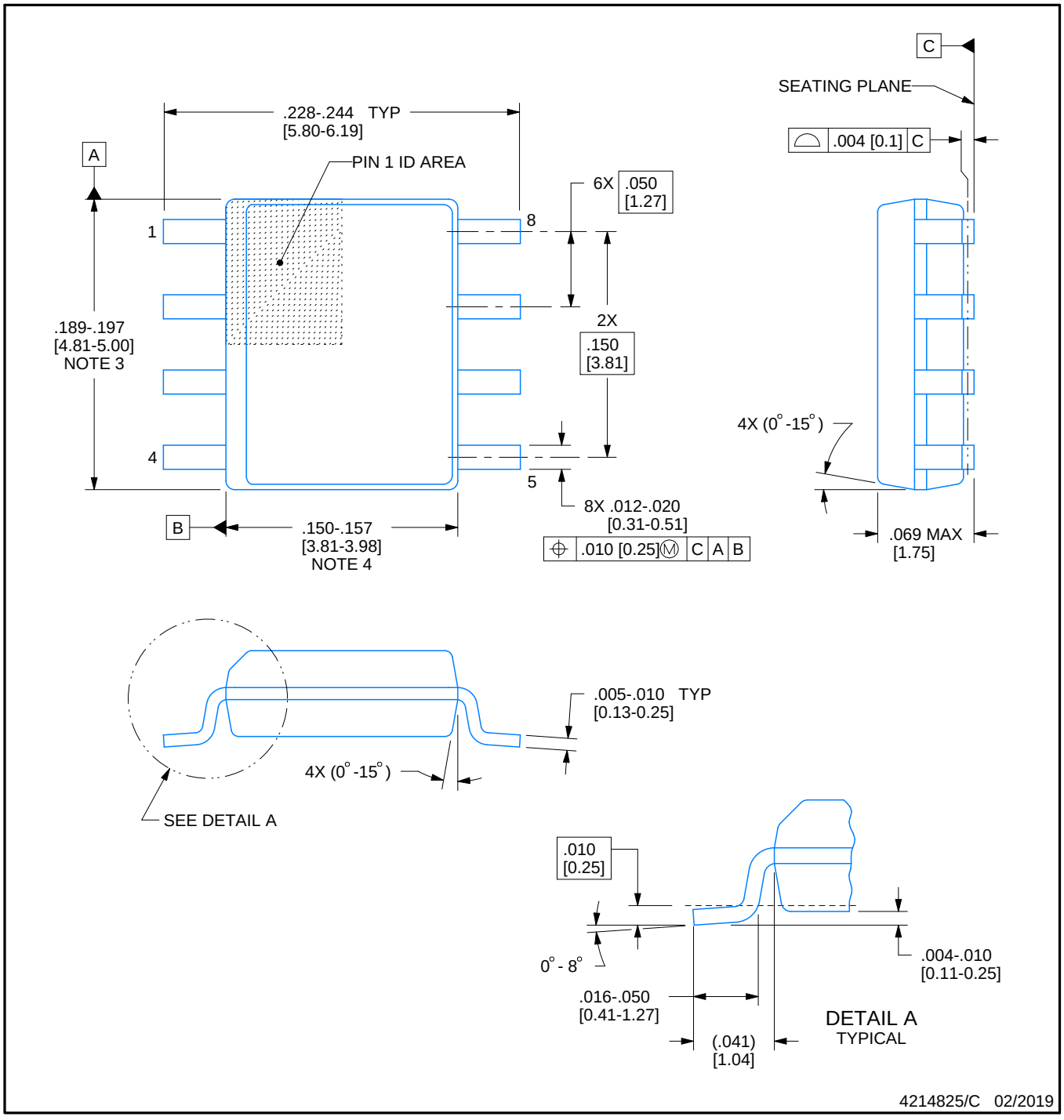


PACKAGE OUTLINE

D0008A

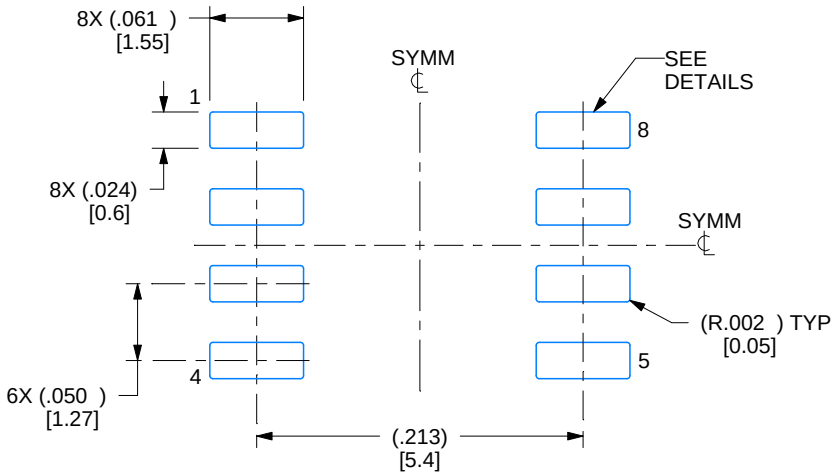
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

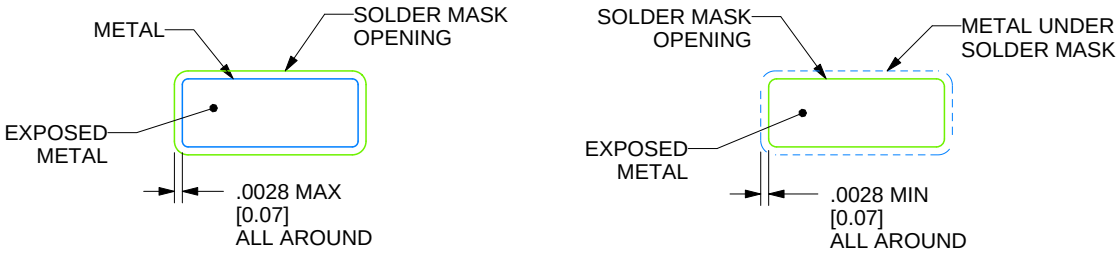


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

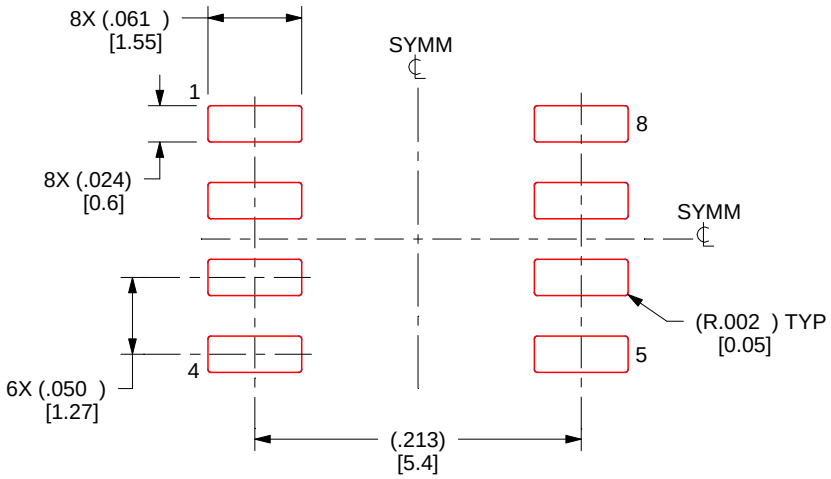
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025