SBAS057A – JANUARY 1996 – REVISED MAY 2007

SoundPLUS™ Stereo Audio DIGITAL-TO-ANALOG CONVERTER With Programmable PLL

FEATURES

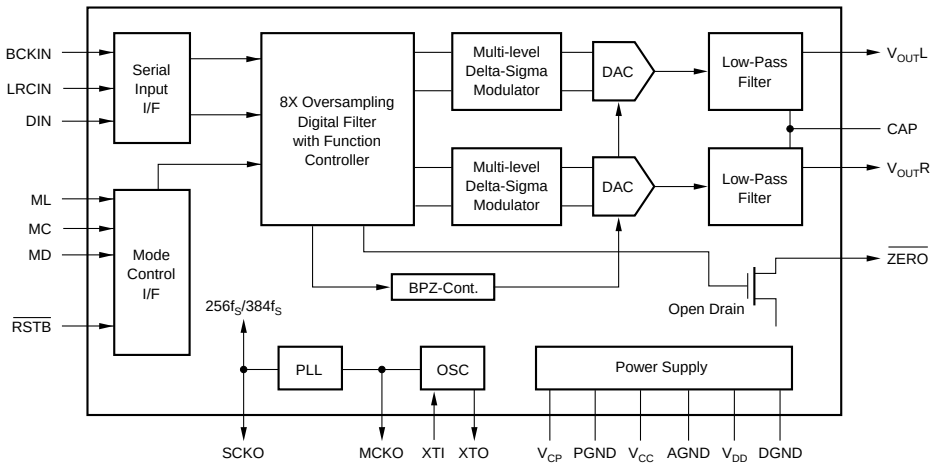
- **ACCEPTS 16-, 20-, OR 24-BIT INPUT DATA**
- **COMPLETE STEREO DAC: Includes Digital Filter and Output Amp**
- **DYNAMIC RANGE: 94dB**
- **MULTIPLE SAMPLING FREQUENCIES:**
  16kHz, 22.05kHz, 24kHz
  32kHz, 44.1kHz, 48kHz
  64kHz, 88.2kHz, 96kHz
- **PROGRAMMABLE PLL CIRCUIT:**
  $256f_S/384f_S$ from 27MHz Master Clock
- **NORMAL OR I²S™ DATA INPUT FORMATS**
- **SELECTABLE FUNCTIONS:**
  Soft Mute
  Digital Attenuator (256 Steps)
  Digital De-emphasis
- **OUTPUT MODE: Left, Right, Mono, Mute**

DESCRIPTION

The PCM1723 is a complete, low-cost, stereo audio digital-to-analog converter (DAC) with a phase-locked loop (PLL) circuit included. The PLL derives either a $256f_S$ or $384f_S$ system clock from an external 27MHz reference frequency. The DAC contains a 3rd-order delta-sigma ($\Delta\Sigma$) modulator, a digital interpolation filter, and an analog output amplifier. The PCM1723 can accept 16-, 20-, or 24-bit input data in either normal or I²S formats.

The digital filter performs an 8X interpolation function and includes selectable features such as soft mute, digital attenuation and digital de-emphasis. The PLL can be programmed for sampling at standard digital audio frequencies as well as one-half and double sampling frequencies.

The PCM1723 is ideal for applications which combine compressed audio and video data such as DVD, DVD-ROM, set-top boxes and MPEG sound cards.



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ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

Power Supply Voltage	+6.5V
$+V_{CC}$ to $+V_{DD}$ Difference	±0.1V
Input Logic Voltage	–0.3V to (V_{DD} + 0.3V)
Input Current (except power supply)	±10mA
Power Dissipation	530mW
Operating Temperature Range	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C
Thermal Resistance, θ_{JA}	+70°C/W

NOTE: (1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

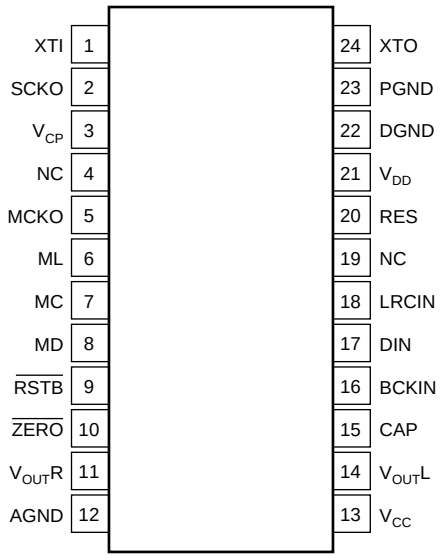
PACKAGE INFORMATION(1)

PRODUCT	PACKAGE	PACKAGE DESIGNATOR
PCM1723E	24-Pin SSOP	DB

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI web site at www.ti.com

PIN CONFIGURATION

TOP VIEW — SSOP



PIN ASSIGNMENTS

PIN	NAME	TYPE	FUNCTION
1	XTI	IN	Master Clock Input.
2	SCKO	OUT	System Clock Out. This output is $256f_S$ or $384f_S$. system clock generated by the internal PLL.
3	V_{CP}	PWR	PLL Power Supply (+5V).
4	NC	N/A	No connection.
5	MCKO	Out	Buffered clock output of crystal oscillator.
6(1)	ML	IN	Latch for serial control data.
7(1)	MC	IN	Clock for serial control data.
8(1)	MD	IN	Data for serial control.
9(1)	$\overline{RSTB}$	IN	Reset Input. When this pin is low, the digital filters and modulators are held in reset.
10	$\overline{ZERO}$	OUT	Zero Data Flag. This pin is low when the input data is continuously zero for more than 65, 535 cycles of BCKIN.
11	$V_{OUT}R$	OUT	Right Channel Analog Output.
12	AGND	GND	Analog Ground.
13	V_{CC}	PWR	Analog Power Supply (+5V).
14	$V_{OUT}L$	OUT	Left Channel Analog Output.
15	CAP		Common pin for analog output amplifiers.
16(2)	BCKIN	IN	Bit clock for clocking in the audio data.
17(2)	DIN	IN	Serial audio data input.
18(2)	LRCIN	IN	Left/Right Word Clock. Frequency is equal to f_S.
19	NC	N/A	No connection.
20	RES	N/A	Reserved for factory use, do not connect.
21	V_{DD}	PWR	Analog Power Supply (+5V).
22	DGND	GND	Digital Ground.
23	PGND	GND	PLL Ground.
24	XTO	Out	Crystal oscillator output.

NOTES: (1) Schmitt trigger input with internal pull-up resistors.
(2) Schmitt triger input.

ELECTRICAL CHARACTERISTICS

All specifications at +25°C, $+V_{CC} = +V_{DD} = +V_{CP} = +5V$, $f_S = 44.1kHz$, and 16-bit input data, SYSCLK = $384f_S$, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1723 MIN	PCM1723 TYP	PCM1723 MAX	UNITS
RESOLUTION		16			Bits
DATA FORMAT					
Audio Data Interface Format			Standard/I²S Selectable		
Data Bit Length			16/20/24 Selectable		
Audio Data Format			MSB First, Binary Two's Complement		
Sampling Frequency (f_S)	Standard f_S	32	44.1	48	kHz
	One-half f_S	16	22.05	24	kHz
	Double f_S	64	88.2	96	kHz
PLL PERFORMANCE					
Master Clock Input Frequency(4)		26.73	27	27.27	MHz
Master Clock Output Frequency		4.096		36.864	MHz
Generated SYSCLK Frequency			$256f_S/384f_S$		
Output Logic Level V_{OH}	$I_{OH} = 2mA$	$V_{DD} – 0.4$			VDC
(MCKO, SCKO) V_{OL}	$I_{OL} = 4mA$			0.5	VDC
Generated SYSCLK Jitter	Standard Dev		±150		ps
Generated SYSCLK Transient(1)	$f_M = 27MHz$			20	ms
Power-Up Time	To Programmed Frequency		15	30	ms
Generated SYSCLK Duty Cycle	$f_M = 27MHz$, $C_L = 15pF$	40	50	60	%
DIGITAL INPUT LOGIC LEVEL			TTL		
DYNAMIC PERFORMANCE(2)					
THD+N at f_S (0dB)	fs = 44.1kHz		–89	–80	dB
	fs = 96kHz		–87		dB
THD+N at –60dB	fs = 44.1kHz		–31		dB
	fs = 96kHz		–29		dB
Dynamic Range (EIAJ Method)	fs = 44.1kHz	90	94		dB
	fs = 96kHz		91		dB
Signal-to-Noise Ratio(3) (EIAJ Method)	fs = 44.1kHz	90	96		dB
	fs = 96kHz		95		dB
Channel Separation	fs = 44.1kHz	88	93		dB
DC ACCURACY					
Gain Error			±1.0	±3.0	% of FSR
Gain Mismatch, Channel-to-Channel			±1.0	±2.0	% of FSR
Bipolar Zero Error	$V_{OUT} = V_{CC}/2$ at BPZ		±30		mV
ANALOG OUTPUT					
Output Voltage	Full Scale (–0dB)		0.62 x V_{CC}		V_{PP}
Center Voltage			$V_{CC}/2$		V_{DC}
Load Impedance	AC Load	5			kΩ
DIGITAL FILTER PERFORMANCE					
Passband				0.445	f_S
Stop Band		0.555			f_S
Passband Ripple				±0.17	dB
Stop Band Attenuation		–35			dB
Delay Time			$11.125/f_S$		sec
De-emphasis Error		–0.2		+0.55	dB
INTERNAL ANALOG FILTER					
–3dB Bandwidth			100		kHz
Passband Response	f = 20kHz		–0.16		dB
POWER SUPPLY REQUIREMENTS					
Voltage Range	$V_{CC} = V_{DD} = V_{CP}$	4.5	5	5.5	VDC
Supply Current: $I_{CC} + I_{DD} + I_{CP}$	$f_S = 44.1kHz$		20	24	mA
TEMPERATURE RANGE					
Operating		–25		+85	°C
Storage		–55		+100	°C

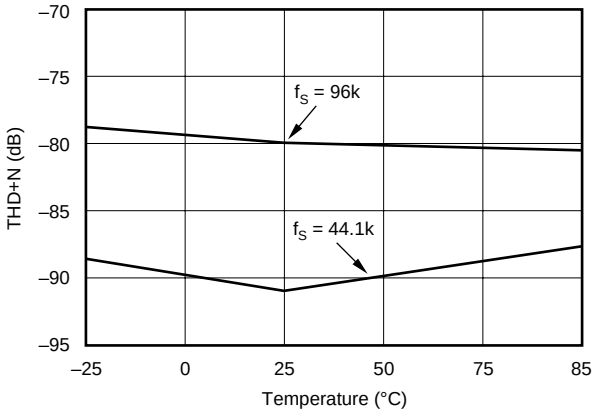
NOTES: (1) Sysclk transient is the maximum frequency lock time when the PLL frequency is changed.
(2) Dynamic performance specs are tested with 20kHz low pass filter and THD+N specs are tested with 30kHz LPF, 400Hz HPF, Average-Mode.
(3) SNR is tested at Infinite Zero Detection off.
(4) PLL evaluations tested with 1ns maximum jitter on the 27MHz input clock.

TYPICAL CHARACTERISTICS

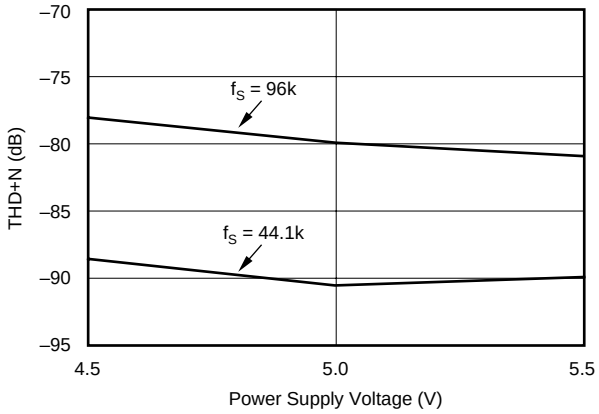
At T_A = +25°C, V_{CC} = V_{DD} = V_{CP} = +5V, f_S = 44.1kHz, 16-bit input data, 384f_S, unless otherwise noted. Measurement bandwidth is 20kHz.

DYNAMIC PERFORMANCE

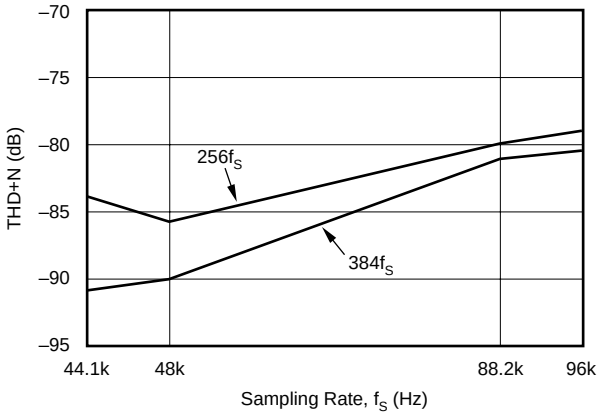
THD+N (0dB) vs TEMPERATURE and
V_{CC} = 5V, 384f_S



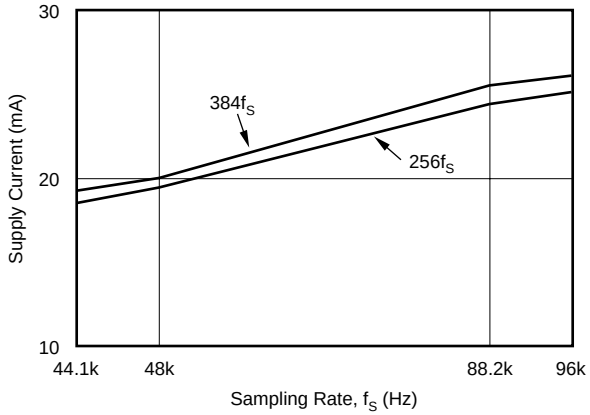
THD+N (0dB) vs POWER SUPPLY VOLTAGE
T_A = 25°C, 384f_S



THD+N (0dB) vs SAMPLING RATE (f_S)
V_{CC} = 5V, T_A = 25°C



POWER SUPPLY CURRENT vs SAMPLING RATE (f_S)
V_{CC} = 5V, T_A = 25°C

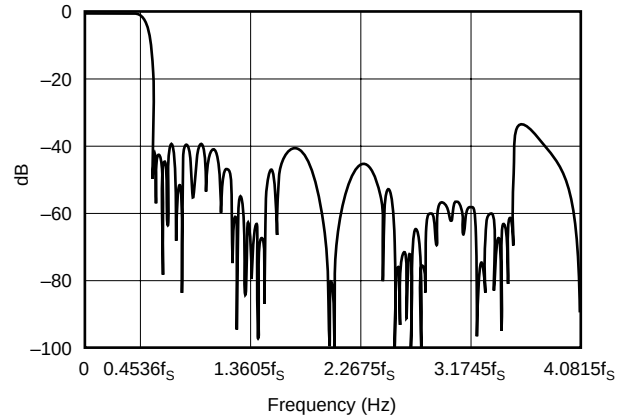


TYPICAL CHARACTERISTICS (Cont.)

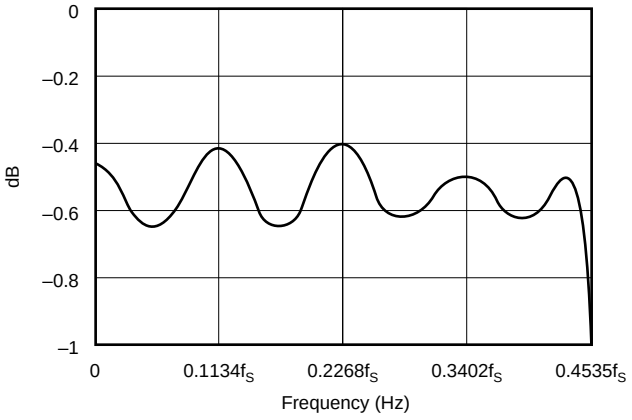
At T_A = +25°C, V_S = +5V, R_L = 44.1kHz, and f_{SYS} = 384f_S, unless otherwise noted.

DIGITAL FILTER

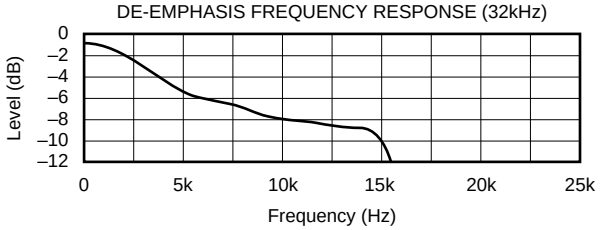
OVERALL FREQUENCY CHARACTERISTIC



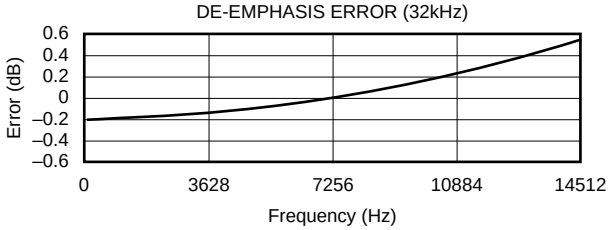
PASSBAND RIPPLE CHARACTERISTIC



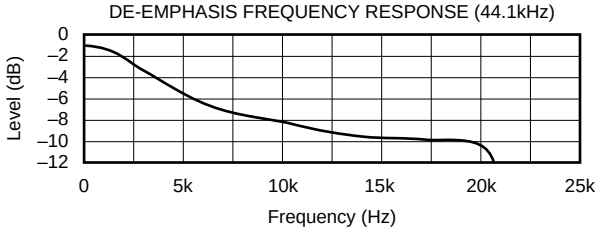
DE-EMPHASIS FREQUENCY RESPONSE (32kHz)



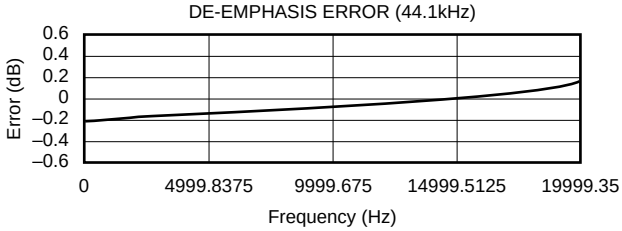
DE-EMPHASIS ERROR (32kHz)



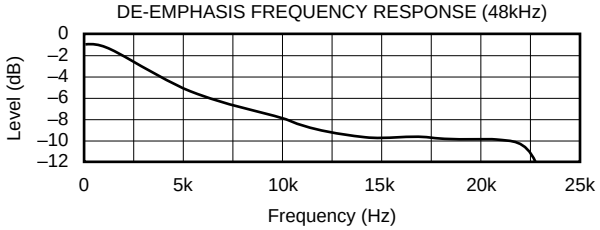
DE-EMPHASIS FREQUENCY RESPONSE (44.1kHz)



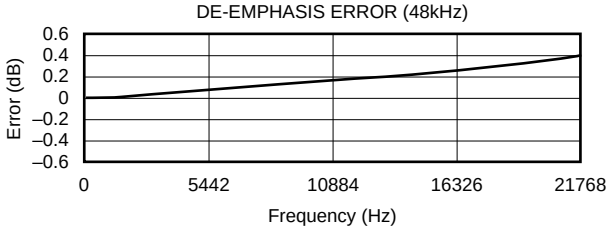
DE-EMPHASIS ERROR (44.1kHz)



DE-EMPHASIS FREQUENCY RESPONSE (48kHz)



DE-EMPHASIS ERROR (48kHz)



TYPICAL CONNECTION DIAGRAM

Figure 1 illustrates the typical connection diagram for the PCM1723 in an MPEG-2 application. The 27MHz master video clock (f_M) drives XTI (pin 1) of the PCM1723. A programmable system clock is generated by the PCM1723 PLL, with SCKO used to drive the MPEG-2 decoder system clock input. The standard audio signals (data, bit clock, and word clock) are generated in the decoder from the PCM1723 system clock, providing synchronization of audio and video signals.

PLL CIRCUIT

The PCM1723 has a programmable internal PLL circuit, as shown in Figure 2. The PLL is designed to accept a 27MHz master clock or crystal oscillator and generate all internal system clocks required to operate the digital filter and ΔΣ modulator, either at $256f_S$ or $384f_S$. If an external master clock is used, XTO must be connected to GND. In both cases, the signal amplitude on XTI must satisfy the specification described in Figure 3. Therefore, careful C1 and C2 determination is required to keep this specification satisfied when

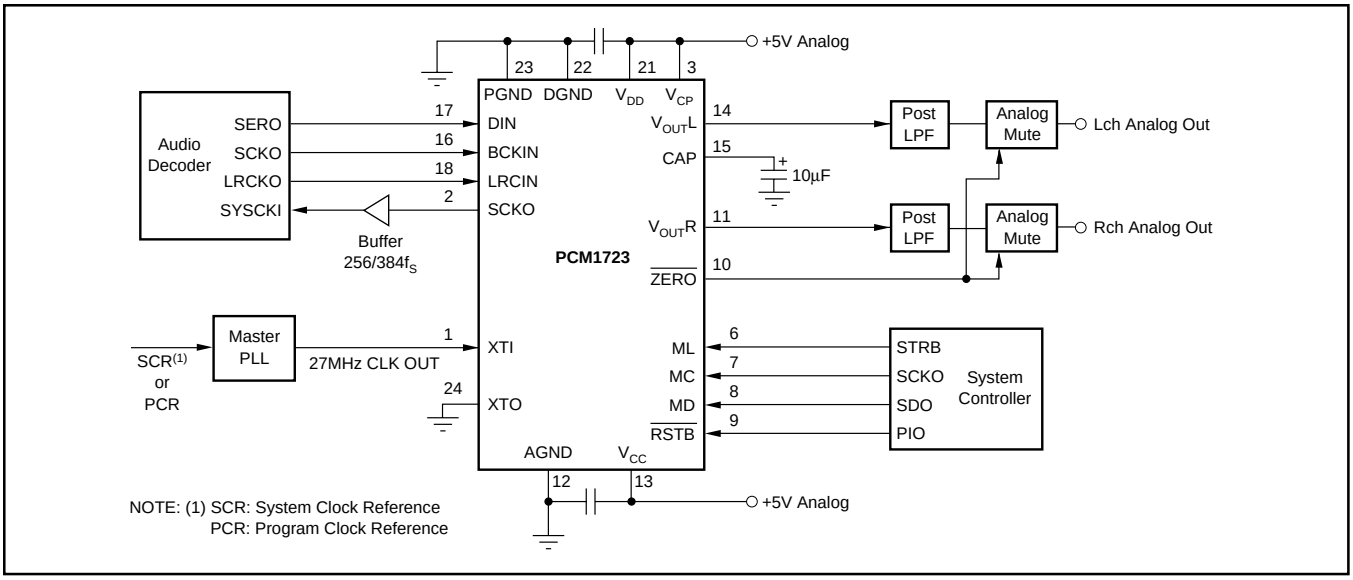


FIGURE 1. Connection Diagram for External Master Clock in a Typical MPEG-2 Application.

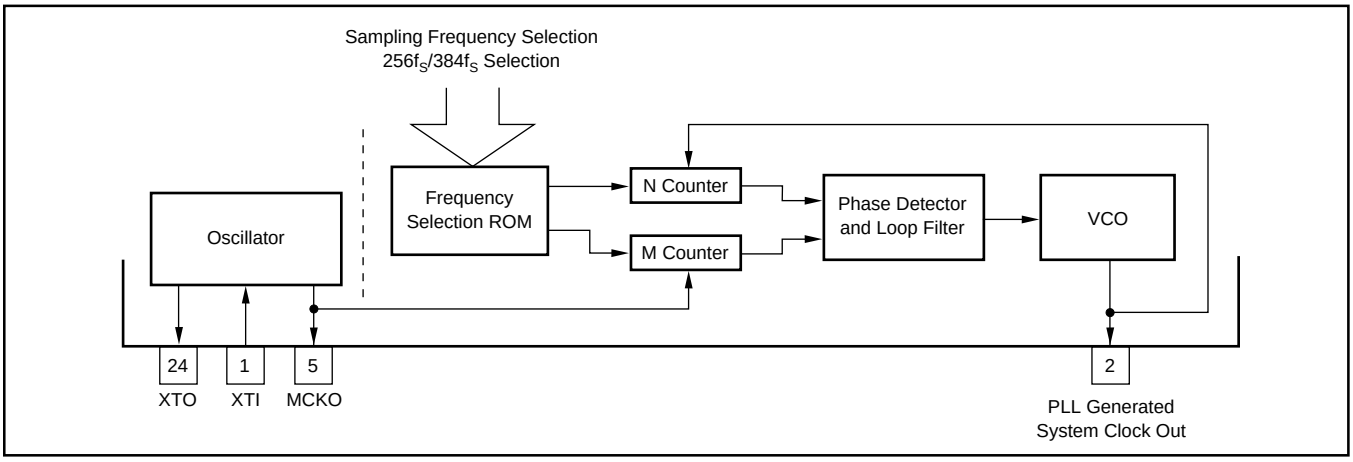


FIGURE 2. PLL Block Diagram.

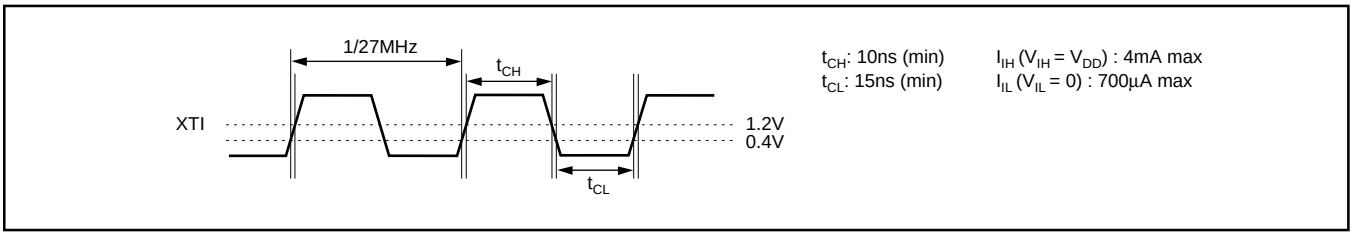


FIGURE 3. XTI Input Timing.

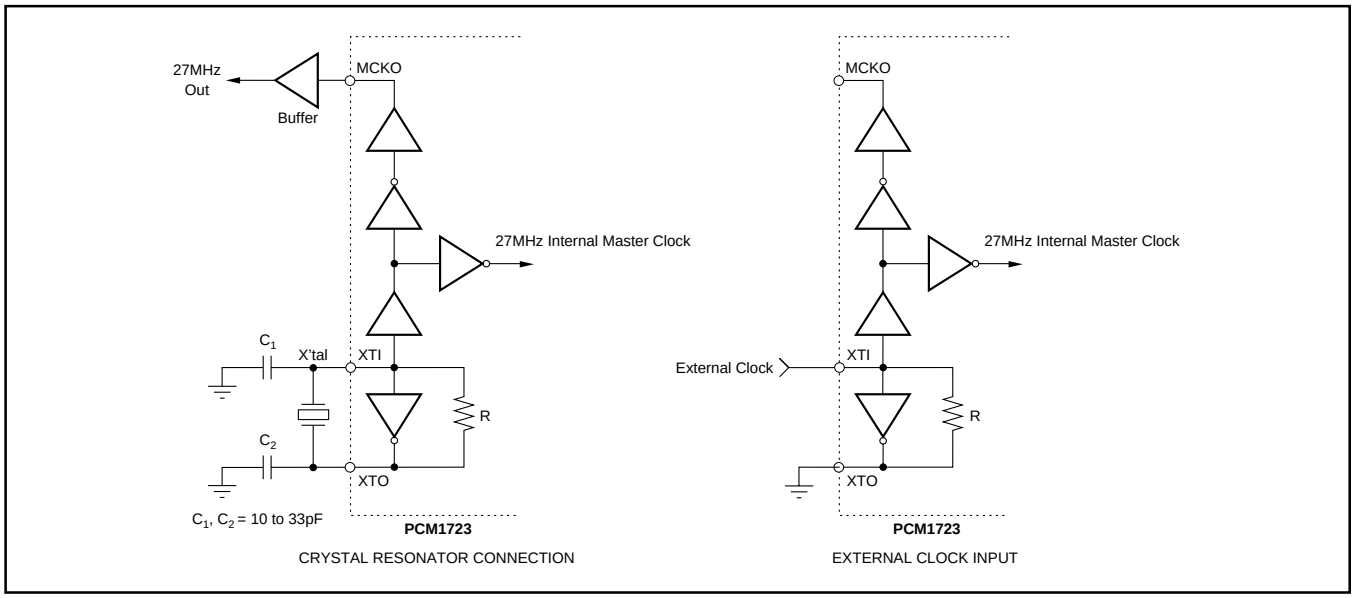


FIGURE 4. System Clock Connection.

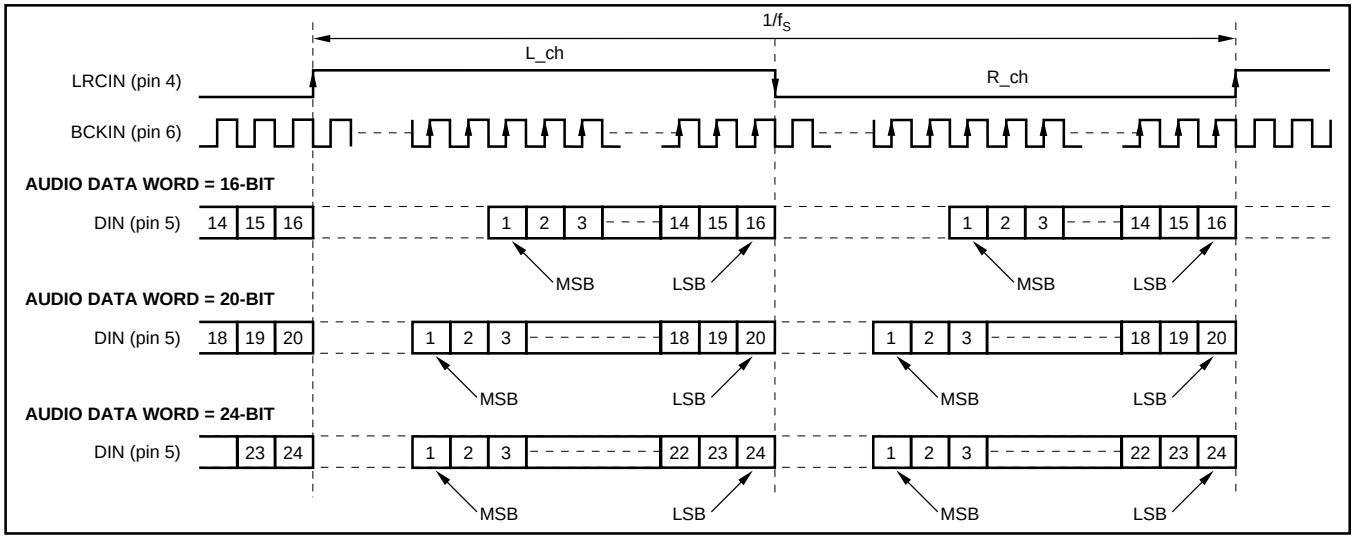


FIGURE 5. Normal Data Input Timing.

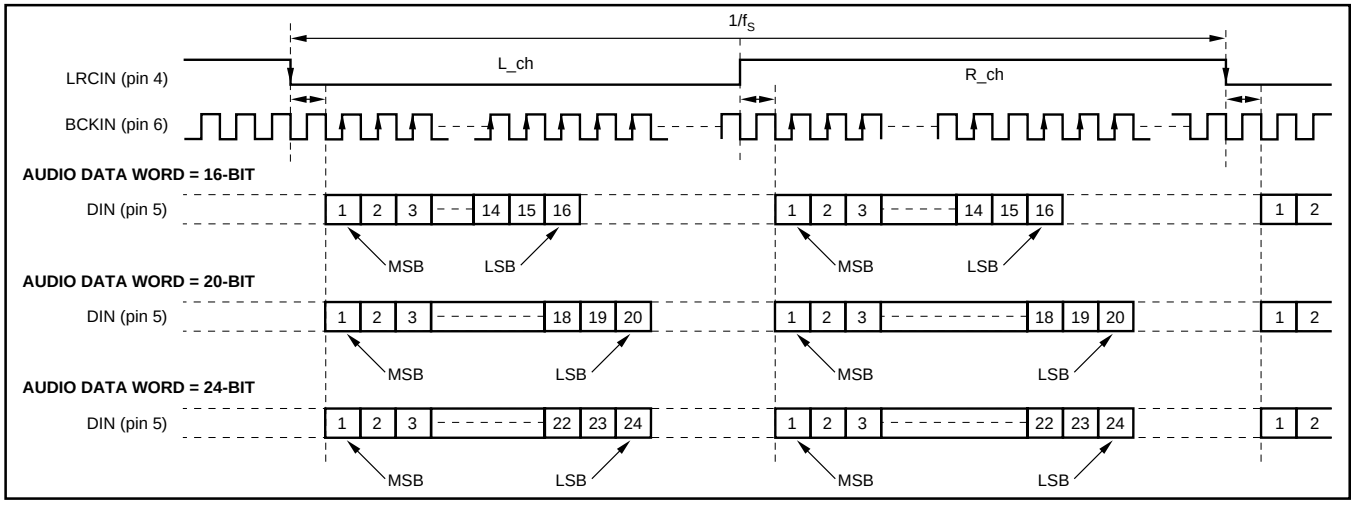
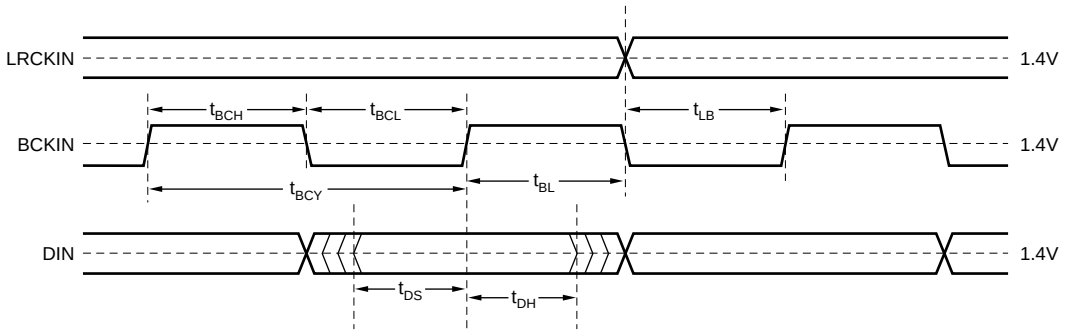


FIGURE 6. I²S Data Input Timing.



BCKIN Pulse Cycle Time	: t_{BCY}	: 100ns (min)
BCKIN Pulse Width High	: t_{BCH}	: 50ns (min)
BCKIN Pulse Width Low	: t_{BCL}	: 50ns (min)
BCKIN Rising Edge to LRCIN Edge	: t_{BL}	: 30ns (min)
LRCIN Edge to BCKIN Rising Edge	: t_{LB}	: 30ns (min)
DIN Set-up Time	: t_{DS}	: 30ns (min)
DIN Hold Time	: t_{DH}	: 30ns (min)

FIGURE 7. Audio Data Input Timing.

using a crystal oscillator. The PLL will directly track any variations in the master clock frequency, and jitter on the system clock is specified at 250ps maximum. Figure 3 illustrates the timing requirements for the 27MHz master clock. Figure 4 illustrates the system clock connections for an external clock or crystal oscillator.

The PCM1723 internal PLL can be programmed for nine different sampling frequencies (LRCIN), as shown in Table I. The internal sampling clocks generated by the various programmed frequencies are shown in Table II. The system clock output frequency for the PCM1723 is 100% accurate. To provide MCKO clock and SCKO clock for external circuit, external buffer circuit is effective to avoid degrading audio performance.

	Sampling Frequencies-LRCIN (kHz)		
Half of Standard Sampling Freq	16	22.05	24
Standard Sampling Freq	32	44.1	48
Double of Standard Sampling Freq	64	88.2	96

TABLE I. Sampling Frequencies.

Sampling Frequency (LRCIN)		System Clock $256f_S$	System Clock $384f_S$
16kHz	Half	4.096MHz	6.144MHz
32kHz	Standard	8.192MHz	12.288MHz
64kHz	Double	16.384MHz	24.576MHz
22.05kHz	Half	5.6448MHz	8.4672MHz
44.1kHz	Standard	11.2896MHz	16.9344MHz
88.2kHz	Double	22.5792MHz	33.8688MHz
24kHz	Half	6.144MHz	9.216MHz
48kHz	Standard	12.288MHz	18.432MHz
96kHz	Double	24.576MHz	36.864MHz

TABLE II. Sampling Frequencies vs Internal System Clock (= Output Frequencies of PLL).

SPECIAL FUNCTIONS

The PCM1723 includes several special functions, including digital attenuation, digital de-emphasis, soft mute, data format selection and input word resolution. These functions are controlled using a three-wire interface. MD (pin 8) is used for the program data, MC (pin 7) is used to clock in the program data, and ML (pin 6) is used to latch in the program data. Table III lists the selectable special functions.

FUNCTION	DEFAULT MODE
Input Audio Data Format Selection Normal Format I^2S Format	Normal Format
Input Audio Data Bit Selection 16/20/24 Bits	16 Bits
Input LRCIN Polarity Selection Lch/Rch = High/Low Lch/Rch = Low/High	Lch/Rch = High/Low
De-emphasis Control	OFF
Soft Mute Control	OFF
Attenuation Control Lch, Rch Individually Lch, Rch Common	0dB Lch, Rch Individually Fixed
Infinite Zero Detection Circuit Control	OFF
Operation Enable (OPE)	Enabled
Sample Rate Selection Internal System Clock Selection $256f_S$ $384f_S$	$384f_S$
Double Sampling Rate Selection Standard Sampling Rate—44.1/48/32kHz Double Sampling Rate—88.2/96/32kHz Half Sampling Rate—22.05/24/16kHz	Standard Sampling Rate
Sampling Frequency 44.1kHz Group 48kHz Group 32kHz Group	44.1kHz
Analog Output Mode L, R, Mono, Mute	Stereo

TABLE III. Selectable Functions.

MAPPING OF PROGRAM REGISTERS

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
MODE0	res	res	res	res	res	A1	A0	LDL	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0
MODE1	res	res	res	res	res	A1	A0	LDR	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
MODE2	res	res	res	res	res	A1	A0	PL3	PL2	PL1	PL0	IW1	IW0	OPE	DEM	MUT
MODE3	res	res	res	res	res	A1	A0	IZD	SF1	SF0	DSR1	DSR0	SYS	ATC	LRP	I^2S

PROGRAM REGISTER BIT MAPPING

The PCM1723 special functions are controlled using four program registers that are 16 bits long. These registers are all loaded using MD. After the 16 data bits are clocked in, ML is used to latch in the data to the appropriate register. Table IV shows the complete mapping of the four registers and Figure 8 illustrates the serial interface timing.

REGISTER NAME	BIT NAME	DESCRIPTION
Register 0	AL (7:0)	DAC Attenuation Data for Lch
	LDL	Attenuation Data Load Control for Lch
	A (1:0)	Register Address
	Res	Reserved
Register 1	AR (7:0)	DAC Attenuation Data for Rch
	LDL	Attenuation Data Load Control for Rch
	A (1:0)	Register Address
	Res	Reserved
Register 2	MUT	Left and Right DACs Soft Mute Control
	DEM	De-emphasis Control
	OPE	Left and Right DACs Operation Control
	IW (1:0)	Input Audio Data Bit Select
	PL (3:0)	Output Mode Select
	A (1:0)	Register Address
	res	Reserved
Register 3	I^2S	Audio Data Format Select
	LRP	Polarity of LRCIN (pin 7) Select
	ATC	Attenuator Control
	SYS	System Clock Select
	DSR (1:0)	Double Sampling Rate Select
	SF (1:0)	Sampling Rate Select
	IZD	Infinite Zero Detection Circuit Control
	A (1:0)	Register Address
	Res	Reserved

TABLE IV. Internal Register Mapping.

REGISTER 0 (A1 = 0, A0 = 0)

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	LDL	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0

Register 0 is used to control left channel attenuation. Bits 0 - 7 (AL0 - AL7) are used to determine the attenuation level. The level of attenuation is given by:

$$ATT = [20 \log10 (ATT\_DATA/255)] \text{ dB}$$

ATTENUATION DATA LOAD CONTROL

Bit 8 (LDL) is used to control the loading of attenuation data in B0:B7. When LDL is set to 0, attenuation data will be loaded into AL0:AL7, but it will not affect the attenuation level until LDL is set to 1. LDR in Register 1 has the same function for right channel attenuation.

Attenuation Level (ATT) can be controlled as following Resistor set AL (R) (7:0).

AL (R) (7:0)	ATT LEVEL
00h	–∞dB (Mute)
01h	–48.16dB
.	.
.	.
.	.
FEh	–0.07dB
FFh	0dB

REGISTER 1 (A1 = 0, A0 = 1)

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	LDR	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0

Register 1 is used to control right channel attenuation. As in Register 1, bits 0 - 7 (AR0 - AR7) control the level of attenuation.

REGISTER 2 (A1 = 1, A0 = 0)

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	PL3	PL2	PL1	PL0	IW1	IW0	OPE	DEM	MUTE

Register 2 is used to control soft mute, de-emphasis, operation enable, input resolution, and output format. Bit 0 is used for soft mute: a HIGH level on bit 0 will cause the output to be muted (this is ramped down in the digital domain, so no *click* is audible). Bit 1 is used to control de-emphasis. A LOW level on bit 1 disables de-emphasis, while a HIGH level enables de-emphasis.

Bit 2 (OPE) is used for operational control. Table V illustrates the features controlled by OPE.

	DATA INPUT	DAC OUTPUT	SOFTWARE MODE INPUT
OPE = 1	Zero	Forced to BPZ(1)	Enabled
	Other	Forced to BPZ(1)	Enabled
OPE = 0	Zero	Controlled by IZD	Enabled
	Other	Normal	Enabled
NOTE: (1) $\Delta\Sigma$ is disconnected from output amplifier.			

TABLE V. Operation Enable (OPE) Function.

OPE controls the operation of the DAC: when OPE is LOW, the DAC will convert all non-zero input data. If the input data is continuously zero for 65,536 cycles of BCKIN, the output will be forced to zero only if IZD is HIGH. When OPE is HIGH, the output of the DAC will be forced to bipolar zero, irrespective of any input data.

	DATA INPUT	DAC OUTPUT
IZD = 1	Zero	Forced to BPZ(1)
	Other	Normal
IZD = 0	Zero	Zero(2)
	Other	Normal

NOTES: (1) ΔΣ is disconnected from output amplifier.
(2) ΔΣ is connected to output amplifier.

TABLE VI. Infinite Zero Detection (IZD) Function.

	DATA INPUT	DAC OUTPUT	SOFTWARE MODE INPUT
RSTB = HIGH	Zero	Controlled by OPE and IZD	Enabled
	Other	Controlled by OPE and IZD	Enabled
RSTB = LOW	Zero	Forced to BPZ(1)	Disabled
	Other	Forced to BPZ(1)	Disabled

NOTE: (1) ΔΣ is disconnected from output amplifier.

TABLE VII. Reset (RSTB) Function.

Bits 3 (IW0) and 4 (IW1) are used to determine input word resolution. PCM1723 can be set up for input word resolutions of 16, 20, or 24 bits:

Bit 4 (IW1)	Bit 3 (IW0)	Input Resolution
0	0	16-bit Data Word
0	1	20-bit Data Word
1	0	24-bit Data Word
1	1	Reserved

Bits 5, 6, 7, and 8 (PL0:3) are used to control output format. The output of PCM1723 can be programmed for 16 different states, as shown in Table VIII.

PL0	PL1	PL2	PL3	Lch OUTPUT	Rch OUTPUT	NOTE
0	0	0	0	MUTE	MUTE	MUTE
0	0	0	1	MUTE	R	
0	0	1	0	MUTE	L	
0	0	1	1	MUTE	(L + R)/2	
0	1	0	0	R	MUTE	
0	1	0	1	R	R	
0	1	1	0	R	L	REVERSE
0	1	1	1	R	(L + R)/2	
1	0	0	0	L	MUTE	
1	0	0	1	L	R	STEREO
1	0	1	0	L	L	
1	0	1	1	L	(L + R)/2	
1	1	0	0	(L + R)/2	MUTE	
1	1	0	1	(L + R)/2	R	
1	1	1	0	(L + R)/2	L	
1	1	1	1	(L + R)/2	(L + R)/2	MONO

TABLE VIII. Programmable Output Format.

REGISTER 3 (A1 = 1, A0 = 1)

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	IZD	SF1	SF0	DSR1	DSR0	SYS	ATC	LRP	I²S

Register 3 is used to control input data format and polarity, attenuation channel control, system clock frequency, sampling frequency, and infinite zero detection.

Bits 0 (I^2S) and 1 (LRP) are used to control the input data format. A LOW on bit 0 sets the format to Normal (MSB-first, right-justified Japanese format), and a HIGH sets the format to I^2S (Philips serial data protocol). Bit 1 (LRP) is used to select the polarity of LRCIN (sample rate clock). When bit 1 is LOW, left channel data are assumed when LRCIN is in a HIGH phase and right channel data are assumed when LRCIN is in a LOW phase. When bit 1 is HIGH, the polarity assumption is reversed.

Bit 2 (ATC) is used for controlling the attenuator. When bit 2 is HIGH, the attenuation data loaded in program Register 0 are used for both left and right channels. When bit 2 is LOW, the attenuation data for each register are applied separately to left and right channels.

Bit 3 (SYS) is the system clock selection. When bit 3 is LOW, the system clock frequency is set to $384f_S$. When bit 3 is HIGH, the system clock frequency is set to $256f_S$.

Bits 4 (DSR0) and 5 (DSR1) are used to control multiples of the sampling rate:

DSR1	DSR0	Multiple	
0	0	Normal	32/44.1/48kHz
0	1	Double	64/88.2/96kHz
1	0	One-half	16/22.05/24kHz
1	1	Reserved	Not Defined

Bits 6 (SF0) and 7 (SF1) are used to select the sampling frequency. Frequency selection must be made with an interval time greater than 20μs.

SF1	SF0	Sampling Frequency	
0	0	44.1kHz group	22.05/44.1/88.2kHz
0	1	48kHz group	24/48/96kHz
1	0	32kHz group	16/32/64kHz
1	1	Reserved	Not Defined

Bit 8 is used to control the infinite zero detection function (IZD).

When IZD is LOW, the zero detect circuit is off. Under this condition, no automatic muting will occur if the input is continuously zero. When IZD is HIGH, the zero detect feature is enabled. If the input data are continuously zero for 65,536 cycles of BCKIN, the output will be immediately forced to a bipolar zero state ($V_{CC}/2$). The zero detection feature is used to avoid noise which may occur when the input is DC. When the output is forced to bipolar zero, there may be an audible click. PCM1723 allows the zero detect feature to be disabled so the user can implement an external muting circuit.

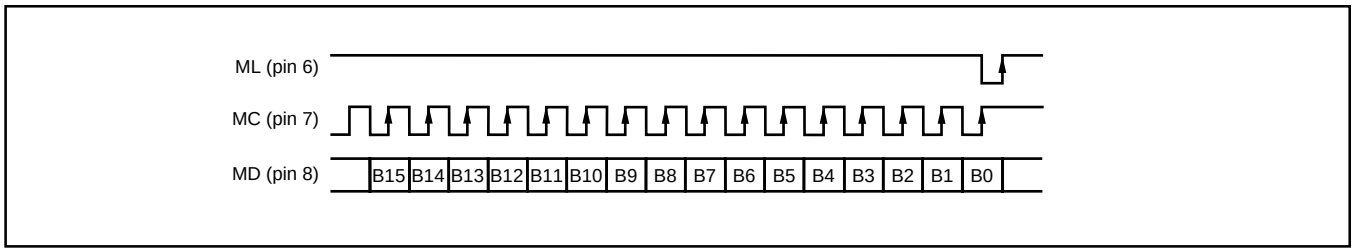
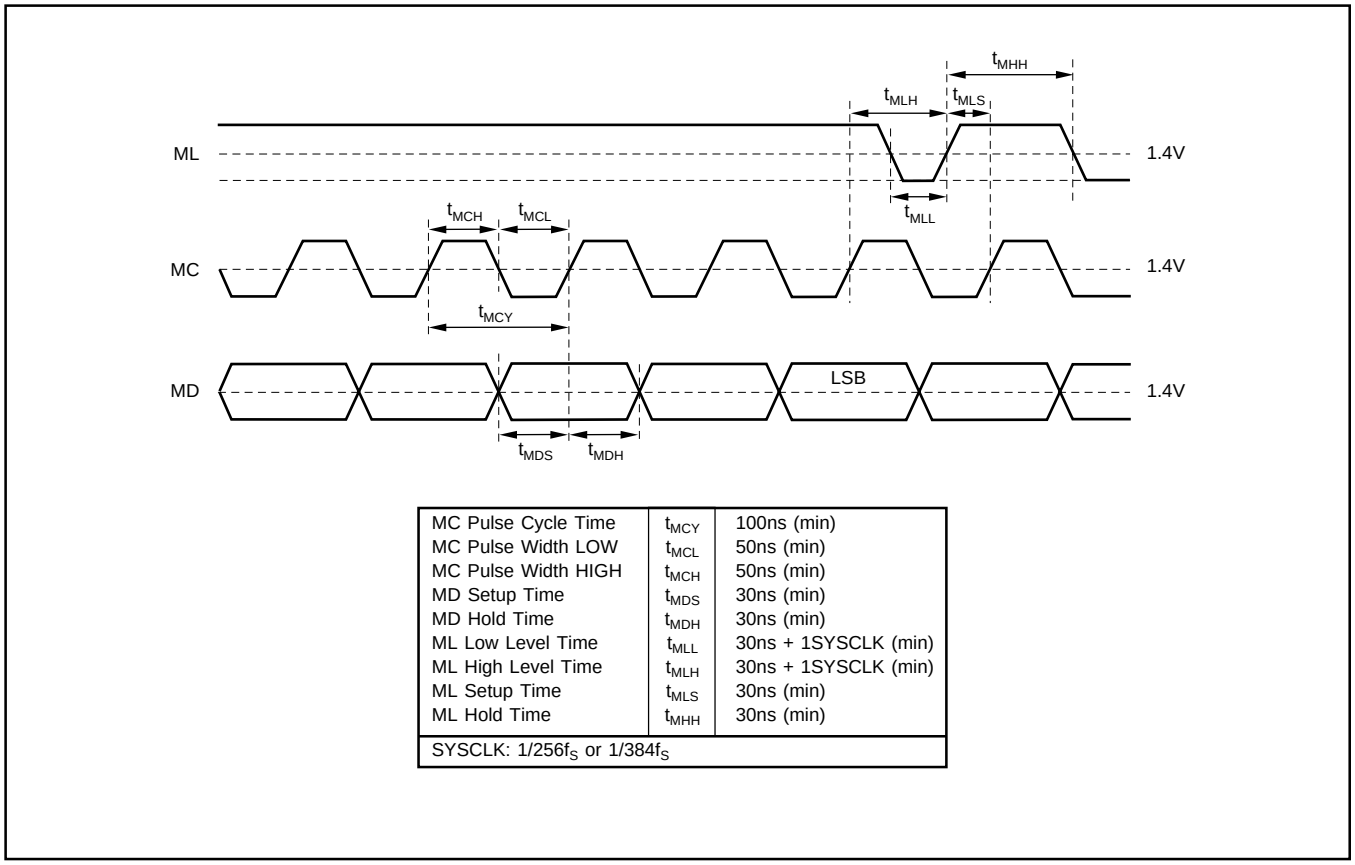


FIGURE 8. Three-Wire Serial Interface.



MC Pulse Cycle Time	t_{MCY}	100ns (min)
MC Pulse Width LOW	t_{MCL}	50ns (min)
MC Pulse Width HIGH	t_{MCH}	50ns (min)
MD Setup Time	t_{MDS}	30ns (min)
MD Hold Time	t_{MDH}	30ns (min)
ML Low Level Time	t_{MLL}	30ns + 1SYSCLK (min)
ML High Level Time	t_{MLH}	30ns + 1SYSCLK (min)
ML Setup Time	t_{MLS}	30ns (min)
ML Hold Time	t_{MHH}	30ns (min)
SYSCLK: $1/256f_S$ or $1/384f_S$		

FIGURE 9. Program Register Input Timing.

APPLICATION CONSIDERATIONS

DELAY TIME

There is a finite delay time in delta-sigma converters. In analog-to-digital converters (ADCs), this is commonly referred to as latency. For a delta-sigma DAC, delay time is determined by the order number of the FIR filter stage, and the chosen sampling rate. The following equation expresses the delay time of PCM1723:

$$t_D = 11.125 \times 1/f_S$$

For f_S = 44.1kHz, t_D = 11.125/44.1kHz = 251.4µs

Applications using data from a disc or tape source, such as CD audio, CD-Interactive, Video CD, DAT, Minidisc, etc., generally are not affected by delay time. For some professional applications such as broadcast audio for studios, it is important for total delay time to be less than 2ms.

OUTPUT FILTERING

For testing purposes all dynamic tests are done on the PCM1723 using a 20kHz low-pass filter. This filter limits the measured bandwidth for THD+N, etc. to 20kHz. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the specifications. The low-pass filter removes out of band noise. Although it is not audible, it may affect dynamic specification numbers.

The performance of the internal low-pass filter from DC to 24kHz is shown in Figure 10. The higher frequency rolloff of the filter is shown in Figure 11. If an application has the PCM1723 driving a wideband amplifier, it is recommended to use an external low-pass filter. A simple 3rd-order filter is shown in Figure 12. For some applications, a passive RC filter or 2nd-order filter may be adequate.

Reset

The PCM1723 has both internal power-on reset circuit and the $\overline{\text{RSTB}}$ pin (pin 9) that accepts an external forced reset by $\overline{\text{RSTB}}$ = LOW. For internal power on reset, initialize (reset) is done automatically at power on V_{DD} >2.2V (typ). During internal reset = LOW, the output of the DAC is invalid and the analog outputs are forced to $V_{CC}/2$. Figure 13 illustrates the timing of internal power on reset.

The PCM1723 accepts an external forced reset when $\overline{\text{RSTB}}$ = L. During $\overline{\text{RSTB}}$ = L, the output of the DAC is invalid and the analog outputs are forced to $V_{CC}/2$ after internal initialize (1024 system clocks count after $\overline{\text{RSTB}}$ = H). Figure 14 illustrates the timing of $\overline{\text{RSTB}}$ pin reset.

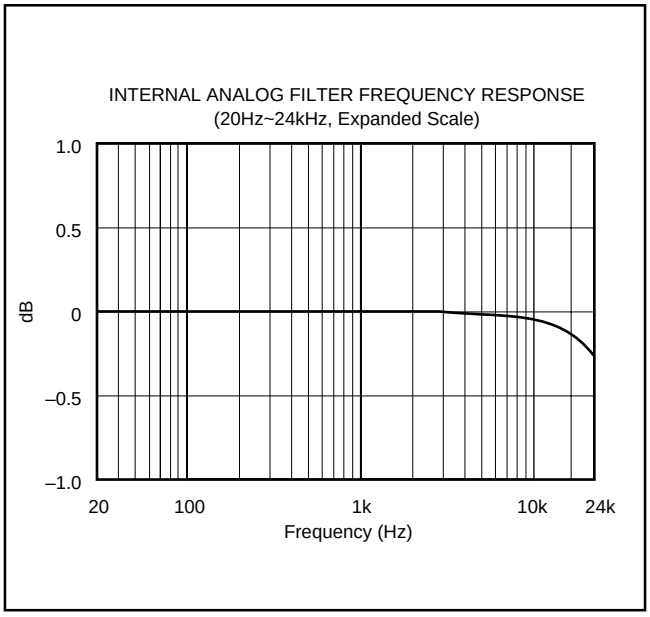


FIGURE 10. Low-Pass Filter Frequency Response.

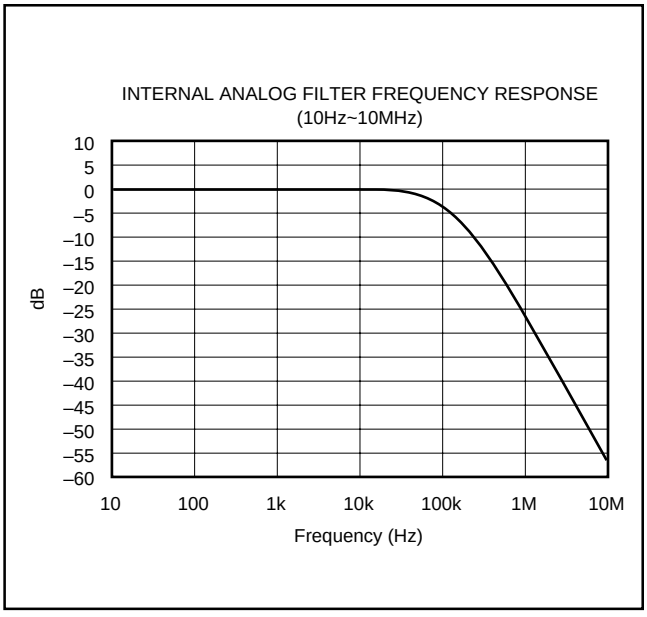


FIGURE 11. Low-Pass Filter Wideband Frequency Response.

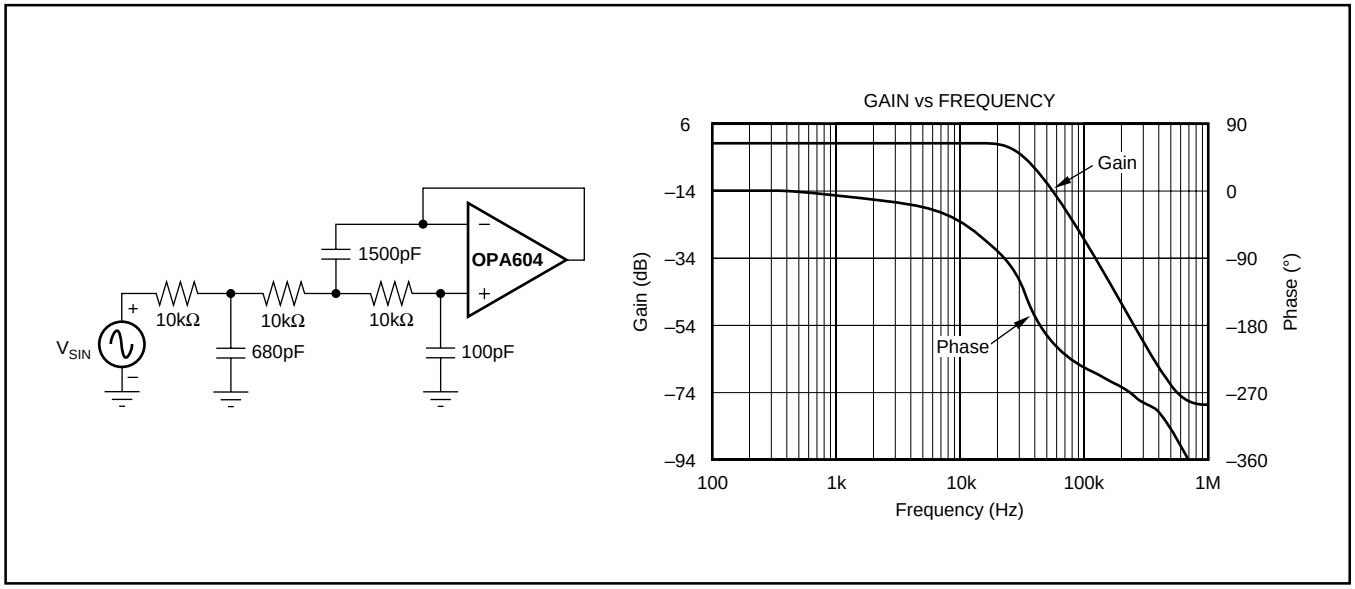


FIGURE 12. 3rd-Order Low-Pass Filter.

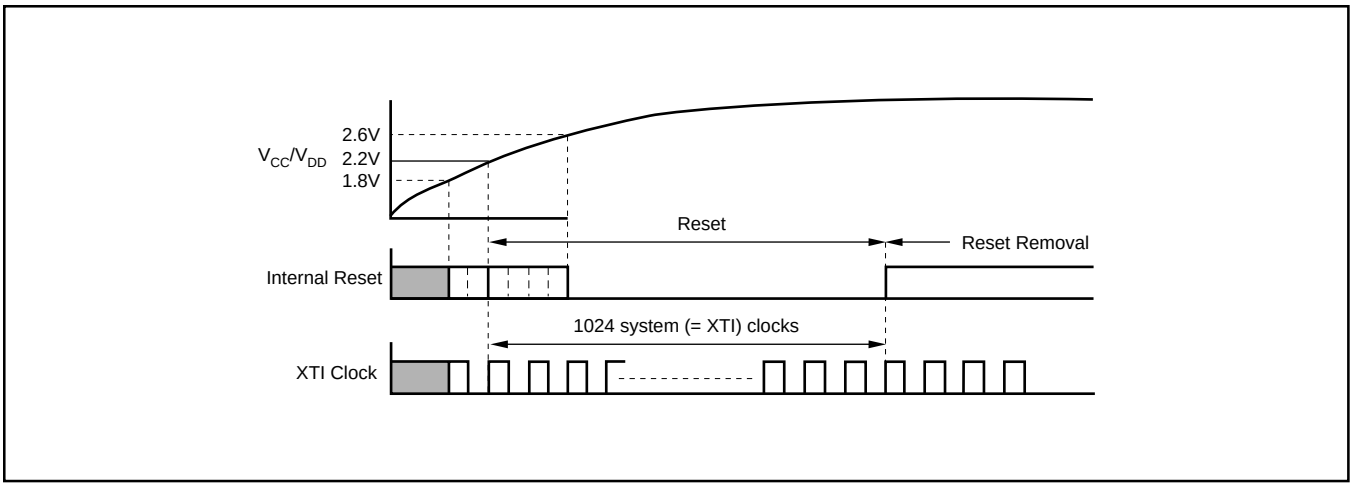


FIGURE 13. Internal Power-On Reset Timing.

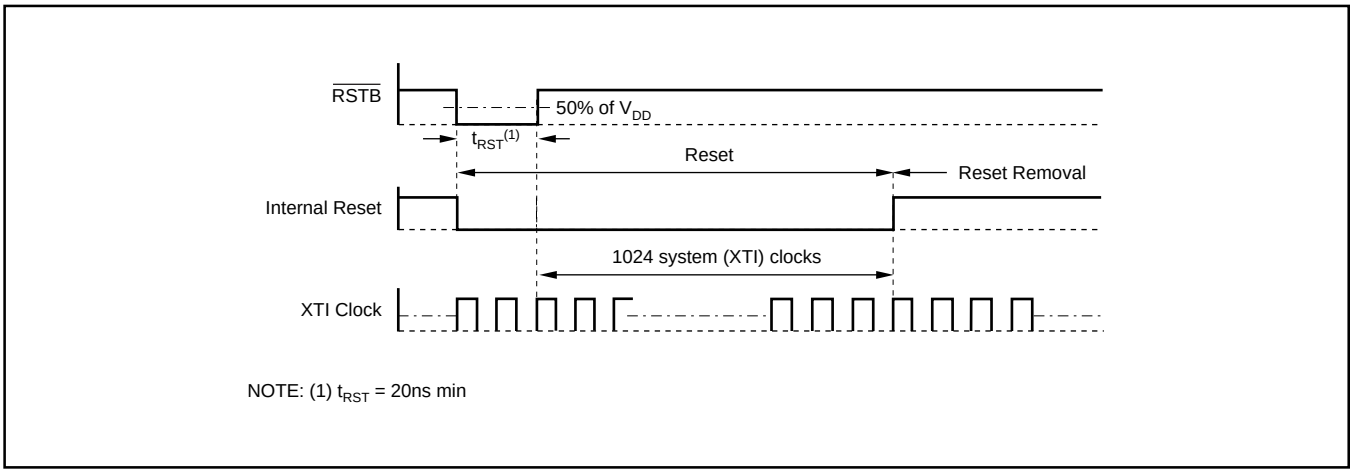


FIGURE 14. RSTB-Pin Reset Timing.

POWER SUPPLY CONNECTIONS

The PCM1723 has three power supply connections: digital (V_{DD}), analog (V_{CC}), and PLL (V_{CP}). Each connection also has a separate ground return pin. It is acceptable to use a common +5V power supply for all three power pins. If separate supplies are used without a common connection, the delta between the supplies during ramp-up time must be less than 0.6V. An application circuit to avoid a power-on latch-up condition is shown in Figure 15.

BYPASSING POWER SUPPLIES

The power supplies should be bypassed as close as possible to the unit. Refer to Figure 18 for optimal values of bypass capacitors. It is also recommended to include a 0.1µF ceramic capacitor in parallel with the 10µF tantalum capacitor.

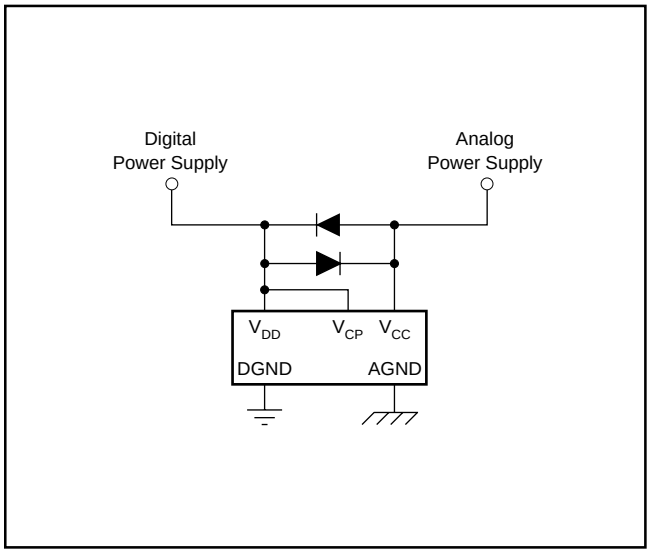


FIGURE 15. Latch-up Prevention Circuit.

THEORY OF OPERATION

The delta-sigma section of the PCM1723 is based on a 5-level amplitude quantizer and a 3rd-order noise shaper. This section converts the oversampled input data to 5-level delta-sigma format.

A block diagram of the 5-level delta-sigma modulator is shown in Figure 16. This 5-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2 level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the internal 8X interpolation filter is $48f_S$ for a $384f_S$ system clock, and $64f_S$ for a $256f_S$ system clock. The theoretical quantization noise performance of the 5-level delta-sigma modulator is shown in Figure 17.

Multi Level Delta Sigma

AC-3 APPLICATION CIRCUIT

A typical application for the PCM1723 is AC-3 5.1 channel audio decoding and playback. This circuit uses the PCM1723 to develop the audio system clock from the 27MHz video clock, with the SCKO pin used to drive the AC-3 decoder and two PCM1720 units, the non-PLL version of the PCM1723.

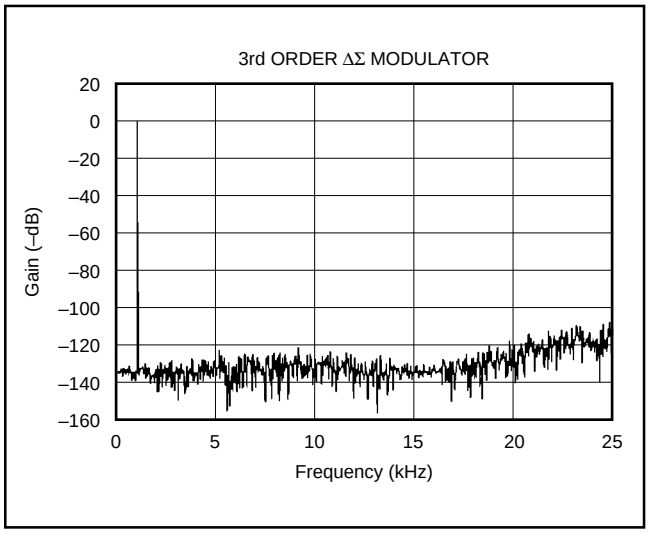


FIGURE 17. Quantization Noise Spectrum.

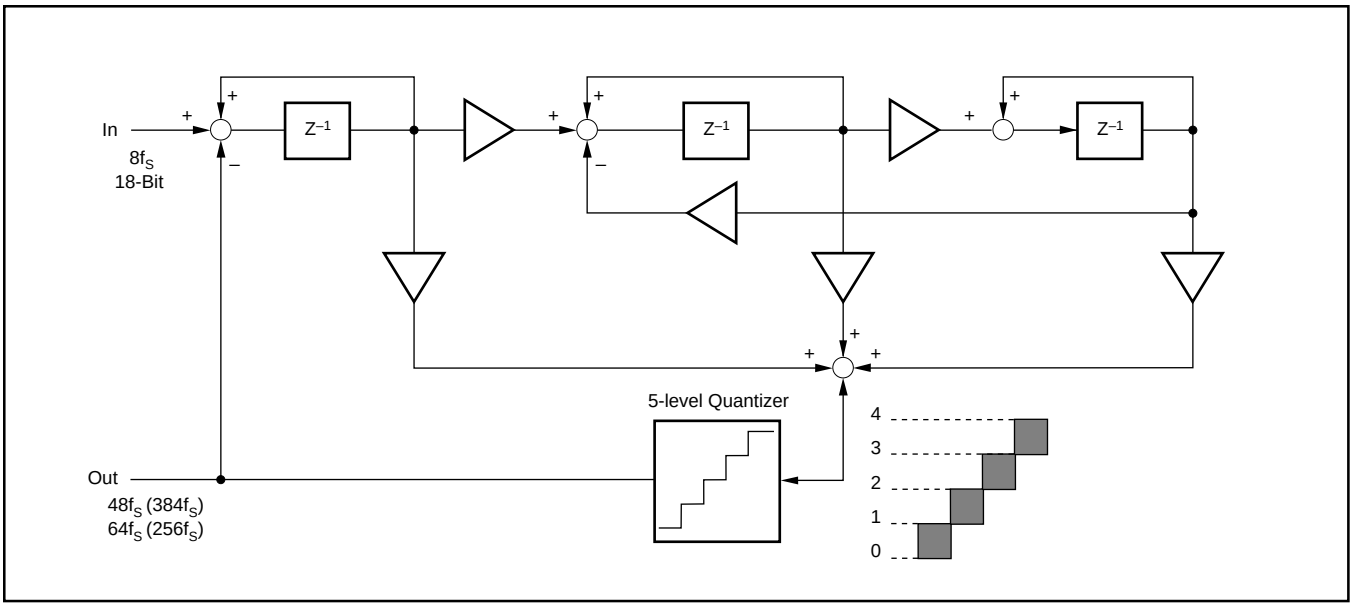


FIGURE 16. 5-Level ΔΣ Modulator Block Diagram.

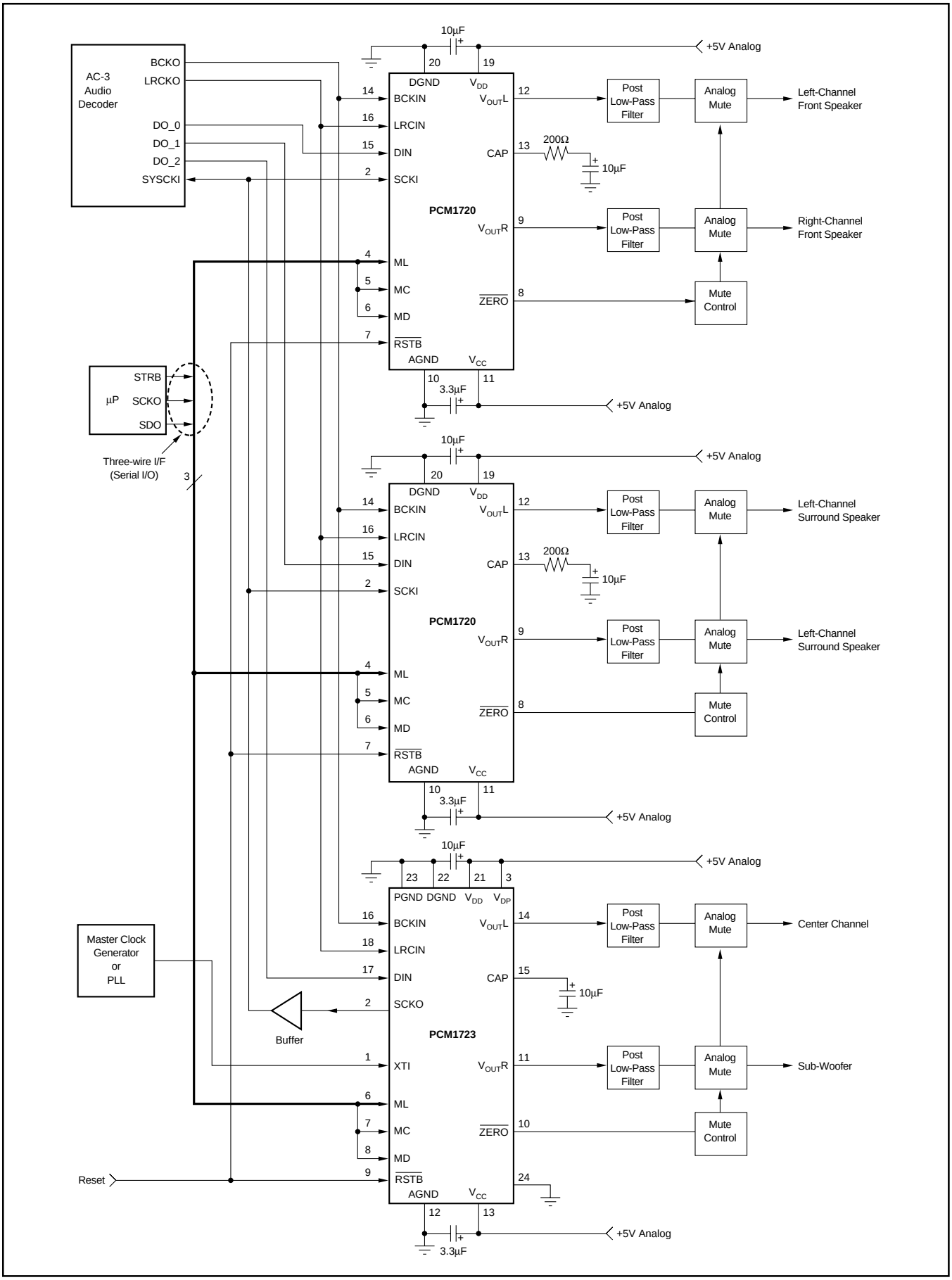


FIGURE 18. Connection Diagram for a 6-Channel AC-3 Application.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
5/07	A	—	Entire Document	Updated format and added missing overbars to RSTB and ZERO pins.
		2	Electrical Characteristics	Added "Selectable" to *Audio Data Interface Format* typical value column.
				Deleted "Selectable" from *Audio Data Format* unit column.
		6	PLL Circuit	Changed "XTO should be connected" to "XTO must be connected."
				Added sentence regarding XTI signal amplitude and C1, C2 determination.
			Figure 3	Changed 2.0V/0.8V to 1.2V/0.4V.
		8	PLL Circuit	Deleted paragraph regarding frequency error.
		10	Register 3	Added sentence to Bit 6 regarding interval time must be greater than 20µs.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCM1723E	Last Time Buy	Production	SSOP (DB) | 24	58 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM1723E
PCM1723E.B	Last Time Buy	Production	SSOP (DB) | 24	58 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM1723E
PCM1723E/2K	Last Time Buy	Production	SSOP (DB) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM1723E
PCM1723E/2K.B	Last Time Buy	Production	SSOP (DB) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM1723E

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

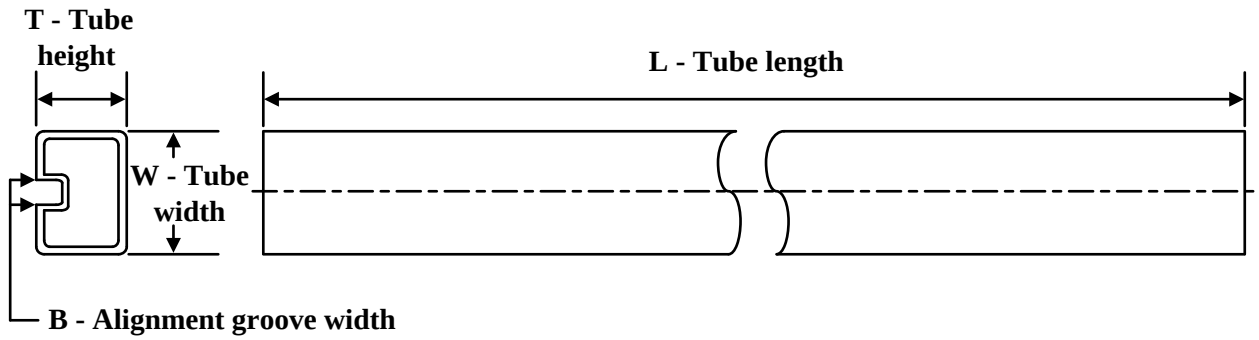
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TUBE



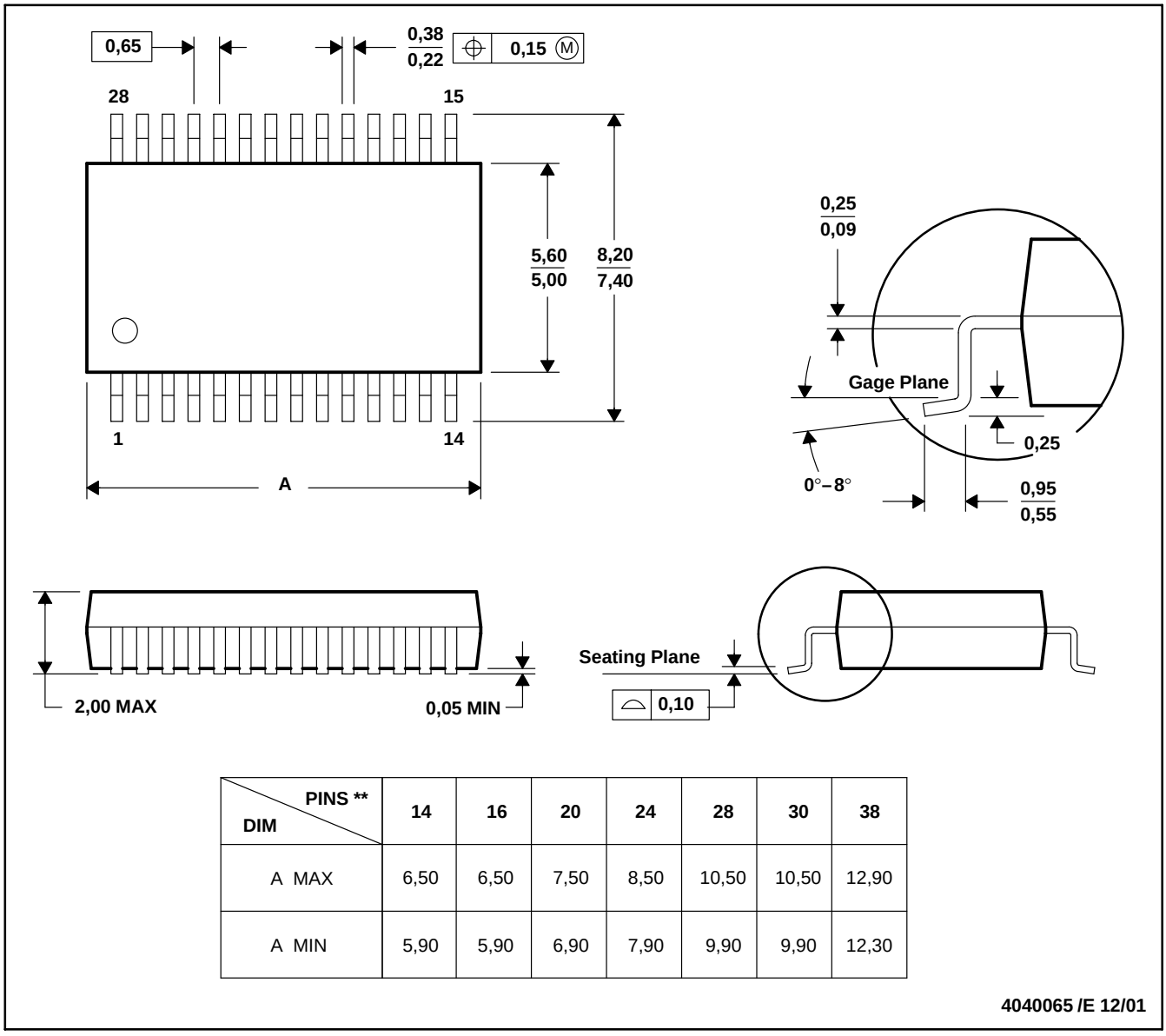
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PCM1723E	DB	SSOP	24	58	500	10.6	500	9.6
PCM1723E.B	DB	SSOP	24	58	500	10.6	500	9.6

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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