10-A, 4.5-V to 14-V INPUT, NON-ISOLATED, ADJUSTABLE WIDE-OUTPUT, SWITCHING REGULATOR

Check for Samples: PTR08100W

FEATURES

- **Up to 10-A Output Current**
- **Wide Input Voltage Range (4.5 V to 14 V)**
- **Wide-Output Voltage Adjust (0.6 V to 5.5 V)**
- **Efficiencies Up To 96%**
- **ON/OFF Inhibit**
- **Undervoltage Lockout (UVLO)**
- **Output Overcurrent Protection (Nonlatching, Auto-Reset)**
- **Ambient Temp. Range: –40°C to 85°C**
- **Space Saving Vertical SIP Package**

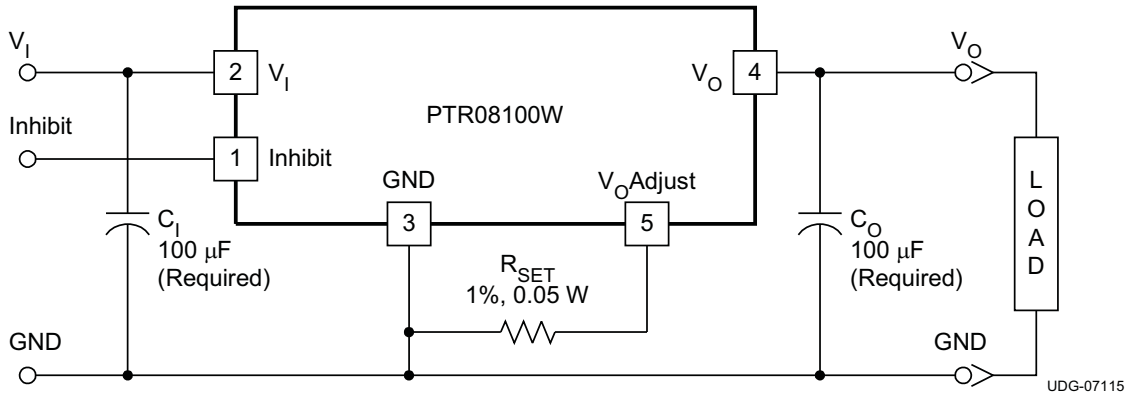
APPLICATIONS

- **Instrumentation**
- **Consumer Electronics**
- **Servers**
- **General-Purpose Circuits**

DESCRIPTION

The PTR08100W is a highly integrated, low-cost switching regulator module that delivers up to 10 A of output current. Occupying approximate PCB area of a standard TO-220 linear regulator IC, the PTR08100W provides output current at a much higher efficiency and with much less power dissipation, thereby eliminating the need for a heat sink. Their small size (0.65 x 0.41 in), high efficiency, and low cost makes these modules attractive for a variety of applications.

The input voltage range of the PTR08100W is from 4.5 V to 14 V, allowing operation from either a 5-V or 12-V input bus. Using state-of-the-art switched-mode power-conversion technology, the PTR08100W can step down to voltages as low as 0.6 V. The output voltage can be adjusted to any voltage over the range, 0.6 V to 5.5 V, using a single external resistor. Operating features include an undervoltage lockout (UVLO), on/off inhibit and output overcurrent protection. Target applications include servers, test and measurement applications, and high-end consumer products.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

				UNIT
T_A	Operating free-air temperature	Over V_I range	-40 to 85	°C
T_{wave}	Wave solder temperature	Surface temperature of module body or pins **(5 seconds maximum)**	260 (2)	
T_{stg}	Storage temperature	Storage temperature of module removed from shipping package	-55 to 125	
T_{pkg}	Packaging temperature	Shipping Tray storage or bake temperature	45	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This product is not compatible with surface-mount reflow solder processes.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_I	Input voltage	4.5	14	V
T_A	Operating free-air temperature	–40	85	°C

PACKAGE SPECIFICATIONS

PTR08100W		UNIT
Weight		2.74 grams
Flammability	Meets UL 94 V-O	
Mechanical shock	Per Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted	250 G (1)
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20-2000 Hz	5 G (1)

(1) Qualification limit.

ELECTRICAL CHARACTERISTICS

at 25°C free-air temperature, V_I = 12 V, V_O = 3.3 V, I_O = I_O(Max), C_I = 100 µF, C_O = 100 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_O	Output current	T_A = 50°C, 200LFM airflow		0		10	A
V_I	Input voltage range	Over I_O range	0.6 V ≤ V_O ≤ 3.6	4.5		14 (1)	V
			3.6 V < V_O ≤ 5.5	V_O /0.83 (2)		14	
$V_{O(adj)}$	Output voltage adjust range	Over I_O range		0.6		5.5	V
V_O	Set-point voltage tolerance	T_A = 25°C				±2 (3)	% V_O
	Temperature variation	-40°C ≤ T_A ≤ +85°C			±0.2		% V_O
	Line regulation	Over V_I range			±0.3		% V_O
	Load regulation	Over I_O range			±0.5		% V_O
	Total output voltage variation	Includes set-point, line, load, –40°C ≤ T_A ≤ +85°C				±3 (3)	% V_O
η	Efficiency	T_A = 25°C, V_I = 5 V, I_O = 5 A	R_{SET} = 267 Ω, V_O = 5 V (2)		92 %		
			R_{SET} = 432 Ω, V_O = 3.3 V (2)		95 %		
			R_{SET} = 619 Ω, V_O = 2.5 V		93 %		
			R_{SET} = 976 Ω, V_O = 1.8 V		91 %		
			R_{SET} = 1.3 kΩ, V_O = 1.5 V		90 %		
			R_{SET} = 1.91 kΩ, V_O = 1.2 V		88 %		
			R_{SET} = 2.87 kΩ, V_O = 1 V		86 %		
			R_{SET} = 10.7 kΩ, V_O = 0.7 V		84 %		
	Output voltage ripple	20 MHz bandwith			50		mV_{PP}
I_{LIM}	Overcurrent threshold	Reset, followed by autorecovery			16		A
	Transient response	2.5 A/µs load step from 50 to 100% $I_O$max	Recovery time		50		µs
			V_O over/undershoot		150		mV
UVLO	Undervoltage lockout	V_I = increasing			4.25	4.4	V
		V_I = decreasing		3.8	3.95		
	Inhibit control (pin 1)	Input high voltage (V_{IH})		2.8		open (4)	V
		Input low voltage (V_{IL})		–0.3		0.6	
		Input low current (I_{IL})			–125		µA
$I_{I(stby)}$	Input standby current	Pin 1 to GND			1		mA
F_S	Switching frequency	Over V_I and I_O ranges			300		kHz
C_I	External input capacitance			100 (5)			µF
C_O	External output capacitance	Non-ceramic		100 (6)		3000 (7)	µF
		Ceramic			22 (6)	100	
		Equivalent series resistance (non-ceramic)		5 (8)			mΩ
MTBF	Calculated reliability	Per Bellcore TR-332, 50% stress, T_A = 40°C, ground benign		13.7			10^6 Hrs

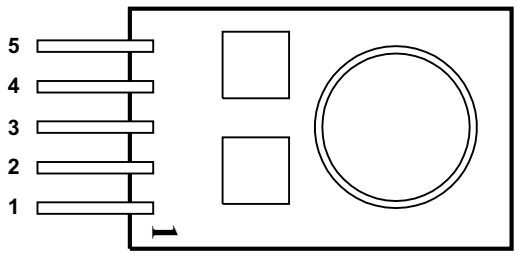
(1) For output voltages less than 1.0 V, the output ripple may increase (up to 2×) when operating at input voltages greater than (V_O ×15).
(2) The minimum input voltage is 4.5 V or (V_O/0.83) V, whichever is greater.
(3) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1% with with 100 ppm/°C or better temperature stability.
(4) This control pin has an internal pullup to the input voltage V_I. If it is left open circuit, the module operates when input power is applied. A small low-leakage (<100 nA) MOSFET is recommended for control. Do not tie the inhibit pin to V_I or to another module's inhibit pin. See the application section for further guidance.
(5) An external 100-µF bulk capacitor is required across the input (V_I and GND) for proper operation. Locate the capacitor close to the module.
(6) An external 100-µF non-ceramic capacitor is required across the output (V_O and GND) for proper operation. Locate the capacitor close to the module. Adding additional capacitance close to the load improves the response of the regulator to load transients.
(7) This is the calculated maximum capacitance. The minimum ESR limitation often results in a lower value. See the capacitor application information for further guidance.
(8) This is the typical ESR for all the non-ceramic capacitance. Use 7 mΩ as the minimum when calculating the total equivalent series resistance (ESR) using the max-ESR values specified by the capacitor manufacturer.

PIN ASSIGNMENT

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
V_I	2	The positive input voltage power node to the module, which is referenced to common GND.
GND	3	This is the common ground connection for the V_I and V_O power connections. It is also the 0 VDC reference for the *Inhibit* and V_O *Adjust* control inputs.
V_O	4	The regulated positive power output with respect to the GND node.
V_OAdjust	5	A 1% resistor must be connected between this pin and GND (pin 3) to set the output voltage of the module higher than 0.6 V. If left open-circuit, the output voltage defaults to this value. The temperature stability of the resistor should be 100 ppm/°C (or better). The set-point range is from 0.6 V to 5.5 V. For information on output voltage adjustment see the related application section. **The *V_OAdjust* pin must never be connected directly to *GND* . The minimum resistance between *V_OAdjust* and *GND* is limited to 240 Ω.**
Inhibit	1	The Inhibit pin is an open-collector/drain-negative logic input that is referenced to GND. Applying a low-level ground signal to this input disables the module's output. When the Inhibit control is active, the input current drawn by the regulator is significantly reduced. If the Inhibit pin is left open-circuit, the module will produce an output voltage whenever a valid input source is applied.

TOP VIEW



TYPICAL CHARACTERISTICS (12-V INPUT) (1) (2)

EFFICIENCY vs OUTPUT CURRENT

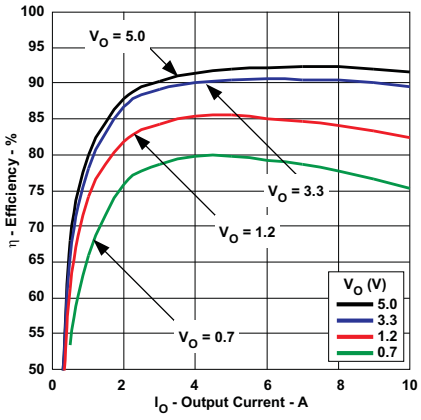


Figure 1.

OUTPUT RIPPLE vs OUTPUT CURRENT

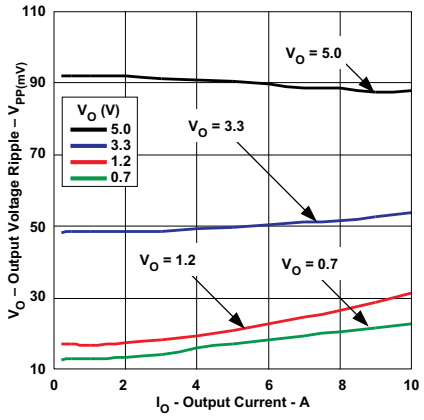


Figure 2.

POWER DISSIPATION vs OUTPUT CURRENT

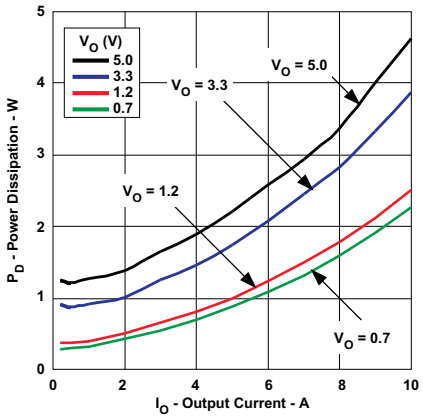


Figure 3.

TEMPERATURE DERATING vs OUTPUT CURRENT

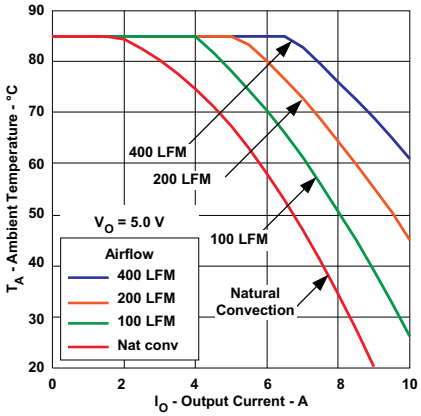


Figure 4.

TEMPERATURE DERATING vs OUTPUT CURRENT

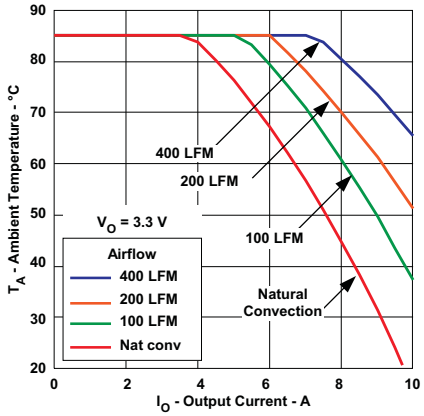


Figure 5.

TEMPERATURE DERATING vs OUTPUT CURRENT

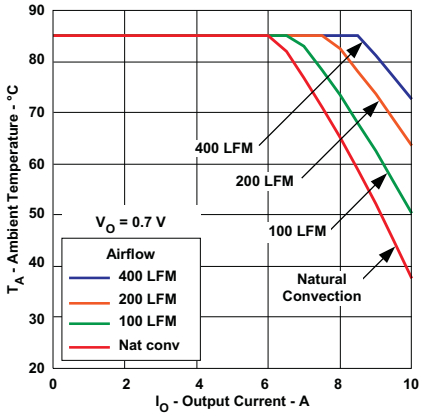


Figure 6.

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 1, Figure 2, and Figure 3.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm × 100 mm double-sided PCB with 1 oz. copper. Applies to Figure 4, Figure 5, Figure 6.

TYPICAL CHARACTERISTICS (5-V INPUT) (1) (2)

EFFICIENCY vs OUTPUT CURRENT

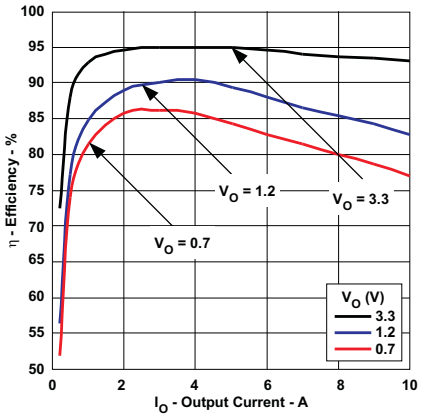


Figure 7.

OUTPUT RIPPLE vs OUTPUT CURRENT

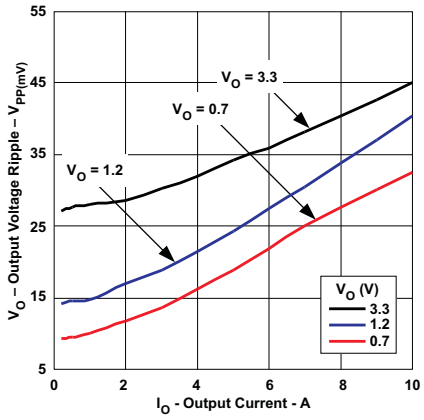


Figure 8.

POWER DISSIPATION vs OUTPUT CURRENT

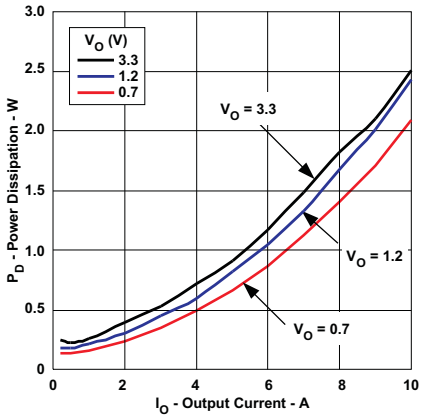


Figure 9.

TEMPERATURE DERATING vs OUTPUT CURRENT

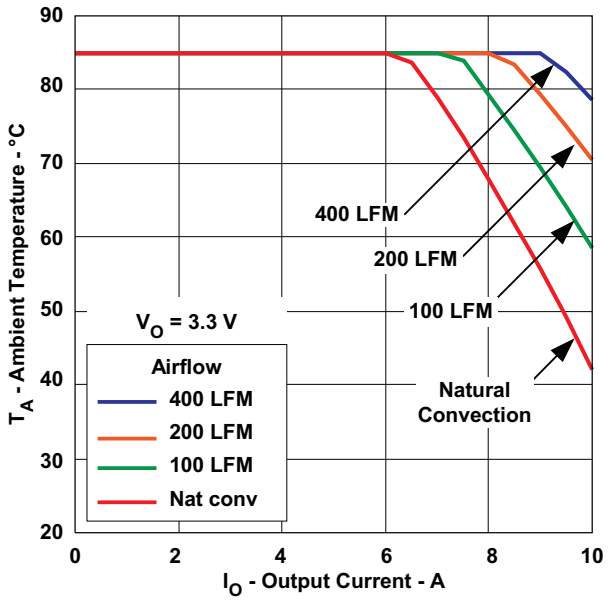


Figure 10.

TEMPERATURE DERATING vs OUTPUT CURRENT

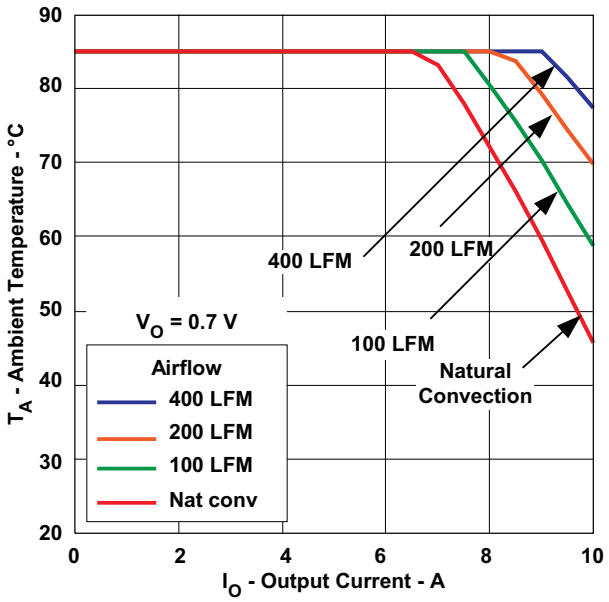


Figure 11.

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 7, Figure 8, and Figure 9.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm × 100 mm double-sided PCB with 1 oz. copper. Applies to Figure 10, Figure 11.

APPLICATION INFORMATION

ADJUSTING THE OUTPUT VOLTAGE

The *V_OAdjust* control (pin 5) sets the output voltage of the PTR08100W product. The adjustment range is from 0.6 V to 5.5 V. The adjustment method requires the addition of a single external resistor, R_{SET}, that must be connected directly between the *V_OAdjust* and *GND* pin 3. Table 1 gives the standard external resistor for a number of common bus voltages, along with the actual voltage the resistance produces.

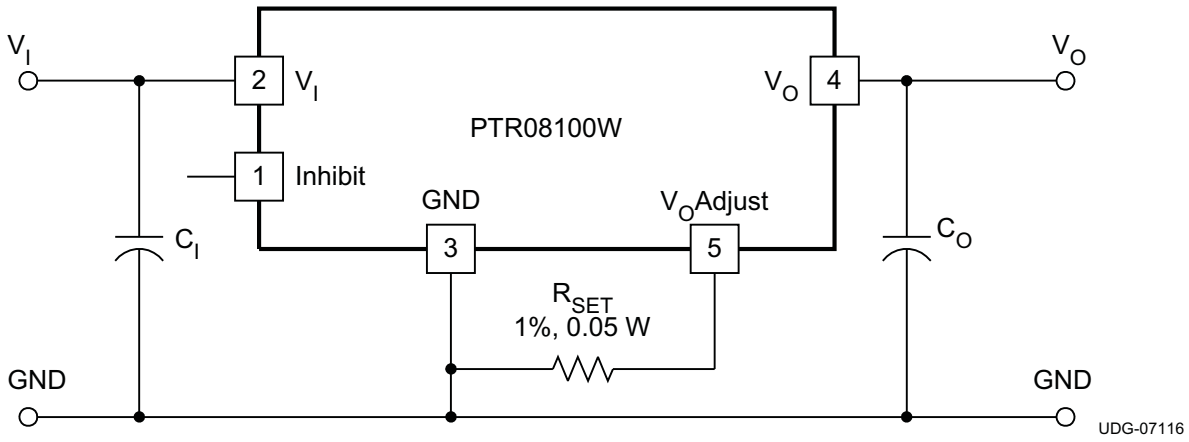
For other output voltages, the value of the required resistor can either be calculated using the following formula, or simply selected from the range of values given in Table 2. Figure 12 shows the placement of the required resistor.

$$R_{SET} = \frac{1.182}{V_O - 0.591} (k\Omega)$$

Table 1. Standard Values of R_{SET} for Common Output Voltages

V_O (V) (Required)	R_{SET} (kΩ) (Standard Value)	V_O(V) (Actual)
5(1)	0.267	5.018
3.3	0.432	3.327
2.5	0.619	2.501
1.8	0.976	1.802
1.5	1.3	1.500
1.2	1.91	1.210
1	2.87	1.003
0.7	10.7	0.701

(1) The minimum input voltage is 4.5 V or (V_O/0.83) V, whichever is greater.



(1) A 0.05-W rated resistor may be used. The tolerance should be 1%, with a temperature stability of 100 ppm/°C (or better). Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 5 and 3 using dedicated PCB traces.

(2) The *V_OAdjust* pin must never be connected directly to *GND*. The minimum resistance between *V_OAdjust* and *GND* is limited to 240 Ω.

(3) Never connect capacitors from *V_OAdjust* to either *GND* or V_O . Any capacitance added to the *V_OAdjust* pin will affect the stability of the regulator.

Figure 12. V_O Adjust Resistor Placement

Table 2. Calculated R_{SET} Resistor Values

V_O Req'd (V)	R_{SET} (kΩ)	V_O Req'd (V)	R_{SET}(kΩ)	V_O Req'd (V)	R_{SET}(kΩ)
0.6	131	2.3	0.692	4.0	0.347
0.7	10.8	2.4	0.653	4.1	0.337
0.8	5.66	2.5	0.619	4.2	0.328
0.9	3.83	2.6	0.588	4.3	0.319
1.0	2.89	2.7	0.560	4.4	0.310
1.1	2.32	2.8	0.535	4.5	0.302
1.2	1.94	2.9	0.512	4.6	0.295
1.3	1.67	3.0	0.491	4.7	0.288
1.4	1.46	3.1	0.471	4.8	0.281
1.5	1.30	3.2	0.453	4.9	0.274
1.6	1.17	3.3	0.436	5.0	0.268
1.7	1.07	3.4	0.421	5.1	0.262
1.8	0.978	3.5	0.406	5.2	0.256
1.9	0.903	3.6	0.393	5.3	0.251
2.0	0.839	3.7	0.380	5.4	0.246
2.1	0.783	3.8	0.368	5.5	0.241
2.2	0.735	3.9	0.357		

CAPACITOR RECOMMENDATIONS FOR THE PTR08100W POWER MODULE

Capacitor Technologies

Electrolytic Capacitors

When using electrolytic capacitors, high-quality, computer-grade electrolytic capacitors are recommended. Aluminum electrolytic capacitors provide adequate decoupling over the frequency range of 2 kHz to 150 kHz, and are suitable when ambient temperatures are above -20°C. For operation below -20°C, tantalum, ceramic, or OS-CON type capacitors are required.

Ceramic Capacitors

The performance of aluminum electrolytic capacitors is less effective above 150 kHz. Multilayer ceramic capacitors have a low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input as well as improve the transient response of the output.

Tantalum, Polymer-Tantalum Capacitors

Tantalum type capacitors may only used on the output bus, and are recommended for applications where the ambient operating temperature is less than 0°C. The AVX TPS series and Kemet capacitor series are suggested over many other tantalum types due to their lower ESR, higher rated surge, power dissipation, and ripple current capability. Tantalum capacitors that have no stated ESR or surge current rating are not recommended for power applications.

Input Capacitor (Required)

The PTR08100W requires a minimum input capacitance of 100 µF. The ripple current rating of the electrolytic capacitor must be at least 750 mArms. An optional 22-µF X5R/X7R ceramic capacitor is recommended to reduce the RMS ripple current. Table 3 includes a preferred list of capacitors by vendor.

Input Capacitor Information

The size and value of the input capacitor is determined by the converter's transient performance capability. The minimum value assumes that the converter is supplied with a responsive, low-inductance input source. The source should have ample capacitive decoupling, and be distributed to the converter via PCB power and ground planes.

Ceramic capacitors should be located as close as possible to the module's input pins, within 0.5 inch (1.3 cm). Adding ceramic capacitance is necessary to reduce the high-frequency ripple voltage at the module's input. This reduces the magnitude of the ripple current through the electroytic capacitor, as well as the amount of ripple current reflected back to the input source. Additional ceramic capacitors can be added to further reduce the RMS ripple current requirement for the electrolytic capacitor.

The main considerations when selecting input capacitors are the RMS ripple current rating, temperature stability, and maintaining less than 100 mΩ of equivalent series resistance (ESR).

Regular tantalum capacitors are not recommended for the input bus. These capacitors require a recommended minimum voltage rating of 2 × (maximum dc voltage + ac ripple). This is standard practice to ensure reliability. No tantalum capacitors were found to have voltage ratings sufficient to meet this requirement.

When the operating temperature is below 0°C, the ESR of aluminum electrolytic capacitors increases. For these applications, OS-CON, poly-aluminum, and polymer-tantalum types should be considered.

Output Capacitor (Required)

The PTR08100W requires a minimum 100 µF of non-ceramic output capacitance. Additional non-ceramic, low-ESR capacitance is recommended for improved performance. See data sheet for maximum capacitance limits. The required capacitance above the minimum is determined by actual transient deviation requirements. Table 3 includes a preferred list of capacitors by vendor.

Output Capacitor Information

When selecting output capacitors, the main considerations are capacitor type, temperature stability, and ESR.

Ceramic output capacitors added for high-frequency bypassing should be located as close as possible to the load to be effective. Ceramic capacitor values below 10 µF should not be included when calculating the total output capacitance value.

When the operating temperature is below 0°C, the ESR of aluminum electrolytic capacitors increases. For these applications, OS-CON, poly-aluminum, and polymer-tantalum types should be considered.

Designing for Fast Load Transients

The transient response of the dc/dc converter has been characterized using a load transient with a di/dt of 2.5 A/µs. The typical voltage deviation for this load transient is given in the Electrical Characteristics table using the minimum required value of output capacitance. As the di/dt of a transient is increased, the response of a converter's regulation circuit ultimately depends on its output capacitor decoupling network. This is an inherent limitation with any dc/dc converter once the speed of the transient exceeds its bandwidth capability.

If the target application specifies a higher di/dt or lower voltage deviation, the requirement can only be met with additional low ESR ceramic capacitor decoupling. Generally, with load steps greater than 100 A/µs, adding multiple 10-µF ceramic capacitors plus 10 × 1 µF, and numerous high frequency ceramics (≤ 0.1 µF) is all that is required to soften the transient higher frequency edges. The PCB location of these capacitors in relation to the load is critical. DSP, FPGA and ASIC vendors identify types, location and amount of capacitance required for optimum performance. Low impedance buses, unbroken PCB copper planes, and components located as close as possible to the high frequency devices are essential for optimizing transient performance.

Table 3. Recommended Input/Output Capacitors (1)

Capacitor Vendor, Type/Series (Style)	Capacitor Characteristics					Quantity		Vendor Number
	Working Voltage (V)	Value (µF)	Max ESR at 100 kHz (Ω)	Max Ripple Current at 85°C (Irms) (mA)	Physical Size (mm)	Input Bus	Output Bus	
Panasonic, Aluminum	25	330	0.090	775	10 × 12,5	1	1	EEUFC1E331
FC (Radial)	35	180	0.090	775	10 × 12,5	1	1	EEUFC1V181
FK (SMD)	25	470	0.080	850	10 × 10,2	1	1	EEVFK1E471P
United Chemi-Con								
PXA-Poly-Aluminum (SMD)	16	150	0.026	3430	10 × 7,7	1	≤ 4	PXA16VC151MJ80TP
PS (Radial)	20	100	0.024	3300	8 × 11,5	1	≤ 4	20PS100MH11
LXZ, Aluminum (Radial)	35	220	0.090	760	10 × 12,5	1	1	LXZ35VB221M10X12LL
Nichicon Aluminum								
HD (Radial)	25	220	0.072	760	8 × 11,5	1	1	UHD1E221MPR
PM (Radial)	35	220	0.090	770	10 × 15	1	1	UPM1V221MHH6
Sanyo								
SVP, Os-con (SMD)	20	100	0.024	3300	8 × 12	1	≤ 4	20SVP100M
SEQP, Os-con (Radial)	20	100	0.024	3300	8 × 12	1	≤ 4	20SEQP100M
TPE, Pos-Cap (SMD)	10	220	0.025	2400	7,3 × 5,7	N/R (2)	≤ 4	10TPE220ML
AVX, Tantalum	10	100	0.100	1090	7,3 × 4,3 × 4,1	N/R (2)	≤ 5	TPSD107M010R0100
TPS (SMD)	10	220	0.100	1414	7,3 × 4,3 × 4,1	N/R (2)	≤ 5	TPSV227M010R0100
	25	68	0.095	1451	7,3 × 4,3 × 4,1	2	≤ 5	TPSV686M025R0080
Kemet								
T520, Poy-Tant (SMD)	10	100	0.080	1200	7,3 × 5,7 × 4	N/R (2)	≤ 5	T520D107M010AS
T495, Tantalum (SMD)	10	100	0.100	1100	7,3 × 5,7 × 4	N/R (2)	≤ 5	T495X107M010AS
Vishay-Sprague	10	150	0.090	1100	7,3 × 6 × 4,1	N/R (2)	≤ 5	594D157X0010C2T
594D, Tantalum (SMD)	25	68	0.095	1600	7,3 × 6 × 4,1	2	≤ 5	594D686X0025R2T
94SP, Organic (Radial)	16	100	0.070	2890	10 × 10,5	1	≤ 5	94SP107X0016FBP
94SVP, Organic (SMD)	20	100	0.025	3260	8 × 12	1	≤ 4	94SVP107X0020E12
Kemet, Ceramic X5R (SMD)	16	10	0.002	–	1210 case	1 (3)	≤ 5	C1210C106M4PAC
	6.3	47	0.002		3225 mm	N/R (2)	≤ 5	C1210C476K9PAC
Murata, Ceramic X5R (SMD)	6.3	100	0.002	–	1210 case	N/R (2)	≤ 3	GRM32ER60J107M
	6.3	47			3225 mm	N/R (2)	≤ 5	GRM32ER60J476M
	16	22				1 (3)	≤ 5	GRM32ER61C226L
	16	10				1 (3)	≤ 5	GRM32DR61C106K
TDK, Ceramic X5R (SMD)	6.3	100	0.002	–	1210 case	N/R (2)	≤ 3	C3225X5ROJ107MT
	6.3	47			3225 mm	N/R (2)	≤ 5	C3225X5ROJ476MT
	16	22				1 (3)	≤ 5	C3225X5R1C226MT
	16	10				1 (3)	≤ 5	C3225X5R1C106MT

(1) **Capacitor Supplier Verification**
Please verify availability of capacitors identified in this table. Capacitor suppliers may recommend alternative part numbers because of limited availability or obsolete products. In some instances, the capacitor product life cycle may be in decline and have short-term consideration for obsolescence.
RoHS, Lead-free and Material Details
Please consult capacitor suppliers regarding material composition, RoHS status, lead-free status, and manufacturing process requirements. Component designators or part number deviations can occur when material composition or soldering requirements are updated.
(2) N/R – Not recommended. The capacitor voltage rating does not meet the minimum operating limits.
(3) Ceramic capacitors are required to complement electrolytic types at the input and to reduce high-frequency ripple current.

Power-Up Characteristics

When configured per the standard application, the PTR08100W power module produces a regulated output voltage following the application of a valid input source voltage. During power up, internal soft-start circuitry slows the rate that the output voltage rises, thereby limiting the amount of in-rush current that can be drawn from the input source. The soft-start circuitry introduces a short time delay (typically 10 ms) into the power-up characteristic. This is from the point that a valid input source is recognized. Figure 13 shows the power-up waveforms for a PTR08100W, operating from a 12-V input and with the output voltage adjusted to 3.3 V. The waveforms were measured with a 6-A constant current load.

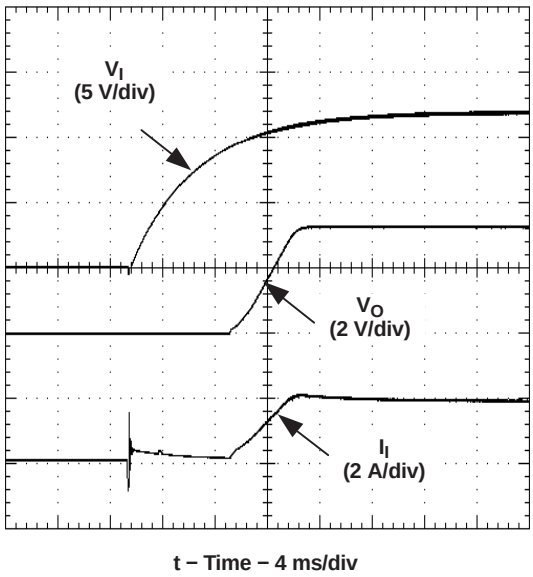


Figure 13. Power-Up Waveforms

Overcurrent Protection

For protection against load faults, the PTR08100W incorporates output overcurrent protection. Applying a load that exceeds the regulator's overcurrent threshold causes the regulated output to shut down. Following shutdown, the module periodically attempts to recover by initiating a soft-start power-up. This is described as a *hiccup* mode of operation, whereby the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the module automatically recovers and returns to normal operation.

Output On/Off Inhibit

For applications requiring output voltage on/off control, the PTR08100W power module incorporates an output on/off Inhibit control (pin 1). The inhibit feature can be used wherever there is a requirement for the output voltage from the regulator to be turned off.

The power module functions normally when the Inhibit pin is left open-circuit, providing a regulated output whenever a valid source voltage is connected to Vin with respect to GND.

Figure 14 shows the typical application of the inhibit function. Note the discrete transistor (Q1). The Inhibit control has its own internal pullup to V_I potential. An open-collector or open-drain device is recommended to control this input.

Turning Q1 on applies a low voltage to the *Inhibit* control pin and disables the output of the module. If Q1 is then turned off, the module will execute a soft-start power-up sequence. A regulated output voltage is produced within 20 msec. Figure 15 shows the typical rise in the output voltage, following the turn off of Q1. The turn off of Q1 corresponds to the rise in the waveform, V_{INH}. The waveforms were measured with a 6-A constant current load.

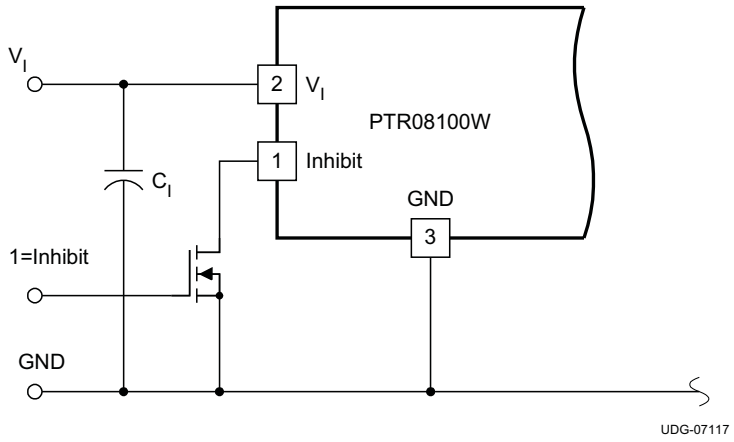


Figure 14. On/Off Inhibit Control Circuit

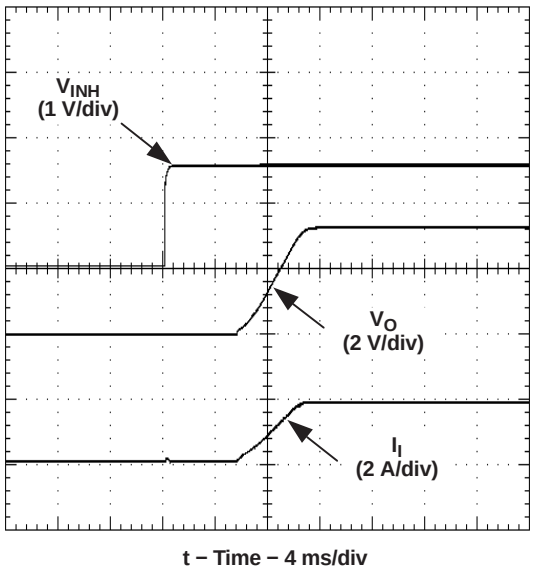


Figure 15. Power Up Response From Inhibit Control

Changes from Revision E (April 2009) to Revision F **Page**

- Deleted *Overtemperature Protection* in FEATURES 1

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTR08100WVD	Active	Production	SIP MODULE (EDN) | 5	80 | TIW TRAY	Exempt	SN	N/A for Pkg Type	-40 to 85	
PTR08100WVD.B	Active	Production	SIP MODULE (EDN) | 5	80 | TIW TRAY	Exempt	SN	N/A for Pkg Type	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

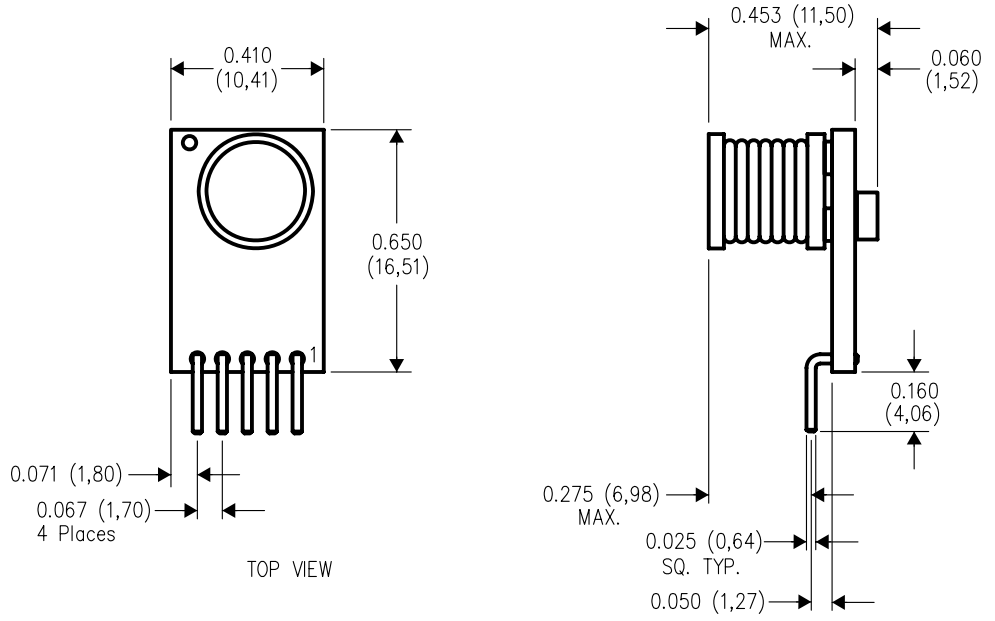
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

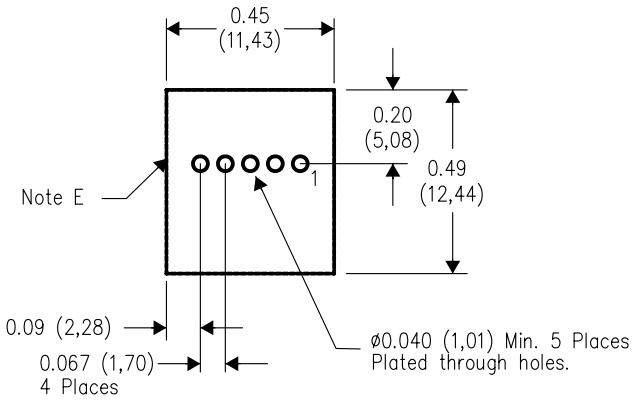
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

EDN (R–PDSS–T5) DOUBLE SIDED MODULE





4208200/A 08/06

NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are SQ 0.025" (0,64).
G. All pins: Material – Phosphor Bronze
Finish – Tin (100%) over Nickel plate

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Last updated 10/2025