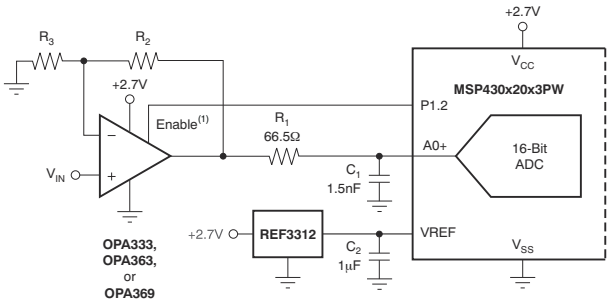
REF33xx 3.9µA, SC70-3, SOT-23-3, and UQFN-8, 30ppm/°C Drift Voltage Reference

1 Features

- Microsize packages: SC70-3, SOT-23-3, UQFN-8
- Low supply current: 3.9µA (typical)
- Extremely low dropout voltage: 110mV (typical)
- High output current: ±5mA
- Low temperature drift: 30ppm/°C (maximum)
- High initial accuracy: ±0.15% (maximum)
- 0.1Hz to 10Hz noise: 35µV_{PP} (REF3312)
- Voltage options: 1.2V, 1.8V, 2.5V, 3V, 3.3V

2 Applications

- Portable equipment
- Tablets and smartphones
- Hard disk drives
- Sensor modules
- Data acquisition systems
- Medical equipment
- Test equipment



REF3312 in a Single-Supply Signal Chain

3 Description

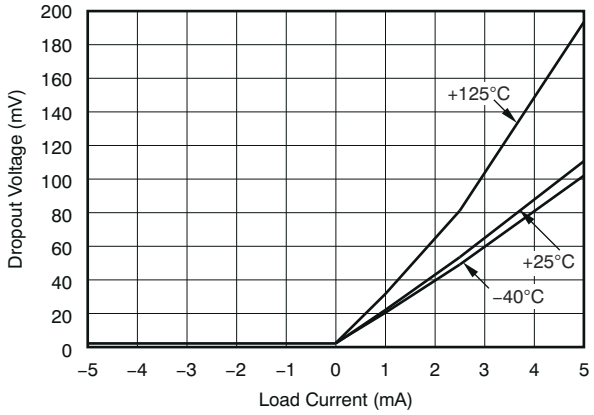
The REF33xx is a low-power, precision, low-dropout voltage reference family available in tiny SC70-3 and SOT-23-3 packages, and in a 1.5mm × 1.5mm UQFN-8 package. Small size and low power consumption (5µA maximum) make the REF33xx ideal for a wide variety of portable and battery-powered applications.

The REF33xx can be operated at a supply voltage 180mV above the specified output voltage under normal load conditions, with the exception of the REF3312, which has a minimum supply voltage of 1.7V. All models are specified for the wide temperature range of –40°C to +125°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
REF33xx	DBZ (SOT-23, 3)	2.92mm × 2.37mm
	DCK (SC70, 3)	2.00mm × 2.10mm
	RSE (UQFN, 8)	1.50mm × 1.50mm

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Dropout Voltage vs Load Current

Table of Contents

4 Device Comparison

PRODUCT	DESCRIPTION
REF3312	1.25V
REF3318	1.8V
REF3320	2.048V
REF3325	2.5V
REF3330	3.0V
REF3333	3.3V

5 Pin Configuration and Functions

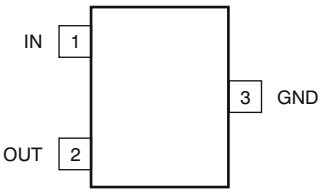


Figure 5-1. REF3312, REF3318, REF3320, REF3325, REF3330, REF3333DBZ Package and DCK Package SOT-23-3, SC70-3 (Top View)

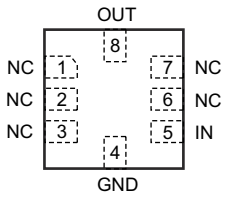


Figure 5-2. REF3312, REF3318, REF3320, REF3325, REF3330, REF3333RSE Package UQFN-8 (Top View)

Table 5-1. Pin Functions

PIN			DESCRIPTION
NAME	DBZ, DCK	RSE	
GND	3	4	Ground
IN	1	5	Input supply voltage
NC	—	1, 2, 3, 6, 7	Not connected
OUT	2	8	Output voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted).(1)

		MIN	MAX	UNIT
Voltage	Input voltage		7.5	V
	Output voltage		5	
Current	Output short-circuit, I_{SC} (2)		180	mA
Temperature	Operating	–50	150	°C
	Junction, T_J		150	
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) See the *Power-Supply Recommendations* section of this data sheet.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{IN}	Supply input voltage(1)	V_{OUT} + 0.2		5.5	V
I_{OUT}	Output current range	–5		5	mA

(1) The minimum supply voltage for the REF3312 is 1.7V.

6.4 Thermal Information

THERMAL METRIC(1)		REF33xx		REF3325, REF3330	UNIT
		DCK (SC70)	DBZ (SOT-23)	RSE (UQFN)	
		3 PINS	3 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	279.7	313.1	61.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	136.3	144.0	32.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.9	109.3	16.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.0	18.2	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.1	107.9	16.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Electrical Characteristics

At T_A = 25°C, V_{IN} = 5V, and I_{LOAD} = 0mA (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REF3312 (1.25V)						
V_{OUT}	Output voltage			1.25		V
	Initial accuracy		–0.15%		0.15%	
	Output voltage noise	f = 0.1Hz to 10Hz		35		μV_{PP}
REF3318 (1.8V)						
V_{OUT}	Output voltage			1.8		V
	Initial accuracy		–0.15%		0.15%	
	Output voltage noise	f = 0.1Hz to 10Hz		50		μV_{PP}
REF3320 (2.048V)						
V_{OUT}	Output voltage			2.048		V
	Initial accuracy		–0.15%		0.15%	
	Output voltage noise	f = 0.1Hz to 10Hz		55		μV_{PP}
REF3325 (2.5V)						
V_{OUT}	Output voltage			2.5		V
	Initial accuracy		–0.15%		0.15%	
	Output voltage noise	f = 0.1Hz to 10Hz		70		μV_{PP}
REF3330 (3.0V)						
V_{OUT}	Output voltage			3.0		V
	Initial accuracy		–0.15%		0.15%	
	Output voltage noise	f = 0.1Hz to 10Hz		84		μV_{PP}
REF3333 (3.3V)						
V_{OUT}	Output voltage			3.3		V
	Initial accuracy		–0.15%		0.15%	
	Output voltage noise	f = 0.1Hz to 10Hz		92		μV_{PP}
REF33xx (REF3312, REF3320, REF3325, REF3330, REF3333, REF3340)						
dV_{OUT}/dT	Output voltage temperature drift	–40°C to 85°C		9	30	ppm/°C
		–40°C to 125°C		8	30	
$\Delta V_{O(\Delta VI)}$	Line regulation	V_{IN} = V_{OUT} + 200mV to 5.5V(1)	–50	6	50	ppm/V
		0°C to +70°C		6		
		–40°C to 85°C		8		
		–40°C to 125°C		30		
$\Delta V_{O(\Delta IL)}$	Load regulation	V_{IN} = V_{OUT} + 200mV(1)	–50	6	50	ppm/mA
		I_{LOAD} = ±5mA, 0°C to 70°C		10		
		–40°C to 85°C		20		
		–40°C to 125°C		20		
	Long-term stability(3)	0h to 1000h at 25°C		55		ppm
dT	Thermal hysteresis(2)			90		ppm
$V_{IN} – V_{OUT}$	Minimum dropout voltage(1)	I_{LOAD} = ±5mA		110	160	mV
		0°C to 70°C		120		
		–40°C to 85°C		135		
		–40°C to 125°C		180		
		I_{LOAD} = ±2mA, –40°C to 85°C			70	
I_{SC}	Short-circuit current	Sourcing and sinking		35		mA

6.5 Electrical Characteristics (continued)

At T_A = 25°C, V_{IN} = 5V, and I_{LOAD} = 0mA (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Capacitive load		0.1		10	µF
	Turn-on settling time	To 0.1% with C_L = 1µF		2		ms
POWER SUPPLY						
V_S	Specified voltage range		V_{OUT} + 0.2[(1)]		5.5	V
	Operating voltage range	I_{LOAD} = 0mA		V_{OUT} + 0.005	5.5	V
I_Q	Current			3.9	5	µA
		–40°C to 85°C		4.4	6.5	
		–40°C to 125°C		4.8	8.5	
TEMPERATURE						
T_A	Specified range		–40		125	°C
	Operating range		–50		150	

(1) The minimum supply voltage for the REF3312 is 1.7V.
(2) The thermal hysteresis procedure is explained in more detail in the Thermal Hysteresis section.
(3) The long-term stability number reduces as the time increases.

6.6 Typical Characteristics

At T_A = 25°C and V_{IN} = 5V, and REF3325 used for typical characteristic measurements (unless otherwise noted).

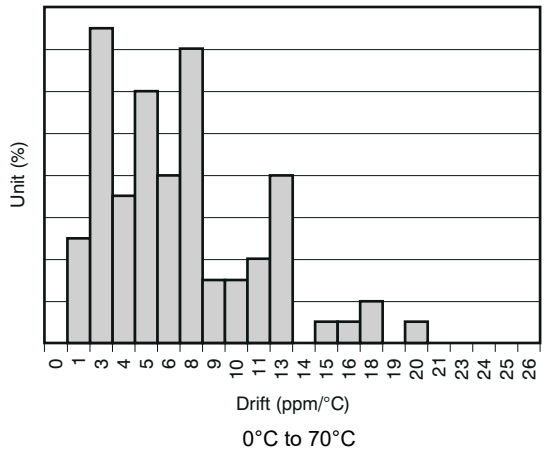


Figure 6-1. Temperature Drift

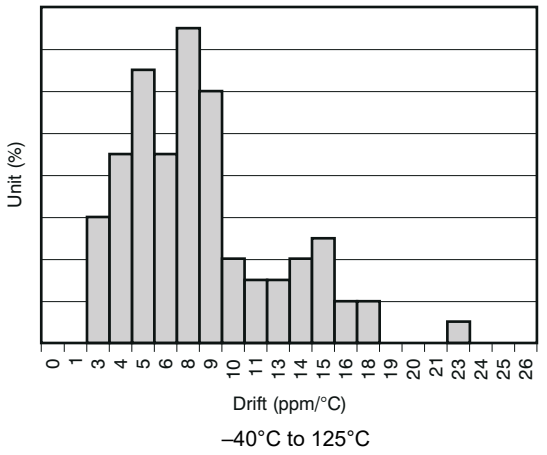


Figure 6-2. Temperature Drift

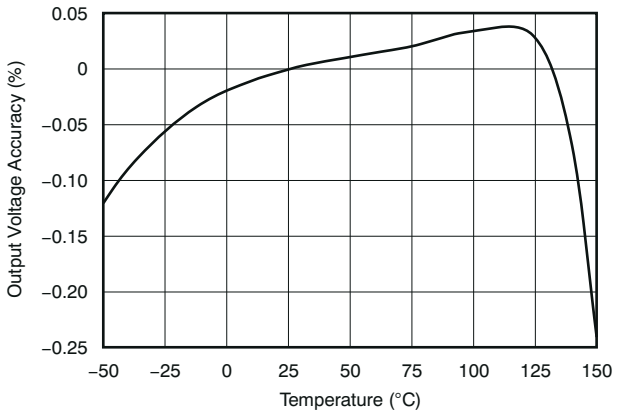


Figure 6-3. Output Voltage Accuracy vs Temperature

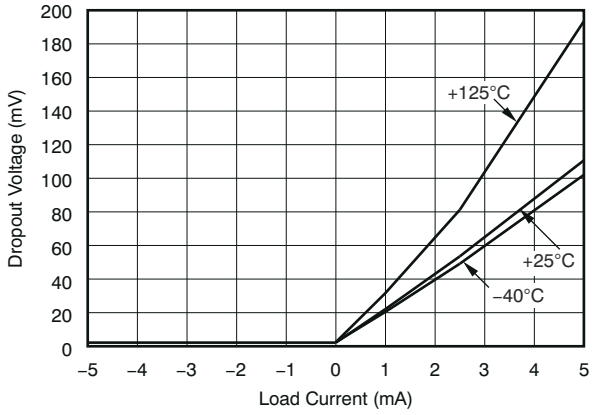


Figure 6-4. Dropout Voltage vs Load Current

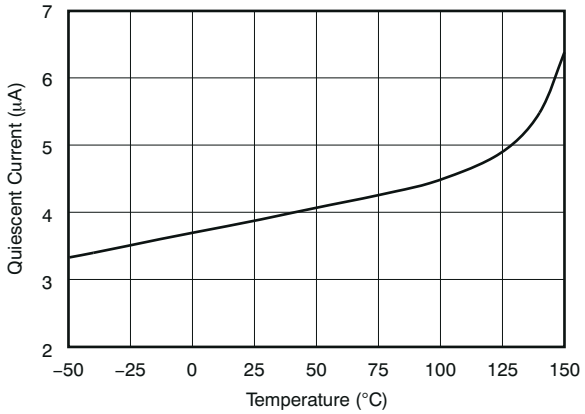


Figure 6-5. Quiescent Current vs Temperature

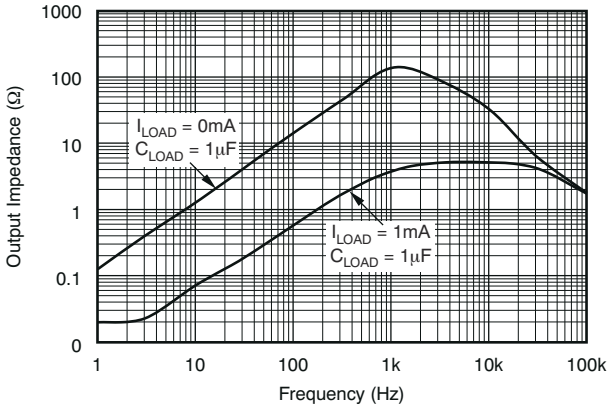


Figure 6-6. Output Impedance vs Frequency

6.6 Typical Characteristics (continued)

At T_A = 25°C and V_{IN} = 5V, and REF3325 used for typical characteristic measurements (unless otherwise noted).

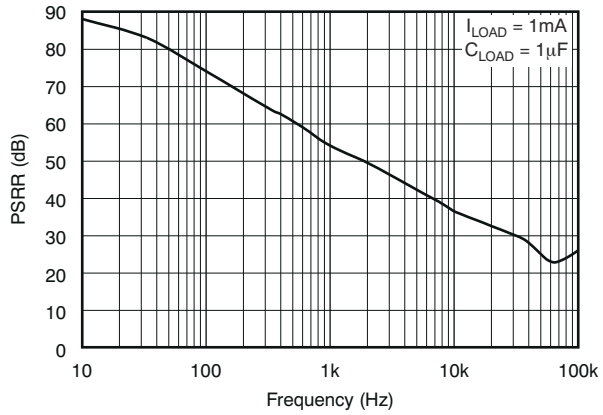


Figure 6-7. Power-Supply Rejection Ratio vs Frequency

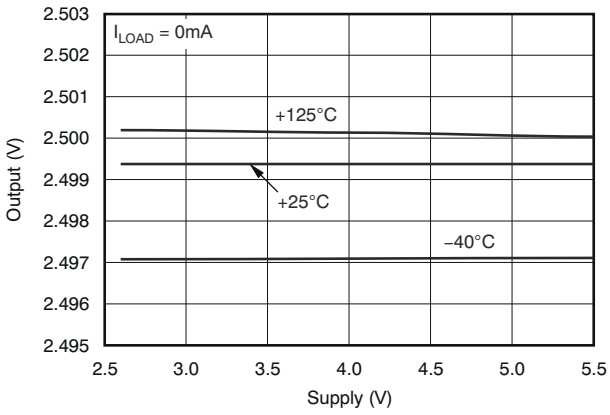


Figure 6-8. Output vs Supply

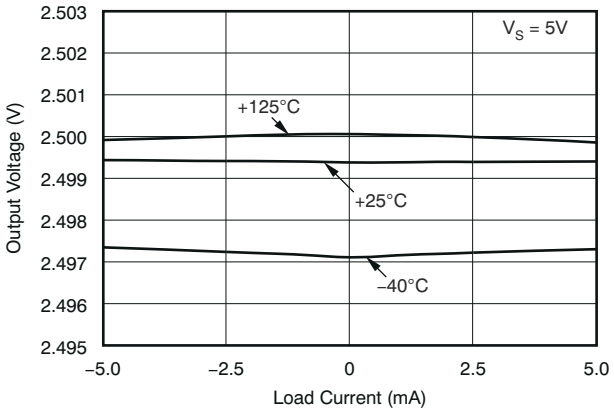
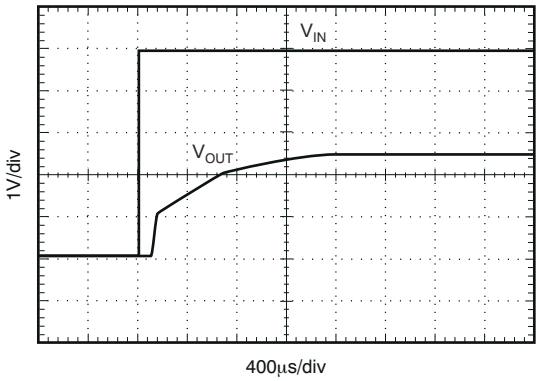


Figure 6-9. Output Voltage vs Load Current



C_L = 1µF Startup

Figure 6-10. Step Response

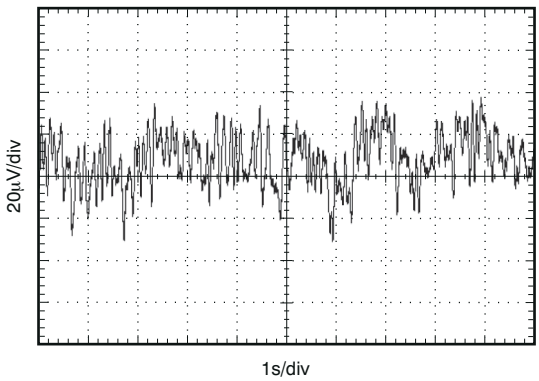
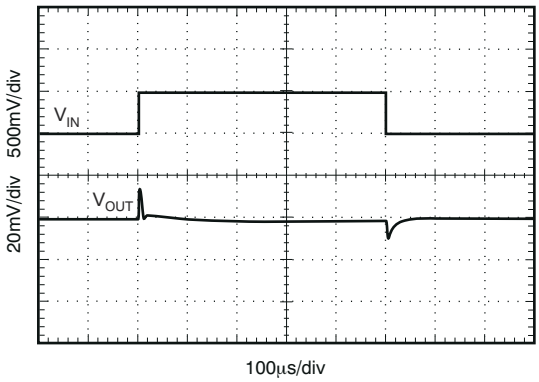


Figure 6-11. 0.1Hz to 10Hz Noise

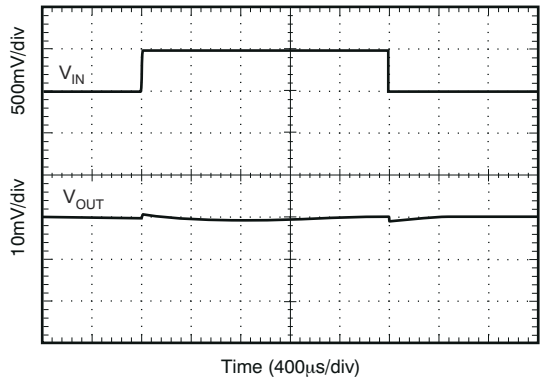


C_L = 1µF, I_{OUT} = 0mA

Figure 6-12. Line Transient

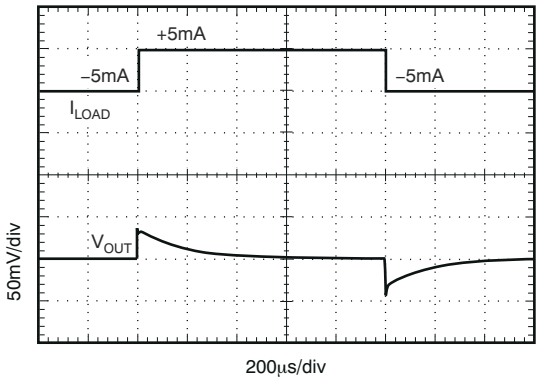
6.6 Typical Characteristics (continued)

At T_A = 25°C and V_{IN} = 5V, and REF3325 used for typical characteristic measurements (unless otherwise noted).



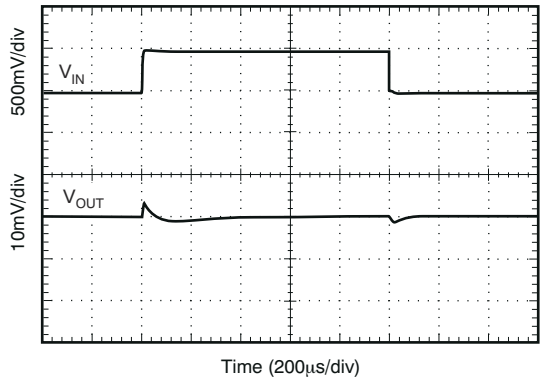
C_{LOAD} = 10µF, I_{OUT} = 0mA

Figure 6-13. Line Transient



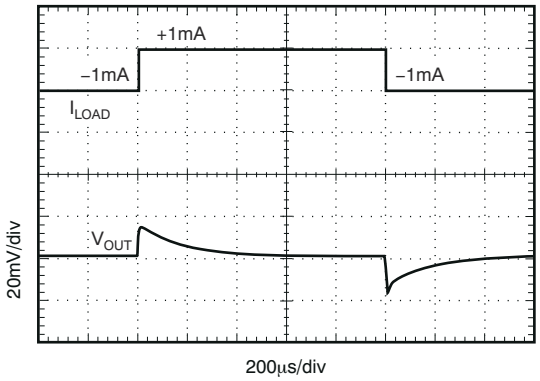
C_L = 1µF, ±5mA Output Pulse

Figure 6-14. Load Transient



C_{LOAD} = 10µF, I_{OUT} = 1mA

Figure 6-15. Line Transient



C_L = 1µF, ±1mA Output Pulse

Figure 6-16. Load Transient

7 Parameter Measurement Information

7.1 Thermal Hysteresis

Thermal hysteresis for the REF33xx is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. It can be expressed as Equation 1:

$$V_{HYST} = \left(\frac{|V_{PRE} - V_{POST}|}{V_{NOM}} \right) \times 10^6 (ppm) \quad (1)$$

where

- V_{HYST} = thermal hysteresis (in units of ppm).
- V_{NOM} = the specified output voltage.
- V_{PRE} = output voltage measured at 25°C pretemperature cycling.
- V_{POST} = output voltage measured after the device cycles from 25°C through the specified temperature range of –40°C to 125°C and returns to 25°C.

8 Detailed Description

8.1 Overview

The REF33xx is a family of low-power, precision band-gap voltage references that are specifically designed for extremely low dropout, excellent initial voltage accuracy with a high output current. A simplified block diagram of the REF33xx is shown in the *Functional Block Diagram* section. Figure 8-1 shows the typical connections for the REF33xx. A supply bypass capacitor ranging from 1µF to 10µF is recommended. The total capacitive load at the output must be between 0.1µF to 10µF to establish output stability.

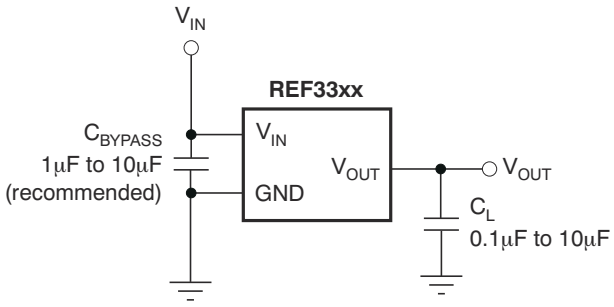
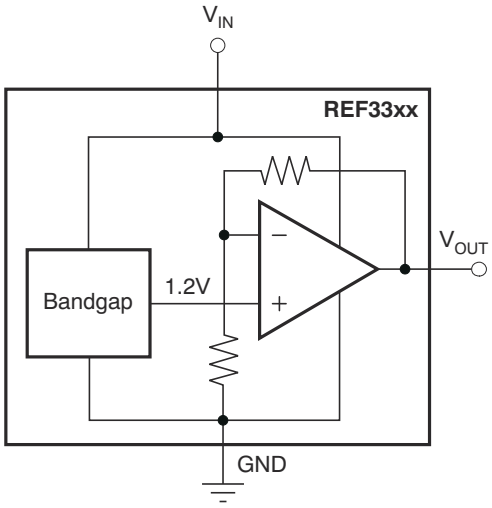


Figure 8-1. Basic Connections

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Start-Up Time

The REF33xx features an advanced start-up circuit. Start-up time is almost independent of load (with a 0.1µF to 10µF load). Upon startup, the current boost circuit forces the output voltage. When the preset voltage is reached, the REF33xx switches to the second stage of output circuitry to precisely set the output voltage. Figure 8-2 shows the start-up time of the REF3325 for three different capacitive loads. In all three cases, the output voltage settles within 2ms.

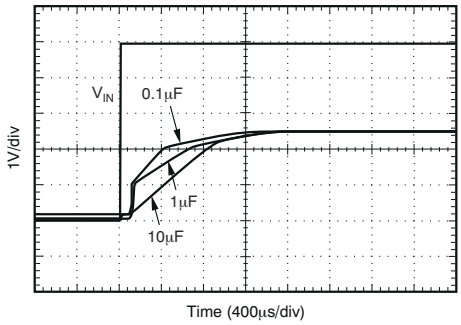


Figure 8-2. Start-Up Time

8.3.2 Low Temperature Drift

The REF33xx is designed for minimal drift error, defined as the change in output voltage over temperature. The drift is calculated using the box method, as described in Equation 2:

$$\text{Drift} = \left(\frac{V_{OUTMAX} - V_{OUTMIN}}{V_{OUT} \times \text{Temperature Range}}\right) \times 10^6 (\text{ppm}) \quad (2)$$

8.3.3 Power Dissipation

The REF33xx family is specified to deliver current loads of ±5mA over the specified input voltage range. The temperature of the device increases according to Equation 3:

$$T_J = T_A + P_D \times R_{\theta JA} \quad (3)$$

where

- T_J = junction temperature (°C)
- T_A = ambient temperature (°C)
- P_D = power dissipation (W)

$$= V_{IN} \times I_Q + (V_{IN} - V_{OUT}) I_{OUT} \quad (4)$$

- $R_{\theta JA}$ = Junction-to-ambient thermal resistance (°C/W)

The REF33xx junction temperature must not exceed the absolute maximum rating of 150°C.

8.3.4 Noise Performance

Typical 0.1Hz to 10Hz voltage noise for each member of the REF33xx family is specified in the *Electrical Characteristics* table. The noise voltage increases with output voltage and operating temperature. Use additional filtering to improve output noise levels. Give special attention to ensure that the output impedance does not degrade output voltage accuracy.

8.4 Device Functional Modes

The REF33xx is powered on when the voltage on the IN pin is greater than V_{OUT} + 0.2V, except for the REF3312, where the minimum supply voltage is 1.7V. The maximum input voltage for the REF33xx is 5.5V. Use a supply bypass capacitor ranging from 1µF to 10µF. The total capacitive load at the output must be from 0.1µF to 10µF to ensure output stability.

9 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The REF33xx is a family of low-power, precision band-gap voltage references that are specifically designed for extremely low dropout, excellent initial voltage accuracy with a high output current. The extremely small size of the SC70-3, SOT-23-3, and UQFN-8 make these references very attractive for space-constrained applications. The following section describes one common application.

9.2 Typical Applications

9.2.1 REF3312 in a Bipolar Signal-Chain Configuration

The circuit in Figure 9-1 consists of a low-power reference and conditioning circuit. This circuit attenuates and level-shifts a bipolar input voltage within the proper input range of a single-supply, low-power, 16-bit ΔΣ analog-to-digital converter (ADC), such as the one inside the MSP430™ integrated circuit (or other similar single-supply ADCs). Precision reference circuits are used to level-shift the input signal, provide the ADC reference voltage, and create a well-regulated supply voltage for the low-power analog circuitry. A low-power, zero-drift op amp circuit is used to attenuate and level-shift the input signal.

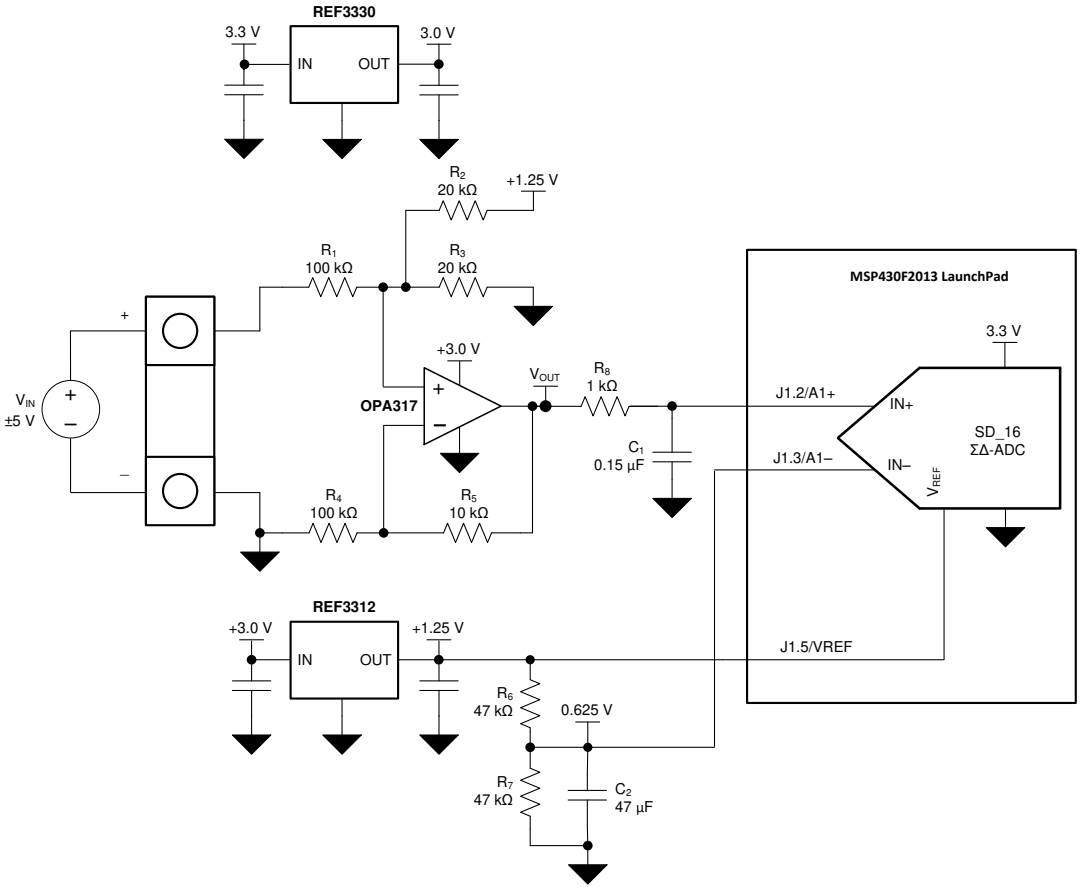


Figure 9-1. Bipolar Signal-Chain Configuration

9.2.1.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 3.3V
- Maximum input voltage: ±6V
- Specified input voltage: ±5V
- ADC reference voltage: 1.25V

9.2.1.2 Detailed Design Procedure

Figure 9-1 depicts a simplified schematic for this design showing the MSP430 ADC inputs and full input conditioning circuitry. The ADC is configured for a bipolar measurement where final conversion result is the differential voltage, V_{DIFF}, between the positive and negative ADC inputs, A1+ and A1–. The bipolar, ground-referenced input signal must be level-shifted and attenuated by the op amp so that the output is biased to V_{REF} / 2 and has a differential voltage that is within the $\pm V_{REF}$ / 2 input range of the ADC. The transfer function for the op-amp circuit simplifies to Equation 5.

$$A1+ = \left(\frac{R_3}{R_2 + R_3}\right)V_{REF} + \left(\frac{R_2 \parallel R_3}{R_1}\right)V_{IN} \quad (5)$$

where

- $R_1 = R_4$
- $R_5 = R_2 \parallel R_3$

The voltage applied to the negative ADC input, A1–, is based on the resistor divider formed by R6 and R7 and is set to V_{REF} / 2 by setting R6 equal to R7, as shown in Equation 6.

$$A1- = \left(\frac{R_7}{R_6 + R_7}\right)V_{REF} = \frac{V_{REF}}{2} \quad (6)$$

9.2.1.2.1 Op Amp Level-Shift Design

The ratio of R_2, R_3, and the V_{REF} voltage determines the voltage on the output of the op amp when the differential input is 0V. Select the components so that V_{OUT} is equal to the V_{REF} / 2 voltage when V_{IN} is equal to 0V, as shown in Equation 7.

$$A1+ = \frac{V_{REF}}{2} = \left(\frac{R_3}{R_2 + R_3}\right)V_{REF} \quad (7)$$

where

- $V_{IN} = 0V$
- $R_2 = R_3$

Solve for the value of R_5 by setting R_3 equal to R_2 in Equation 5, as shown in Equation 8:

$$R_5 = \left(\frac{R_2 \times R_2}{R_2 + R_2}\right) = \frac{{R_2}^2}{2 \times R_2} = \frac{R_2}{2} \quad (8)$$

9.2.1.2.2 Differential Input Attenuator Design

V_{DIFF} is the difference between the two inputs, as shown in Equation 9:

$$V_{DIFF} = (A1+) - (A1-) = \left(\frac{R_3}{R_2 + R_3}\right)V_{REF} + \left(\frac{R_2 \parallel R_3}{R_1}\right)V_{IN} - \frac{V_{REF}}{2} \quad (9)$$

When the ratio of R_3 and R_2 equals the ratio of R_7 and R_6, Equation 9 simplifies to Equation 11.

That is, if:

$$\left(\frac{R_3}{R_2 + R_3}\right)V_{REF} = \left(\frac{R_7}{R_6 + R_7}\right)V_{REF} = \frac{1}{2}V_{REF} \quad (10)$$

Then:

$$V_{DIFF} = \left(\frac{R_2 \parallel R_3}{R_1}\right)V_{IN} \quad (11)$$

Determine the ratio of R_1, R_2, and R_3 by setting A1+ equal to the maximum V_{DIFF} for a full-scale positive or negative input voltage, VIN_MAX, as shown in Equation 12:

$$A1+ = V_{DIFF\_MAX} = \left(\frac{R_2 \parallel R_3}{R_1}\right)V_{IN\_MAX} \quad (12)$$

R_2 equals R_3; therefore, Equation 12 simplifies to R_2 / 2, resulting in Equation 13:

$$V_{DIFF\_MAX} = \left(\frac{R_2}{2 \times R_1}\right)V_{IN\_MAX} \quad (13)$$

9.2.1.2.3 Input Filtering

Both inputs feature first-order, low-pass, antialiasing filters that limit the bandwidth and noise of the input signals applied to the ADC. The A1+ filter is formed by R_8 and C_1 and the equation for the –3dB cutoff frequency is shown in Equation 14:

$$f_{-3dB\_A1+} = \frac{1}{2 \times \pi \times R_8 \times C_1} \quad (14)$$

The A1– input filter is formed by C_2 and the parallel combination of the R_6 and R_7 resistors, as shown in Equation 15:

$$f_{-3dB\_A1-} = \frac{1}{2 \times \pi \times \left(\frac{R_6}{2}\right) \times C_2} \quad (15)$$

9.2.1.2.4 Component Selection

9.2.1.2.4.1 Voltage References

The REF33xx series of precision low-power voltage references pair well with the low power consumption of the MSP430, while achieving the target accuracy goals. The 16-bit converter in the MSP430F2013 accepts an external reference voltage from 1V to 1.5V with a typical reference input of 1.25V, as shown in Table 9-1.

Table 9-1. SD16_A, External Reference Input (MSP430F20x3)

PARAMETER(1)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{REF(I)}$	Input voltage range	VCC = 3V, SD16REFON = 0	1	1.25	1.5	V
$I_{REF(I)}$	Input current	VCC = 3V, SD16REFON = 0			50	nA

(1) Over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted).

The REF3312 provides the desired 1.25V reference voltage for the MSP430 ADC. The accuracy of the REF3312 output, shown in the *Electrical Characteristics*, directly affects the accuracy of the entire system and must be less than the desired unadjusted error goals. The REF3312 maximum ±0.15% initial accuracy specification is equal to the unadjusted error design goal of 0.15%, indicating that most of the error budget in this design must be devoted to the reference accuracy.

The 3.3V system supply voltage that powers the MSP430 can also supply other devices, and therefore can have regulation and noise issues. The REF3330 creates an accurate and stable 3.0V output used by the op amp, REF3312, and other low-power analog circuitry. The REF33xx series has a drop-output voltage of V_{OUT} + 200mV; therefore, as long as the input supply remains above 3.2V, the REF3330 produces a regulated 3.0V output. The output current for the REF33xx series is specified at ±5mA, as shown in Figure 6-9, and is sufficient for the REF3312 and a low-power op amp.

9.2.1.2.4.2 Op Amp

The OPA317 op amp is used because of low offset voltage, low offset voltage drift, CMRR, and low power consumption. The dc specifications for the OPA317 can be seen in the Texas Instruments *Low Offset, Rail-to-Rail I/O Operational Amplifier Precision Catalog* datasheet, available for download from www.ti.com. The maximum offset of 100µV accounts for only 0.001% of the full-scale signal, and the low-drift reduces temperature drift effects. Therefore, as previously mentioned, most of the error in this design is from the reference accuracy and passive component tolerances.

9.2.1.2.5 Input Attenuation and Level Shifting

For this design, the bipolar ±5V input must be attenuated and level shifted so the differential voltage is within the input range of $\pm V_{REF}$ / 2, or ±0.625V. The accuracy of the op amp output and ADC input can degrade near the supply rails and V_{REF} voltage, so the output is designed to produce a 0.125V to 1.125V output, or ±0.5V for a ±5V input. Scaling the output this way also increases the allowable input range to ±6V, and allows for some underscale and overscale voltage measurement and protection.

Use Equation 13 to scale the ±5V input to a ±0.5V differential voltage, as shown in Equation 16.

$$0.5\text{V} = \left(\frac{\text{R}_2}{2 \times 100\text{k}\Omega}\right) \times 5\text{V} \tag{16}$$

where

- $R_1 = R_4 = 100\text{k}\Omega$

R_1 and R_4 dominate the input impedance for this design and are therefore selected to be 100kΩ. Higher values can be selected to increase the input impedance at the expense of input noise.

With the value for R_2 and R_3 selected as 20kΩ, the value for R_5 is calculated, as shown in Equation 17:

$$\text{R}_5 = \left(\frac{\text{R}_2}{2}\right) \times 10\text{k}\Omega \tag{17}$$

where

- $R_2 = R_3 = 20\text{k}\Omega$

For A1– to equal to V_{REF} / 2, R_6 must equal R_7. Two 47kΩ resistors are used to conserve power without creating an impedance too weak to drive the ADC input.

9.2.1.2.6 Input Filtering

The MSP430 ADC is configured to run from the 1.1MHz SMCLK with an oversampling rate (OSR) of 256, yielding a sample rate of roughly 4.3kHz. The input filter cutoff frequency is set to 1kHz to limit the input signal bandwidth, as shown in Equation 19. R_8 is 1kΩ to provide isolation from the capacitive load of the low-pass filter, thereby reducing stability concerns.

$$\text{f}_{-3\text{dB\_A1}+} = 1\text{kHz} = \frac{1}{2 \times \pi \times \text{R}_8 \times \text{C}_1} \tag{18}$$

where

$$\text{C}_1 = \frac{1}{2 \times \pi \times 1\text{k}\Omega \times 1\text{kHz}} = 159\text{nF} \tag{19}$$

Reduce C_1 to 150nF so that it is a standard value.

The A1– input of the delta-sigma (ΔΣ) converter is not buffered, and therefore requires a large capacitor to supply the charge for the internal sampling capacitor. A 47µF capacitor is selected, resulting in the cutoff frequency illustrated in Equation 20.

$$f_{-3dB\_A1-} = \frac{1}{2 \times \pi \times \left(\frac{R_6}{2}\right) \times C_2} = 0.144Hz \quad (20)$$

In applications that cannot tolerate such a low-frequency cutoff, and therefore a long start-up time, buffer the A1– input with another OPA317 to properly drive the ADC input with a lower-input capacitor.

9.2.1.2.7 Passive Component Tolerances and Materials

Resistors R_1, R_2, R_3, R_4, R_5, R_6, and R_7 directly affect the accuracy of the circuit. To meet the unadjusted accuracy goals of 0.2%, the resistors used are 0.1%. Select 0.1% resistors for the construction of the difference amplifier circuit to provide a common-mode rejection ratio (CMRR) of at least 60dB.

9.2.1.3 Application Curves

9.2.1.3.1 DC Performance

The measured dc performance and calculated error of the circuit is shown in Figure 9-2 and Figure 9-3, respectively. By applying a two-point gain and offset calibration over the specified ±5V input range, the calibrated error is shown in Figure 9-4. The uncalibrated results show errors of 138µV, or 0.0138%FSR. The calibrated results with a simple two-point calibration show errors under 5µV, or 0.0005%FSR, in the specified input range of ±5V.

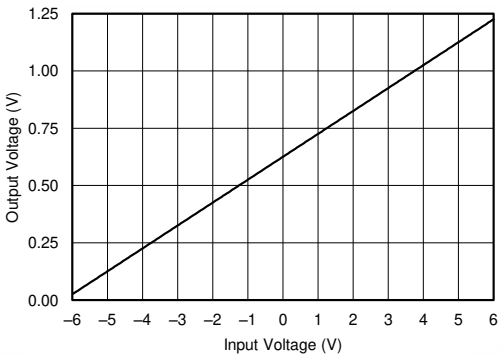


Figure 9-2. Measured DC Transfer Function with ±6V Input

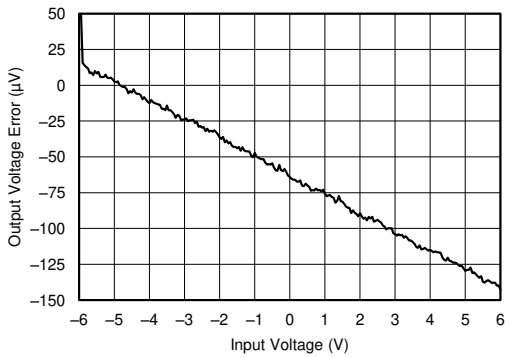


Figure 9-3. Measured Output Error with ±6V Input

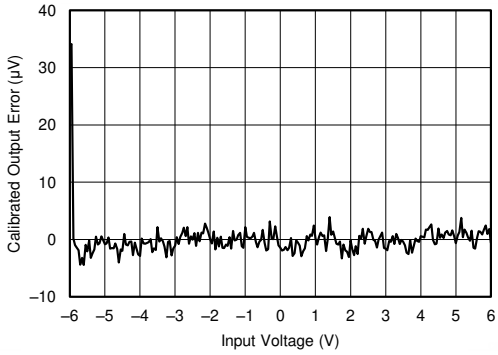


Figure 9-4. Calibrated Output Error with ±6V Input

9.2.1.3.2 AC Performance

The ac transfer function for the attenuation and level-shifting circuit is shown in Figure 9-5.

The low-frequency ac CMRR performance is measured to be 62dB, as shown in Figure 9-6.

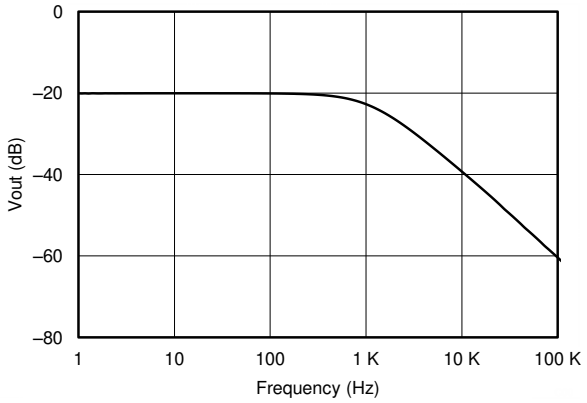


Figure 9-5. Measured AC Transfer Function

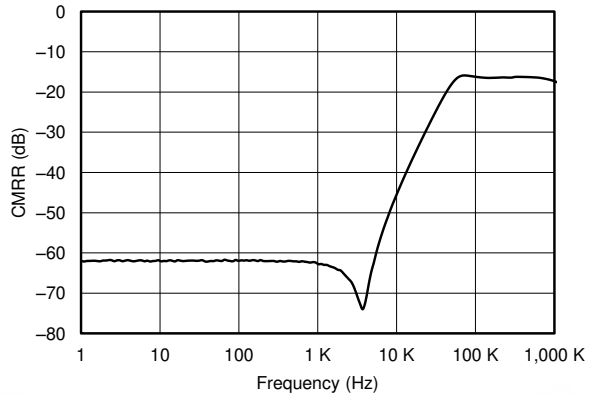


Figure 9-6. Measured AC CMRR Results

9.3 Power-Supply Recommendations

The REF33xx family of voltage references features extremely low dropout voltage, except for the REF3312. The REF3312 has a minimum supply requirement of 1.7V. These references can be operated with a supply 110mV above the output voltage with a 5mA load (typical). For loaded conditions, a typical dropout voltage versus load graph is illustrated in Figure 6-4 of the *Typical Characteristics*.

If the supply voltage connected to the IN pin is rapidly moved when the REF33xx is connected to a capacitive load, a reverse voltage can discharge through the OUT pin and into the REF33xx. This voltage does not damage the REF33xx, provided that the voltage is less than or equal to 5V.

9.4 Layout

9.4.1 Layout Guidelines

For optimal performance of this design, follow standard printed circuit board (PCB) layout guidelines, including proper decoupling close to all integrated circuits and adequate power and ground connections with large copper pours. Select a PCB size with connectors that connect directly to the MSP430 LaunchPad™.

Figure 9-7 shows an example of a PCB layout for a data acquisition system using the REF33xx.

Some key considerations are:

- Connect a low-ESR, 1µF ceramic capacitor at the IN pin for bypass, and a ceramic capacitor from 0.1µF to 10µF at the OUT pin for stability of the REF33xx.
- Decouple other active devices in the system per the device specifications.
- Use a solid ground plane helps distribute heat and reduces EMI noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Minimize trace length between the reference and bias connections to the ADC to reduce noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

9.4.2 Layout Example

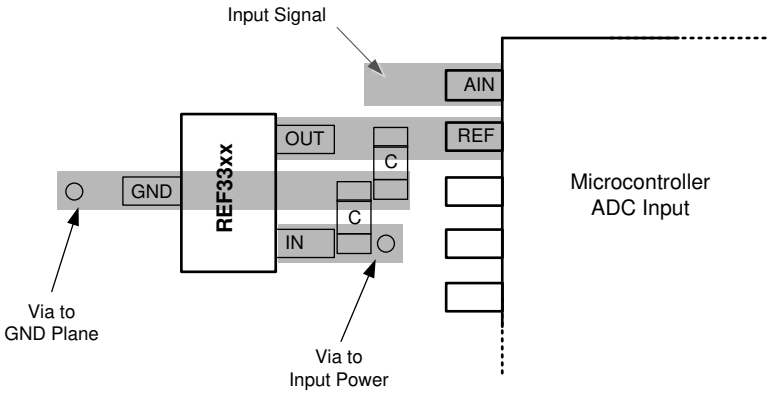


Figure 9-7. Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

- Texas Instruments, *1.8V, 700nA, Zerø-Crossover Rail-to-Rail I/O Operational Amplifier* datasheet
- Texas Instruments, *1.8V, 7MHz, 90dB CMRR, Single-Supply Rail-to-Rail I/O Operational Amplifier* datasheet
- Texas Instruments, *High-Speed, Precision, Gain of 0.2 Level Translation Difference Amplifier* datasheet
- Texas Instruments, *OPAx333 1.8V, microPower, CMOS Operational Amplifiers, Zero-Drift Series* datasheet

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (August 2019) to Revision I (April 2026)	Page
• Updated the numbering format for tables, figures, equations, and cross-references throughout the document	1
• Moved the REF3312, REF3318, REF3320, REF3325, REF3330, and REF3333 devices to the REF33 product folder on TI.com and updated the datasheet header	1
• Changed *Device Information* table to *Package Information*	1

Changes from Revision G (December 2016) to Revision H (August 2019)	Page
• Changed maximum operating current value in *Recommended Operating Conditions* section	5
• Changed table title to REF33xx (REF3312, REF3320, REF3325, REF3330, REF3333, REF3340)	6

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF3312AIDBZR	Active	Production	null (null) |	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33A
REF3312AIDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33A
REF3312AIDBZT	Active	Production	null (null) |	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33A
REF3312AIDBZT.A	Active	Production	SOT-23 (DBZ) | 3	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33A
REF3312AIDBZT1G4	Active	Production	null (null) |	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33A
REF3312AIDBZT1G4.A	Active	Production	SOT-23 (DBZ) | 3	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33A
REF3312AIDCKR	Active	Production	null (null) |	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R12
REF3312AIDCKR.A	Active	Production	SC70 (DCK) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R12
REF3312AIDCKR1G4	Active	Production	null (null) |	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R12
REF3312AIDCKR1G4.A	Active	Production	SC70 (DCK) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R12
REF3312AIDCKT	Active	Production	null (null) |	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R12
REF3312AIDCKT.A	Active	Production	SC70 (DCK) | 3	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R12
REF3312AIRSER	Active	Production	null (null) |	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	5G
REF3312AIRSER.A	Active	Production	UQFN (RSE) | 8	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	5G
REF3312AIRSERG4	Active	Production	null (null) |	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	5G
REF3312AIRSERG4.A	Active	Production	UQFN (RSE) | 8	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	5G
REF3312AIRSET	Active	Production	null (null) |	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	5G
REF3312AIRSET.A	Active	Production	UQFN (RSE) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	5G
REF3318AIDBZR	Active	Production	null (null) |	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33B
REF3318AIDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33B
REF3318AIDBZT	Active	Production	null (null) |	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33B
REF3318AIDBZT.A	Active	Production	SOT-23 (DBZ) | 3	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33B
REF3318AIDBZTG4	Active	Production	null (null) |	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33B
REF3318AIDBZTG4.A	Active	Production	SOT-23 (DBZ) | 3	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33B
REF3318AIDCKR	Active	Production	null (null) |	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R18
REF3318AIDCKR.A	Active	Production	SC70 (DCK) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R18
REF3318AIDCKRG4	Active	Production	null (null) |	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R18
REF3318AIDCKRG4.A	Active	Production	SC70 (DCK) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R18
REF3318AIDCKT	Active	Production	null (null) |	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R18

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF3318AIDCKT.A	Active	Production	SC70 (DCK) | 3	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R18
REF3320AIDBZR	Active	Production	null (null) |	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33C
REF3320AIDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33C
REF3320AIDBZT	Active	Production	null (null) |	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33C
REF3320AIDBZT.A	Active	Production	SOT-23 (DBZ) | 3	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33C
REF3320AIDBZT1G4	Active	Production	null (null) |	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33C
REF3320AIDBZT1G4.A	Active	Production	SOT-23 (DBZ) | 3	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33C
REF3320AIDCKR	Active	Production	null (null) |	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R20
REF3320AIDCKR.A	Active	Production	SC70 (DCK) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R20
REF3320AIDCKRG4	Active	Production	null (null) |	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R20
REF3320AIDCKRG4.A	Active	Production	SC70 (DCK) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R20
REF3320AIDCKT	Active	Production	null (null) |	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R20
REF3320AIDCKT.A	Active	Production	SC70 (DCK) | 3	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R20
REF3325AIDBZR	Active	Production	null (null) |	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33D
REF3325AIDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33D
REF3325AIDBZR1G4	Active	Production	null (null) |	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33D
REF3325AIDBZR1G4.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33D
REF3325AIDBZT	Active	Production	null (null) |	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33D
REF3325AIDBZT.A	Active	Production	SOT-23 (DBZ) | 3	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33D
REF3325AIDCKR	Active	Production	null (null) |	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R25
REF3325AIDCKR.A	Active	Production	SC70 (DCK) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R25
REF3325AIDCKR1G4	Active	Production	null (null) |	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R25
REF3325AIDCKR1G4.A	Active	Production	SC70 (DCK) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R25
REF3325AIDCKT	Active	Production	null (null) |	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R25
REF3325AIDCKT.A	Active	Production	SC70 (DCK) | 3	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R25
REF3325AIRSER	Active	Production	null (null) |	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	GN
REF3325AIRSER.A	Active	Production	UQFN (RSE) | 8	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	GN
REF3325AIRSERG4	Active	Production	null (null) |	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	GN
REF3325AIRSERG4.A	Active	Production	UQFN (RSE) | 8	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	GN
REF3330AIDBZR	Active	Production	null (null) |	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33E
REF3330AIDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33E

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
REF3330AIDBZRG4	Active	Production	null (null) |	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33E
REF3330AIDBZRG4.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33E
REF3330AIDBZT	Active	Production	null (null) |	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33E
REF3330AIDBZT.A	Active	Production	SOT-23 (DBZ) | 3	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33E
REF3330AIDCKR	Active	Production	null (null) |	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R30
REF3330AIDCKR.A	Active	Production	SC70 (DCK) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R30
REF3330AIDCKR1G4	Active	Production	null (null) |	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R30
REF3330AIDCKR1G4.A	Active	Production	SC70 (DCK) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R30
REF3330AIDCKT	Active	Production	null (null) |	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R30
REF3330AIDCKT.A	Active	Production	SC70 (DCK) | 3	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R30
REF3330AIRSER	Active	Production	null (null) |	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EN
REF3330AIRSER.A	Active	Production	UQFN (RSE) | 8	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EN
REF3330AIRSERG4	Active	Production	null (null) |	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EN
REF3330AIRSERG4.A	Active	Production	UQFN (RSE) | 8	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EN
REF3333AIDBZR	Active	Production	null (null) |	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33F
REF3333AIDBZR.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33F
REF3333AIDBZRG4	Active	Production	null (null) |	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33F
REF3333AIDBZRG4.A	Active	Production	SOT-23 (DBZ) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33F
REF3333AIDBZT	Active	Production	null (null) |	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33F
REF3333AIDBZT.A	Active	Production	SOT-23 (DBZ) | 3	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33F
REF3333AIDCKR	Active	Production	null (null) |	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33
REF3333AIDCKR.A	Active	Production	SC70 (DCK) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33
REF3333AIDCKRG4	Active	Production	null (null) |	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33
REF3333AIDCKRG4.A	Active	Production	SC70 (DCK) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33
REF3333AIDCKT	Active	Production	null (null) |	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33
REF3333AIDCKT.A	Active	Production	SC70 (DCK) | 3	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	R33

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

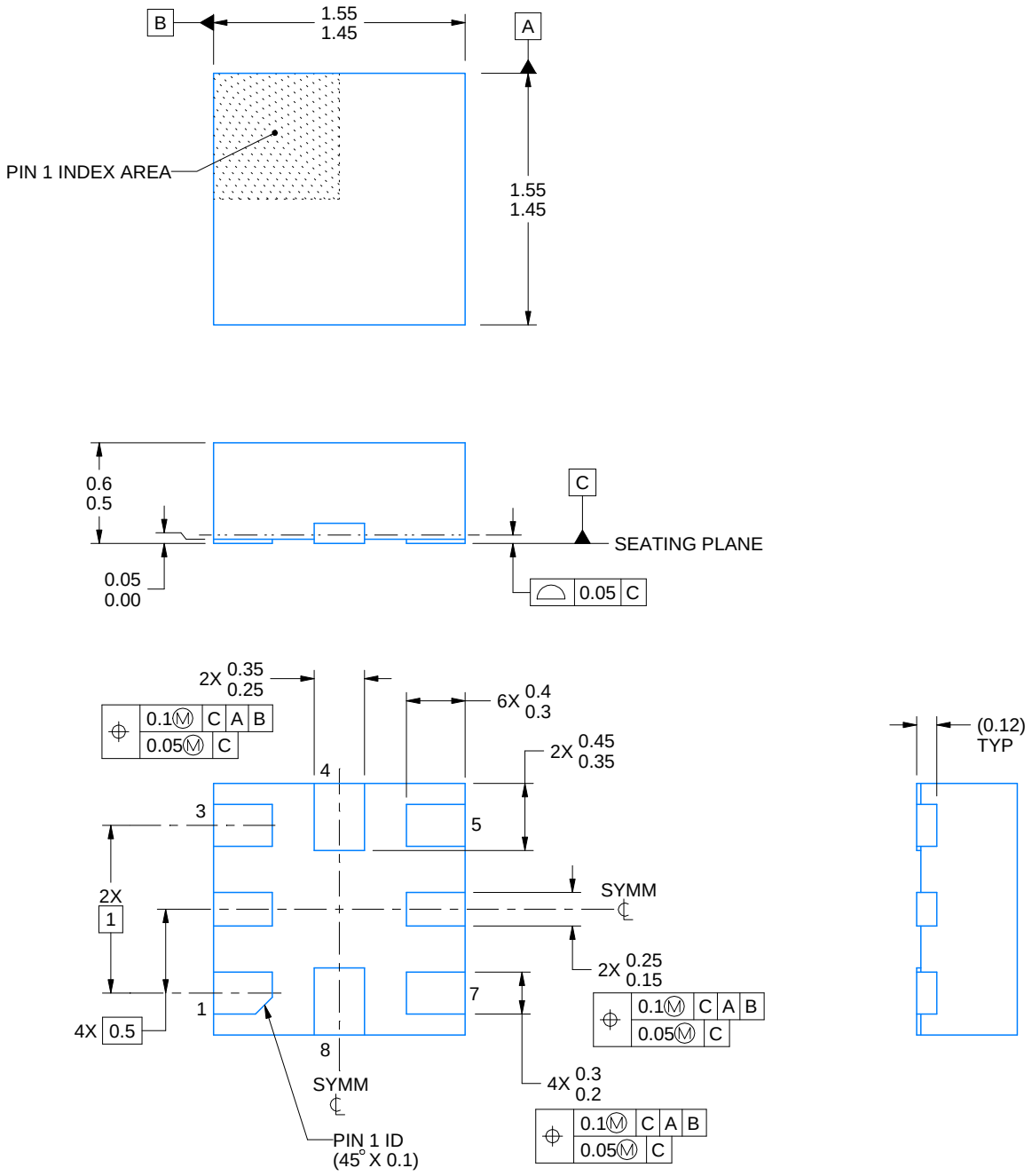
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

RSE0008A

PACKAGE OUTLINE

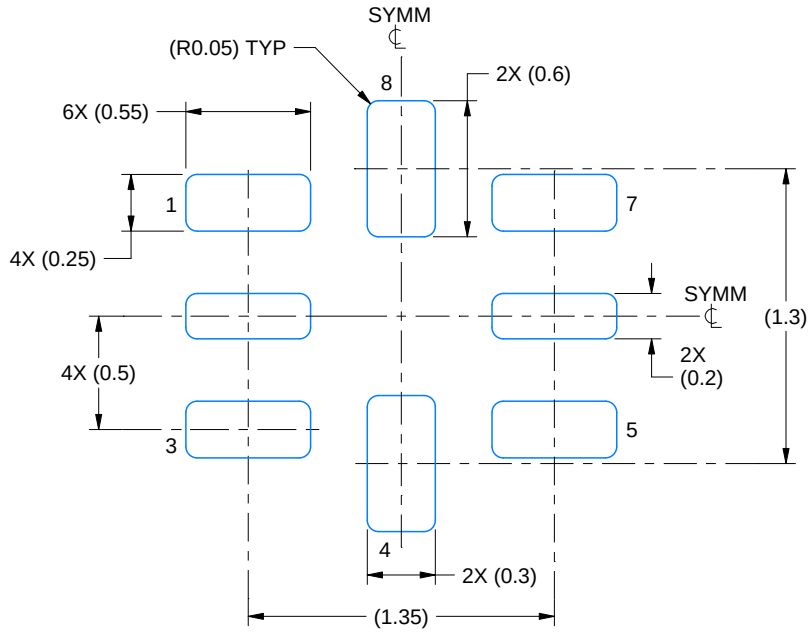
UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

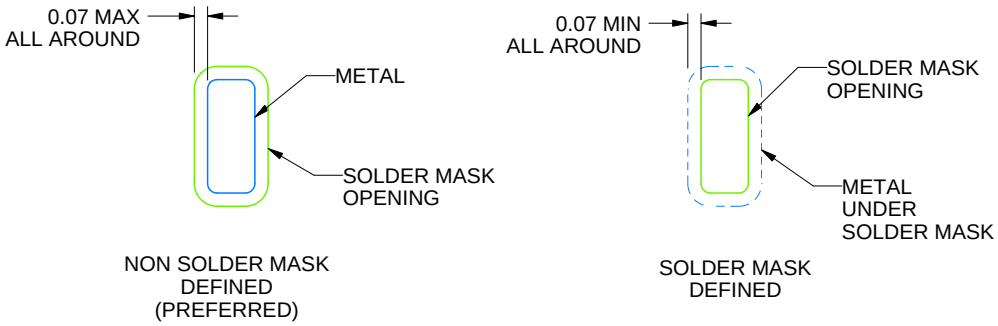


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X

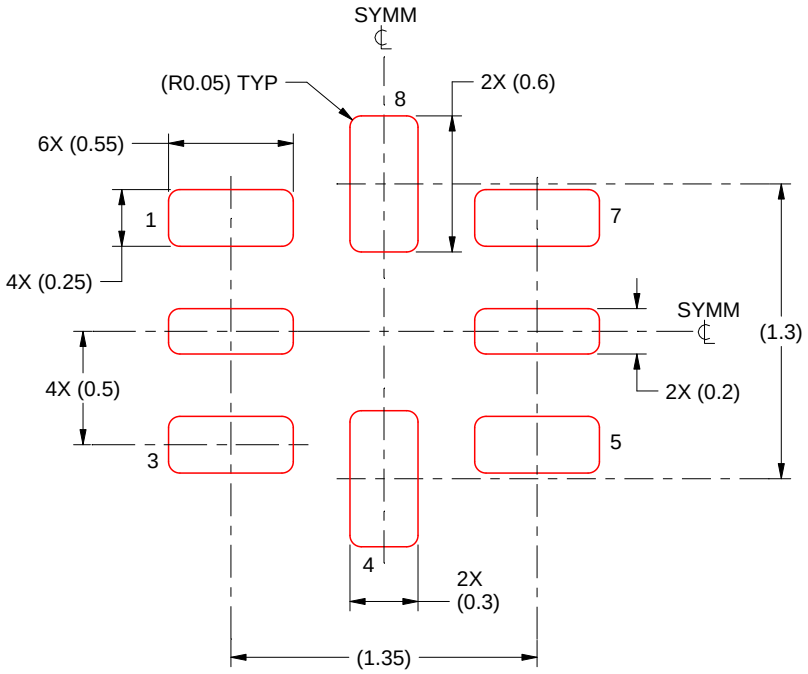


SOLDER MASK DETAILS
NOT TO SCALE

4220323/B 03/2018

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

4220323/B 03/2018

NOTES: (continued)

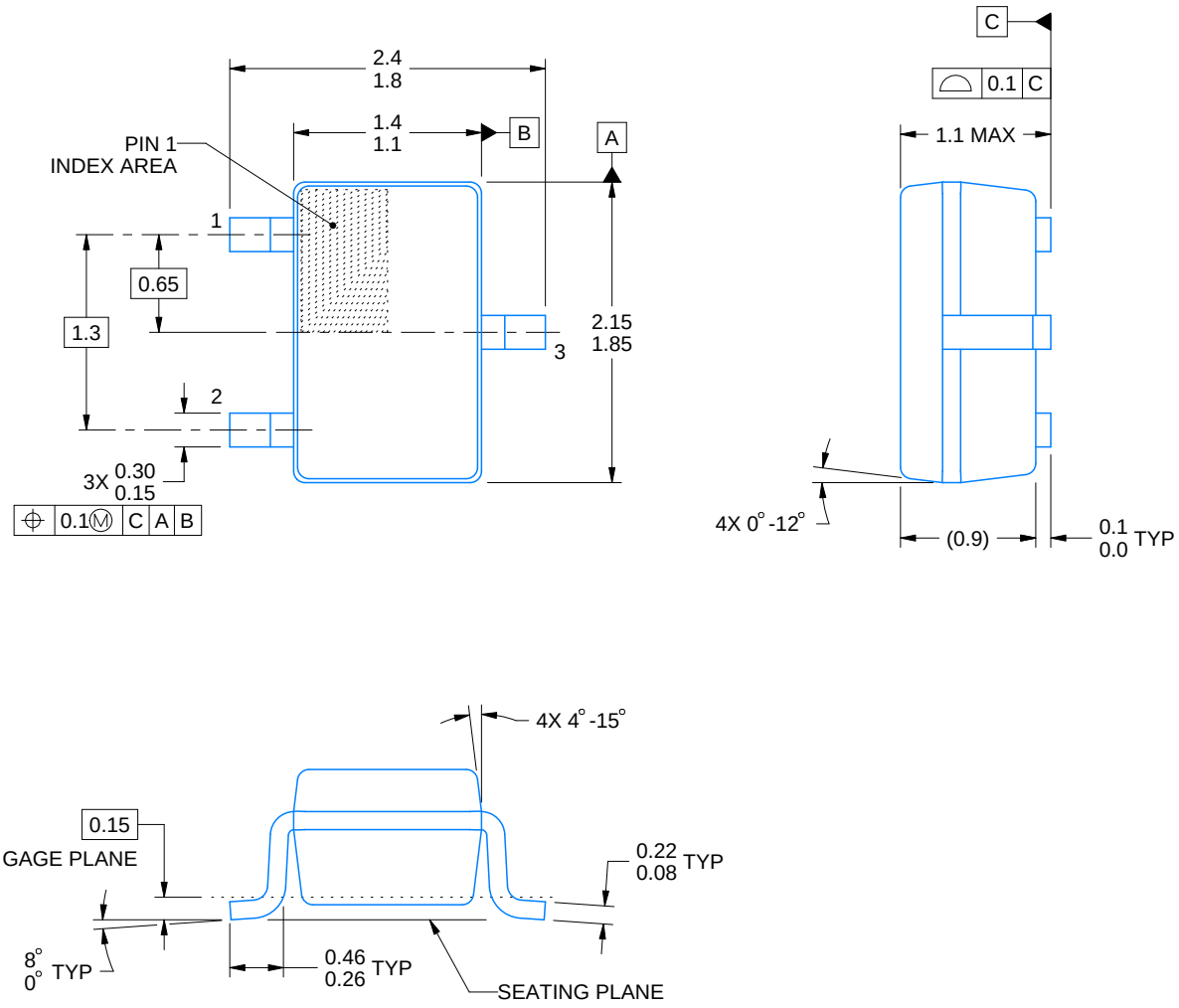
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DCK0003A

SOT-SC70 - 1.1 max height

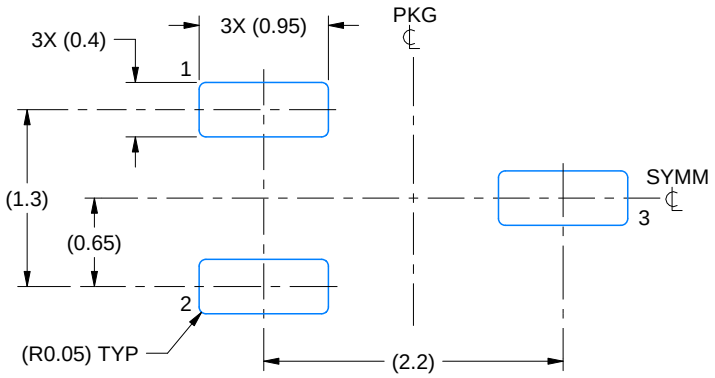
SMALL OUTLINE TRANSISTOR SC70



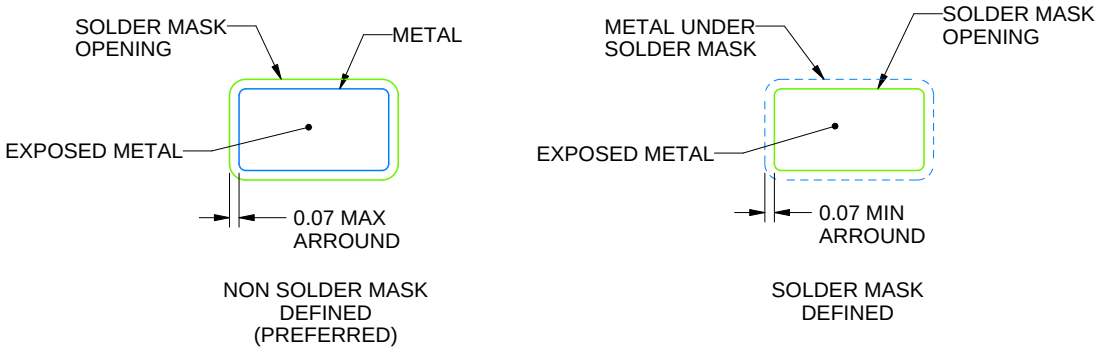
4220745/F 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

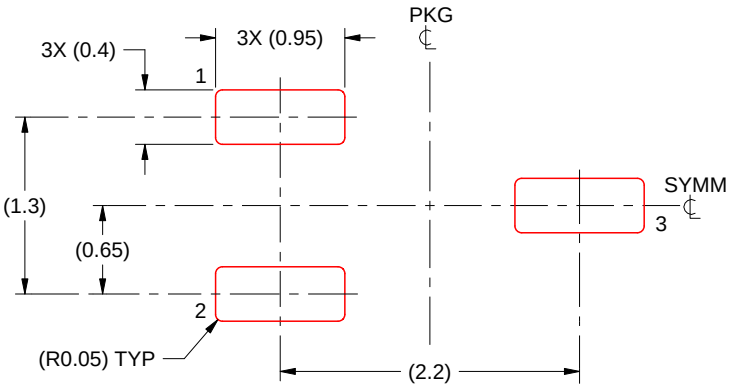


SOLDER MASK DETAILS

4220745/F 11/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4220745/F 11/2024

NOTES: (continued)

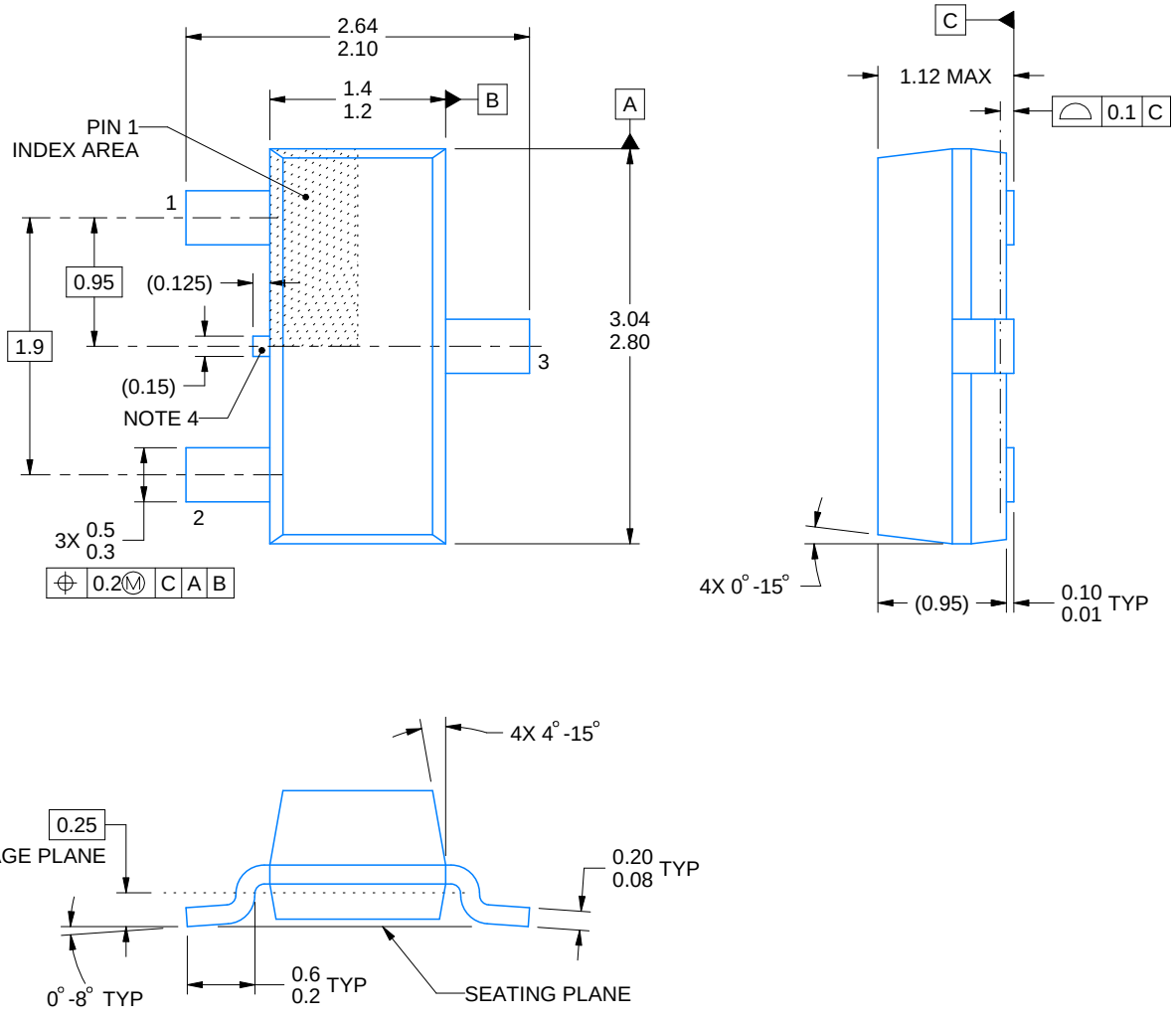
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

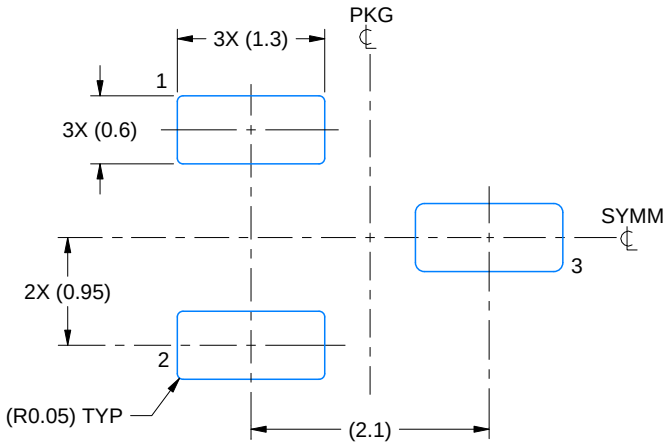
SMALL OUTLINE TRANSISTOR



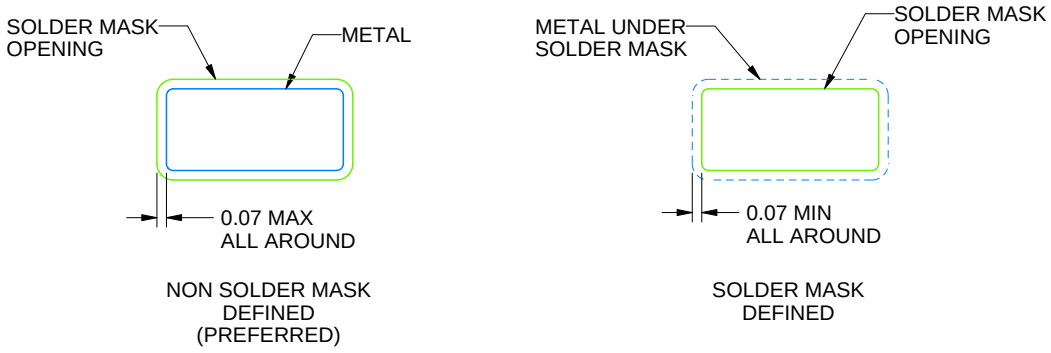
4214838/F 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
SCALE:15X

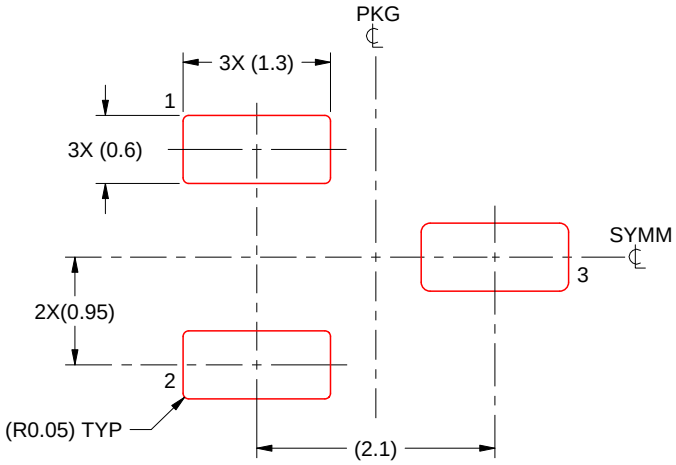


SOLDER MASK DETAILS

4214838/F 08/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/F 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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