- **Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Eliminates the Need for 3-State Overlap Protection**
- **pnp Inputs Reduce dc Loading**
- **Open-Collector Versions of ′ALS244 and ′AS244**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AS760 . . . J PACKAGE
SN74ALS760, SN74AS760 . . . DW OR N PACKAGE
(TOP VIEW)

1$\overline{\text{OE}}$	1	20	V$_{\text{CC}}$
1A1	2	19	2$\overline{\text{OE}}$
2Y4	3	18	1Y1
1A2	4	17	2A4
2Y3	5	16	1Y2
1A3	6	15	2A3
2Y2	7	14	1Y3
1A4	8	13	2A2
2Y1	9	12	1Y4
GND	10	11	2A1
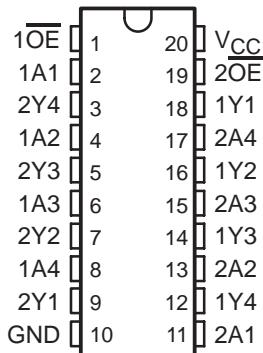
SN54AS760 . . . FK PACKAGE
(TOP VIEW)
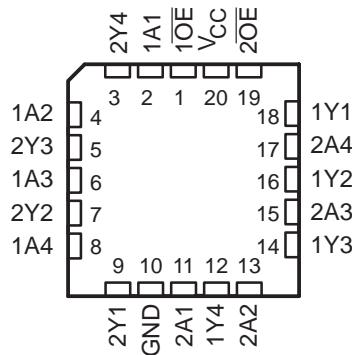
Top pins (left to right): 2Y4 (3), 1A1 (2), 1$\overline{\text{OE}}$ (1), V$_{\text{CC}}$ (20), 2$\overline{\text{OE}}$ (19)

Left			Right
1A2	4	18	1Y1
2Y3	5	17	2A4
1A3	6	16	1Y2
2Y2	7	15	2A3
1A4	8	14	1Y3

Bottom pins (left to right): 2Y1 (9), GND (10), 2A1 (11), 1Y4 (12), 2A2 (13)

description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters by eliminating the need for 3-state overlap protection. With the ′AS756 and SN74AS757, these devices provide the choice of selected combinations of inverting outputs, symmetrical active-low output-enable ($\overline{\text{OE}}$) inputs, and complementary OE and $\overline{\text{OE}}$ inputs.

The SN54AS760 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS760 and SN74AS760 are characterized for operation from 0°C to 70°C.

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TEXAS INSTRUMENTS

SN54AS760, SN74ALS760, SN74AS760
OCTAL BUFFERS AND LINE DRIVERS
WITH OPEN-COLLECTOR OUTPUTS

SDAS141A – DECEMBER 1983 – REVISED JANUARY 1995

logic symbol†

1OE — 1 → EN

1A1 — 2 — 18 — 1Y1
1A2 — 4 — 16 — 1Y2
1A3 — 6 — 14 — 1Y3
1A4 — 8 — 12 — 1Y4

2OE — 19 → EN

2A1 — 11 — 9 — 2Y1
2A2 — 13 — 7 — 2Y2
2A3 — 15 — 5 — 2Y3
2A4 — 17 — 3 — 2Y4
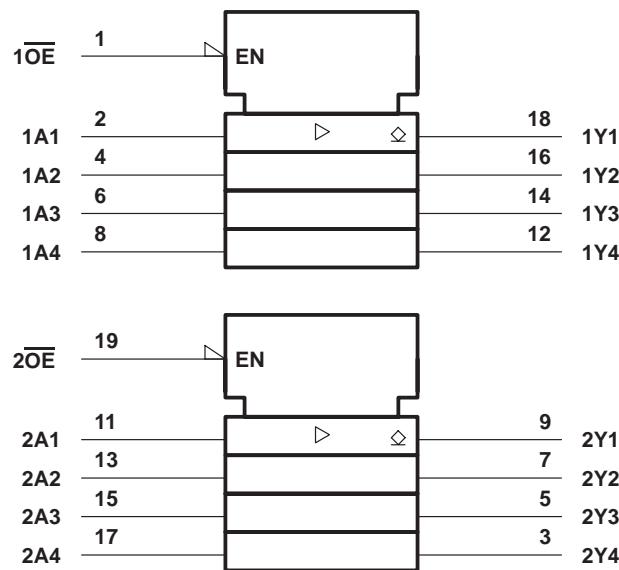
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)
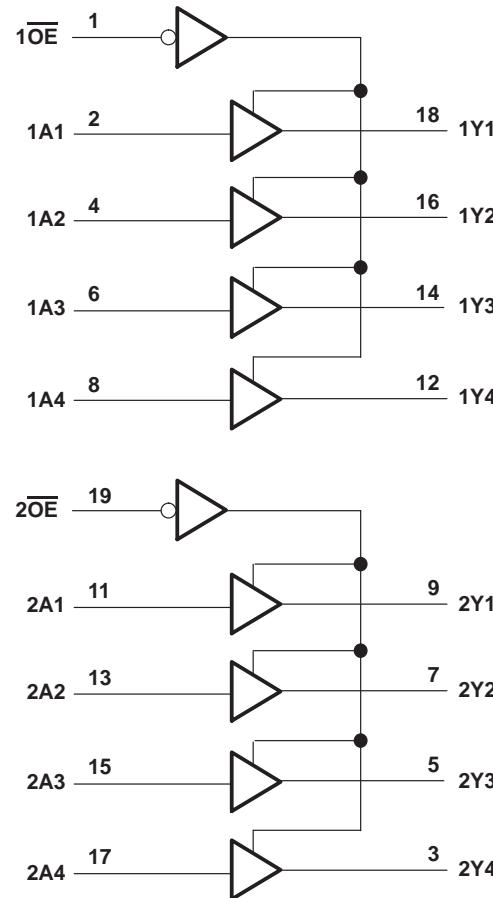
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} .... 7 V
Input voltage, V_I .... 7 V
Off-state output voltage .... 7 V
Operating free-air temperature range, T_A: SN74ALS760 .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN74ALS760			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage			5.5	V
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74ALS760			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = – 18 mA			– 1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1	mA
I_{OL}	V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4	V
		I_{OL} = 24 mA		0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			– 0.1	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		9	15	mA
		Outputs low		15	19	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX‡		UNIT
			SN74ALS760		
			MIN	MAX	
t_{PLH}	A	Y	5	15	ns
t_{PHL}			5	12	
t_{PLH}	$\overline{OE}$	Y	5	16	ns
t_{PHL}			5	13	

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage, V_{CC} .... 7 V
Input voltage, V_I .... 7 V
Off-state output voltage .... 7 V
Operating free-air temperature range, T_A: SN54AS760 .... –55°C to 125°C
                                            SN74AS760 .... 0°C to 70°C
Storage temperature range .... –65°C to 150°C

§ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

TEXAS INSTRUMENTS

recommended operating conditions

		SN54AS760			SN74AS760			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS760			SN74AS760			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 48 mA			0.55				V
			I_{OL} = 64 mA						0.55	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	$\overline{OE}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A					−1			−1	
I_{CC}		V_{CC} = 5.5 V	Outputs high		20	32		20	32	mA
			Outputs low		60	94		60	94	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX‡				UNIT
			SN54AS760		SN74AS760		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	19.5	3	18.5	ns
t_{PHL}			1	7	1	6	
t_{PLH}	$\overline{OE}$	Y	3	19.5	3	18.5	ns
t_{PHL}			1	8	1	7	

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES

LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS

LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS

LOAD CIRCUIT
FOR 3-STATE OUTPUTS

$R_L = R1 = R2$

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PULSE DURATIONS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
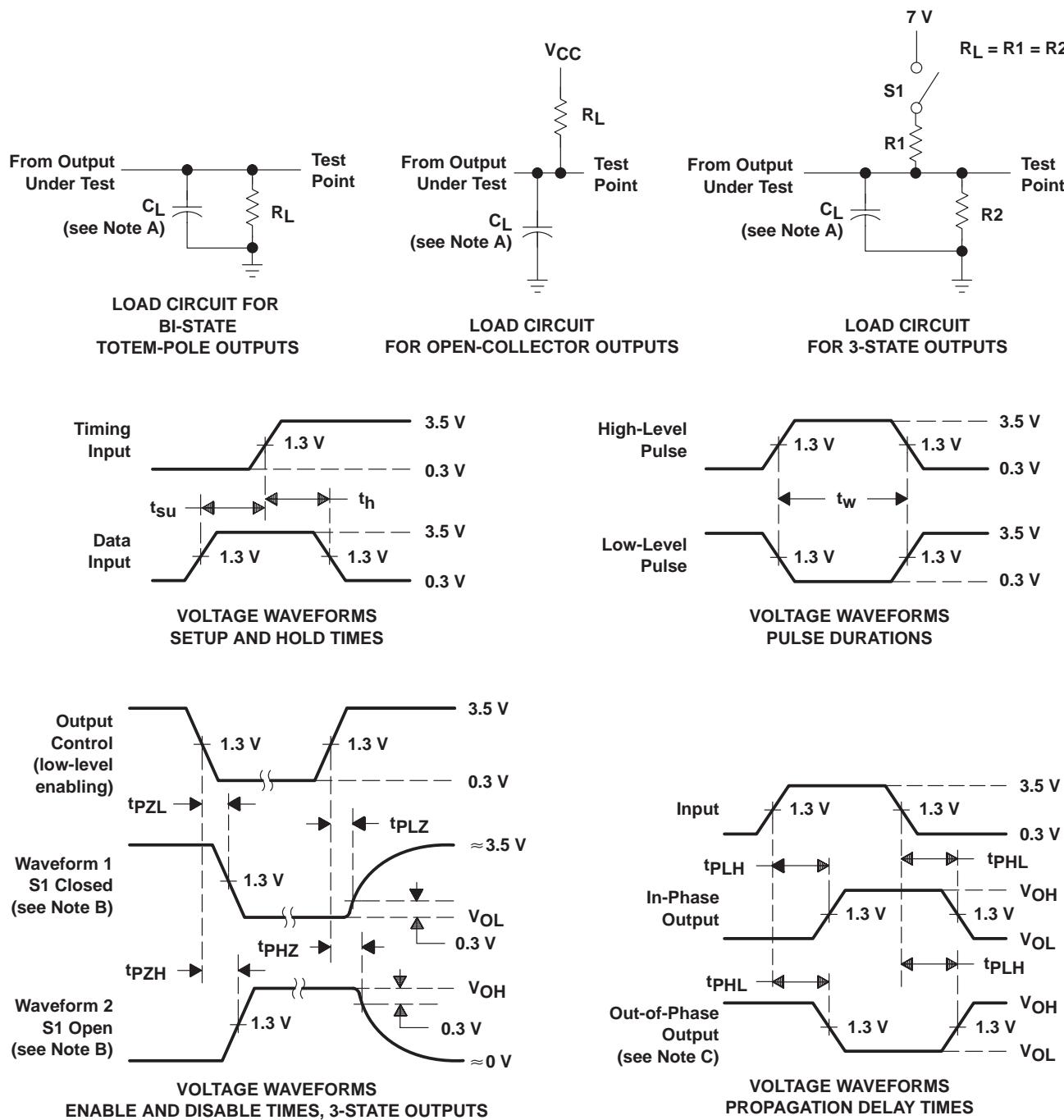
NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
   D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
   E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number (1)	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-87767012A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-87767012A SNJ54AS 760FK
5962-8776701RA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8776701RA SNJ54AS760J
SN74ALS760DW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS760
SN74ALS760DW.A	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS760
SN74ALS760DWG4	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS760
SN74ALS760N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS760N
SN74ALS760N.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS760N
SN74AS760DW	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	0 to 70	AS760
SN74AS760DWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS760
SN74AS760DWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS760
SN74AS760N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74AS760N
SN74AS760N.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74AS760N
SN74AS760NSR	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74AS760
SN74AS760NSR.A	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74AS760
SNJ54AS760FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-87767012A SNJ54AS 760FK
SNJ54AS760FK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-87767012A SNJ54AS 760FK
SNJ54AS760J	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8776701RA SNJ54AS760J
SNJ54AS760J.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8776701RA SNJ54AS760J

(1) Status: For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AS760, SN74AS760 :

● Catalog : SN74AS760

● Military : SN54AS760

NOTE: Qualified Version Definitions:

  ● Catalog - TI's standard catalog product

  ● Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS
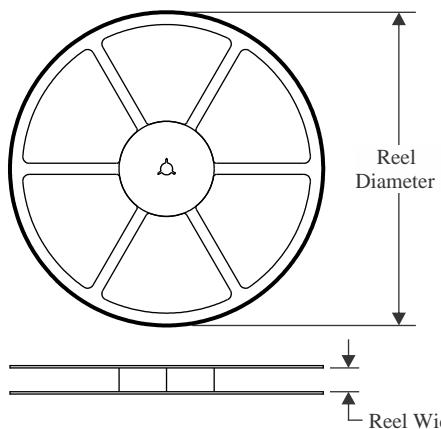
TAPE DIMENSIONS
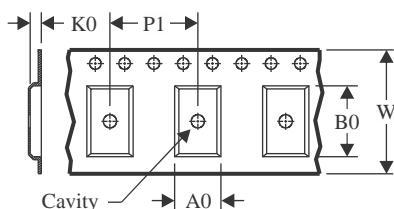
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
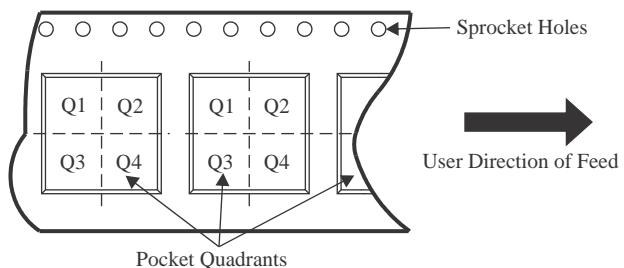
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AS760DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AS760NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AS760DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AS760NSR	SOP	NS	20	2000	356.0	356.0	45.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-87767012A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74ALS760DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS760DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS760DWG4	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS760N	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS760N.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74AS760N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AS760N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54AS760FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AS760FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

MECHANICAL DATA

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70
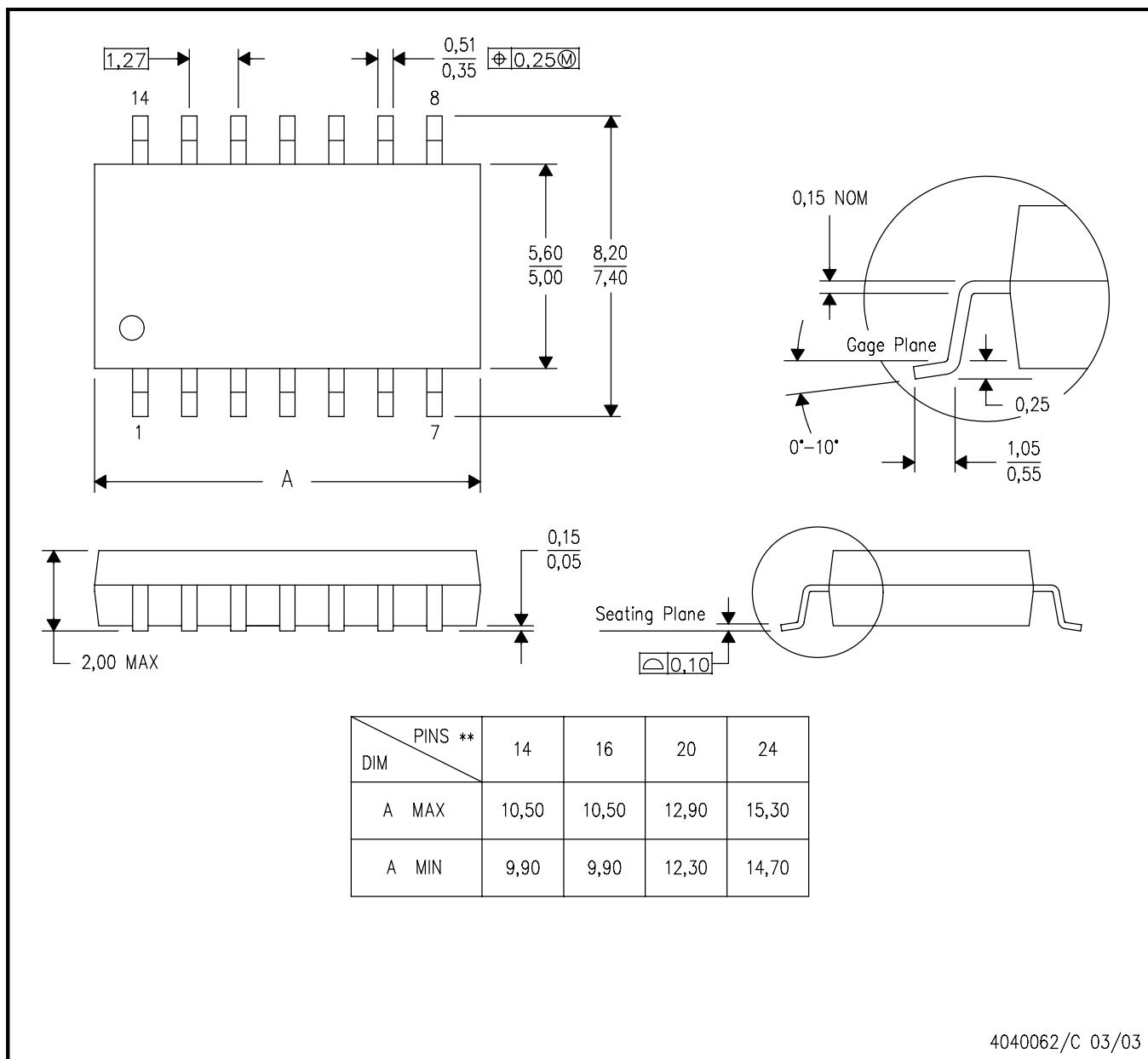
4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)   CERAMIC DUAL IN-LINE PACKAGE
14 LEADS SHOWN

DIM	PINS **	14	16	18	20
A		0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B	MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B	MIN	——	——	——	——
C	MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C	MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

1   7

$\dfrac{0.065 \ (1,65)}{0.045 \ (1,14)}$

C

0.005 (0,13) MIN

$\dfrac{0.060 \ (1,52)}{0.015 \ (0,38)}$

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

$\dfrac{0.026 \ (0,66)}{0.014 \ (0,36)}$

0.100 (2,54)

A

0°-15°

$\dfrac{0.014 \ (0,36)}{0.008 \ (0,20)}$
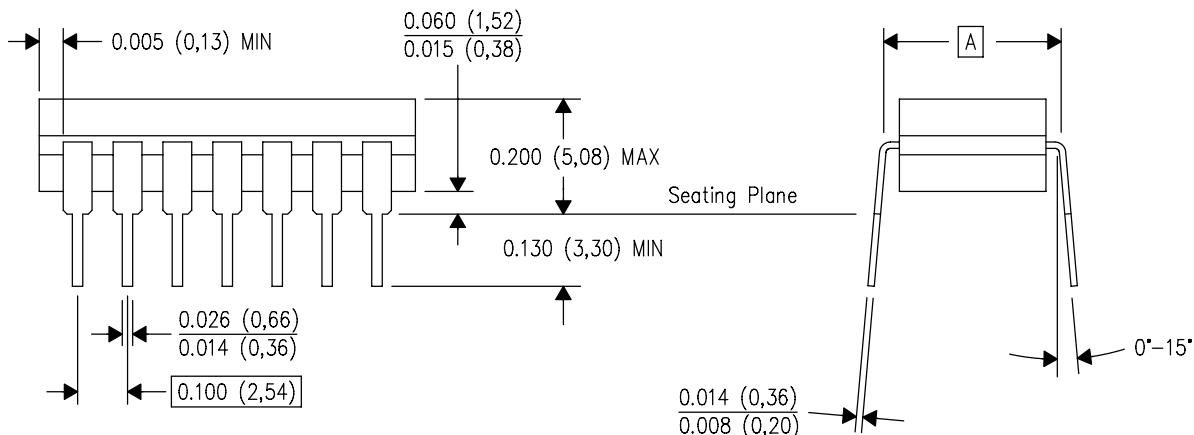
4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package is hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK 20

8.89 x 8.89, 1.27 mm pitch

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.
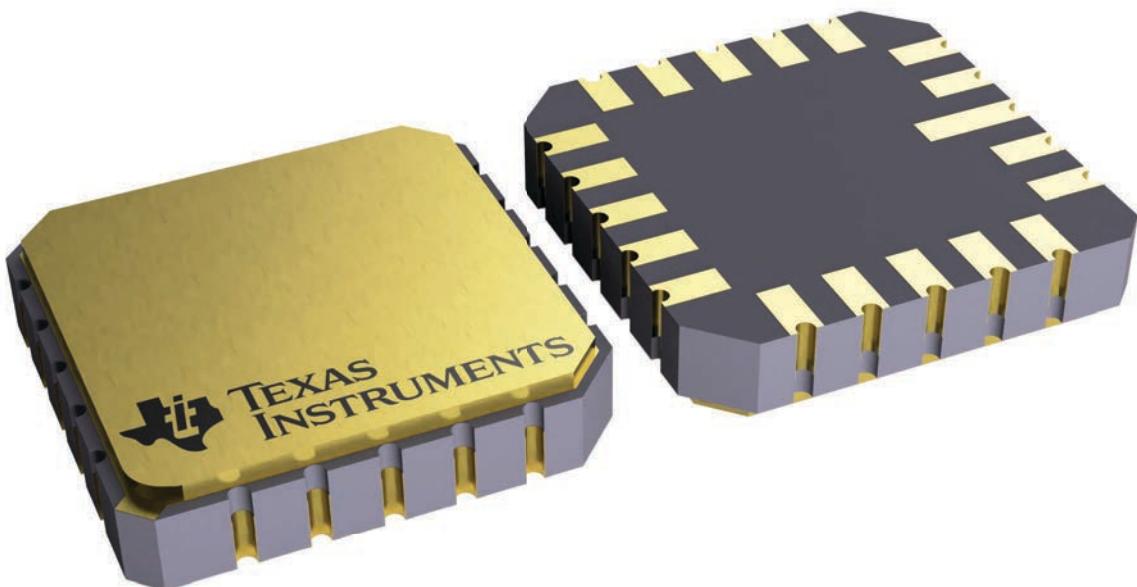
4229370VA\

N (R−PDIP−T**)

PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

DIM / PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION ⚠C	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14) ⚠D

0.045 (1,14) / 0.030 (0,76) ⚠D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option ⚠D

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
   B. This drawing is subject to change without notice.
   ⚠C Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
   ⚠D The 20 pin end lead shoulder width is a vendor option, either half or full width.

10.63 / 9.97 TYP

A

PIN 1 ID
AREA

1

18X 1.27

20

13.0
12.6
NOTE 3

2X
11.43

10

11

B

7.6
7.4
NOTE 4

20X 0.51 / 0.31

⊕ 0.25 Ⓜ C A B

C

SEATING PLANE

⌒ 0.1 C

2.65 MAX

0.33 / 0.10 TYP

SEE DETAIL A

0.25
GAGE PLANE

0° - 8°

1.27
0.40

0.3
0.1

DETAIL A
TYPICAL

4220724/A   05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

20X (2)

SYMM

1

20X (0.6)

18X (1.27)

20

(R0.05)
TYP

SYMM

10

11

(9.3)
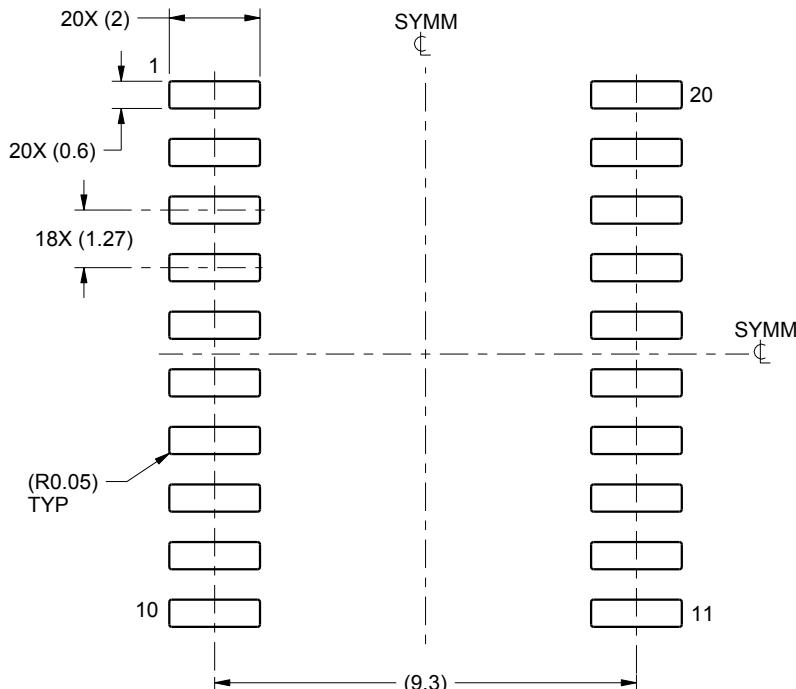
LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED
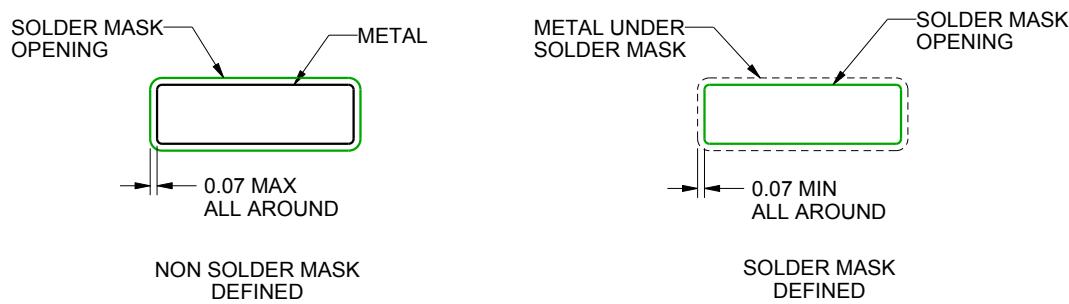
SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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