SNx4HC373 Octal Transparent D-Type Latches With 3-State Outputs

1 Features

- Wide operating voltage range of 2V to 6V
- High-current 3-state true outputs can drive up to 15 LSTTL loads
- Low power consumption, 80µA max I_{CC}
- Typical t_{pd} = 13ns
- ±6mA output drive at 5V
- Low input current of 1µA max
- Eight high-current latches in a single package
- Full parallel access for loading

2 Description

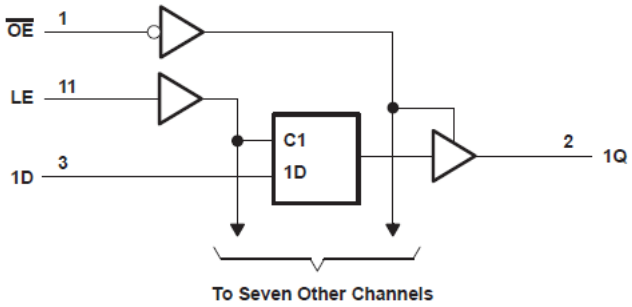
These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'HC373 devices are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE(2)
SN74HC373	DW (SOIC, 20)	12.80 mm × 7.50 mm
	DB (SSOP, 20)	7.20 mm × 5.30 mm
	N (PDIP, 20)	25.40 mm × 6.35 mm
	NS (SOP, 20)	15.00 mm × 5.30 mm
	PW (TSSOP, 20)	6.50 mm × 4.40 mm
SN54HC373	J (CDIP, 20)	26.92 mm × 6.92 mm
	FK (LCCC, 20)	8.89 mm × 8.45 mm
	W (CFP, 20)	13.72 mm × 6.92 mm

(1) For more information, see Section 10.
(2) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)

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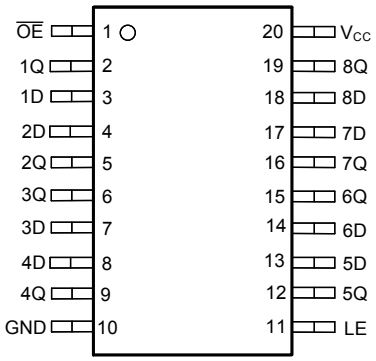
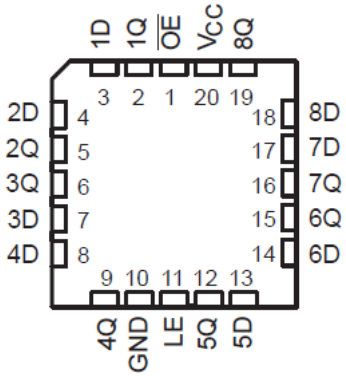
3 Pin Configuration and Functions



J, W, FK, DB, DW, N, NS, or PW package
20--Pin CDIP, CFP, LCCC, SSOP, SOIC, PDIP, SO, or TSSOP
Top View



FK package
20-Pin LCCC
Top View

Table 3-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
$\overline{OE}$	1	Input	Output enable, active low
1Q	2	Output	Output for channel 1
1D	3	Input	Input for channel 1
2D	4	Input	Input for channel 2
2Q	5	Output	Output for channel 2
3Q	6	Output	Output for channel 3
3D	7	Input	Input for channel 3
4D	8	Input	Input for channel 4
4Q	9	Output	Output for channel 4
GND	10	—	Ground
LE	11	Input	Latch enable
5Q	12	Output	Output for channel 5
5D	13	Input	Input for channel 5
6D	14	Input	Input for channel 6
6Q	15	Output	Output for channel 6
7Q	16	Output	Output for channel 7
7D	17	Input	Input for channel 7
8D	18	Input	Input for channel 8
8Q	19	Output	Output for channel 8
V_{CC}	20	—	Positive supply

1. I = input, O = output, P = power, FB = feedback, GND = ground, N/A = not applicable

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4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < 0$ or $V_I > V_{CC}$		±20	mA
I_{OK}	Output clamp current(2)	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Section 4.2” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)(1)

			SN54HC373			SN74HC373			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5			0.5	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 6 V			1.8			1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise and fall time	V_{CC} = 2 V			1000			1000	ns
		V_{CC} = 4.5 V			500			500	
		V_{CC} = 6 V			400			400	
T_A	Operating free-air temperature		–55		125	–55		125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

4.3 Thermal Information

THERMAL METRIC		SN74HC373					UNIT
		DW (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	
		20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1)	109.1	122.7	84.6	113.4	131.8	°C/W
$R_{\theta JC\ (top)}$	Junction-to-case (top) thermal resistance	76	81.6	72.5	78.6	72.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.6	77.5	65.3	78.4	82.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	51.5	46.1	55.3	47.1	21.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	77.1	77.1	65.2	78.1	82.4	°C/W

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4.3 Thermal Information (continued)

THERMAL METRIC		SN74HC373					UNIT
		DW (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	
		20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

4.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC373		SN74HC373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 µA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		3.7		3.7		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		5.2		5.2		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.4	
		I_{OL} = 7.8 mA	6 V		0.15	0.26		0.4		0.4	
I_I	V_I = V_{CC} or 0		6 V			±0.1	±100		±1000		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		6 V			±0.01	±0.5		±10		±10	µA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		160	µA
C_i			2 V to 6 V		3	10		10		10	pF

4.5 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HC373		SN74HC373		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	2 V	80		120		120		ns
		4.5 V	16		24		24		
		6 V	14		20		20		
t_{su}	Setup time, data before LE↓	2 V	50		75		75		ns
		4.5 V	10		15		15		
		6 V	9		13		13		
t_h	Hold time, data after LE↓	2 V	20		26		26		ns
		4.5 V	10		13		13		
		6 V	10		13		13		

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4.6 Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 5-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC373		SN74HC373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	2 V		58	150		225		225	ns
			4.5 V		15	30		45		45	
			6 V		13	26		38		38	
	LE	Any Q	2 V		73	175		265		265	
			4.5 V		18	35		53		53	
			6 V		15	30		45		45	
t_{en}	$\overline{OE}$	Any Q	2 V		65	150		225		225	ns
			4.5 V		17	30		45		45	
			6 V		14	26		38		38	
t_{dis}	$\overline{OE}$	Any Q	2 V		50	150		225		225	ns
			4.5 V		15	30		45		45	
			6 V		13	26		38		38	
t_t		Any Q	2 V		28	60		90		90	ns
			4.5 V		8	12		18		18	
			6 V		6	10		15		15	

4.7 Switching Characteristics

over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 5-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC373		SN74HC373		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	2 V		82	200		300		300	ns
			4.5 V		22	40		60		60	
			6 V		19	34		51		51	
	LE	Any Q	2 V		100	225		335		335	
			4.5 V		24	45		67		67	
			6 V		20	38		57		57	
t_{en}	$\overline{OE}$	Any Q	2 V		90	200		300		300	ns
			4.5 V		23	40		60		60	
			6 V		19	34		51		51	
t_t		Any Q	2 V		45	210		315		315	ns
			4.5 V		17	42		63		63	
			6 V		13	36		53		53	

4.8 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	No load	100	pF

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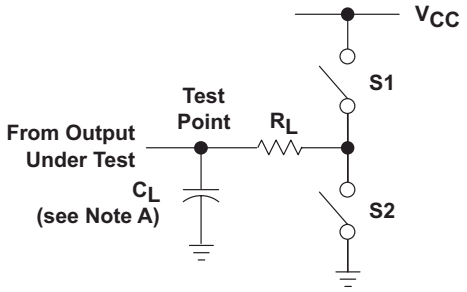
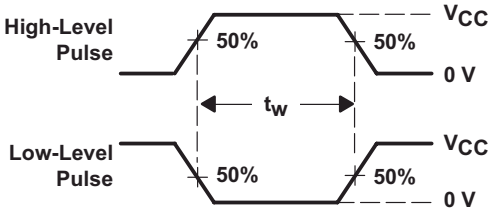
5 Parameter Measurement Information

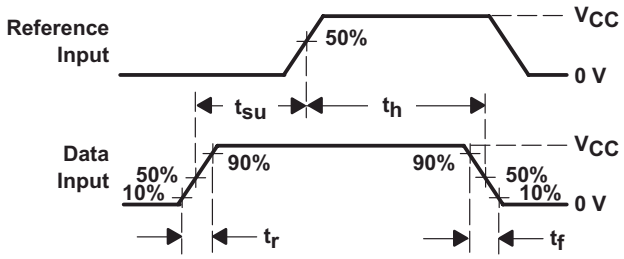


LOAD CIRCUIT

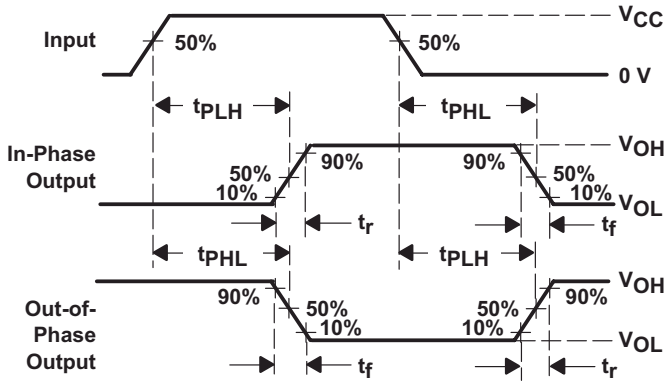
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		––	50 pF or 150 pF	Open	Open



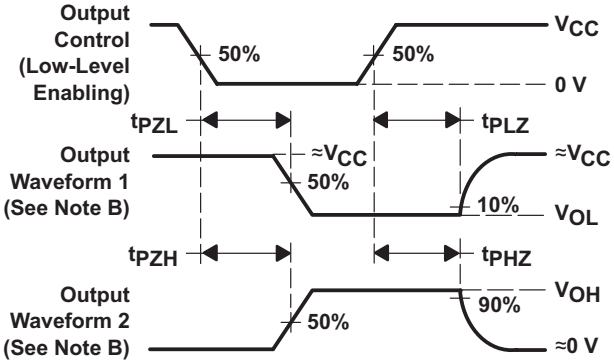
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 5-1. Load Circuit and Voltage Waveforms

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6 Detailed Description

6.1 Overview

The SNx4HC373 contains eight D-type latches. All channels share a latch enable (LE) and output enable ($\overline{OE}$) input.

When the latch is enabled (LE is high), data is allowed to pass through from the D inputs to the Q outputs.

When the latch is disabled (LE is low), the Q outputs hold the last state they had regardless of changes at the D inputs.

If the latch enable (LE) input is held low during startup, the output state of all channels is unknown until the latch enable (LE) input is driven high with valid input signals at all data (D) inputs.

When the outputs are enabled ($\overline{OE}$ is low), the outputs are actively driving low or high.

When the outputs are disabled ($\overline{OE}$ is high), the outputs are set into the high-impedance state.

The active low output enable ($\overline{OE}$) does not have any impact on the stored state in the latches.

6.2 Functional Block Diagram

6.3 Feature Description

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6.4 Device Functional Modes

Table 6-1. Function Table

INPUTS(1)			OUTPUT(2)
$\overline{OE}$	LE	D	Q
L	H	L	L
L	H	H	H
L	L	X	Q_0 (3)
H	X	X	Z

(1) L = input low, H = input high, ↑ = input transitioning from low to high, ↓ = input transitioning from high to low, X = don't care
(2) L = output low, H = output high, Q_0 = previous state, Z = high impedance
(3) At startup, Q_0 is unknown

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

In this application, the SNx4HC373 is used to control an 8-bit data bus.

Outputs can be held in the high-impedance state, held in the last known state, or change together with the data inputs, depending on the control inputs at LE and $\overline{OE}$ coming from the bus controller.

7.2 Typical Application

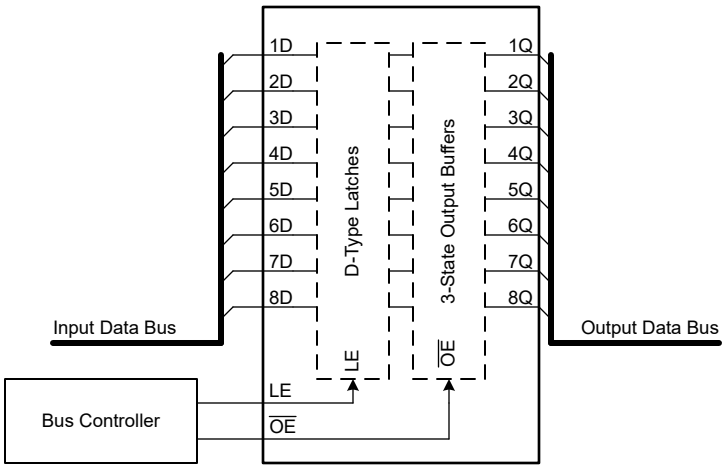

Figure 7-1. Typical Application Block Diagram

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7.2.1 Design Requirements

7.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SNx4HC373 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SNx4HC373 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SNx4HC373 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in *CMOS Power Consumption and Cpd Calculation*.

Thermal increase can be calculated using the information provided in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

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7.2.1.2 Input Considerations

Input signals must cross to be considered a logic LOW, and to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SNx4HC373 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

7.2.1.3 Output Considerations

The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

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7.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SNx4HC373 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$)Ω. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

7.2.3 Application Curves

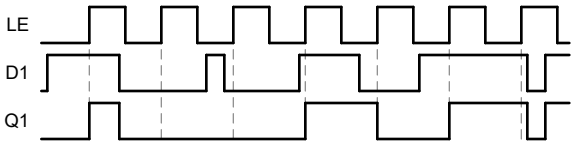

Figure 7-2. Application Timing Diagram

7.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

7.4 Layout

7.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

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7.4.2 Layout Example

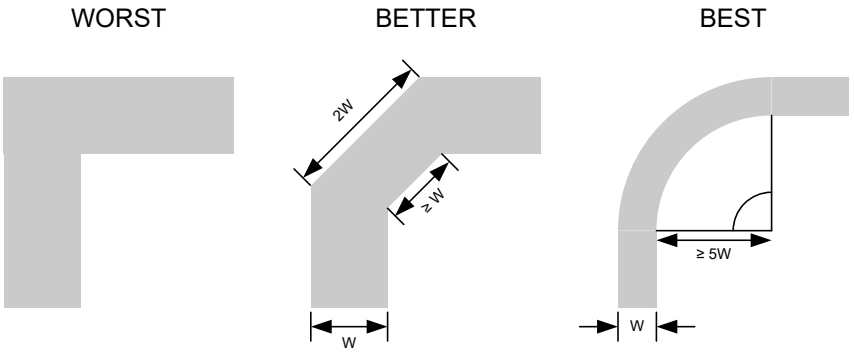

Figure 7-3. Example trace corners for improved signal integrity

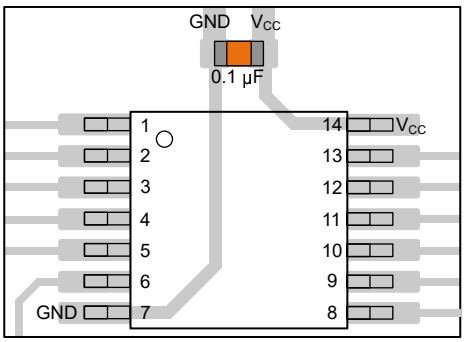

Figure 7-4. Example bypass capacitor placement for TSSOP and similar packages

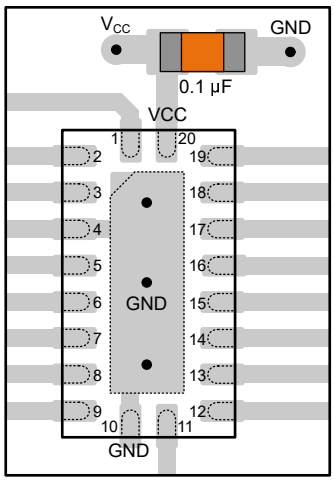

Figure 7-5. Example bypass capacitor placement for WQFN and similar packages

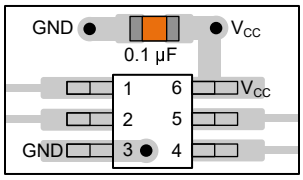

Figure 7-6. Example bypass capacitor placement for SOT, SC70 and similar packages

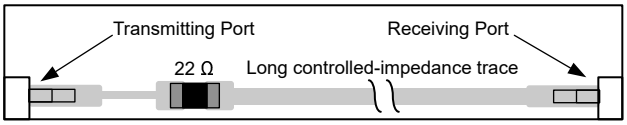

Figure 7-7. Example damping resistor placement for improved signal integrity

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8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application report
- Texas Instruments, *Designing With Logic* application report

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (April 2022) to Revision G (February 2025)	Page
• Updated SN74AC32 operating temperature to 125°C and respective values in *Electrical Characteristics* table, *Recommended Operating Conditions* table, *Timing Characteristics* table, and *Switching Characteristics* tables	1
• Added *Pin Functions* table	3

Changes from Revision E (January 2022) to Revision F (April 2022)	Page
• Junction-to-ambient thermal resistance values increased. DW was 58 is now 109.1, DB was 70 is now 122.7, N was 69 is now 84.6, NS was 60 is now 113.4, PW was 83 is now 131.8	4

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8407201VRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8407201VRA SNV54HC373J
5962-8407201VRA.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8407201VRA SNV54HC373J
5962-8407201VSA	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8407201VSA SNV54HC373W
5962-8407201VSA.A	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8407201VSA SNV54HC373W
84072012A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84072012A SNJ54HC 373FK
8407201RA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8407201RA SNJ54HC373J
8407201SA	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8407201SA SNJ54HC373W
JM38510/65403B2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65403B2A
JM38510/65403B2A.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65403B2A
JM38510/65403BRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65403BRA
JM38510/65403BRA.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65403BRA
M38510/65403B2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65403B2A
M38510/65403BRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65403BRA
SN54HC373J	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC373J
SN54HC373J.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC373J
SN74HC373DBR	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC373

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HC373DBR.A	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC373
SN74HC373DW	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	-40 to 85	HC373
SN74HC373DWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC373
SN74HC373DWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC373
SN74HC373DWRE4	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC373
SN74HC373N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC373N
SN74HC373N.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC373N
SN74HC373NE4	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC373N
SN74HC373NSR	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC373
SN74HC373NSR.A	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC373
SN74HC373NSRE4	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC373
SN74HC373PW	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	-40 to 85	HC373
SN74HC373PWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC373
SN74HC373PWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC373
SN74HC373PWRE4	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC373
SNJ54HC373FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84072012A SNJ54HC 373FK
SNJ54HC373FK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84072012A SNJ54HC 373FK
SNJ54HC373J	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8407201RA SNJ54HC373J
SNJ54HC373J.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8407201RA SNJ54HC373J
SNJ54HC373W	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8407201SA SNJ54HC373W
SNJ54HC373W.A	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8407201SA SNJ54HC373W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HC373, SN54HC373-SP, SN74HC373 :

- Catalog : SN74HC373, SN54HC373
- Military : SN54HC373
- Space : SN54HC373-SP

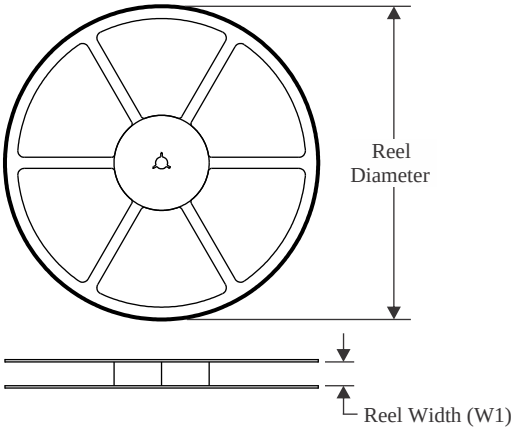
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

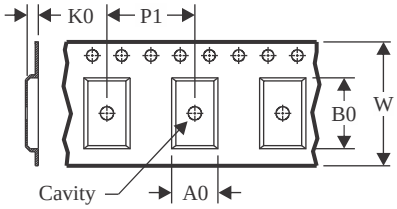
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

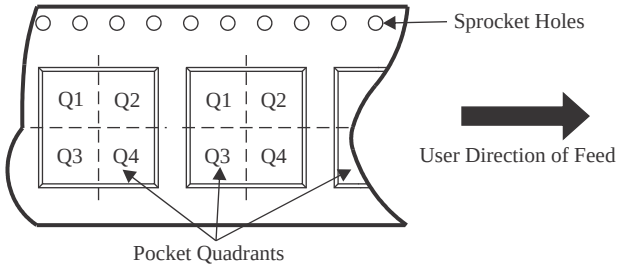


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

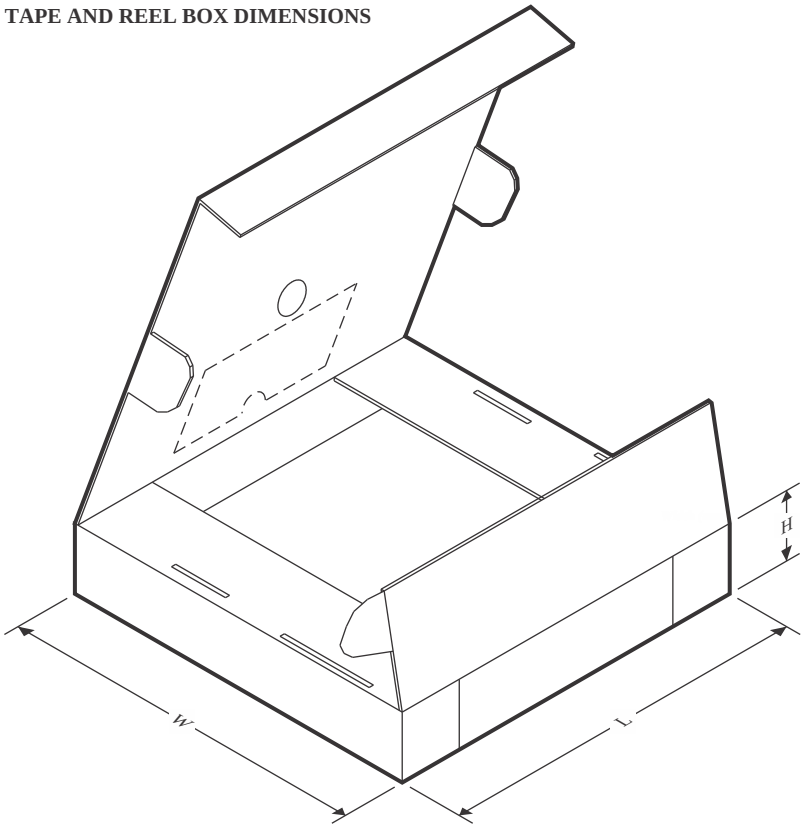
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC373DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74HC373DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74HC373NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74HC373PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

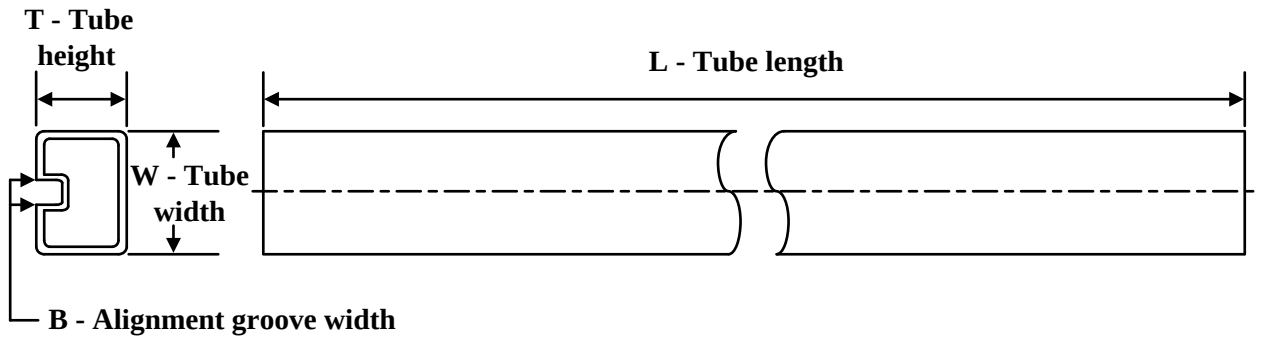
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC373DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74HC373DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74HC373NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74HC373PWR	TSSOP	PW	20	2000	353.0	353.0	32.0

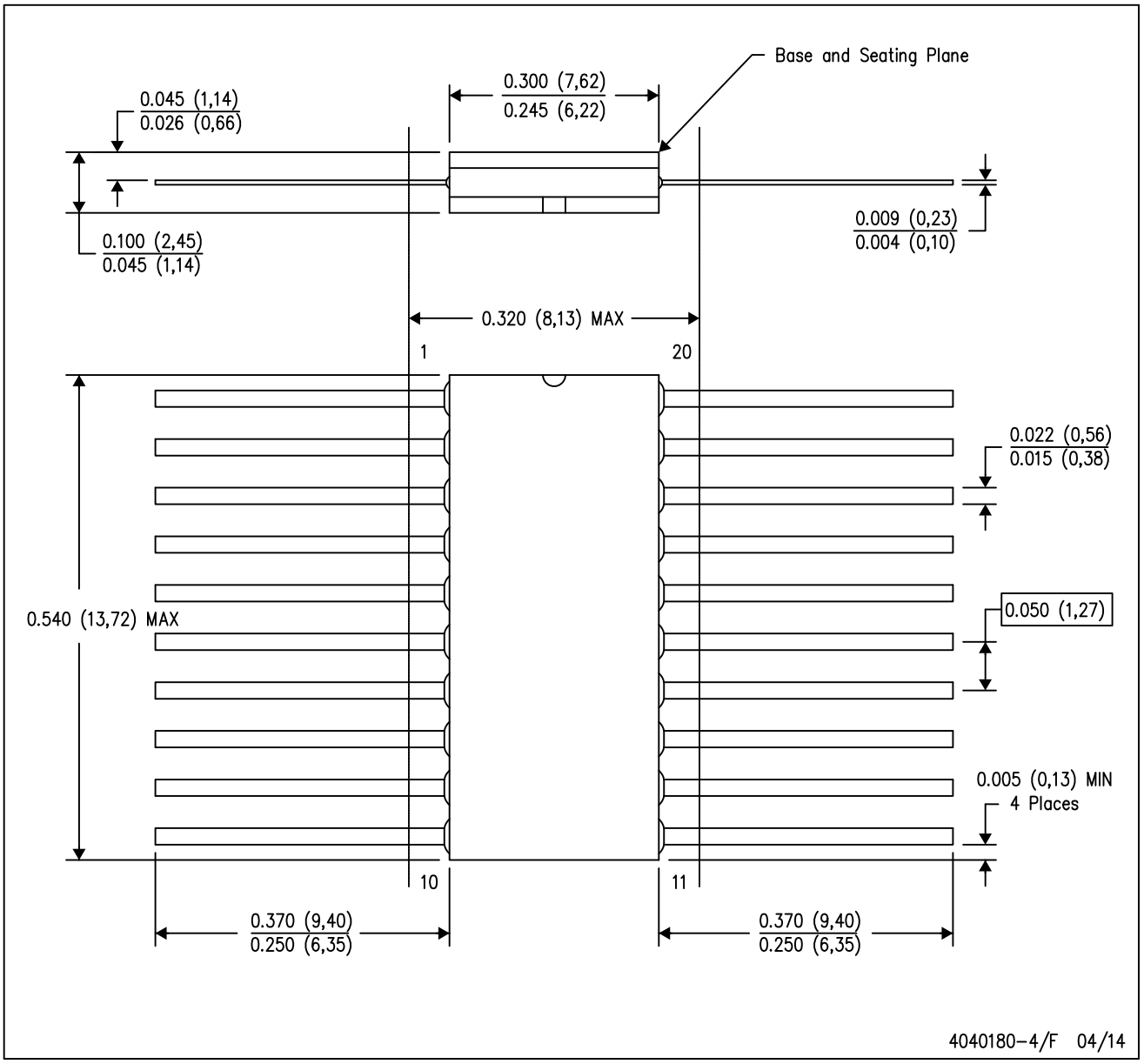
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-8407201VSA	W	CFP	20	25	506.98	26.16	6220	NA
5962-8407201VSA.A	W	CFP	20	25	506.98	26.16	6220	NA
84072012A	FK	LCCC	20	55	506.98	12.06	2030	NA
8407201SA	W	CFP	20	25	506.98	26.16	6220	NA
JM38510/65403B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/65403B2A.A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/65403B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74HC373N	N	PDIP	20	20	506	13.97	11230	4.32
SN74HC373N.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74HC373NE4	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54HC373FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC373FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC373W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54HC373W.A	W	CFP	20	25	506.98	26.16	6220	NA

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



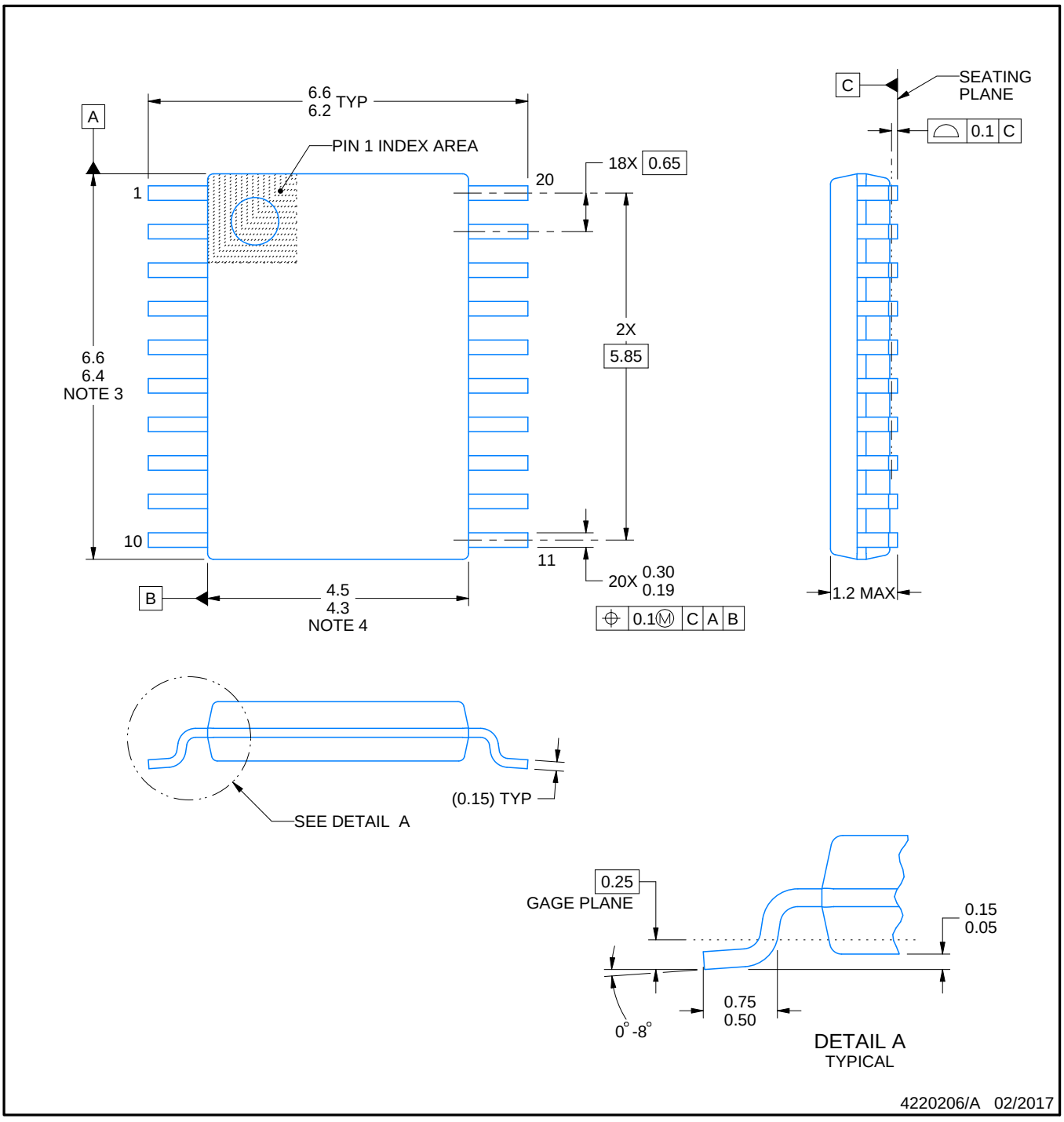
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

PACKAGE OUTLINE

PW0020A

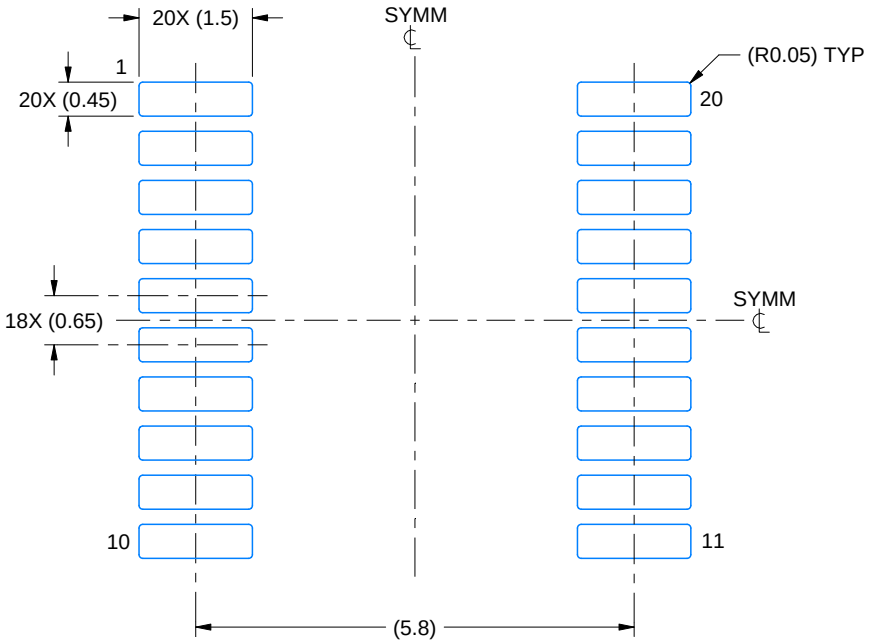
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

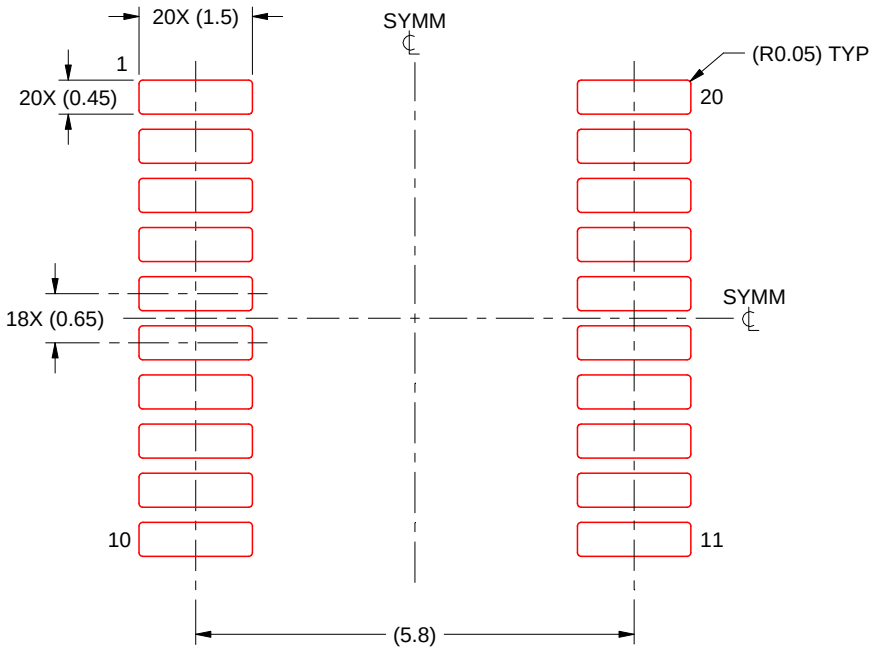
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



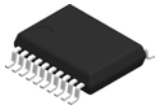
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

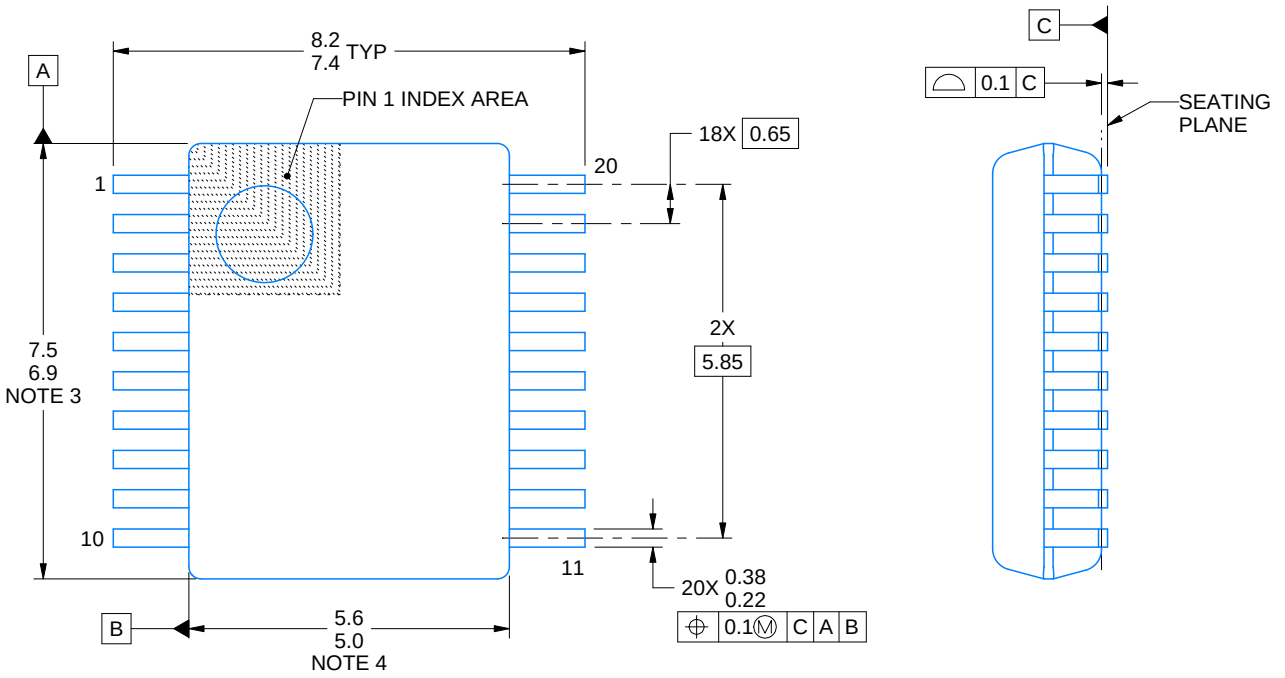
DB0020A

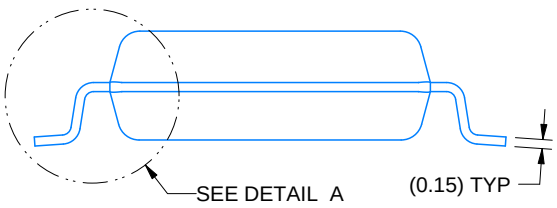


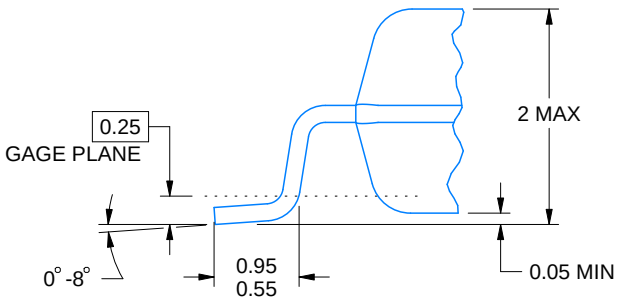
PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE





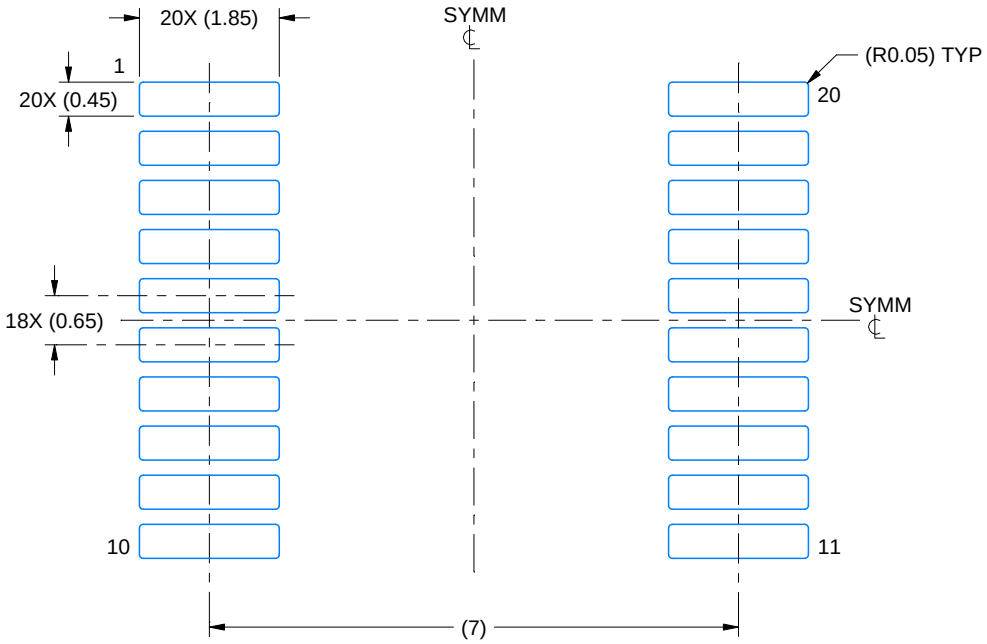


DETAIL A
TYPICAL

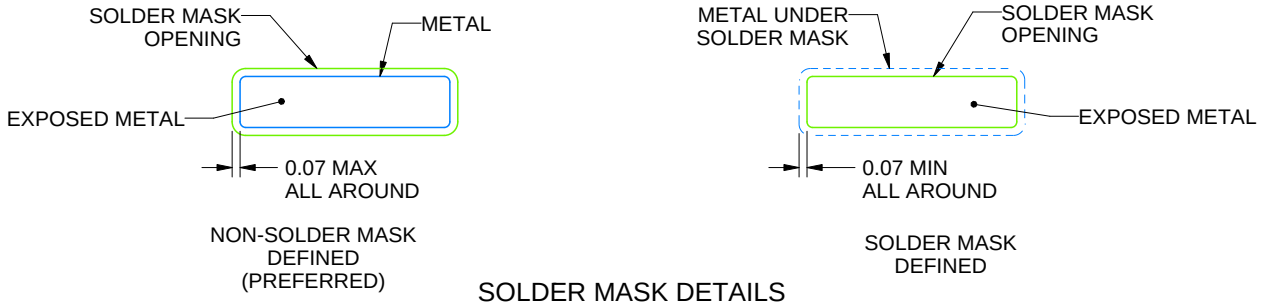
4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

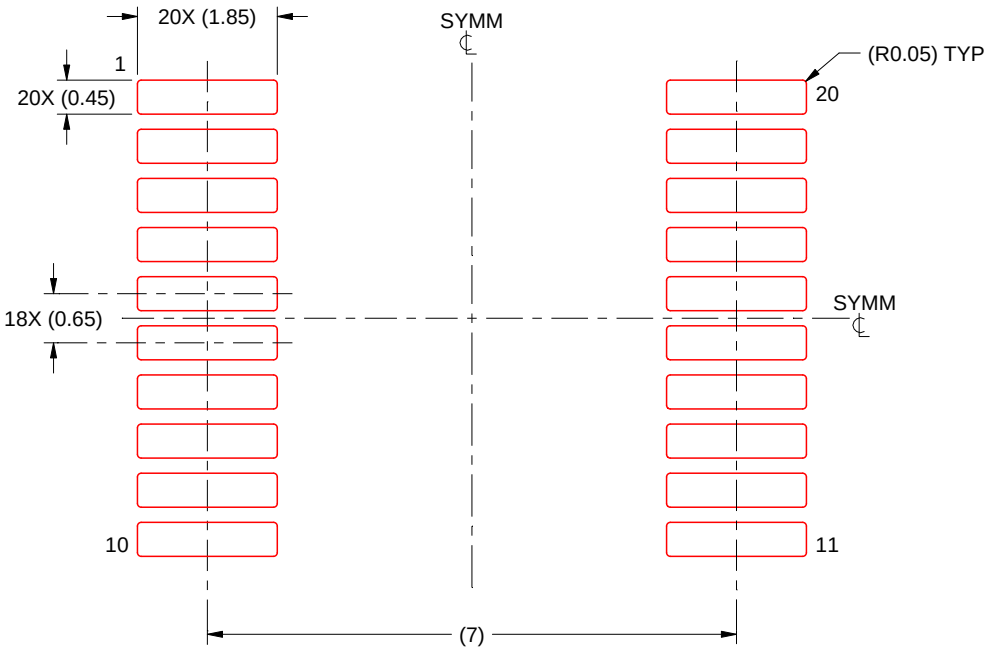
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

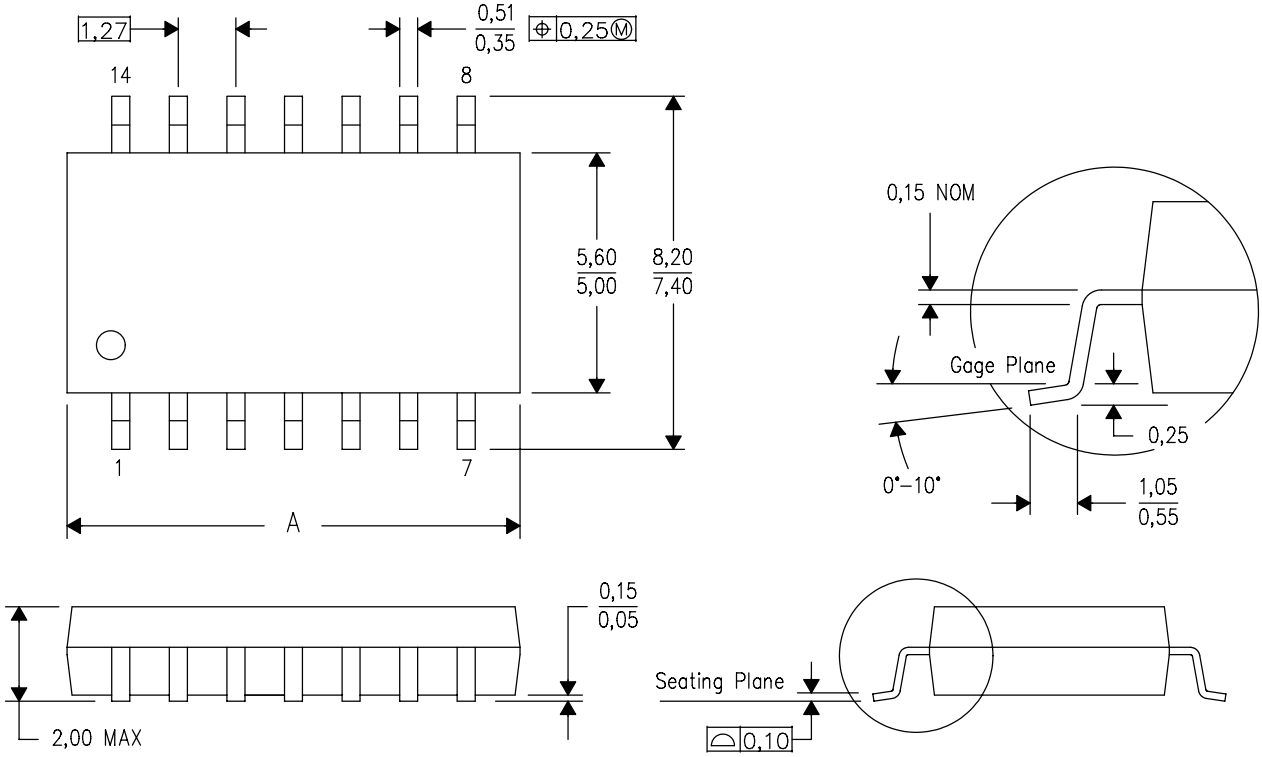
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

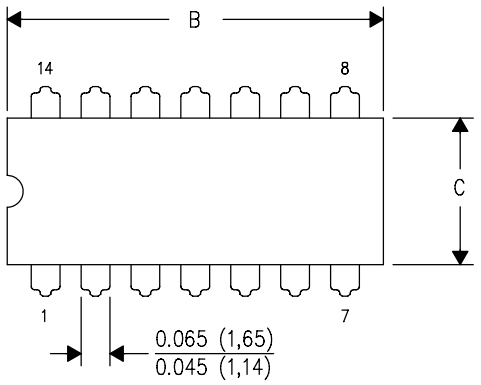
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

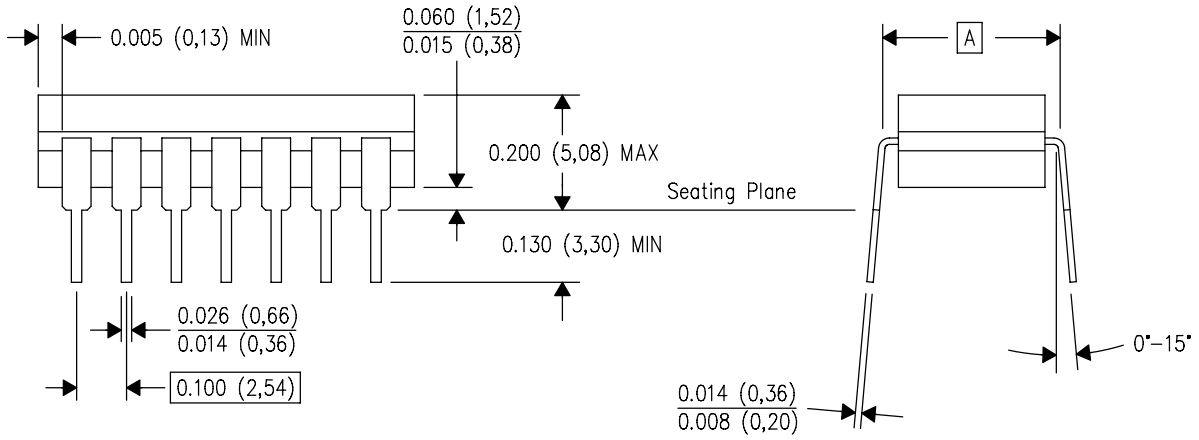
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

GENERIC PACKAGE VIEW

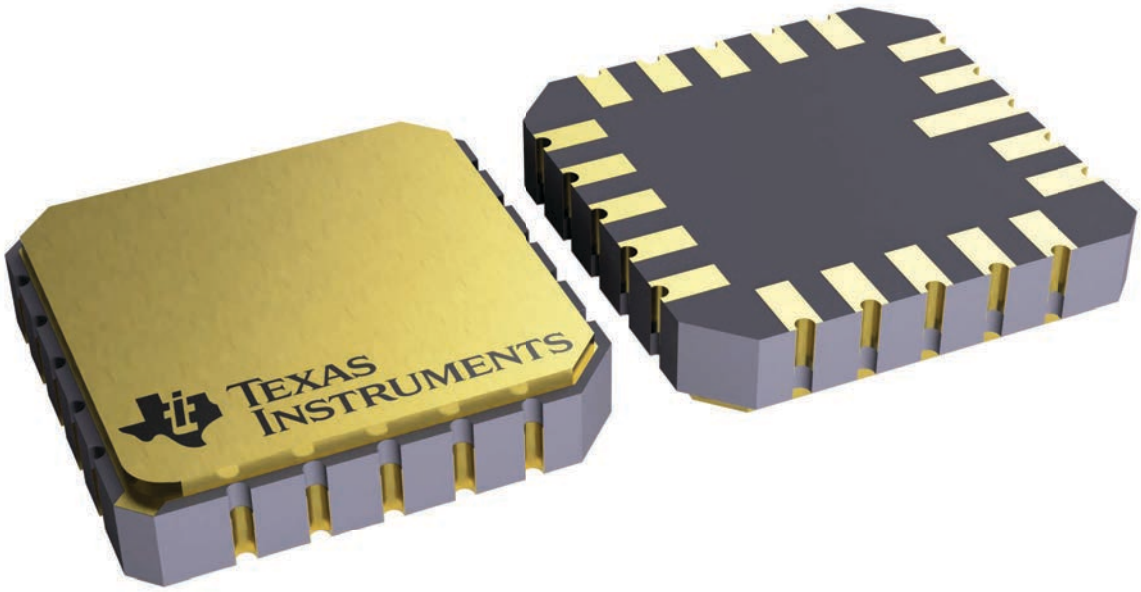
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

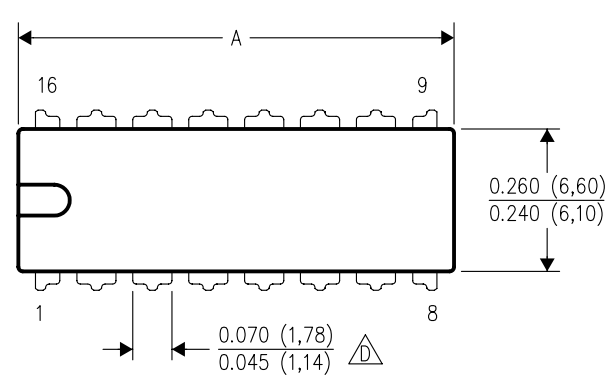


4229370VA\

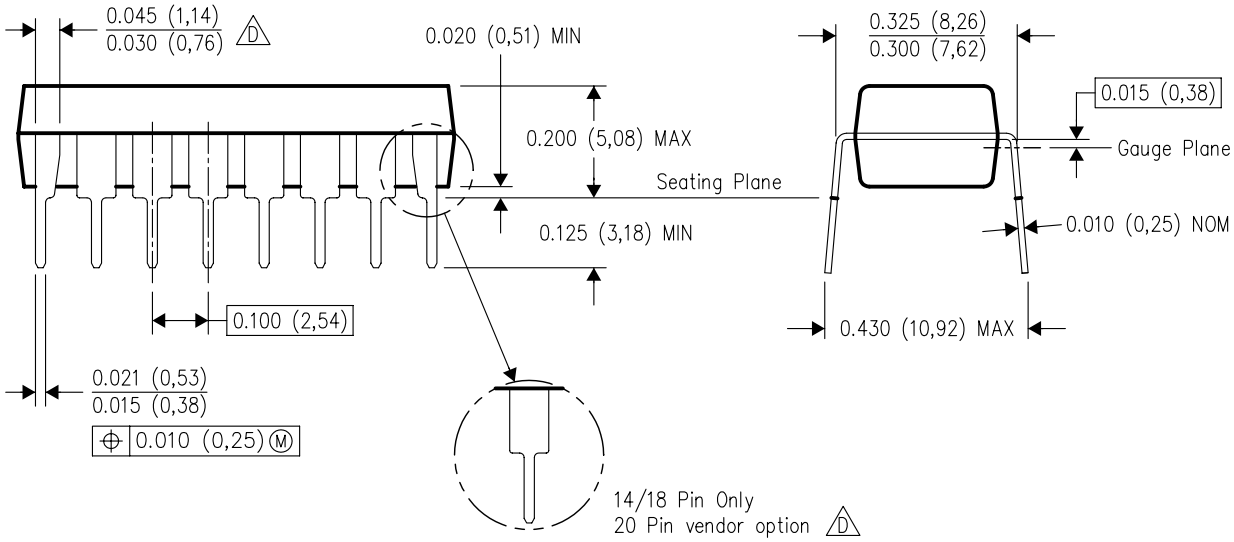
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

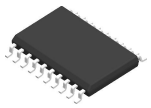


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

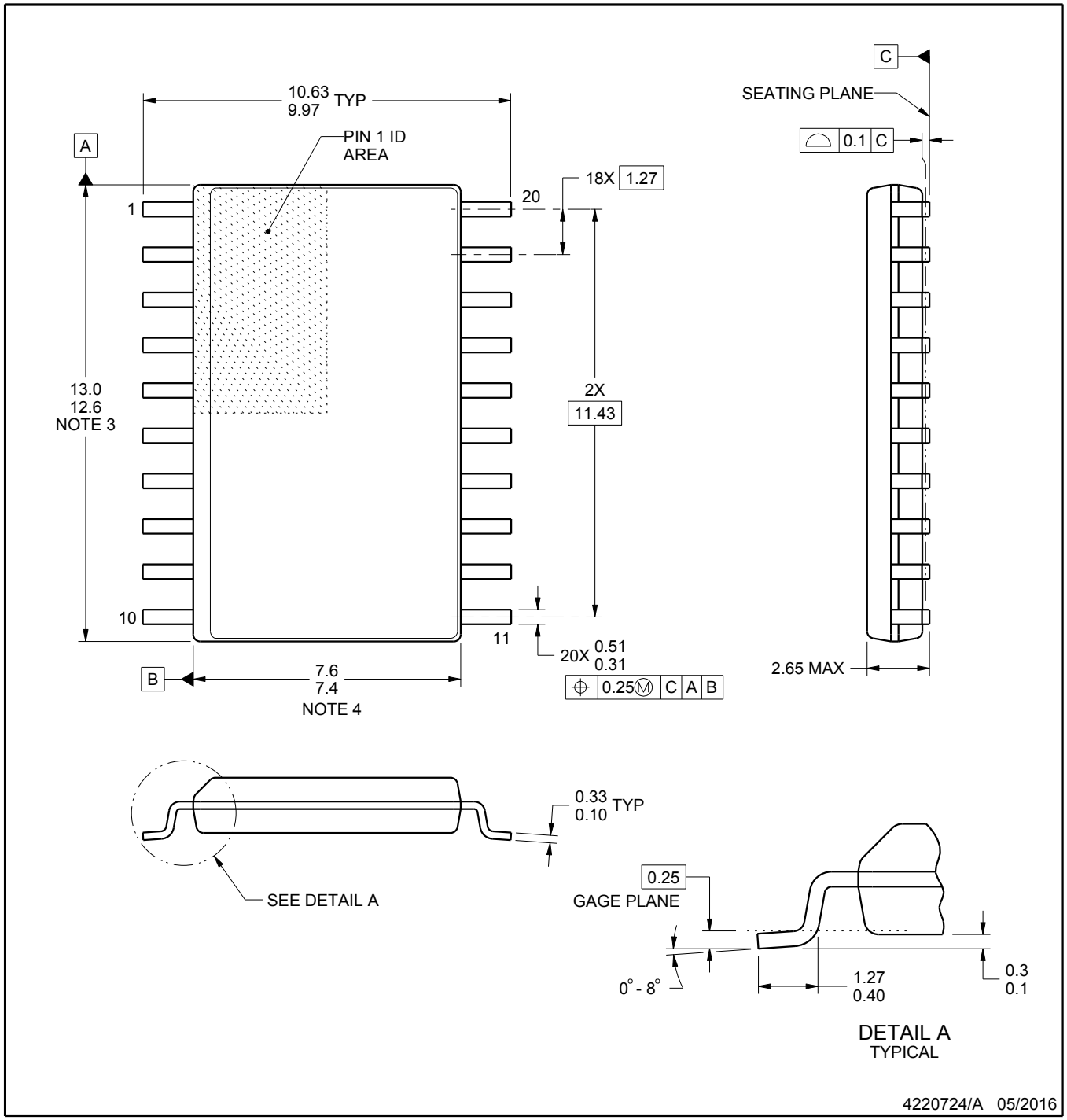


PACKAGE OUTLINE

DW0020A

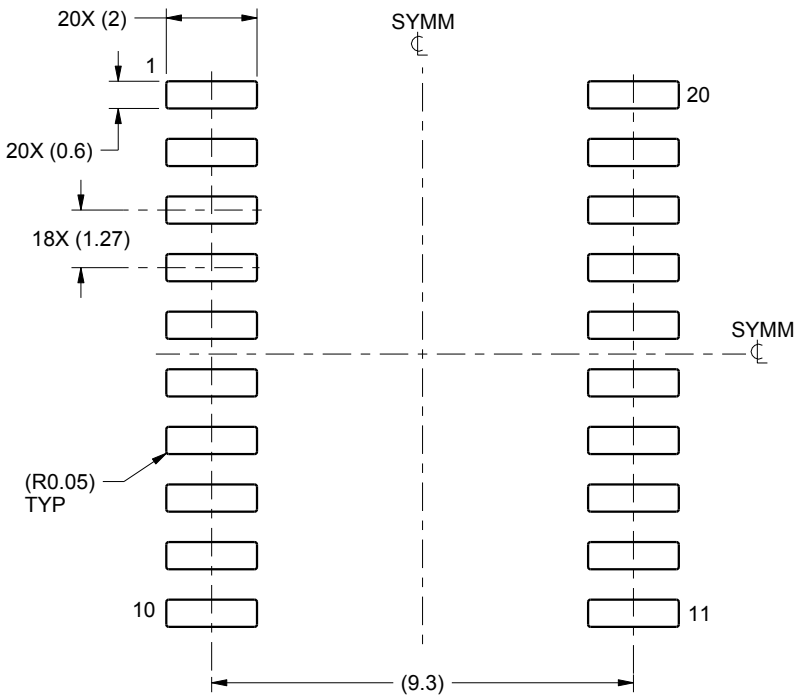
SOIC - 2.65 mm max height

SOIC

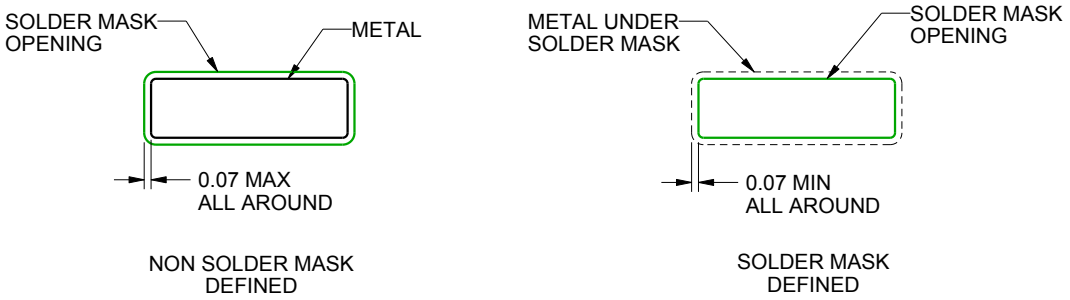


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

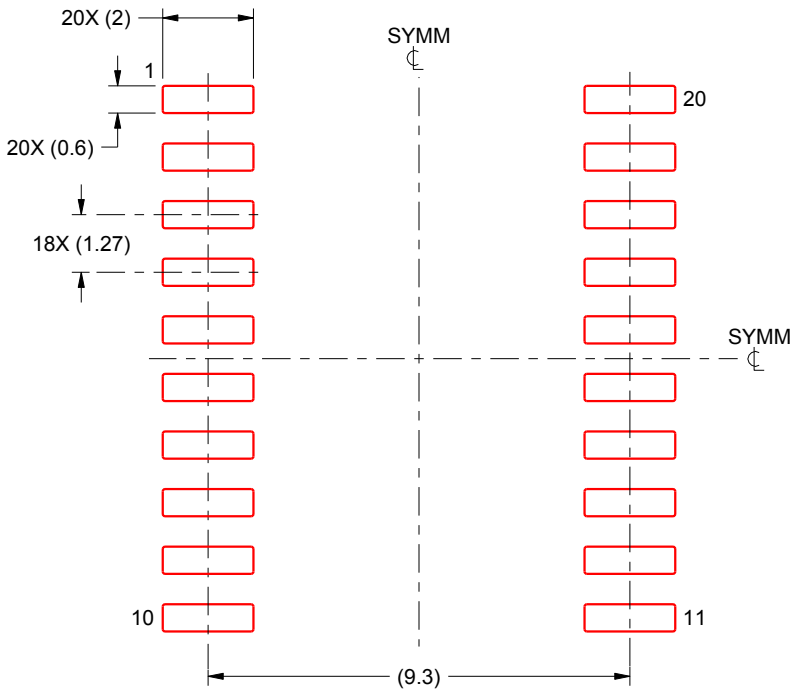


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025