

SN55LBC173 QUADRUPLE LOW-POWER DIFFERENTIAL RECEIVER

SGLS081A – MARCH 1995 – REVISED JUNE 2000

- Meets EIA Standards RS-422-A, RS-423-A, RS-485, and CCITT V.11
- Designed to Operate With Pulse Durations as Short as 20 ns
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- Input Sensitivity . . . ± 200 mV
- Low-Power Consumption . . . 20 mA Max
- Open-Circuit Fail-Safe Design
- Pin Compatible With SN75173 and AM26LS32

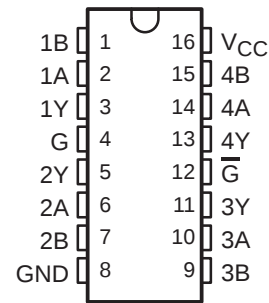
description

The SN55LBC173 is a monolithic quadruple differential line receiver with 3-state outputs designed to meet the requirements of the EIA standards RS-422-A, RS-423-A, RS-485, and CCITT V.11. This device is optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. The four receivers share two ORed enable inputs, one active when high, the other active when low. Each receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ± 200 mV over a common-mode input voltage range of 12 V to -7 V. Fail-safe design ensures that if the inputs are open circuited, the output is always high. The SN55LBC173 is designed using the Texas Instruments proprietary LinBiCMOS™ technology that provides low power consumption, high switching speeds, and robustness.

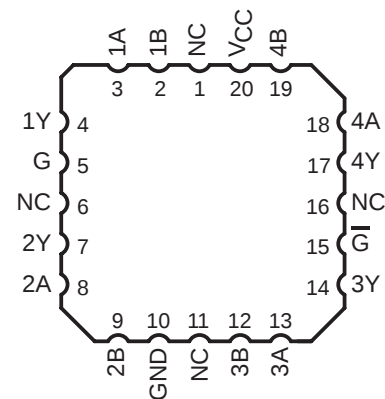
This device offers optimum performance when used with the SN55LBC172M quadruple line driver. The SN55LBC173 is available in the 16-pin CDIP (J), the 16-pin CPAK (W), or the 20-pin LCCC (FK) packages.

The SN55LBC173 is characterized over the military temperature range of -55°C to 125°C .

J OR W PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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SN55LBC173

QUADRUPLE LOW-POWER DIFFERENTIAL RECEIVER

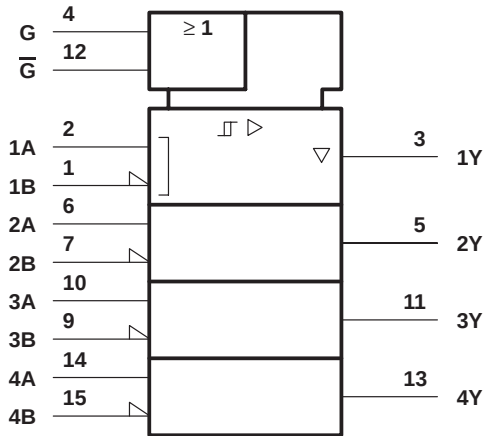
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FUNCTION TABLE
(each receiver)

DIFFERENTIAL INPUTS A – B	ENABLES		OUTPUT Y
	G	$\overline{G}$	
$V_{ID} \geq 0.2\text{ V}$	H X	X L	H H
$-0.2\text{ V} < V_{ID} < 0.2\text{ V}$	H X	X L	? ?
$V_{ID} \leq -0.2\text{ V}$	H X	X L	L L
X	L	H	Z
Open circuit	H X	X L	H H

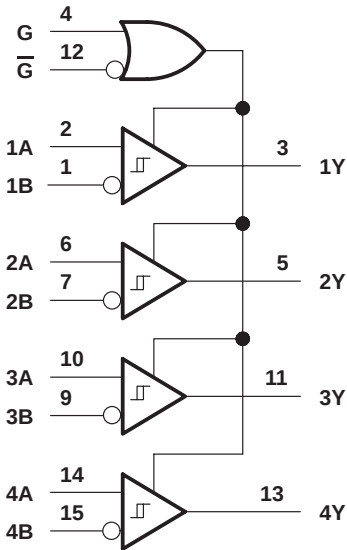
H = high level, L = low level, X = irrelevant,
Z = high impedance (off), ? = indeterminate

logic symbol†

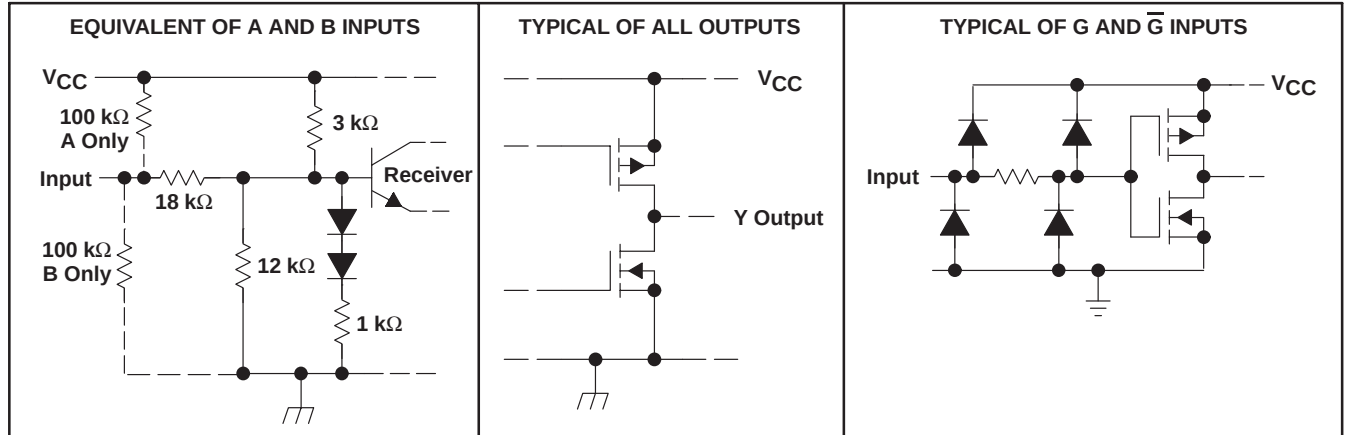


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the J or W package.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1)	–0.3 V to 7 V
Input voltage, V_I (A or B inputs)	± 25 V
Differential input voltage, V_{ID} (see Note 2)	± 25 V
Data and control voltage range	–0.3 V to 7 V
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	–55°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.

2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 125^\circ\text{C}$ POWER RATING
FK	1375 mW	11.0 mW/°C	275 mW
J	1375 mW	11.0 mW/°C	275 mW
W	1000 mW	8.0 mW/°C	200 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}	–7		12	V
Differential input voltage, V_{ID}			± 6	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}				V
High-level output current, I_{OH}			–8	mA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	–55		125	°C

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QUADRUPLE LOW-POWER DIFFERENTIAL RECEIVER

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	$I_O = -8 \text{ mA}$			0.2	V
V_{IT-}	Negative-going input threshold voltage	$I_O = 8 \text{ mA}$	-0.2			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)			45		mV
V_{IK}	Enable input clamp voltage	$I_I = -18 \text{ mA}$	-0.9	-1.5		V
V_{OH}	High-level output voltage	$V_{ID} = 200 \text{ mV}$, $I_{OH} = -8 \text{ mA}$	3.5	4.5		V
V_{OL}	Low-level output voltage	$V_{ID} = -200 \text{ mV}$, $I_{OL} = 8 \text{ mA}$		0.3	0.5	V
		$V_{ID} = -200 \text{ mV}$, $I_{OL} = 8 \text{ mA}$, $T_A = 125^\circ\text{C}$			0.7	
I_{OZ}	High-impedance-state output current	$V_O = 0 \text{ V to } V_{CC}$			± 20	μA
I_I	Bus input current	A or B inputs	$V_{IH} = 12 \text{ V}$, $V_{CC} = 5 \text{ V}$, Other inputs at 0 V	0.7	1	mA
			$V_{IH} = 12 \text{ V}$, $V_{CC} = 0 \text{ V}$, Other inputs at 0 V	0.8	1	
			$V_{IH} = -7 \text{ V}$, $V_{CC} = 5 \text{ V}$, Other inputs at 0 V	-0.5	-0.8	
			$V_{IH} = -7 \text{ V}$, $V_{CC} = 0 \text{ V}$, Other inputs at 0 V	-0.4	-0.8	
I_{IH}	High-level input current	$V_{IH} = 5 \text{ V}$			± 20	μA
I_{IL}	Low-level input current	$V_{IL} = 0 \text{ V}$			-20	μA
I_{OS}	Short-circuit output current	$V_O = 0$	-80	-120		mA
I_{CC}	Supply current	Outputs enabled, $I_O = 0$, $V_{ID} = 5 \text{ V}$		11	20	mA
		Outputs disabled		0.9	1.4	

[†] All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

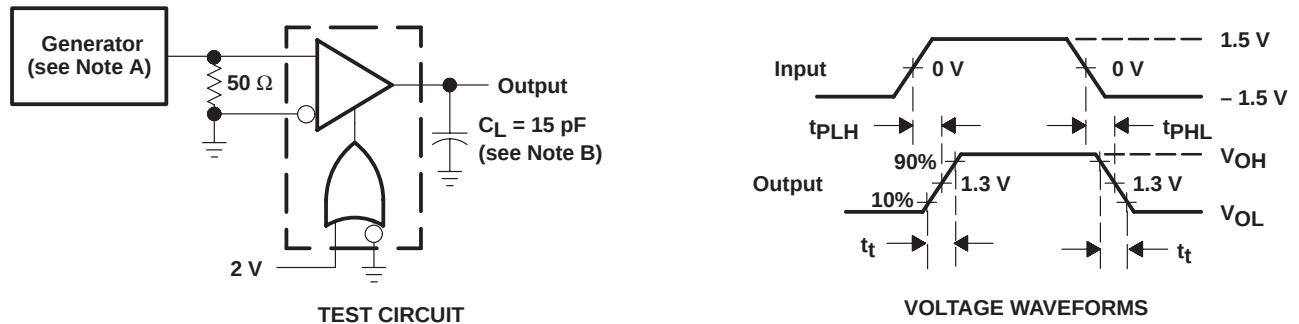
switching characteristics, $V_{CC} = 5 \text{ V}$, $C_L = 15 \text{ pF}$

PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output	25°C	11	22	30	ns
		-55°C to 125°C	11		35	
t_{PLH}	Propagation delay time, low-to-high-level output	25°C	11	22	35	ns
		-55°C to 125°C	11		35	
t_{pZH}	Output enable time to high level	25°C		17	40	ns
		-55°C to 125°C			45	
t_{pZL}	Output enable time to low level	25°C		18	30	ns
		-55°C to 125°C			35	
t_{pHZ}	Output disable time from high level	25°C		30	40	ns
		-55°C to 125°C			55	
t_{pLZ}	Output disable time from low level	25°C		25	40	ns
		-55°C to 125°C			45	
$t_{sk(p)}$	Pulse skew ($ t_{PHL} - t_{PLH} $)	25°C		0.5	6	ns
		-55°C to 125°C			7	
t_t	Transition time	25°C		5	10	ns
		-55°C to 125°C			16	



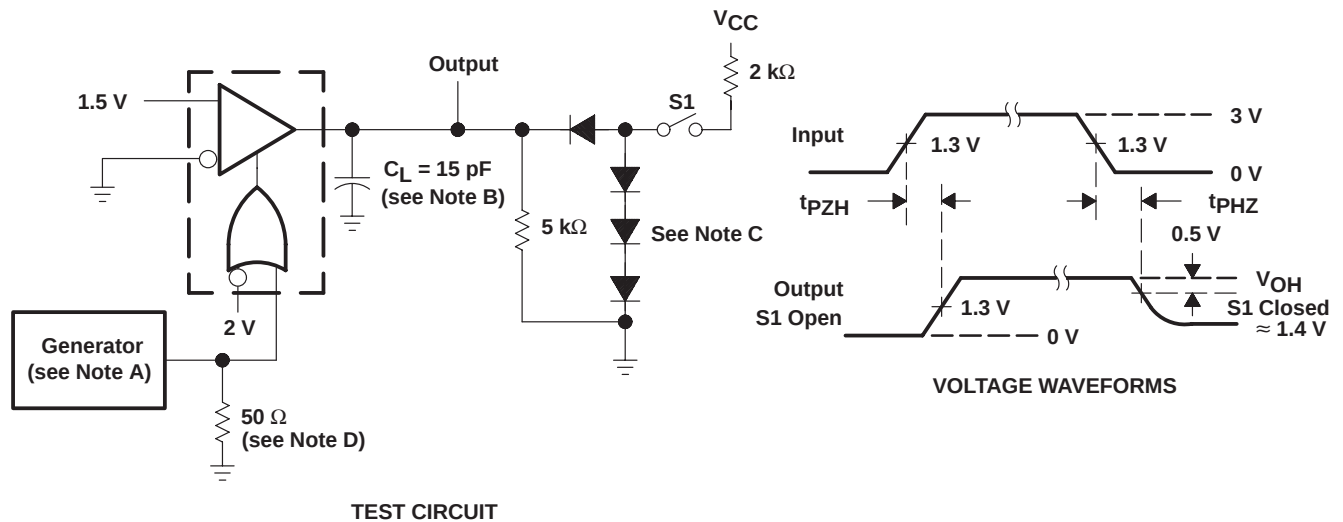
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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle $\leq 50\%$, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 1. t_{pd} and t_t Test Circuit and Voltage Waveforms



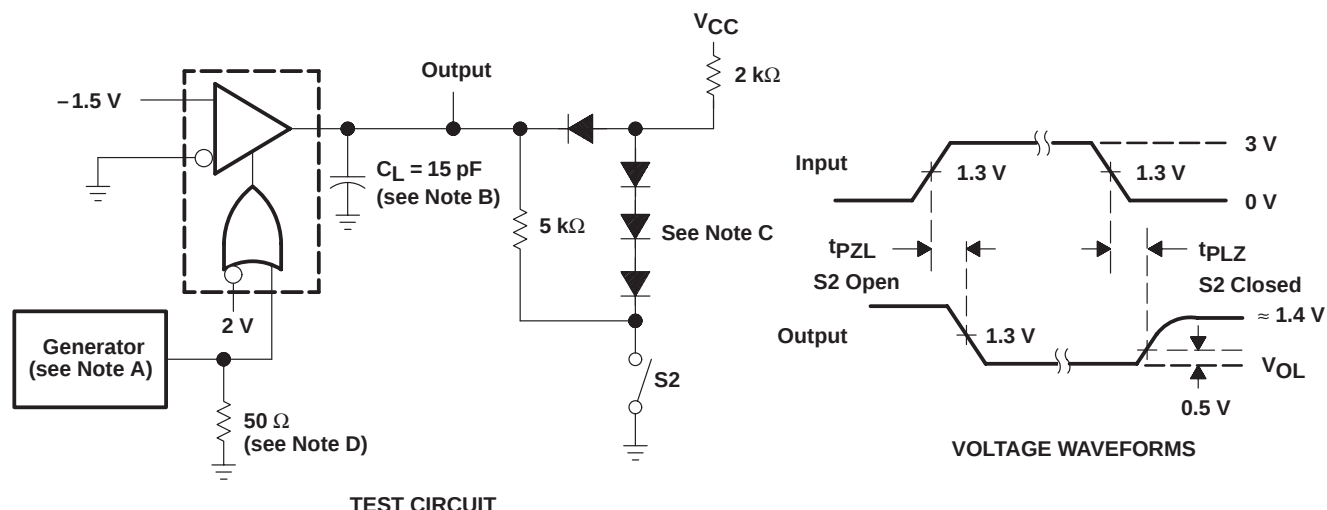
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle $\leq 50\%$, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.
D. To test the active-low enable $\overline{G}$, ground $\overline{G}$ and apply an inverted input waveform to $\overline{G}$.

Figure 2. t_{pZH} and t_{pHZ} Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≤ 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.
 C. All diodes are 1N916 or equivalent.
 D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

Figure 3. t_{pZL} and t_{pLZ} Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

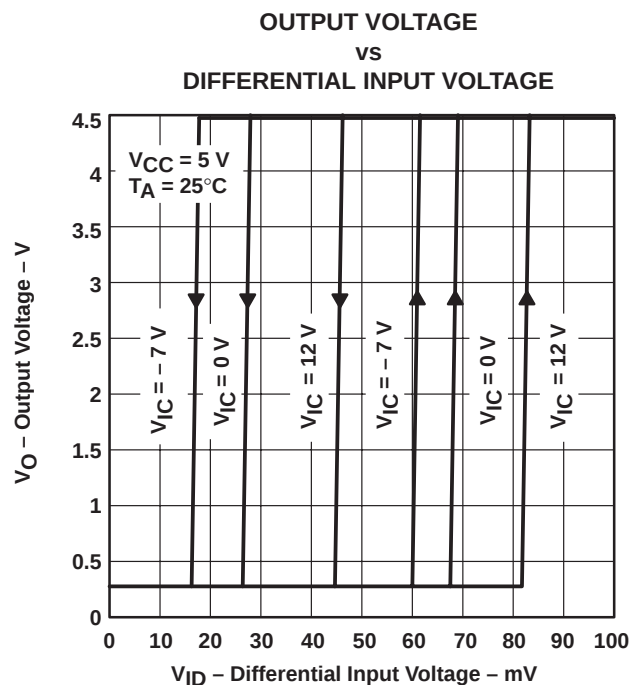


Figure 4

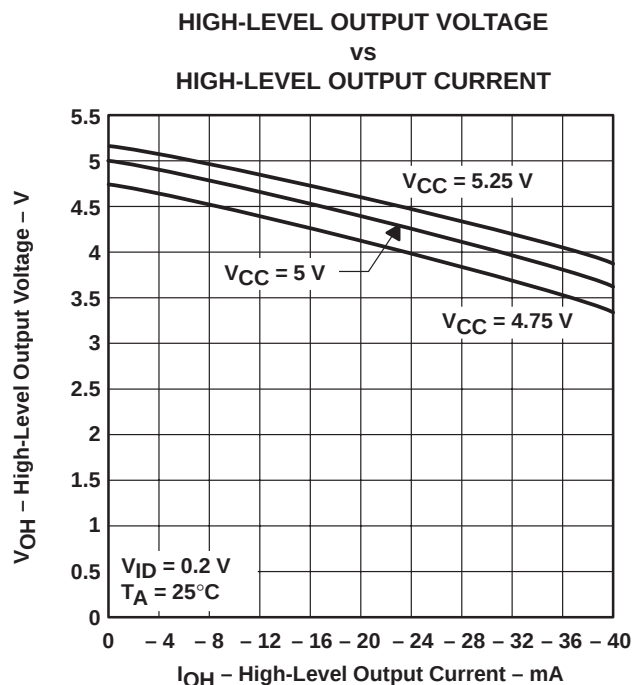


Figure 5

TYPICAL CHARACTERISTICS

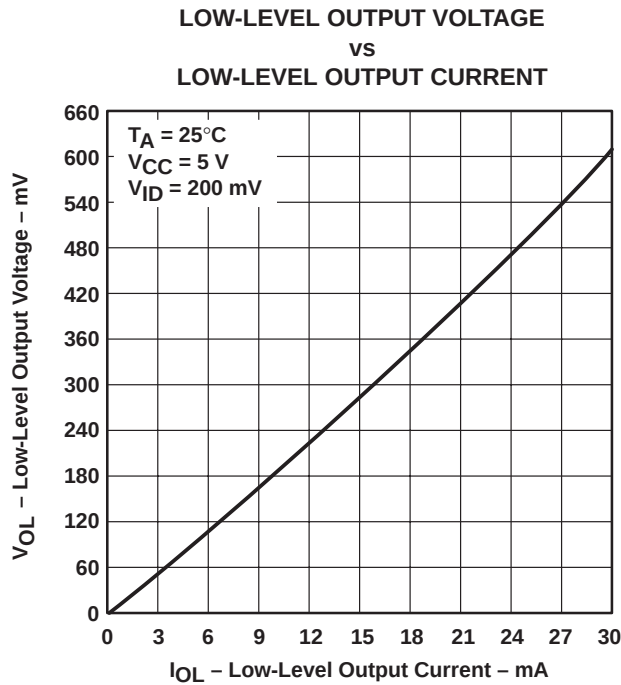


Figure 6

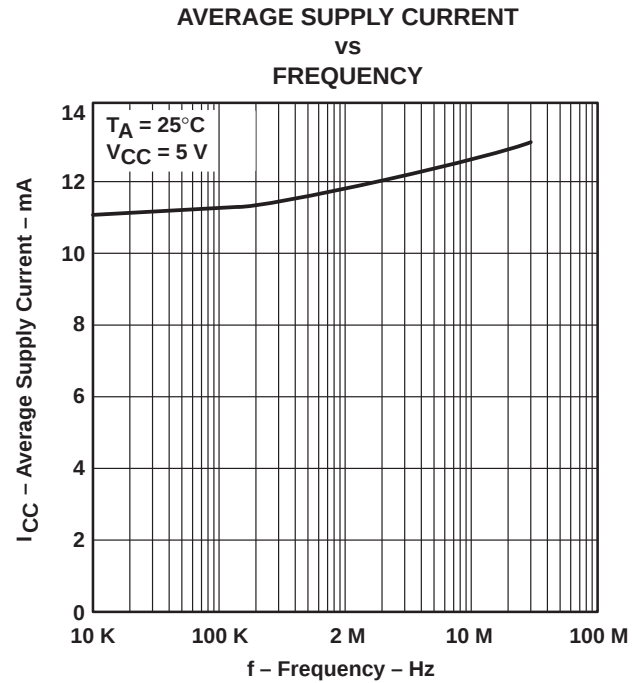


Figure 7

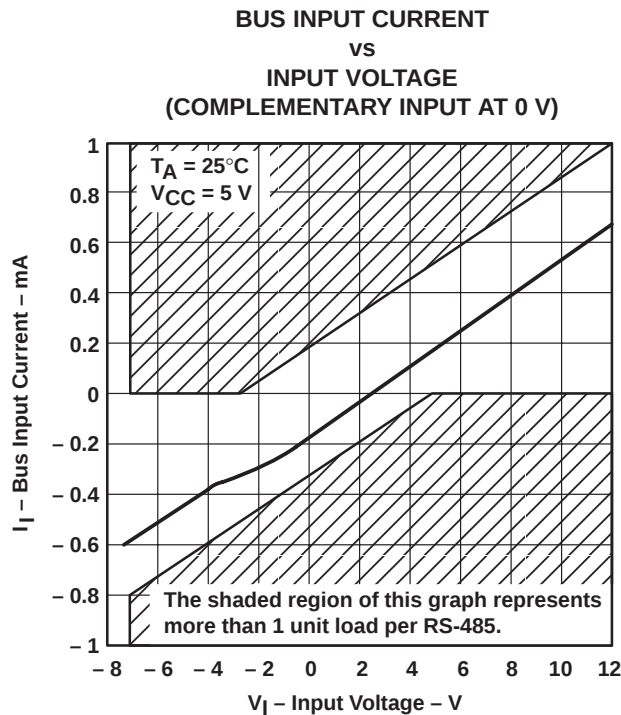


Figure 8

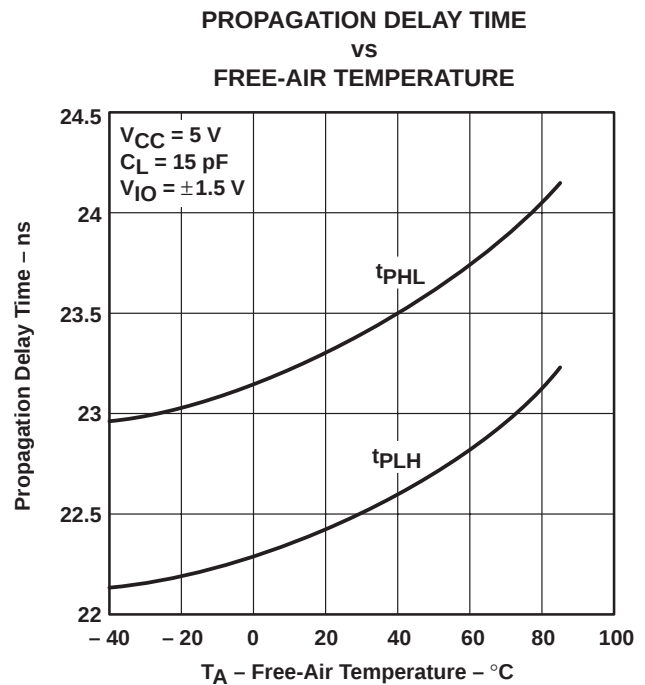


Figure 9

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9076604Q2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9076604Q2A SNJ55 LBC173FK
5962-9076604QEA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9076604QE A SNJ55LBC173J
5962-9076604QFA	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9076604QF A SNJ55LBC173W
SNJ55LBC173FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9076604Q2A SNJ55 LBC173FK
SNJ55LBC173FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 9076604Q2A SNJ55 LBC173FK
SNJ55LBC173J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9076604QE A SNJ55LBC173J
SNJ55LBC173J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9076604QE A SNJ55LBC173J
SNJ55LBC173W	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9076604QF A SNJ55LBC173W
SNJ55LBC173W.A	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9076604QF A SNJ55LBC173W

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN55LBC173 :

- Catalog : [SN75LBC173](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

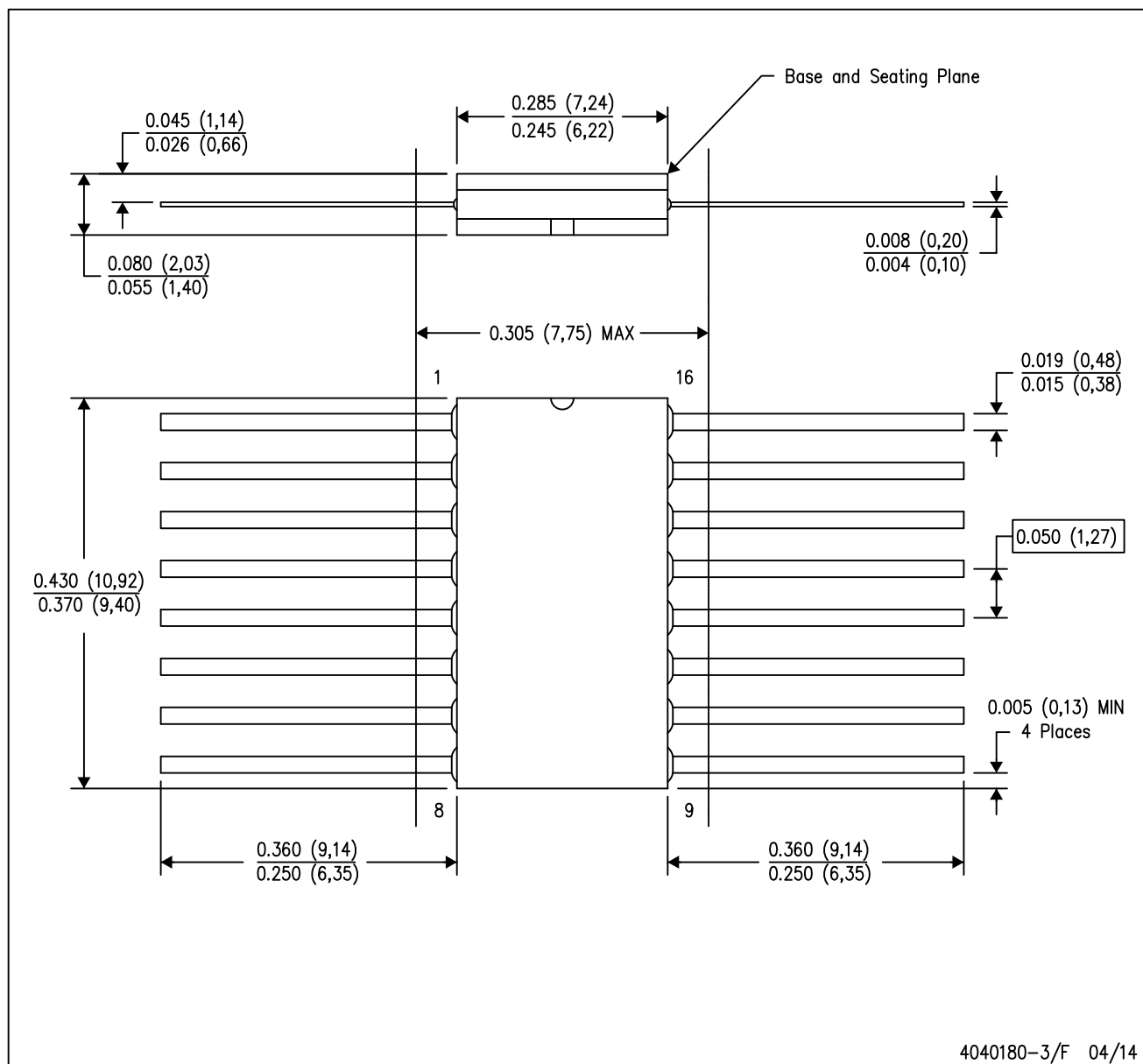
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9076604Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9076604QFA	W	CFP	16	25	506.98	26.16	6220	NA
SNJ55LBC173FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ55LBC173FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ55LBC173W	W	CFP	16	25	506.98	26.16	6220	NA
SNJ55LBC173W.A	W	CFP	16	25	506.98	26.16	6220	NA

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP2-F16

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

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