

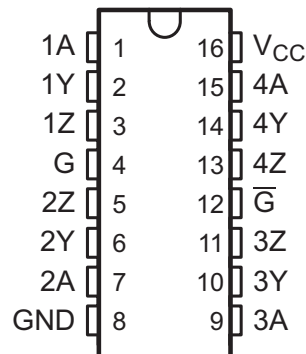
HIGH-SPEED DIFFERENTIAL LINE DRIVER

Check for Samples: [SN55LVDS31-SP](#)

FEATURES

- QML-V Qualified, SMD 5962-97621
- Meet or Exceed the Requirements of ANSI TIA/EIA-644 Standard
- Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and 100-Ω Load
- Typical Output Voltage Rise and Fall Times of 500 ps (400 Mbps)
- Typical Propagation Delay Times of 1.7 ns
- Operate From a Single 3.3-V Supply
- Power Dissipation 25 mW Typical Per Driver at 200 MHz
- Driver at High Impedance When Disabled or With $V_{CC} = 0$
- Bus-Terminal ESD Protection Exceeds 8 kV
- Low-Voltage TTL (LVTTTL) Logic Input Levels
- Cold Sparring for Space and High Reliability Applications Requiring Redundancy

J OR W PACKAGE
(TOP VIEW)



DESCRIPTION

The SN55LVDS31 is a differential line driver that implements the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as TIA/EIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. This driver will deliver a minimum differential output voltage magnitude of 247 mV into a 100-Ω load when enabled.

The intended application of this device and signaling technique is both point-to-point and multidrop (one driver and multiple receivers) data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The SN55LVDS31 is characterized for operation from -55°C to 125°C .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



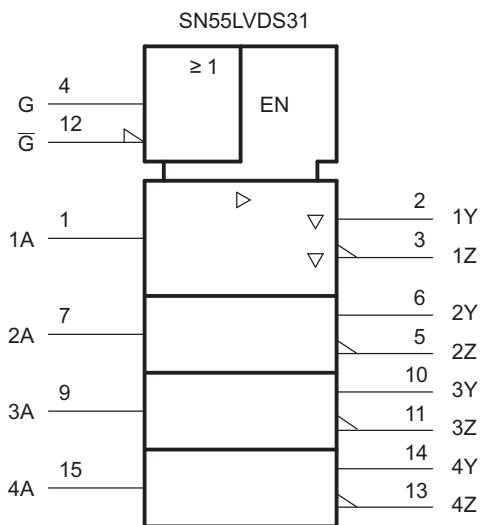
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	CDIP - J	5962-9762101VEA	5962-9762101VEA
	CFP - W	5962-9762101VFA	5962-9762101VFA

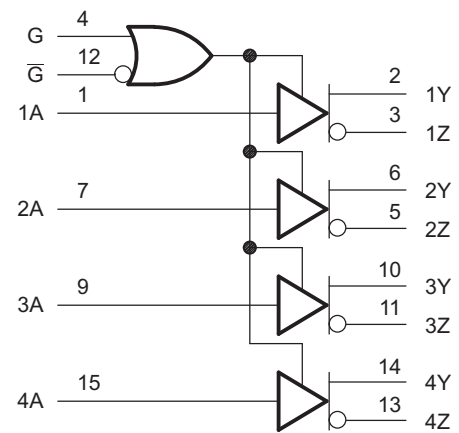
- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Logic Symbol



This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN55LVDS31 Logic Diagram (Positive Logic)



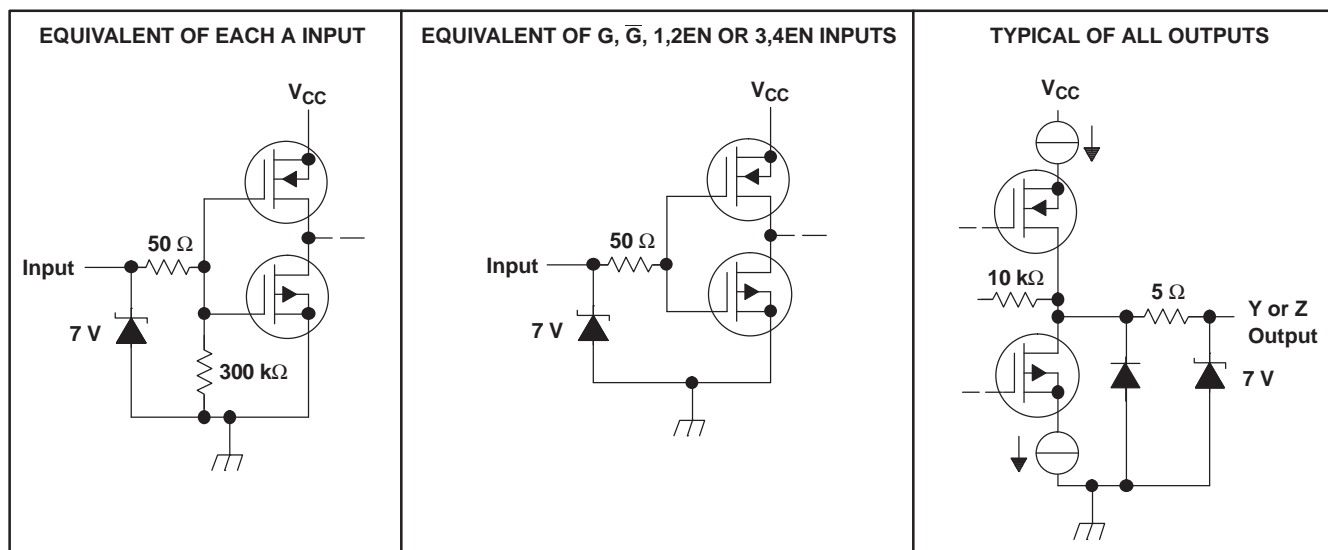
FUNCTION TABLE

Table 1. SN55LVDS31⁽¹⁾

INPUT A	ENABLES		OUTPUTS	
	G	G	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z
Open	H	X	L	H
Open	X	L	L	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

	UNIT
V _{CC} Supply voltage range ⁽²⁾	–0.5 V to 4 V
V _I Input voltage range	–0.5 V to V _{CC} + 0.5 V
Continuous total power dissipation	See Dissipation Rating Table
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
T _{stg} Storage temperature range	–65°C to 150°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages, except differential I/O bus voltages, are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ⁽¹⁾ ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING	T _A = 125°C POWER RATING
J	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
W	1000 mW	8 mW/°C	640 mW	520 mW	200 mW

- (1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
V _{CC} Supply voltage	3	3.3	3.6	V
V _{IH} High-level input voltage	2			V
V _{IL} Low-level input voltage			0.8	V
T _A Operating free-air temperature	–55		125	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OD} Differential output voltage magnitude	R _L = 100 Ω, See Figure 2	247	340	454	mV
ΔV _{OD} Change in differential output voltage magnitude between logic states	R _L = 100 Ω, See Figure 2	–50		50	mV
V _{OC(SS)} Steady-state common-mode output voltage	See Figure 3	1.125	1.2	1.375	V
ΔV _{OC(SS)} Change in steady-state common-mode output voltage between logic states	See Figure 3	–50		50	mV
V _{OC(PP)} Peak-to-peak common-mode output voltage	See Figure 3		50		mV
I _{CC} Supply current	V _I = 0.8 V or 2 V, Enabled, No load		9	20	mA
	V _I = 0.8 or 2 V, R _L = 100 Ω, Enabled		25	35	
	V _I = 0 or V _{CC} , Disabled		0.25	1	
I _{IH} High-level input current	V _{IH} = 2		4	20	μA
I _{IL} Low-level input current	V _{IL} = 0.8 V		0.1	10	μA
I _{OS} Short-circuit output current	V _{O(Y)} or V _{O(Z)} = 0		–4	–24	mA
	V _{OD} = 0			±12	
I _{OZ} High-impedance output current	V _O = 0 or 2.4 V			±1	μA
I _{O(OFF)} Power-off output current	V _{CC} = 0, V _O = 2.4 V			±4	μA
C _i Input capacitance			3		pF

- (1) All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$R_L = 100 \Omega$, $C_L = 10 \text{ pF}$, See Figure 2	0.5	1.4	4	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1	1.7	4.5	ns
t_r	Differential output signal rise time (20% to 80%)		0.4	0.5	1	ns
t_f	Differential output signal fall time (80% to 20%)		0.4	0.5	1	ns
$t_{sk(p)}$	Pulse skew ($ t_{PHL} - t_{PLH} $)			0.3	0.6	ns
$t_{sk(o)}$	Channel-to-channel output skew ⁽²⁾		0.3	0.6	ns	
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 4		5.4	15	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			2.5	15	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output			8.1	17	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			7.3	15	ns

(1) All typical values are at $T_A = 25^\circ\text{C}$ and with $V_{CC} = 3.3 \text{ V}$.

(2) $t_{sk(o)}$ is the maximum delay time difference between drivers on the same device.

PARAMETER MEASUREMENT INFORMATION

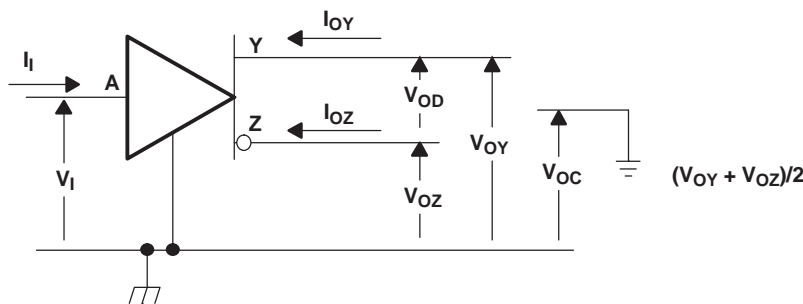
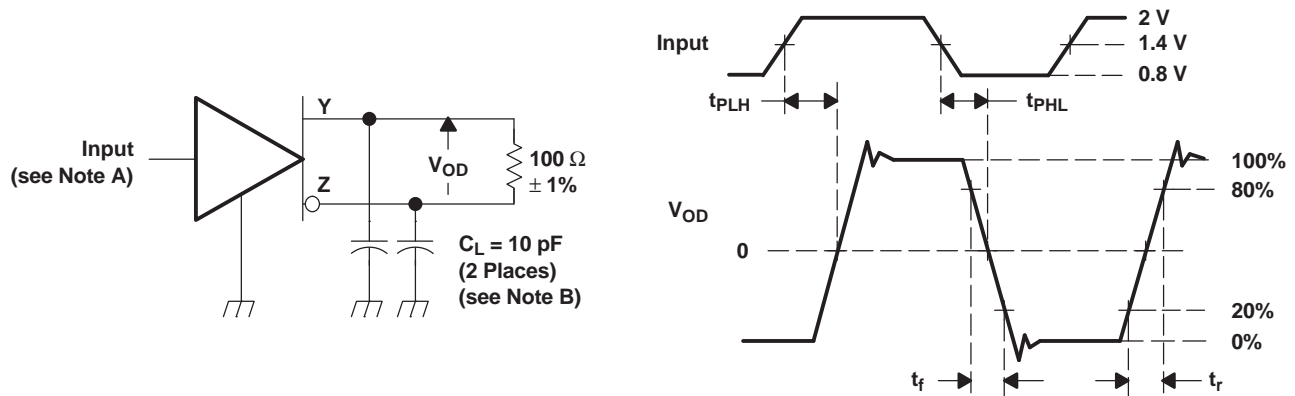


Figure 1. Voltage and Current Definitions

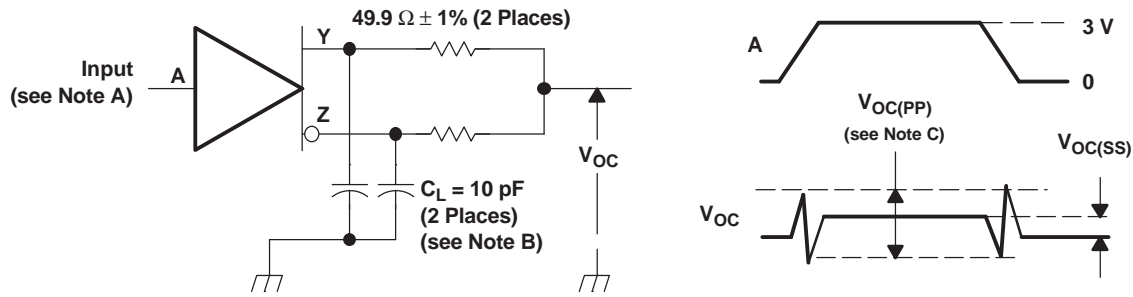


NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1 \text{ ns}$, pulse repetition rate (PRR) = 50 Mpps, pulse width = $10 \pm 0.2 \text{ ns}$.

B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

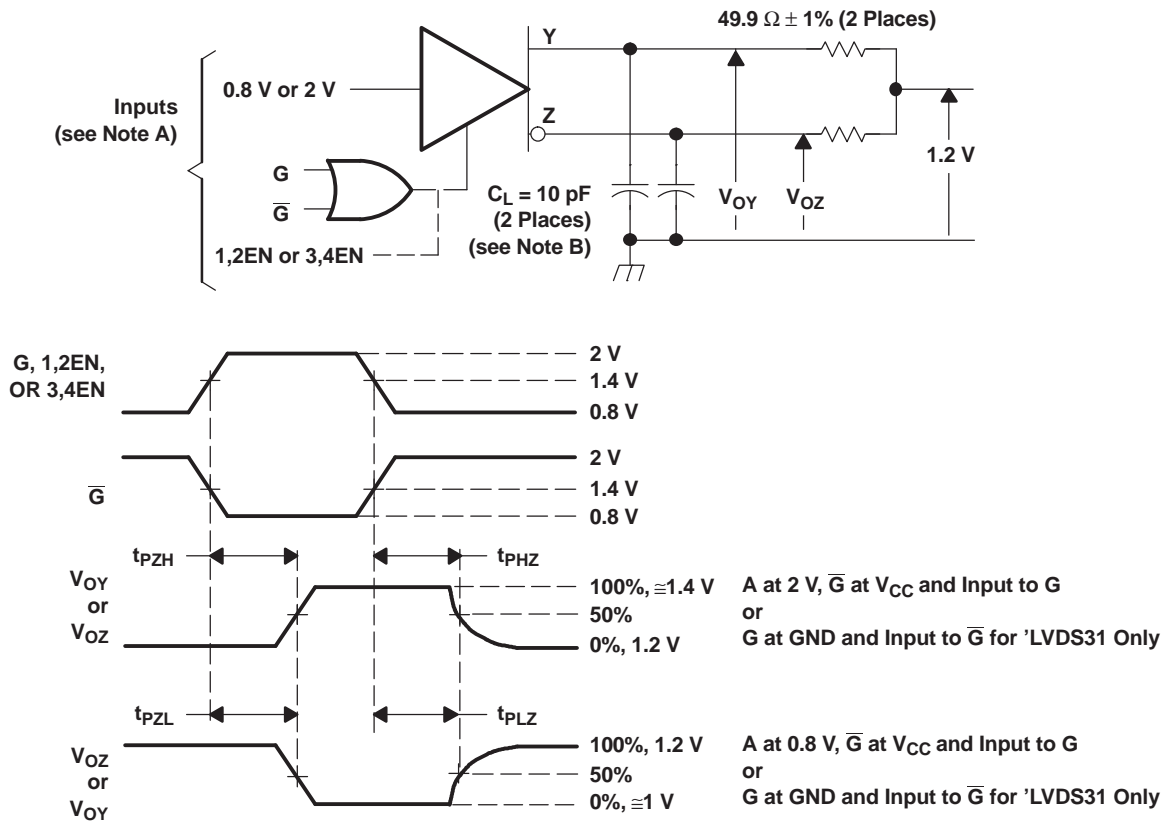
Figure 2. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

PARAMETER MEASUREMENT INFORMATION (continued)



- NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.
 B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.
 C. The measurement of $V_{OC(PP)}$ is made on test equipment with a -3 -dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



- NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f < 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns.
 B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

Figure 4. Enable-/Disable-Time Circuit and Definitions

TYPICAL CHARACTERISTICS

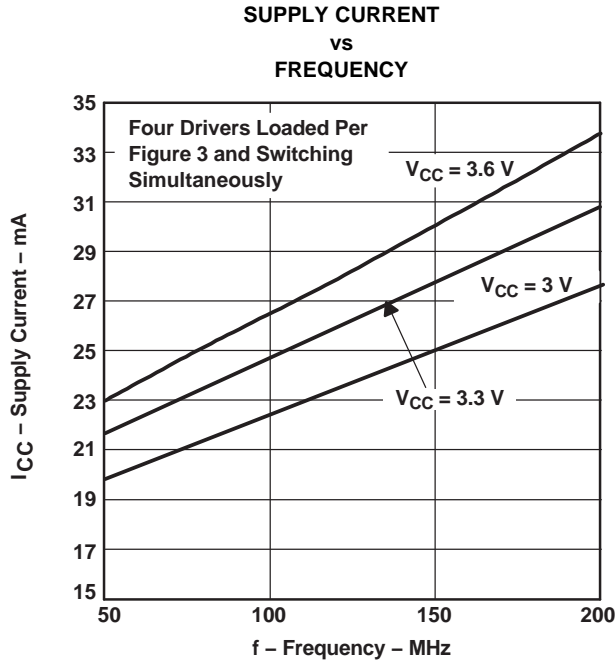


Figure 5.

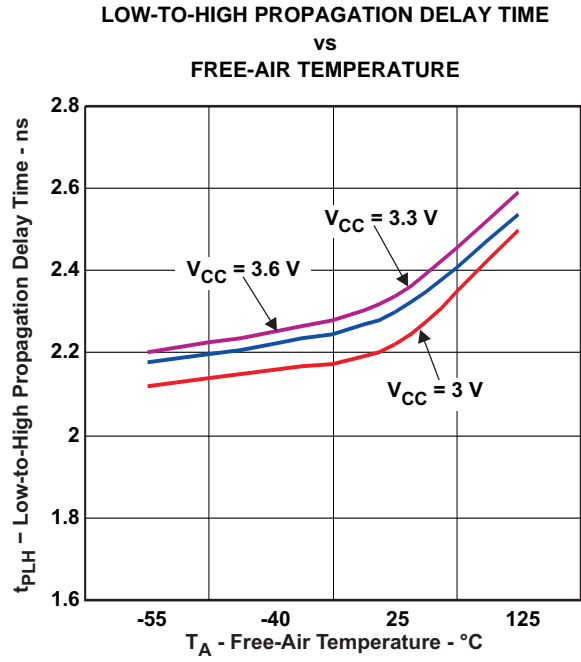


Figure 6.

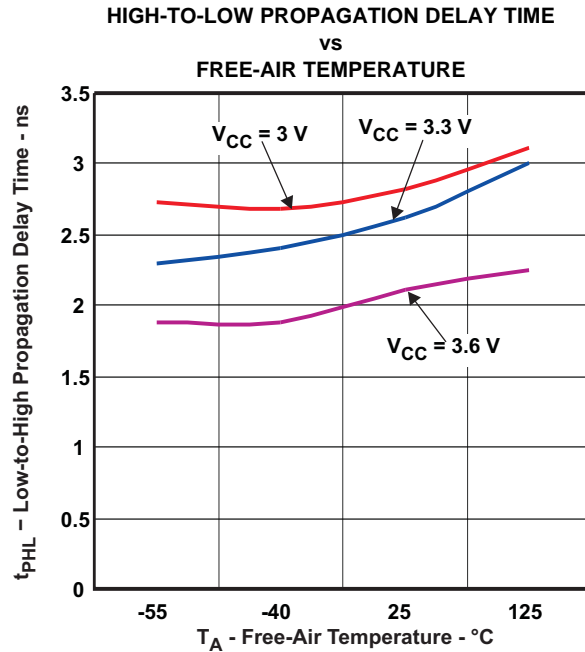
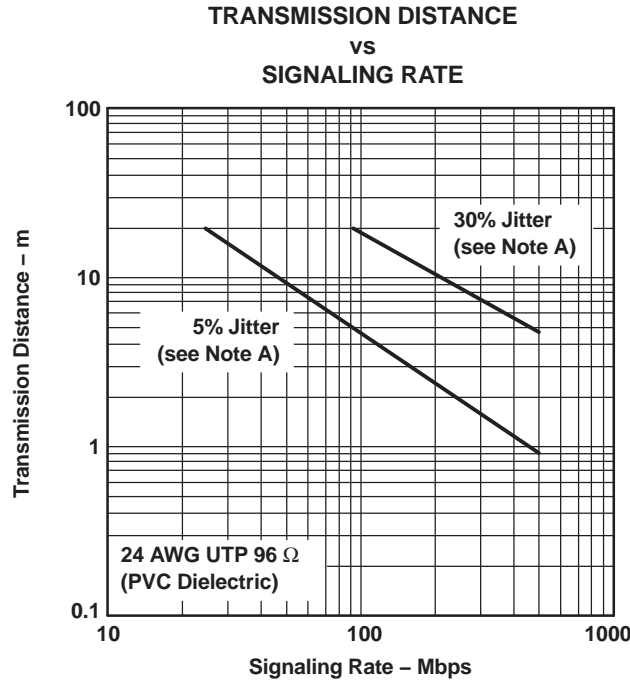


Figure 7.

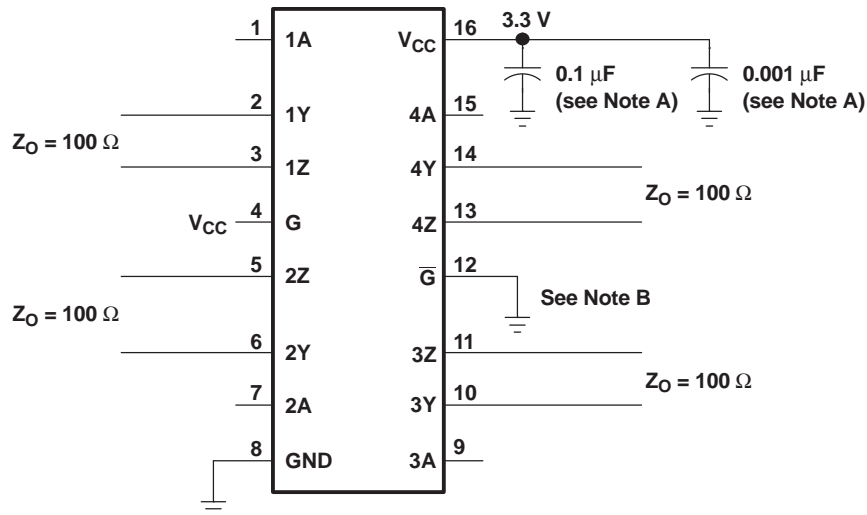
APPLICATION INFORMATION

The SN55LVDS31 is generally used as a building block for high-speed point-to-point data transmission where ground differences are less than 1 V. The SN55LVDS31 can interoperate with RS-422, PECL, and IEEE-P1596. Drivers/receivers approach ECL speeds without the power and dual supply requirements.



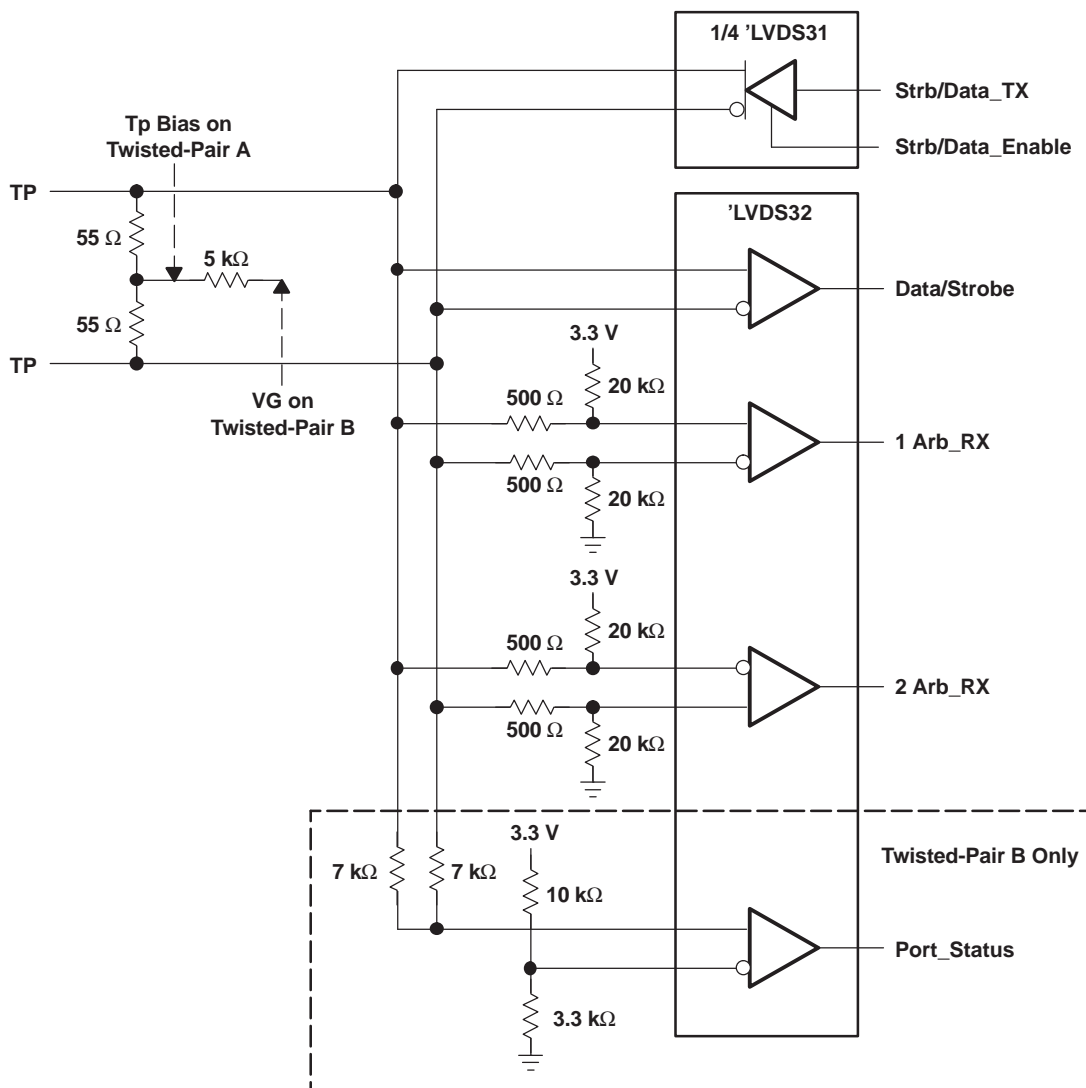
A. This parameter is the percentage of distortion of the unit interval (UI) with a pseudorandom data pattern.

Figure 8. Typical Transmission Distance Versus Signaling Rate



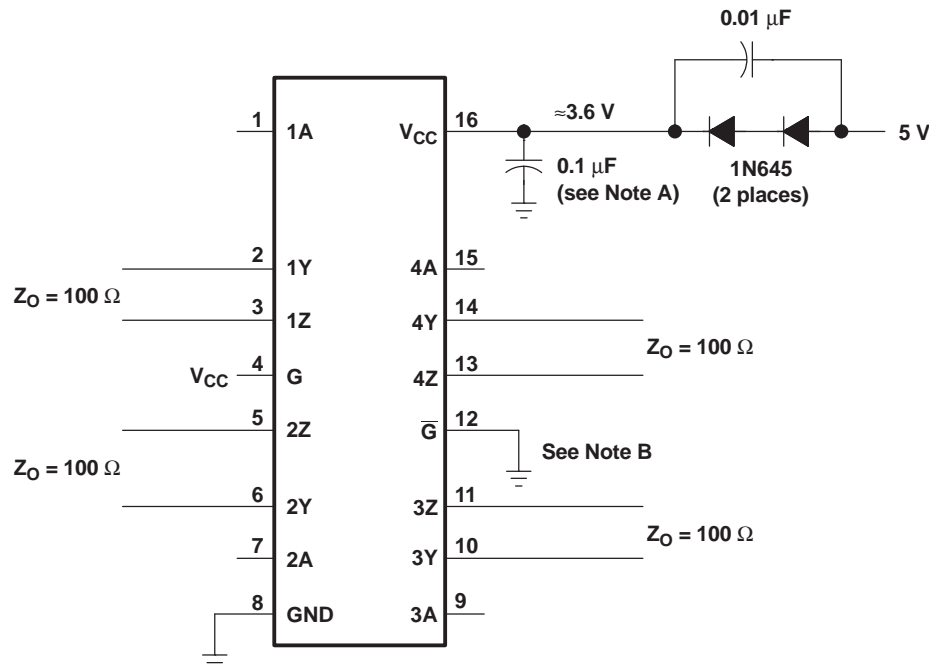
- NOTES: A. Place a 0.1- μ F and a 0.001- μ F Z5U ceramic, mica, or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitors should be located as close as possible to the device terminals.
 B. Unused enable inputs should be tied to V_{CC} or GND, as appropriate.

Figure 9. Typical Application Circuit Schematic



- NOTES: A. Resistors are leadless, thick film (0603), 5% tolerance.
 B. Decoupling capacitance is not shown, but recommended.
 C. V_{CC} is 3 V to 3.6 V.
 D. The differential output voltage of the 'LVDS31 can exceed that specified by IEEE1394.

Figure 10. 100-Mbps IEEE 1394 Transceiver



- Place a 0.1-μF Z5U ceramic, mica, or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitor should be located as close as possible to the device terminals.
- Unused enable inputs should be tied to V_{CC} or GND, as appropriate.

Figure 11. Operation With 5-V Supply

COLD SPARING

Systems using cold sparing have a redundant device electrically connected without power supplied. To support this configuration, the spare must present a high-input impedance to the system so that it does not draw appreciable power. In cold sparing, voltage may be applied to an I/O before and during power up of a device. When the device is powered off, V_{CC} must be clamped to ground and the I/O voltages applied must be within the specified recommended operating conditions.

RELATED INFORMATION

IBIS modeling is available for this device. Contact the local TI sales office or the TI Web site at www.ti.com for more information.

For more application guidelines, see the following documents:

- *Low-Voltage Differential Signaling Design Notes* ([SLLA014](#))
- *Interface Circuits for TIA/EIA-644 (LVDS)* ([SLLA038](#))
- *Reducing EMI With LVDS* ([SLLA030](#))
- *Slew Rate Control of LVDS Circuits* ([SLLA034](#))
- *Using an LVDS Receiver With RS-422 Data* ([SLLA031](#))

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9762101VFA	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9762101VF A SNV55LVDS31W

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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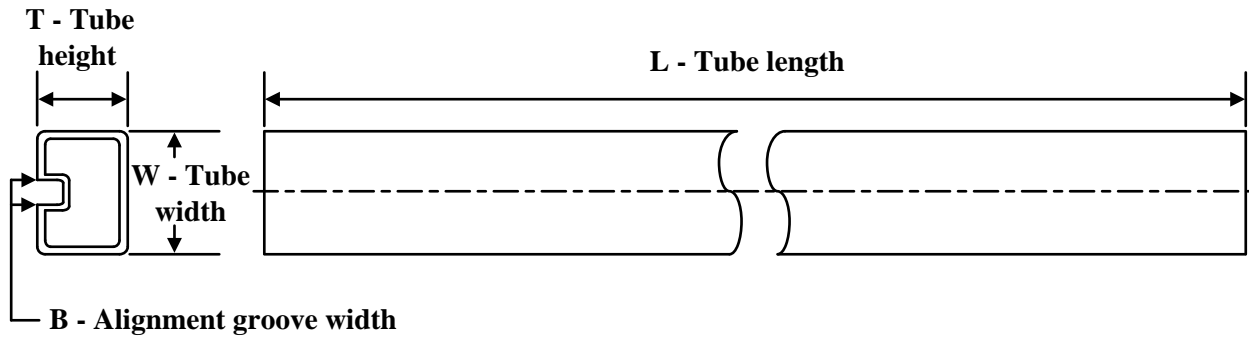
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OTHER QUALIFIED VERSIONS OF SN55LVDS31-SP :

- Catalog : [SN55LVDS31](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

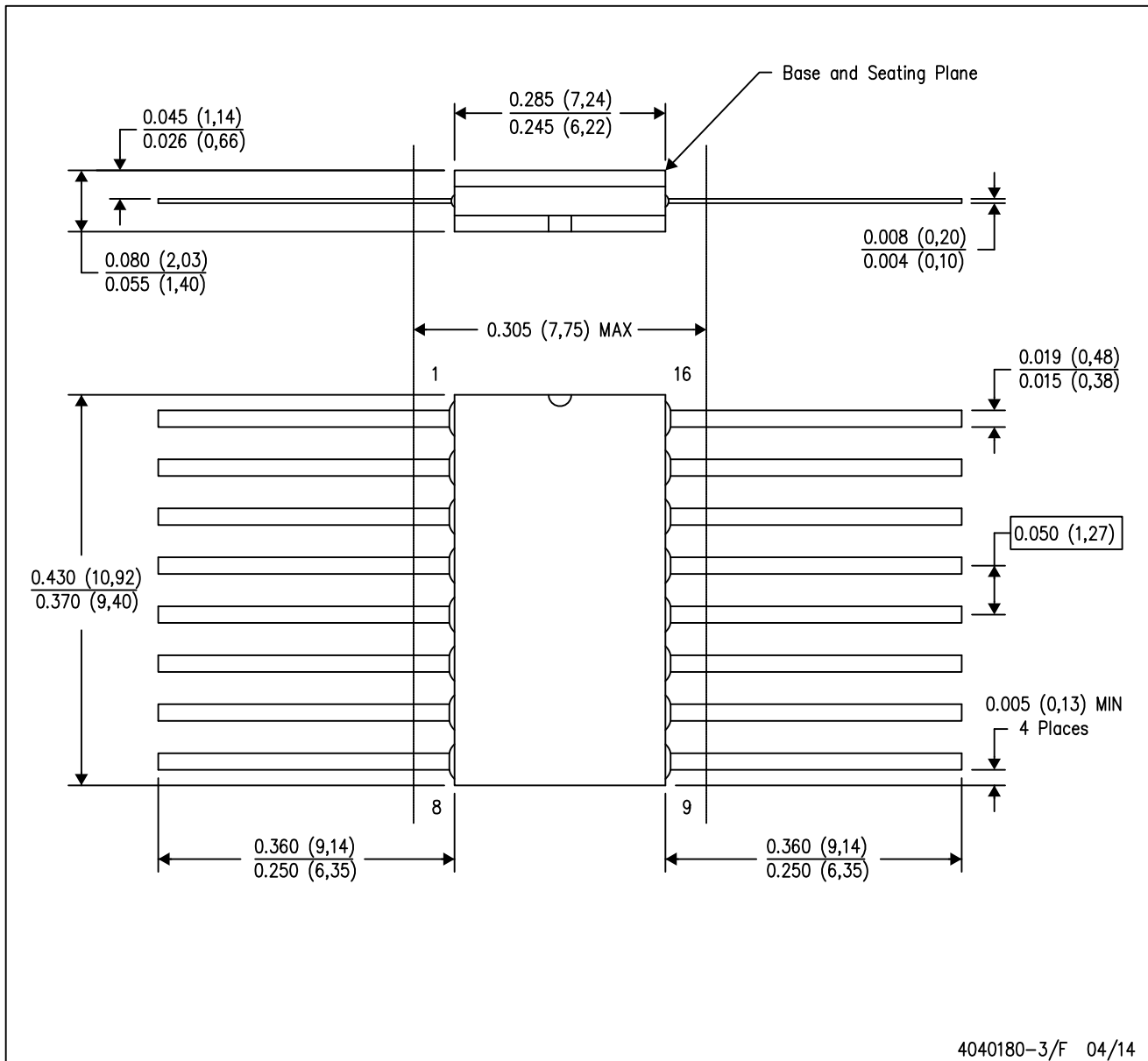
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9762101VFA	W	CFP	16	25	506.98	26.16	6220	NA

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP2-F16

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Last updated 10/2025