

## SN65HVDA1040B-Q1 EMC-Optimized High-Speed CAN Bus Transceiver

### 1 Features

- AEC-Q100 Qualified for automotive applications
  - Temperature grade 0:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $T_A$
  - HBM ESD classification level:
    - 3A Level for all pins except 5, 6, and 7
    - 3B Level for pins 5, 6 and 7
  - CDM ESD classification level C6
- Meets or exceeds the requirements of ISO 11898-2 and -5
- GIFT/ICT compliant
- Low-current standby mode with bus wakeup,  $<12\ \mu\text{A}$  maximum
- High electromagnetic compliance (EMC)
- SPLIT voltage source for common-mode stabilization of bus through split termination
- Digital inputs compatible with 3.3-v and 5-v microprocessors
- Package options: SOIC
- Protection features
  - Bus-fault protection of  $-27\ \text{V}$  to  $40\ \text{V}$
  - TXD dominant time-out
  - Thermal shutdown protection
  - Power up and power down glitch-free bus inputs and outputs
  - High bus input impedance with low  $V_{CC}$  (ideal passive behavior on bus when unpowered)

### 2 Applications

- GMW3122 Dual-wire CAN physical layer
- SAE J2284 High-speed CAN for automotive applications
- SAE J1939 Standard data bus interface
- ISO 11783 Standard data bus interface
- NMEA 2000 Standard data bus interface

### 3 Description

The SN65HVDA1040B-Q1 device meets or exceeds the specifications of the ISO 11898 standard for use in applications employing a controller area network (CAN). As a CAN transceiver, this device provides differential transmit capability to the bus and differential receive capability to a CAN controller at signaling rates up to 1 megabit per second (Mbps). The signaling rate of a line is the number of voltage transitions that are made per second, expressed in the units bps (bits per second).

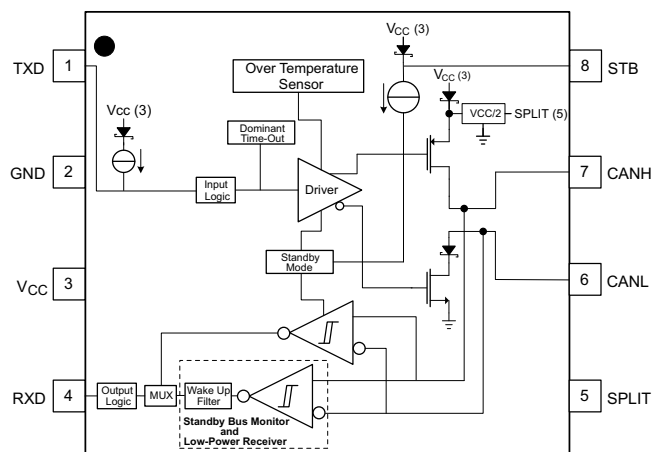
The device is designed for operation in especially harsh environments and includes many device protection features such as undervoltage lock out (UVLO), over-temperature thermal shutdown, wide common-mode range, and loss of ground protection. The bus pins are also protected against external cross-wiring, shorts to  $-27\ \text{V}$  to  $40\ \text{V}$ , and voltage transients according to ISO 7637. The device is qualified for use in automotive applications.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65HVDA1040B-Q1	SOIC (8)	4.90 mm x 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Block Diagram



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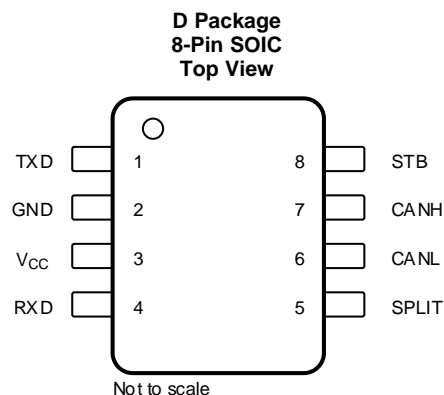
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2019	*	Initial release.

## 5 Pin Configuration and Functions



### Pin Functions

PIN		TYPE	DESCRIPTION
NAME	SOIC		
TXD	1	I	CAN transmit data input (low for dominant bus state, high for recessive bus state)
GND	2	GND	Ground connection
V <sub>CC</sub>	3	Supply	Transceiver 5-V supply voltage input
RXD	4	O	CAN receive data output (low in dominant bus state, high in recessive bus state)
SPLIT	5	O	Common-mode stabilization output
CANL	6	I/O	Low-level CAN bus line
CANH	7	I/O	High-level CAN bus line
STB	8	I	Standby mode select pin (active high)
NC	—	NC	No connect

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	−0.3	6	V
	Voltage range at bus terminals (CANH, CANL, SPLIT)	−27	40	V
I <sub>O</sub>	Receiver output current		20	mA
V <sub>I</sub>	Voltage input, ISO 7637 transient pulse <sup>(2)</sup> (CANH, CANL)	−150	100	V
V <sub>I</sub>	Voltage input (TXD, STB)	−0.3	6	V
T <sub>J</sub>	Junction temperature	−40	150	°C
T <sub>stg</sub>	Storage temperature	−40	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Tested in accordance with ISO 7637 test pulses 1, 2, 3a, 3b per IBEE system level test (Pulse 1 = −100 V, Pulse 2 = 100 V, Pulse 3a = −150 V, Pulse 3b = 100 V). If DC may be coupled with ac transients, externally protect the bus pins within the absolute maximum voltage range at any bus terminal. This device has been tested with dc bus shorts to 40 V with leading common-mode chokes. If common-mode chokes are used in the system and the bus lines may be shorted to DC, ensure that the choke type and value in combination with the node termination and shorting voltage either will not create inductive flyback outside of voltage maximum specification or use an external transient-suppression circuit to protect the transceiver from the inductive transients.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	Pins 7 and 6 <sup>(2)</sup>	±12000
			Pin 5 <sup>(3)</sup>	±10000
			All pins	±4000
		Charged-device model (CDM), per AEC Q100-011		±1500
		IEC 61000-4-2 according to IBEE CAN EMC test specification	Pins 7 and 6 connected to pin 2	±7000

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
- (2) Test method based upon JEDEC Standard 22 Test Method A114F and AEC-Q100-002, CANH and CANL bus pins stressed with respect to each other and GND.
- (3) Test method based upon JEDEC Standard 22 Test Method A114F and AEC-Q100-002, SPLIT pin stressed with respect to GND.

### 6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		4.75	5.25	V
V <sub>I</sub> or V <sub>IC</sub>	Voltage at any bus terminal (separately or common mode)		−12	12	V
V <sub>IH</sub>	High-level input voltage	TXD, STB	2	5.25	V
V <sub>IL</sub>	Low-level input voltage	TXD, STB	0	0.8	V
V <sub>ID</sub>	Differential input voltage		−6	6	V
I <sub>OH</sub>	High-level output current	Driver	−70		mA
		Receiver (RXD)	−2		
I <sub>OL</sub>	Low-level output current	Driver		70	mA
		Receiver (RXD)		2	
T <sub>A</sub>	Operating free-air temperature range	See <a href="#">Thermal Information</a>	−40	125	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>			SN65HVDA1040B-Q1	UNIT
			D (SOIC)	
			8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Low-K thermal resistance <sup>(2)</sup>	140	°C/W
		High-K thermal resistance <sup>(3)</sup>	112	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		56	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		50	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter		13	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter		55	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		–	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, Low-K board, as specified in JESD51-3, in an environment described in JESD51-2a.
- (3) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

## 6.5 Electrical Characteristics

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
<b>SUPPLY</b>						
$I_{CC}$	5-V supply current	Standby mode	STB at $V_{CC}$ , $V_I = V_{CC}$	6	12	μA
		Dominant	$V_I = 0$ V, 60-Ω load, STB at 0 V	50	70	mA
		Recessive	$V_I = V_{CC}$ , No load, STB at 0 V	6	10	
$UV_{VCC}$	Undervoltage reset threshold		2.8		4	V
<b>DRIVER</b>						
$V_{O(D)}$	Bus output voltage (dominant)	CANH	$V_I = 0$ V, STB at 0 V, $R_L = 60$ Ω, See <a href="#">Figure 3</a> and <a href="#">Figure 16</a>	2.9	3.4	V
		CANL		0.8	1.75	
$V_{O(R)}$	Bus output voltage (recessive)	$V_I = 3$ V, STB at 0 V, $R_L = 60$ Ω, See <a href="#">Figure 3</a> and <a href="#">Figure 16</a>	2	2.5	3	V
$V_O$	Bus output voltage (standby mode)	STB at $V_{CC}$ , $R_L = 60$ Ω, See <a href="#">Figure 3</a> and <a href="#">Figure 16</a>	–0.1		0.1	V
$V_{OD(D)}$	Differential output voltage (dominant)	$V_I = 0$ V, $R_L = 60$ Ω, STB at 0 V, See <a href="#">Figure 3</a> , <a href="#">Figure 16</a> , and <a href="#">Figure 4</a>	1.5		3	V
		$V_I = 0$ V, $R_L = 45$ Ω, STB at 0 V, See <a href="#">Figure 3</a> , <a href="#">Figure 16</a> , and <a href="#">Figure 4</a>	1.4		3	
$V_{OD(R)}$	Differential output voltage (recessive)	$V_I = 3$ V, STB at 0 V, $R_L = 60$ Ω, See <a href="#">Figure 3</a> and <a href="#">Figure 16</a>	–0.012		0.012	V
		$V_I = 3$ V, STB at 0 V, No load	–0.5		0.05	
$V_{SYM}$	Output symmetry (dominant or recessive) ( $V_{O(CANH)}$ + $V_{O(CANL)}$ )	STB at 0 V, $R_L = 60$ Ω, See <a href="#">Figure 14</a>	0.9 $V_{CC}$	$V_{CC}$	1.1 $V_{CC}$	V
$V_{OC(ss)}$	Steady-state common-mode output voltage	STB at 0 V, $R_L = 60$ Ω, See <a href="#">Figure 9</a>	2	2.5	3	V
$\Delta V_{OC(ss)}$	Change in steady-state common-mode output voltage	STB at 0 V, $R_L = 60$ Ω, See <a href="#">Figure 9</a>		30		mV
$V_{IH}$	High-level input voltage, TXD input		2			V
$V_{IL}$	Low-level input voltage, TXD input				0.8	V
$I_{IH}$	High-level input current, TXD input	$V_I$ at $V_{CC}$	–2		2	μA
$I_{IL}$	Low-level input current, TXD input	$V_I$ at 0 V	–50		–10	μA
$I_{O(off)}$	Power-off TXD output current	$V_{CC}$ at 0 V, TXD at 5 V			1	μA

(1) All typical values are at 25°C with a 5-V supply.

## Electrical Characteristics (continued)

over recommended operating conditions including operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$I_{OS(ss)}$ Short-circuit steady-state output current, Dominant	$V_{CANH} = -12\text{ V}$ , CANL open, TXD = low, See <a href="#">Figure 12</a>	–120	–85		mA
	$V_{CANH} = 12\text{ V}$ , CANL open, TXD = low, See <a href="#">Figure 12</a>		0.4	1	
	$V_{CANL} = -12\text{ V}$ , CANH open, TXD = low, See <a href="#">Figure 12</a>	–1	–0.6		
	$V_{CANL} = 12\text{ V}$ , CANH open, TXD = low, See <a href="#">Figure 12</a>		75	120	
	$V_{CANH} = 0\text{ V}$ , CANL open, TXD = low, See <a href="#">Figure 12</a>	–100	–75		
	$V_{CANL} = 32\text{ V}$ , CANH open, , TXD = low, See <a href="#">Figure 12</a>		75	125	
$I_{OS(ss)}$ Short-circuit steady-state output current, Recessive	$-20\text{ V} \leq V_{CANH} \leq 32\text{ V}$ , CANL open, TXD = high, See <a href="#">Figure 12</a>	–10		10	mA
	$-20\text{ V} \leq V_{CANL} \leq 32\text{ V}$ , CANH open, TXD = high, See <a href="#">Figure 12</a>	–10		10	
$C_O$ Output capacitance	See receiver input capacitance				
<b>RECEIVER</b>					
$V_{IT+}$ Positive-going input threshold voltage, high-speed mode	STB at 0 V, See <a href="#">Table 1</a>		800	900	mV
$V_{IT-}$ Negative-going input threshold voltage, high-speed mode	STB at 0 V, See <a href="#">Table 1</a>	500	650		mV
$V_{hys}$ Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )		100	125		mV
$V_{IT}$ Input threshold voltage, standby mode	STB at $V_{CC}$	500		1150	mV
$V_{OH}$ High-level output voltage	$I_O = -2\text{ mA}$ , See <a href="#">Figure 7</a>	4	4.6		V
$V_{OL}$ Low-level output voltage	$I_O = 2\text{ mA}$ , See <a href="#">Figure 7</a>		0.2	0.4	V
$I_{I(off)}$ Power-off bus input current (unpowered bus leakage current)	CANH = CANL = 5 V, $V_{CC}$ at 0 V, TXD at 0 V			3	$\mu\text{A}$
$I_{O(off)}$ Power-off RXD leakage current	$V_{CC}$ at 0 V, RXD at 5 V			20	$\mu\text{A}$
$C_I$ Input capacitance to ground (CANH or CANL)	TXD at 3 V, $V_I = 0.4 \sin(4E6\pi t) + 2.5\text{ V}$		13		pF
$C_{ID}$ Differential input capacitance	TXD at 3 V, $V_I = 0.4 \sin(4E6\pi t)$		6		pF
$R_{ID}$ Differential input resistance	TXD at 3 V, STB at 0 V	30		80	k $\Omega$
$R_{IN}$ Input resistance (CANH or CANL)	TXD at 3 V, STB at 0 V	15	30	40	k $\Omega$
$R_{I(m)}$ Input resistance matching $[1 - (R_{IN(CANH)} / R_{IN(CANL)})] \times 100\%$	$V_{(CANH)} = V_{(CANL)}$	–3%	0%	3%	
<b>STB PIN</b>					
$V_{IH}$ High-level input voltage, STB input		2			V
$V_{IL}$ Low-level input voltage, STB input				0.8	V
$I_{IH}$ High-level input current	STB at 2 V	–10		0	$\mu\text{A}$
$I_{IL}$ Low-level input current	STB at 0.8 V	–10		0	$\mu\text{A}$
<b>SPLIT PIN</b>					
$V_O$ Output voltage	$-250\text{ }\mu\text{A} < I_O < 250\text{ }\mu\text{A}$	0.3 $V_{CC}$	0.5 $V_{CC}$	0.7 $V_{CC}$	V
$I_{O(stb)}$ Leakage current, standby mode	STB at 2 V, $-12\text{ V} \leq V_O \leq 12\text{ V}$	–5		5	$\mu\text{A}$

## 6.6 Power Dissipation Characteristics

 over recommended operating conditions,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted)

	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_D$ Average power dissipation	$V_{CC} = 5\text{ V}$ , $T_J = 27^\circ\text{C}$ , $R_L = 60\text{ }\Omega$ , STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, $C_L$ at RXD = 15 pF		112		mW
	$V_{CC} = 5.5\text{ V}$ , $T_J = 130^\circ\text{C}$ , $R_L = 45\text{ }\Omega$ , STB at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, $C_L$ at RXD = 15 pF			170	
Thermal shutdown temperature			185		$^\circ\text{C}$

## 6.7 Switching Characteristics

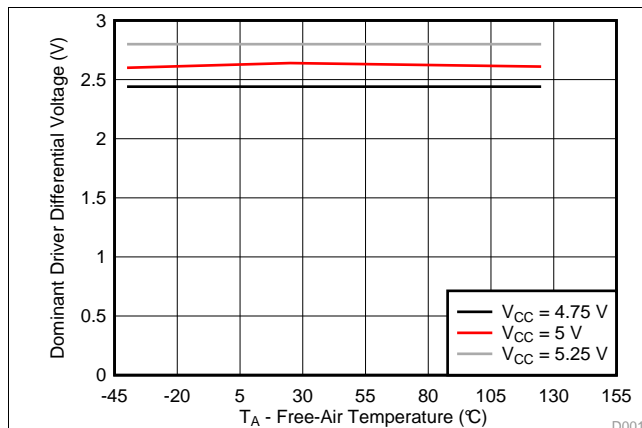
over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
DEVICE SWITCHING CHARACTERISTICS						
t <sub>d(LOOP1)</sub>	Total loop delay, driver input to receiver output, recessive to dominant	STB at 0 V, See <a href="#">Figure 10</a>	90	230	ns	
t <sub>d(LOOP2)</sub>	Total loop delay, driver input to receiver output, dominant to recessive	STB at 0 V, See <a href="#">Figure 10</a>	90	230	ns	
DRIVER SWITCHING CHARACTERISTICS						
t <sub>PLH</sub>	Propagation delay time, low-to-high level output	STB at 0 V, See <a href="#">Figure 5</a>	25	65	120	ns
t <sub>PHL</sub>	Propagation delay time, high-to-low level output	STB at 0 V, See <a href="#">Figure 5</a>	25	45	120	ns
t <sub>r</sub>	Differential output signal rise time	STB at 0 V, See <a href="#">Figure 5</a>		25		ns
t <sub>f</sub>	Differential output signal fall time	STB at 0 V, See <a href="#">Figure 5</a>		45		ns
t <sub>en</sub>	Enable time from standby mode to normal mode and transmission of dominant	See <a href="#">Figure 8</a>			10	μs
t <sub>(dom)</sub>	Dominant time-out <sup>(1)</sup>	↓V <sub>I</sub> , See <a href="#">Figure 11</a>	300	450	700	μs
RECEIVER SWITCHING CHARACTERISTICS						
t <sub>PLH</sub>	Propagation delay time, low-to-high-level output	STB at 0 V , See <a href="#">Figure 7</a>	60	90	130	ns
t <sub>PHL</sub>	Propagation delay time, high-to-low-level output	STB at 0 V , See <a href="#">Figure 7</a>	45	70	130	ns
t <sub>r</sub>	Output signal rise time	STB at 0 V , See <a href="#">Figure 7</a>		8		ns
t <sub>f</sub>	Output signal fall time	STB at 0 V , See <a href="#">Figure 7</a>		8		ns
t <sub>BUS</sub>	Dominant time required on bus for wakeup from standby	STB at V <sub>CC</sub> , See <a href="#">Figure 13</a>	1		5	μs

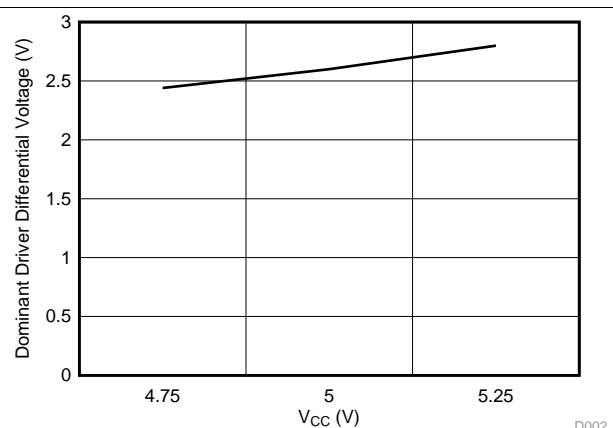
- (1) The TXD dominant time-out ( $t_{(dom)}$ ) disables the driver of the transceiver once the TXD has been dominant longer than  $t_{(dom)}$ , which releases the bus lines to recessive, preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after TXD has been returned HIGH (recessive). While this protects the bus from local faults, locking the bus dominant, it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where 5 successive dominant bits are followed immediately by an error frame. This, along with the  $t_{(dom)}$  minimum, limits the minimum bit rate. The minimum bit rate may be calculated by:

$$\text{Minimum Bit Rate} = 11 / t_{(dom)} = 11 \text{ bits} / 300 \mu\text{s} = 37 \text{ kbps}$$

## 6.8 Typical Characteristics

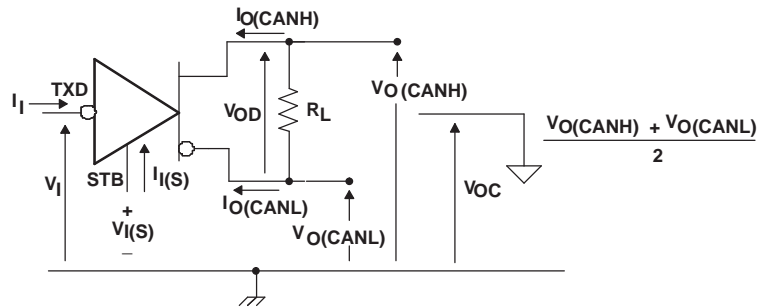


**Figure 1. Dominant Driver Differential Voltage vs Free-Air Temperature**

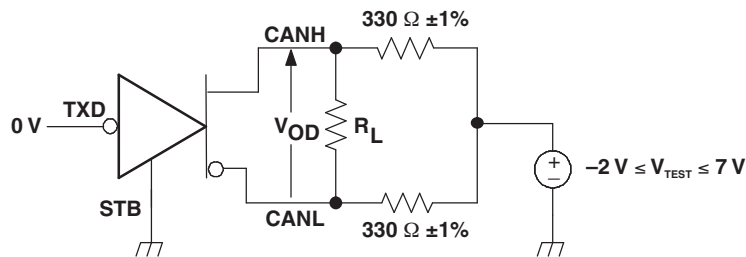


**Figure 2. Driver Differential Voltage vs. Supply Voltage**

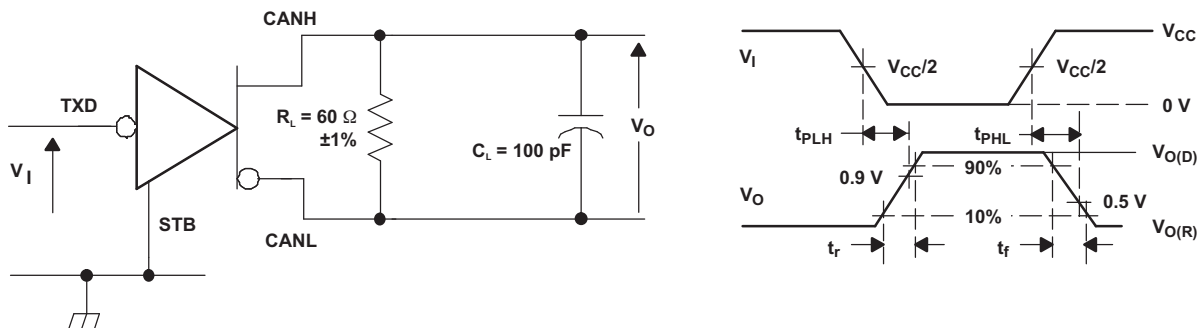
## 7 Parameter Measurement Information



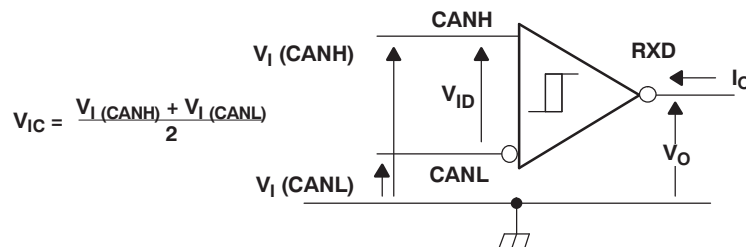
**Figure 3. Driver Voltage, Current, and Test Definition**



**Figure 4. Driver  $V_{OD}$  Test Circuit**



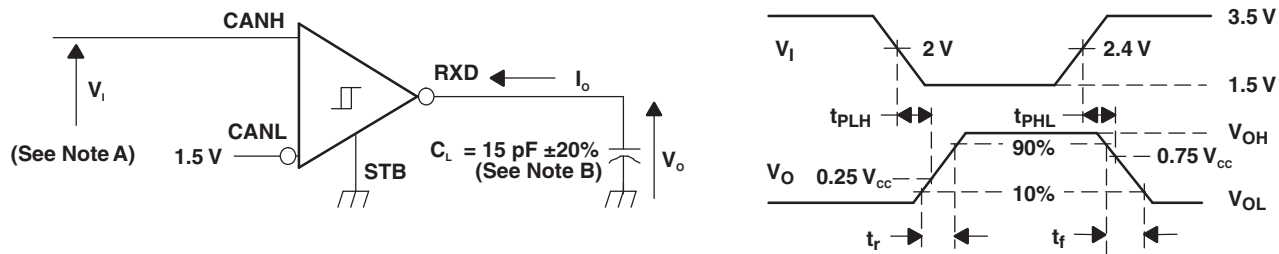
**Figure 5. Driver Test Circuit and Voltage Waveforms**



**Figure 6. Receiver Voltage and Current Definitions**



## Parameter Measurement Information (continued)

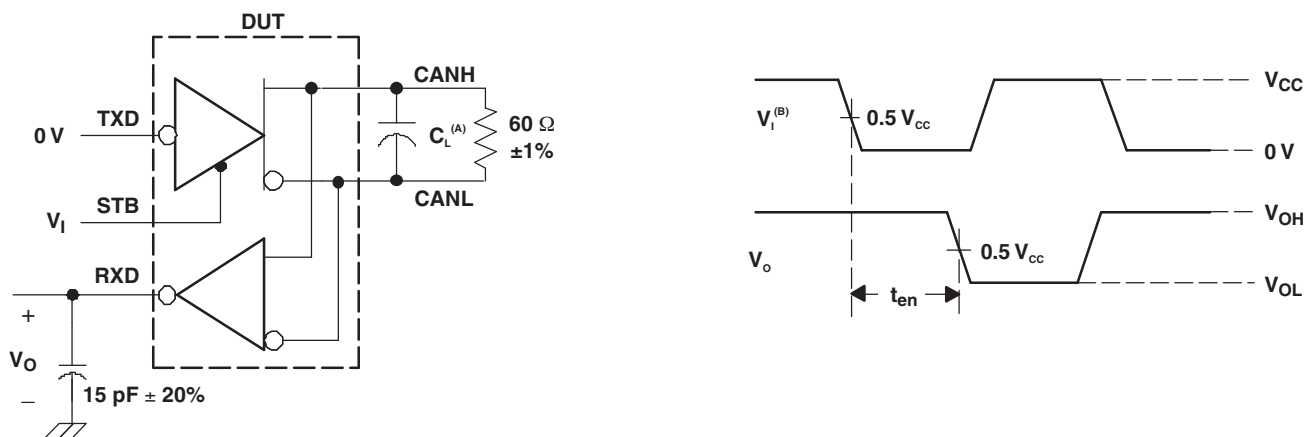


- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  125 kHz, 50% duty cycle,  $t_r \leq$  6 ns,  $t_f \leq$  6 ns,  $Z_O = 50 \Omega$ .
- B.  $C_L$  includes instrumentation and fixture capacitance within  $\pm 20\%$ .

Figure 7. Receiver Test Circuit and Voltage Waveforms

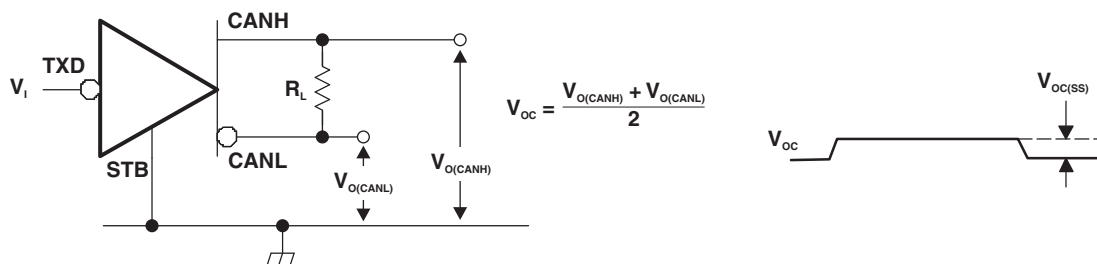
Table 1. Differential Input Voltage Threshold Test

INPUT			OUTPUT	
$V_{CANH}$	$V_{CANL}$	$ V_{ID} $	R	
-11.1 V	-12 V	900 mV	L	$V_{OL}$
12 V	11.1 V	900 mV	L	
-6 V	-12 V	6 V	L	
12 V	6 V	6 V	L	
-11.5 V	-12 V	500 mV	H	$V_{OH}$
12 V	11.5 V	500 mV	H	
-12 V	-6 V	6 V	H	
6 V	12 V	6 V	H	
Open	Open	X	H	



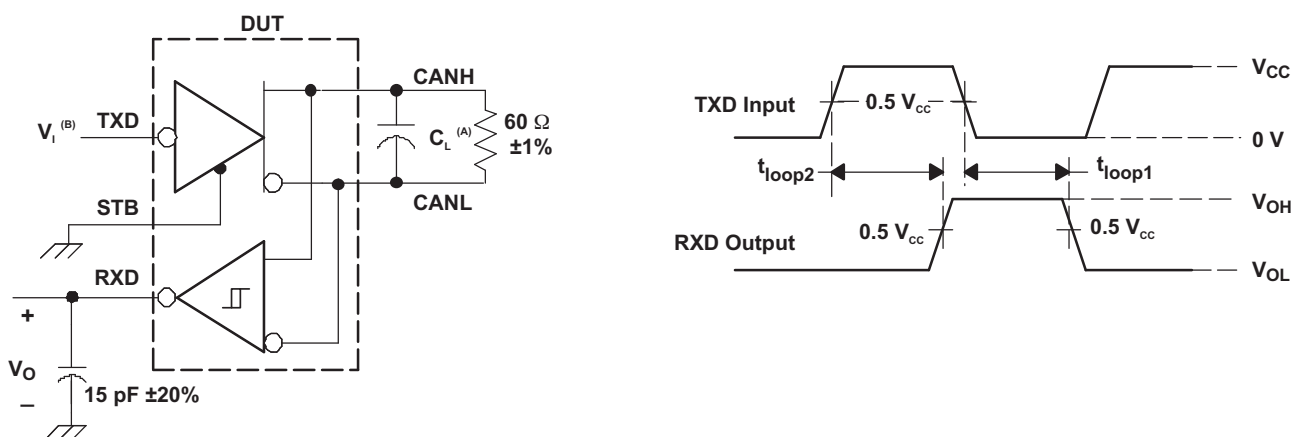
- A.  $C_L = 100$  pF and includes instrumentation and fixture capacitance within  $\pm 20\%$ .
- B. All  $V_i$  input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq$  6 ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

Figure 8.  $t_{en}$  Test Circuit and Waveforms



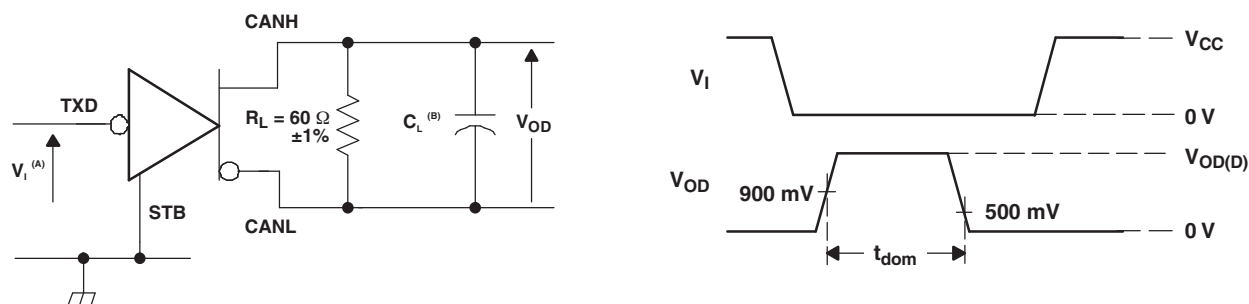
NOTE: All  $V_I$  input pulses are from 0 V to  $V_{CC}$  and supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 6$  ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

**Figure 9. Common-Mode Output Voltage Test and Waveforms**



- $C_L = 100$  pF and includes instrumentation and fixture capacitance within  $\pm 20\%$ .
- All  $V_I$  input pulses are from 0 V to  $V_{CC}$  and supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 6$  ns, pulse repetition rate (PRR) = 125 kHz, 50% duty cycle.

**Figure 10.  $t_{LOOP}$  Test Circuit and Waveforms**



- All  $V_I$  input pulses are from 0 V to  $V_{CC}$  and supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 6$  ns, pulse repetition rate (PRR) = 500 Hz, 50% duty cycle.
- $C_L = 100$  pF includes instrumentation and fixture capacitance within  $\pm 20\%$ .

**Figure 11. Dominant Time-Out Test Circuit and Waveforms**

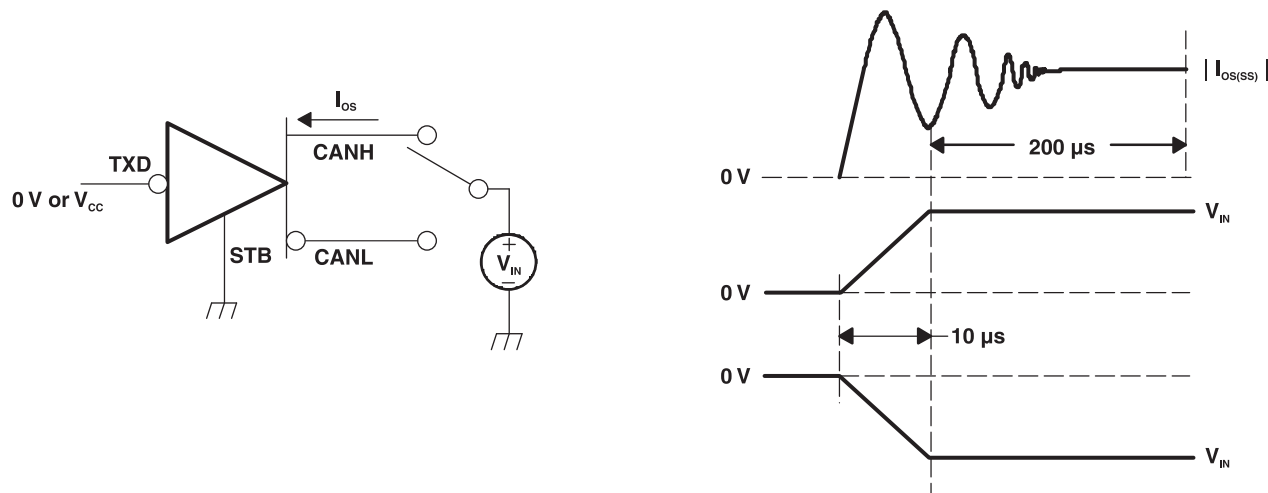
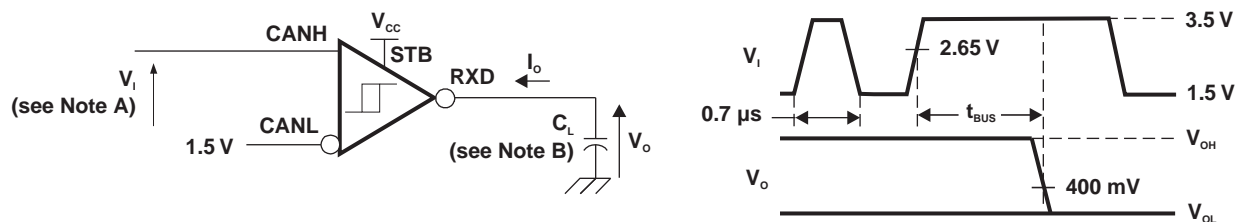
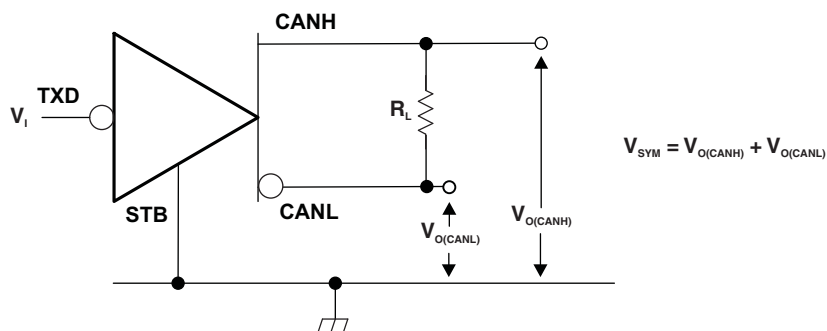


Figure 12. Driver Short-Circuit Current Test and Waveforms



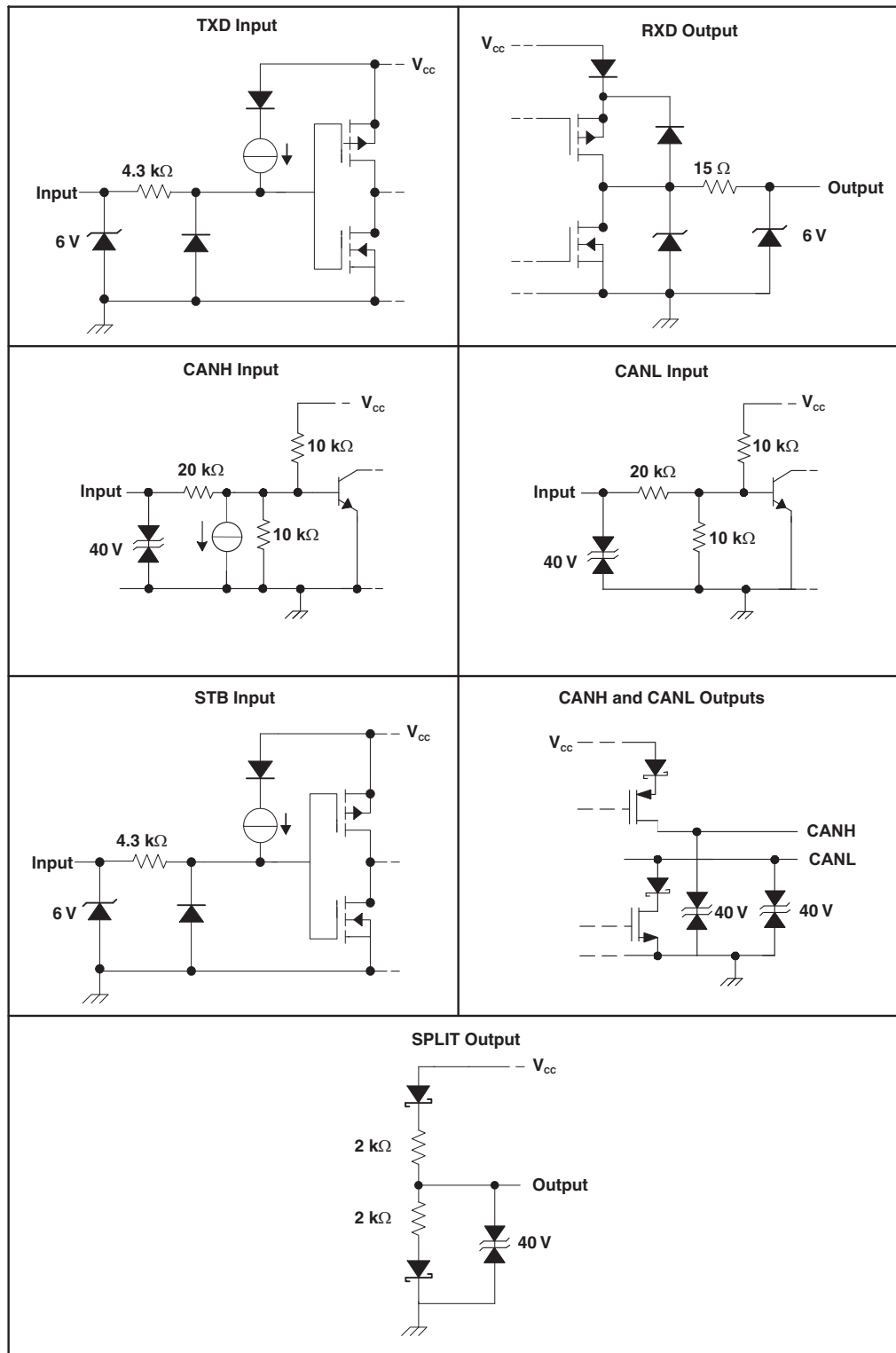
- A. For  $V_I$  bit width  $\leq 0.7 \mu\text{s}$ ,  $V_O = V_{OH}$ . For  $V_I$  bit width  $\geq 5 \mu\text{s}$ ,  $V_O = V_{OL}$ .  $V_I$  input pulses are supplied from a generator with the following characteristics:  $t_r/t_f < 6 \text{ ns}$ .
- B.  $C_L = 15 \text{ pF}$  and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

Figure 13.  $t_{BUS}$  Test Circuit and Waveforms



- A. All  $V_I$  input pulses are from  $0 \text{ V}$  to  $V_{CC}$  and supplied by a generator having the following characteristics:  $t_r/t_f \leq 6 \text{ ns}$ , pulse repetition rate (PRR) =  $250 \text{ kHz}$ , 50% duty cycle.

Figure 14. Driver Output Symmetry Test Circuit



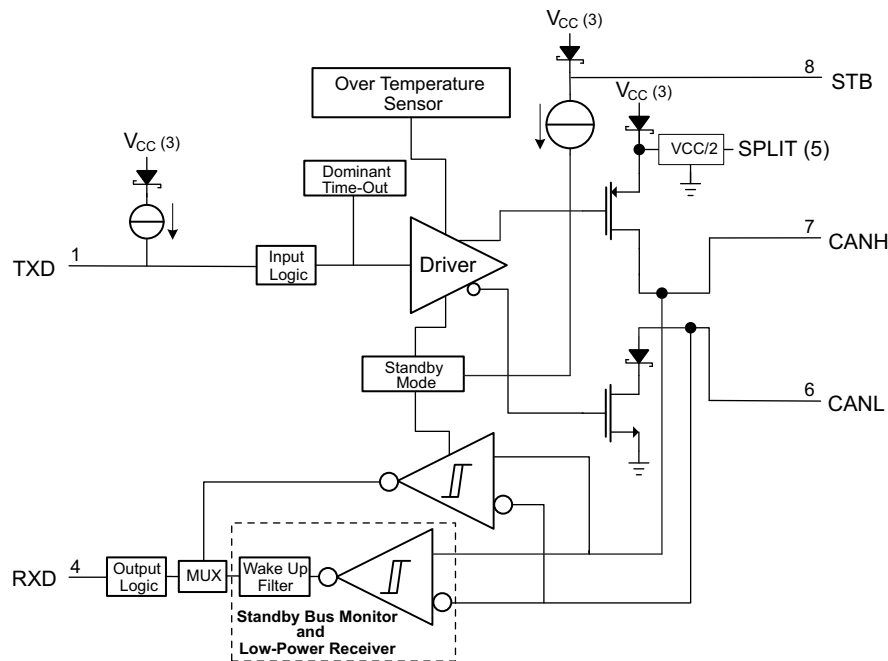
**Figure 15. Equivalent Input and Output Schematic Diagrams**

## 8 Detailed Description

### 8.1 Overview

The SN65HVDA1040B-Q1 CAN transceiver is compatible with the ISO 11898-2 high-speed CAN (Controller Area Network) physical layer standard. The device is designed to interface between the differential bus lines in controller area network and the CAN protocol controller at data rates up to 1 Mbps.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Operating Modes

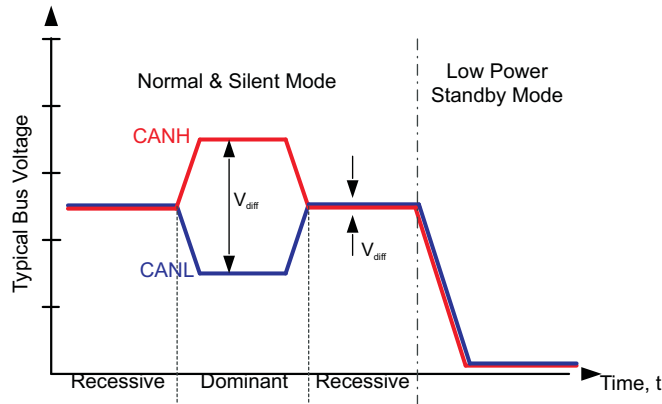
The device has two main operating modes: normal mode and standby mode. Operating mode selection is made through the STB input pin.

**Table 2. Operating Modes**

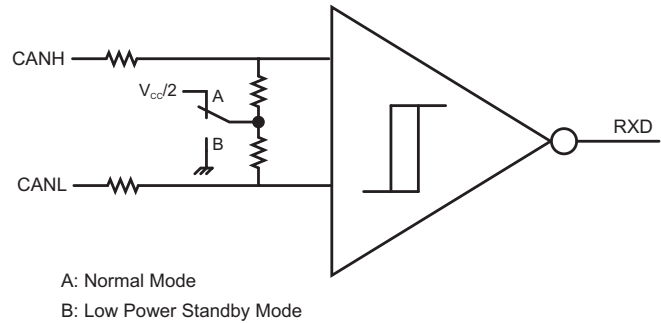
STB PIN	MODE	DRIVER	RECEIVER	RXD PIN
LOW	NORMAL	Enabled (On)	Enabled (On)	Mirrors CAN bus
HIGH	STANDBY	Disabled (Off)	Low-power wake-up receiver and bus monitor enabled (On)	Low = wake-up request received High = no wake-up request received

##### 8.3.1.1 Bus States by Mode

The CAN bus has three valid states during powered operation depending on the mode of the device. In normal mode the bus may be dominant (logic low) where the bus lines are driven differentially apart or recessive (logic high) where the bus lines are biased to  $V_{CC}/2$  through the high-ohmic internal input resistors  $R_{IN}$  of the receiver. The third state is low-power standby mode where the bus lines is biased to GND through the high-ohmic internal input resistors  $R_{IN}$  of the receiver.



**Figure 16. Bus States (Physical Bit Representation)**



**Figure 17. Simplified Common-Mode Bias and Receiver Implementation**

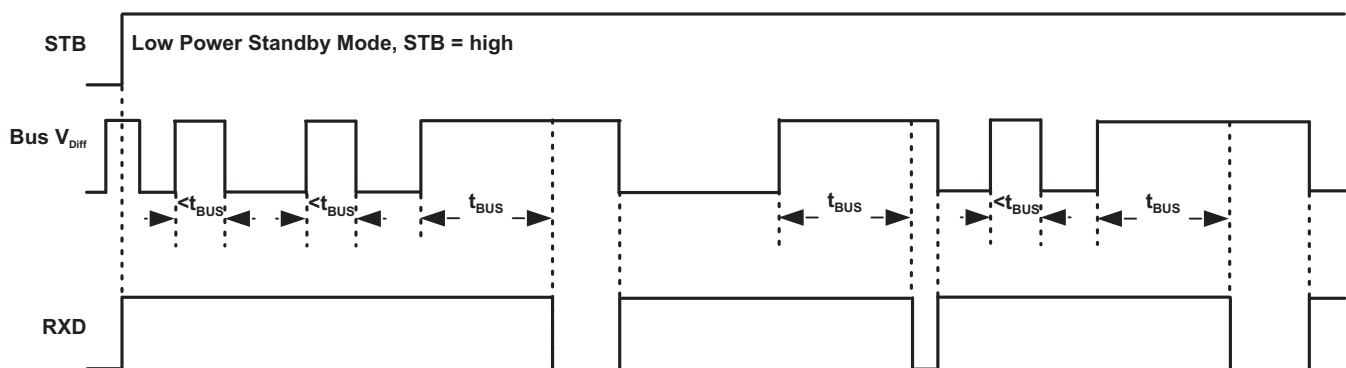
### 8.3.1.2 Normal Mode

This is the normal operating mode of the device. It is selected by setting STB low. The CAN driver and receiver are fully operational and CAN communication is bidirectional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD. In recessive state the bus pins are biased to  $0.5 \times V_{CC}$ . In dominant state the bus pins (CANH and CANL) are driven differentially apart. Logic high is equivalent to recessive on the bus and logic low is equivalent to a dominant (differential) signal on the bus.

The SPLIT pin is biased to  $0.5 \times V_{CC}$  for bus common-mode bus voltage bias stabilization in split termination network applications (see [Application and Implementation](#)).

### 8.3.1.3 Standby Mode and RXD Wake-Up Request

This is the low-power mode of the device. It is selected by setting STB high. The CAN driver and main receiver are turned off and bidirectional CAN communication is not possible. The low-power receiver and bus monitor are enabled to allow for wake-up requests through the bus. A wake-up request is output to RXD (driven low) for any dominant bus transmissions longer than the filter time  $t_{BUS}$ . The local protocol controller (MCU) should monitor RXD for transitions and then reactivate the device to normal mode based on the wake-up request. The CAN bus pins are weakly pulled to GND and the SPLIT pin is off (floating).



**Figure 18. Standby Mode Low-Power Receiver and Bus Monitor Behavior**

## 8.3.2 Protection Features

### 8.3.2.1 TXD Dominant State Time-Out

During normal mode (the only mode in which the CAN driver is active) the TXD dominant time-out circuit prevents the transceiver from blocking network communication in event of a hardware or software failure where TXD is held dominant longer than the time-out period  $t_{DST}$ . The dominant time-out circuit is triggered by a falling edge on TXD. If no rising edge is seen before the time-out constant of the circuit expires ( $t_{DST}$ ), the CAN bus driver is disabled, thus freeing the bus for communication between other network nodes. The CAN driver is re-activated when a recessive signal is seen on the TXD pin, thus clearing the dominant state time-out. The CAN bus pins are biased to recessive level during a TXD dominant state time-out and SPLIT remains on.

#### NOTE

The maximum dominant TXD time allowed by the TXD Dominant state time-out limits the minimum possible data rate of the device. The CAN protocol allows a maximum of 11 successive dominant bits (on TXD) for the worst case, where 5 successive dominant bits are followed immediately by an error frame. This, along with the  $t_{(dom)}$  minimum, limits the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate =  $11/t_{(dom)}$

### 8.3.2.2 Thermal Shutdown

If the junction temperature of the device exceeds the thermal shutdown threshold the device turns off the CAN driver circuits, including the SPLIT pin. This condition is cleared when the temperature drops below the thermal shutdown temperature of the device.

### 8.3.2.3 Undervoltage Lockout and Unpowered Device

The device has undervoltage detection and lockout on the  $V_{CC}$  supply. If an undervoltage condition is detected on  $V_{CC}$ , the device protects the bus.

The TXD pin is pulled up to  $V_{CC}$  to force a recessive input level if the pin floats. The STB is pulled up to  $V_{CC}$  to force the device in standby mode (low power) if the pin floats.

The bus pins (CANH, CANL, and SPLIT) all have extremely low leakage currents when the device is unpowered, so it does not load down the bus, but be an *ideal passive* load to the bus. This is critical, especially if some nodes of the network are unpowered while the rest of the network remains in operation.

## 8.4 Device Functional Modes

**Table 3. Driver Function Table<sup>(1)</sup>**

INPUTS		OUTPUTS		BUS STATE
TXD	STB	CANH	CANL	
L	L	H	L	Dominant
H	L	Z	Z	Recessive
Open	L	Z	Z	Recessive
X	H or Open	Y	Y	Recessive

(1) H = high level, L = low level, X = irrelevant, Y = weak pulldown to GND, ? = indeterminate, Z = high impedance

**Table 4. Receiver Function Table**

DIFFERENTIAL INPUTS $V_{ID} = V(CANH) - V(CANL)$	STB	OUTPUT RXD	BUS STATE
$V_{ID} \geq 0.9 \text{ V}$	L	L	Dominant
$V_{ID} \geq 1.15 \text{ V}$	H or Open	L	Dominant
$0.5 \text{ V} < V_{ID} < 0.9 \text{ V}$	X	?	?
$V_{ID} \leq 0.5 \text{ V}$	X	H	Recessive
Open	X	H	Recessive



## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

#### 9.1.1 Using With 3.3-V Microcontrollers

The input level threshold for the digital input pins of this device are 3.3-V compatible, however a few application considerations must be taken if using this device with 3.3-V microcontrollers. Both TXD and STB input pins have internal pullup sources to  $V_{CC}$ . Some microcontroller vendors recommend using an open-drain configuration on their I/O pins in this case even though the pullup limits the current. As such care must be taken at the application level that TXD and STB have sufficient pullup to meet system timing requirements for CAN. The internal pullup on TXD especially may not be sufficient to overcome the parasitic capacitances and allow for adequate CAN timing; thus, an additional external pullup may be required. Care should also be taken with the RXD pin of the microcontroller as the RXD output of this device drives the full  $V_{CC}$  range (5 V). If the microcontroller RXD input pin is not 5-V tolerant, this must be addressed at the application level. Other options include using a CAN transceiver from TI with I/O level adapting or a 3.3-V CAN transceiver.

#### 9.1.2 Using SPLIT With Split Termination

The SPLIT pin voltage output provides  $0.5 \times V_{CC}$  in normal mode. The circuit may be used by the application to stabilize the common-mode voltage of the bus by connecting it to the center tap of split termination for the CAN network (see [Figure 19](#) and [Figure 20](#)). This pin provides a stabilizing recessive voltage drive to offset leakage currents of unpowered transceivers or other bias imbalances that might bring the network common-mode voltage away from  $0.5 \times V_{CC}$ . Using this feature in a CAN network improves electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltage levels at the start of message transmissions.

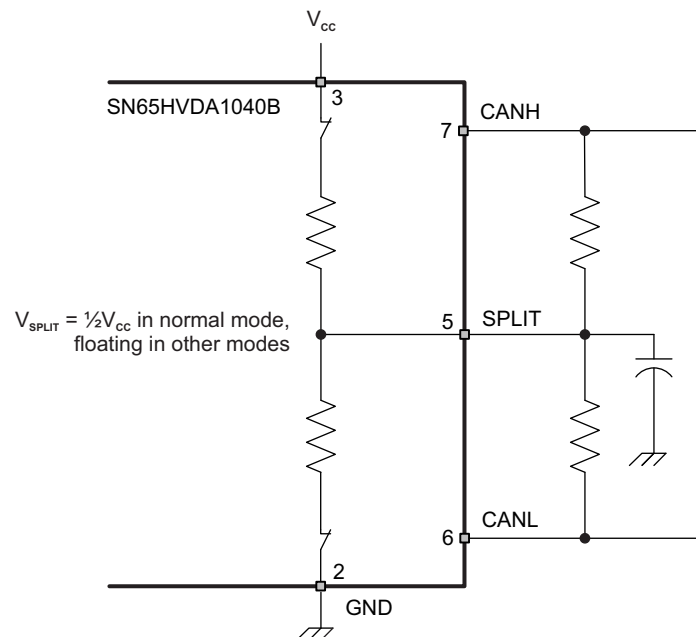
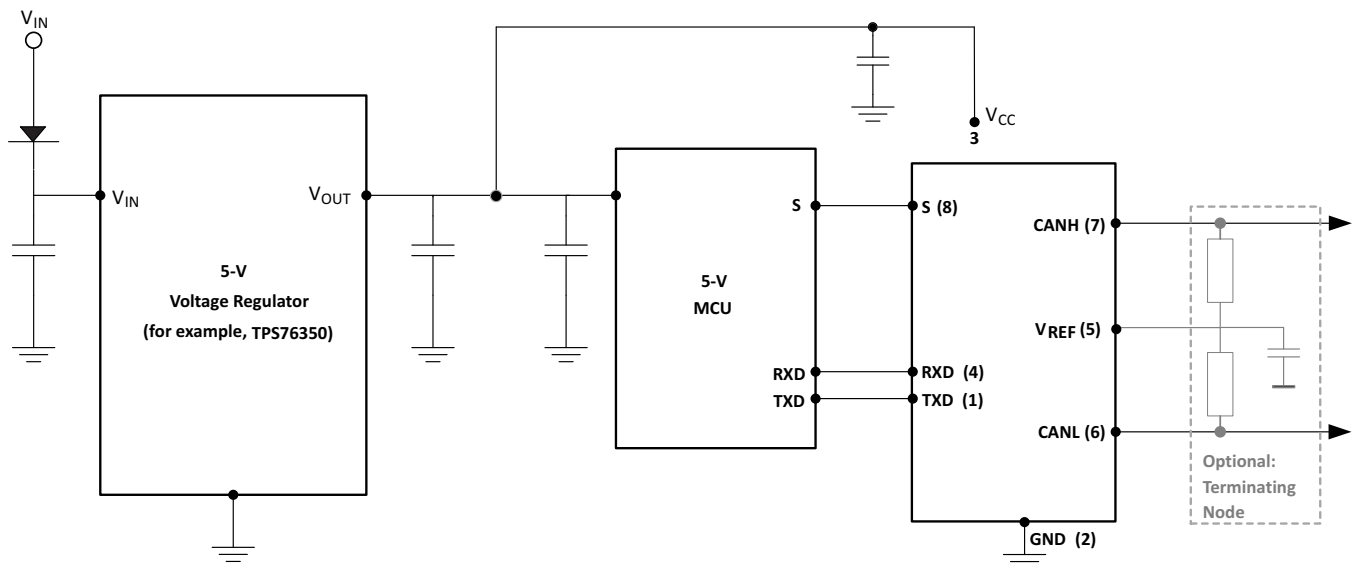


Figure 19. Split Pin Stabilization Circuitry and Application

## 9.2 Typical Application

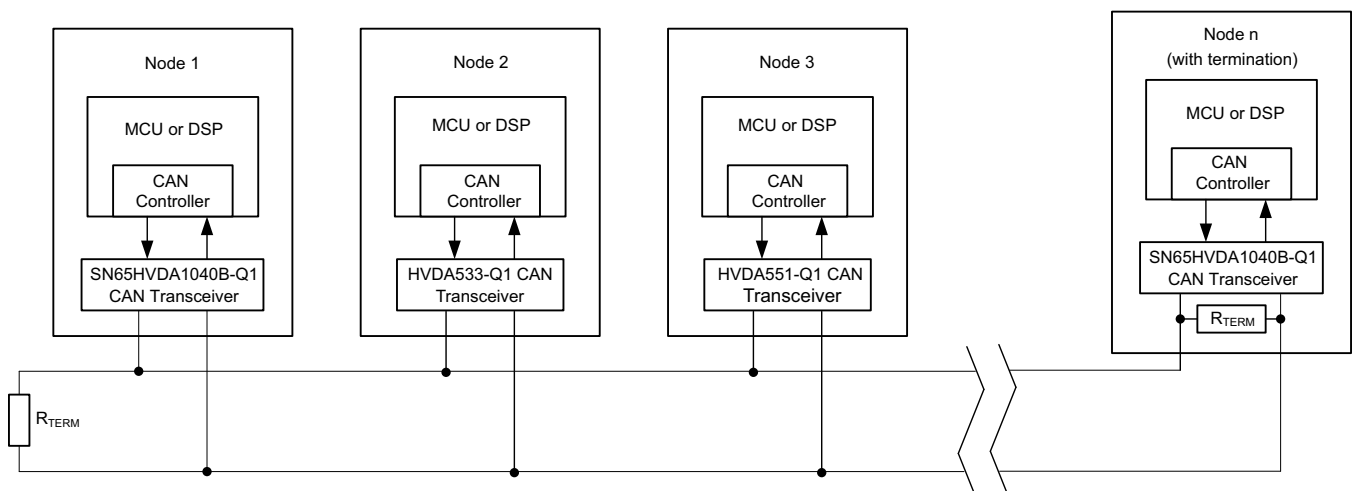


**Figure 20. Typical Application Using Split Termination for Stabilization**

### 9.2.1 Design Requirements

#### 9.2.1.1 Bus Loading, Length, and Number of Nodes

The ISO 11898 Standard specifies up to 1 Mbps data rate, maximum bus length of 40 meters, maximum drop line (stub) length of 0.3 meters, and a maximum of 30 nodes. However, with careful network design, the system may have longer cables, longer stub lengths, and many more nodes to a bus. Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898 standard. They have made system-level trade-offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CANopen, CAN Kingdom, DeviceNet, and NMEA200.



### Figure 21. Typical CAN Bus Drawing

## Typical Application (continued)

A high number of nodes requires a transceiver with high input impedance and wide common-mode range such as the SN65HVDA1040B-Q1 CAN transceiver. ISO 11898-2 specifies the driver differential output with a 60- $\Omega$  load (two 120- $\Omega$  termination resistors in parallel) and the differential output must be greater than 1.5 V. The SN65HVDA1040B-Q1 device is specified to meet the 1.5-V requirement with a 60- $\Omega$  load, and additionally specified with a differential output voltage minimum of 1.2 V across a common-mode range of –2 V to 7 V through a 330- $\Omega$  coupling network. This network represents the bus loading of 90 SN65HVDA1040B-Q1 transceivers based on their minimum differential input resistance of 30 k $\Omega$ . Therefore, the SN65HVDA1040B-Q1 supports up to 90 transceivers on a single bus segment with margin to the 1.2-V minimum differential input voltage requirement at each node.

For CAN network design, margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes may be lower. Bus length may also be extended beyond the original ISO 11898 standard of 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1-km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898 CAN standard.

### 9.2.1.2 CAN Termination

The ISO 11898 standard specifies the interconnect to be a twisted pair cable (shielded or unshielded) with 120- $\Omega$  characteristic impedance ( $Z_0$ ). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus the termination must be carefully placed so that it is not removed from the bus.

Termination is typically a 120- $\Omega$  resistor at each end of the bus. If filtering and stabilization of the common-mode voltage of the bus is desired, then split termination may be used (see [Figure 22](#) and [Using SPLIT With Split Termination](#)).

Care should be taken when determining the power ratings of the termination resistors. A typical worst case fault condition is if the system power supply and ground were shorted across the termination resistance which would result in much higher current through the termination resistance than the CAN transceiver's current limit.

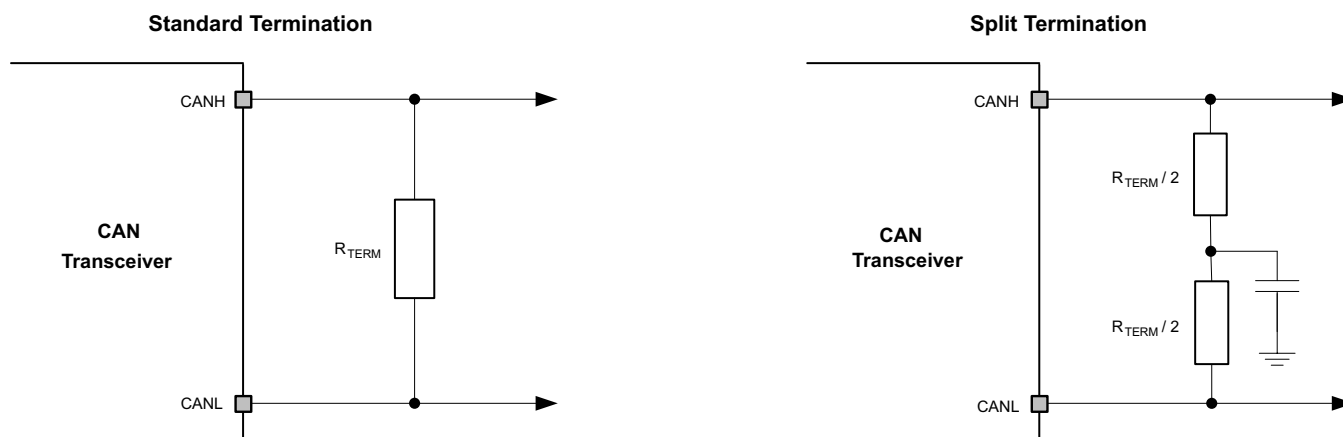


Figure 22. CAN Termination Schematic

### 9.2.1.3 Loop Propagation Delay

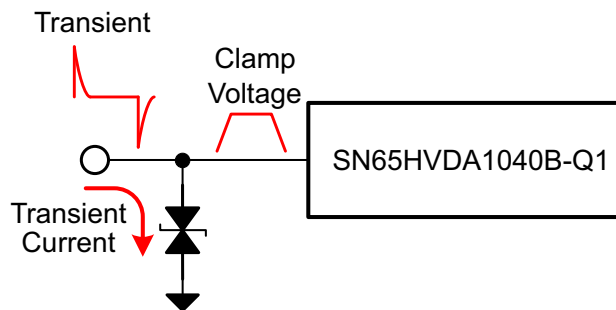
Transceiver loop delay is a measure of the overall device propagation delay, consisting of the delay from the driver input (the TXD pin) to the differential outputs (the CANH and CANL pins), plus the delay from the receiver inputs (the CANH and CANL) to its output (the RXD pin). A typical loop delay for the SN65HVDA1040B-Q1 transceiver is displayed in [Figure 24](#) and [Figure 25](#).

## Typical Application (continued)

### 9.2.2 Detailed Design Procedure

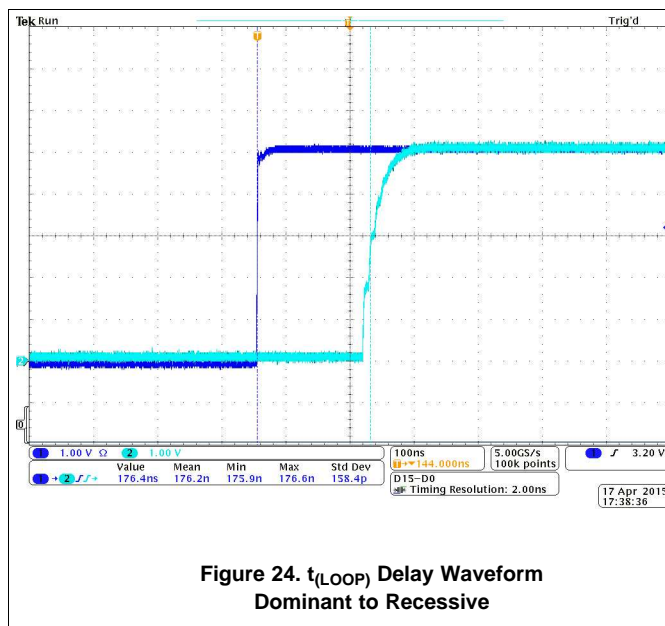
#### 9.2.2.1 Transient Voltage Suppressor (TVS) Diodes

Transient voltage suppressors are the preferred protection components for a CAN bus due to their low capacitance, which allows them to be designed into every node of a multinode network without requiring a reduction in data rate. With response times of a few picoseconds and power ratings of up to several kilowatts, TVS diodes present the most effective protection against ESD, burst, and surge transients.

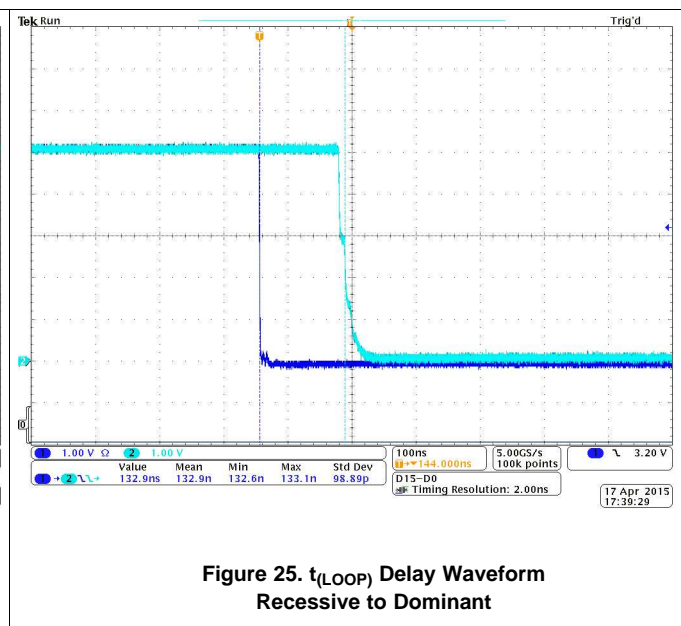


**Figure 23. Transient Voltage Suppressor (TVS) Diodes Schematic**

### 9.2.3 Application Curves



**Figure 24.  $t_{(LOOP)}$  Delay Waveform Dominant to Recessive**



**Figure 25.  $t_{(LOOP)}$  Delay Waveform Recessive to Dominant**

## 10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100-nF ceramic capacitor located as close as possible to the  $V_{CC}$  supply pins as possible. The TPS76350 device is a linear voltage regulator suitable for the 5-V supply rail.

## 11 Layout

### 11.1 Layout Guidelines

In order for the PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3-MHz to 3-GHz, high-frequency layout techniques must be applied during PCB design. On-chip IEC ESD protection is good for laboratory and portable equipment but is usually not sufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices at the bus connectors. Placement at the connector also prevents these harsh transient events from propagating further into the PCB and system.

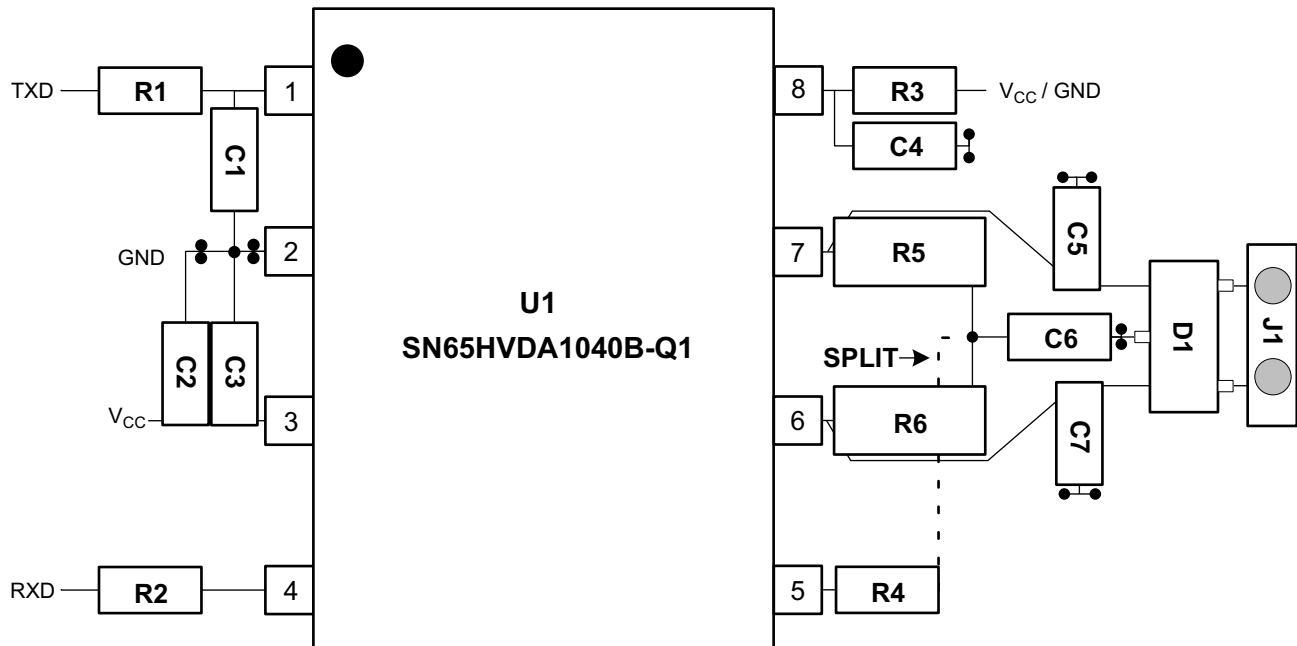
- Use  $V_{CC}$  and ground planes to provide low inductance.

#### NOTE

High-frequency current follows the path of least inductance and not the path of least resistance.

- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device. An example placement of the Transient Voltage Suppression (TVS) device indicated as D1 (either bidirectional diode or varistor solution) and bus filter capacitors C5 and C7 are shown in [Figure 26](#).
- The bus transient protection and filtering components should be placed as close to the bus connector, J1, as possible. This prevents transients, ESD and noise from penetrating onto the board and disturbing other devices.
- Bus termination: [Figure 22](#) shows split termination. This is where the termination is split into two resistors, R5 and R6, with the center or split tap of the termination connected to ground through capacitor C6. Split termination provides common-mode filtering for the bus. When termination is placed on the board instead of directly on the bus, care must be taken to ensure the terminating node is not removed from the bus as this causes signal integrity issues if the bus is not properly terminated on both ends.
- Bypass and bulk capacitors should be placed as close as possible to the supply pins of transceiver, examples include C2 and C3 ( $V_{CC}$ ).
- Use at least two vias for  $V_{CC}$  and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.
- To limit current of digital lines, serial resistors may be used. Examples are R1, R2, R3, and R4.
- To filter noise on the digital IO lines, a capacitor may be used close to the input side of the IO as shown by C1 and C4.
- Because the internal pullup and pulldown biasing of the device is weak for floating pins, an external 1-k $\Omega$  to 10-k $\Omega$  pullup or pulldown resistor should be used to bias the state of the pin more strongly against noise during transient events.
- Pin 1: If an open-drain host processor is used to drive the TXD pin of the device an external pullup resistor between 1 k $\Omega$  and 10 k $\Omega$  should be used to drive the recessive input state of the device.
- Pin 5: SPLIT should be connected to the center point of a split termination scheme to help stabilize the common-mode voltage to  $V_{CC}/2$ . If SPLIT is unused it should be left floating.
- Pin 8: Is shown assuming the mode pin, STB, is used. If the device only used in normal mode, R3 is not needed and the pads of C4 could be used for the pulldown resistor to GND.

## 11.2 Layout Example



**Figure 26. Typical CAN Bus Layout Example**

## 11.3 ESD Protection

A typical application that employs a CAN bus network may require some form of ESD, burst, and surge protection to shield the CAN transceiver against unwanted transients that can potentially damage the transceiver. To help shield the SN65HVDA1040B-Q1 transceiver against these high energy transients, transient voltage suppressors can be implemented on the CAN differential bus terminals. These devices help absorb the impact of a ESD, burst, and/or surge strike.

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN65HVDA1040BQDRQ1</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A1040B
SN65HVDA1040BQDRQ1.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A1040B

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVDA1040BQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVDA1040BQDRQ1	SOIC	D	8	2500	353.0	353.0	32.0



**D0008A**

# PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

**D0008A**

### SOIC - 1.75 mm max height

## SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



## SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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