

SNx4AHC594 8-Bit Shift Registers With Output Registers

1 Features

- Operating range 2V to 5.5V V_{CC}
- 8-bit serial-in, parallel-out shift registers with storage
- Independent direct overriding clears on shift and storage registers
- Independent clocks for shift and storage registers
- Latch-up performance exceeds 100mA per JESD 78, class II
- ESD protection exceeds JESD 22
 - 2000V human-body model (A114-A)
 - 1000V charged-device model (C101)

2 Applications

- Network Switches
- Power Infrastructures
- PCs and Notebooks
- LED Displays
- Servers

3 Description

The SNx4AHC594 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clear (SRCLR, RCLR) inputs are provided on the shift and storage registers. A serial (Q_H') output is provided for cascading purposes.

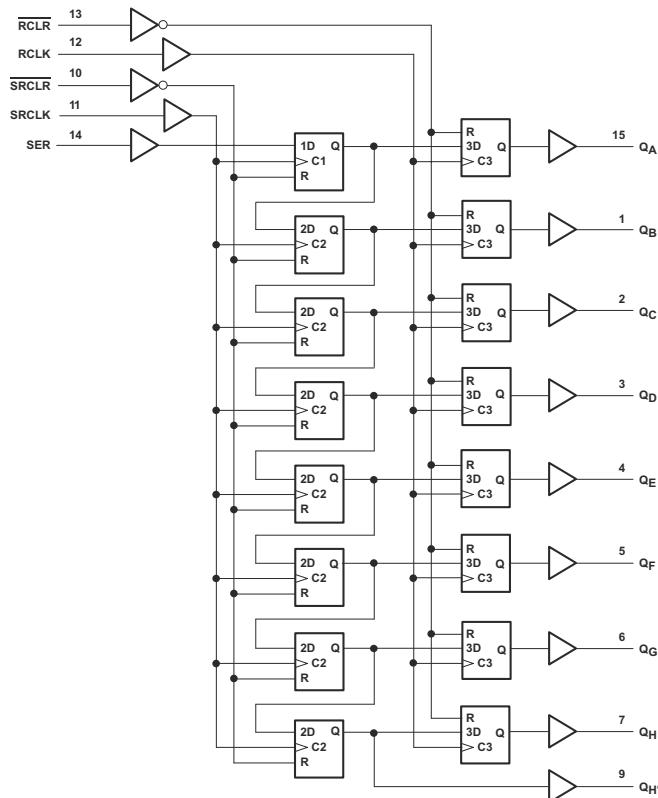
Device Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE ⁽³⁾
SNx4AHC594	D (SOIC, 16)	9.90 mm × 6mm	9.90 mm × 3.90 mm
	DB (SSOP, 16)	6.20 mm × 7.8mm	6.20 mm × 5.30 mm
	N (PDIP, 16)	19.31 mm × 9.4mm	19.31 mm × 6.35 mm
	NS (SOP, 16)	5mm × 6.4mm	5mm × 4.4mm
	PW (TSSOP, 16)	5.00 mm × 6.4mm	5.00 mm × 4.40 mm

(1) For more information, see [Section 11](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.

(3) The body size (length × width) is a nominal value and does not include pins.



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

Simplified Schematic



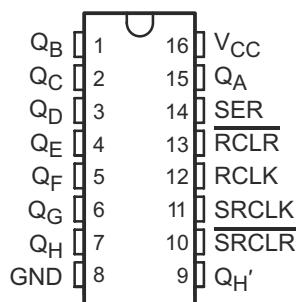
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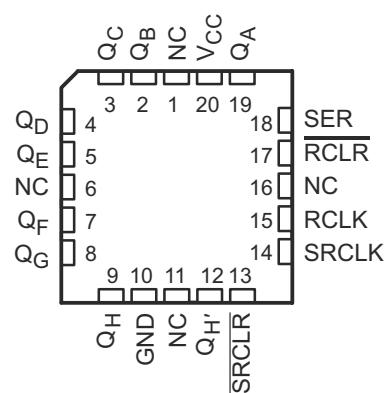
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4 Pin Configuration and Functions

SN54AHC594 . . . J OR W PACKAGE
SN74AHC594 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AHC594 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

Table 4-1. Pin Functions

Name	Pin			I/O	Description
	SN54AHC594	J, W	D, DB, N, NS, PW		
GND	10	8	8	—	Ground Pin
NC	1	—	—	—	No connect
	6				
	11				
	16				
Q _A	19	15	15	O	Q _A Output
Q _B	2	1	1	O	Q _B Output
Q _C	3	2	2	O	Q _C Output
Q _D	4	3	3	O	Q _D Output
Q _E	5	4	4	O	Q _E Output
Q _F	7	5	5	O	Q _F Output
Q _G	8	6	6	O	Q _G Output
Q _H	9	7	7	O	Q _H Output
Q _{H'}	12	9	9	O	Q _{H'} Output
RCLK	15	12	12	I	RCLK Input
RCLR	17	13	13	I	RCLR Input
SER	18	14	14	I	SER Input
SRCLK	14	11	11	I	SRCLK Input
SRCLR	13	10	10	I	SRCLR Input
V _{CC}	20	16	16	—	Power pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	7	V
V _I	Input voltage range ⁽²⁾		-0.5	7	V
V _O	Output voltage range ⁽²⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-20	mA
I _{OK}	Output clamp current	V _O < 0 or V _O > V _{CC}		±20	mA
I _O	Continuous output current	V _O = 0 to V _{CC}		±25	mA
	Continuous current through V _{CC} or GND			±75	mA
T _{stg}	Storage temperature range		-65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		SN54AHC594 ⁽²⁾		SN74AHC594		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	1.5		V
		V _{CC} = 3 V	2.1	2.1		
		V _{CC} = 5.5 V	3.85	3.85		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	0.5		V
		V _{CC} = 3 V	0.9	0.9		
		V _{CC} = 5.5 V	1.65	1.65		
V _I	Input voltage	0	5.5	0	5.5	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	-50	-50	μA	mA
		V _{CC} = 3 V ± 0.3 V	-4	-4		
		V _{CC} = 5.5 V ± 0.5 V	-8	-8		
I _{OL}	Low-level output current	V _{CC} = 2 V	50	50	μA	mA
		V _{CC} = 3 V ± 0.3 V	4	4		
		V _{CC} = 5.5 V ± 0.5 V	8	8		
Δt/Δv	Input transition rise and fall time	V _{CC} = 3 V ± 0.3 V	100	100	ns/V	ns/V
		V _{CC} = 5.5 V ± 0.5 V	20	20		

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	T _A	SN54AHC594 ⁽²⁾		SN74AHC594		UNIT
		MIN	MAX	MIN	MAX	
	Operating free-air temperature	-55	125	-40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, (SCBA004).

(2) Product Preview

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74AHC594					UNIT
	D	DB	N	NS	PW	
	16 PINS					
R _{θJA}	Junction-to-ambient thermal resistance	80.2	97.5	47.5	79.1	135.9
R _{θJC(top)}	Junction-to-case (top) thermal resistance	39.1	47.7	34.9	35.4	70.3
R _{θJB}	Junction-to-board thermal resistance	27.7	48.1	27.5	39.9	81.3
Ψ _{JT}	Junction-to-top characterization parameter	9.9	9.8	19.8	5.4	22.5
Ψ _{JB}	Junction-to-board characterization parameter	37.4	47.6	27.4	39.5	80.8
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	n/a

(1) For more information about traditional and new thermal metrics, see the TI application report *IC Package Thermal Metrics* (SPRA953).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHC594 ⁽²⁾		SN74AHC594		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		2.48		
	I _{OH} = -8 mA	4.5 V	3.94			3.8		3.8		
	Q _A – Q _H I _{OH} = -8 mA		3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 µA	2 V		0.1		0.1		0.1		V
		3 V		0.1		0.1		0.1		
		4.5 V		0.1		0.1		0.1		
	I _{OL} = 4 mA	3 V		0.36		0.5		0.44		
	I _{OL} = 8 mA	4.5 V		0.36		0.5		0.44		
				0.36		0.5		0.44		
I _I	V _I = 5.5 V or GND	0 to 5.5 V		±0.1		±1 ⁽¹⁾		±1	µA	
I _{CC}	V _I = V _{CC} or GND I _O = 0	5.5 V		4		40		40	µA	
C _i	V _I = V _{CC} or GND	5 V	2	10				10	pF	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

(2) Product Preview

5.6 Timing Requirements, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

			$T_A = 25^\circ\text{C}$		SN54AHC594 ⁽²⁾		SN74AHC594		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse Duration	RCLK or SRCLK high or low	5.5		5.5		5.5		ns
		RCLR or \bar{SRCLR} low	5		5		5		
t_{su}	Setup time	SER before SRCLK \uparrow	3.5		3.5		3.5		ns
		SRCLK \uparrow before RCLK \uparrow ⁽¹⁾	8		8.5		8.5		
		SRCLR low before SRCLK \uparrow	8		9		9		
		SRCLR high (inactive) before SRCLK \uparrow	4.2		4.8		4.8		
		RCLR high (inactive) before RCLK \uparrow	4.6		5.3		5.3		
t_h	Hold time, data after CLK \uparrow	SER after SRCLK \uparrow	1.5		1.5		1.5		ns

(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

(2) Product Preview

5.7 Timing Requirements, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

			$T_A = 25^\circ\text{C}$		SN54AHC594 ⁽²⁾		SN74AHC594		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse Duration	RCLK or SRCLK high or low	5		5		5		ns
		RCLR or \bar{SRCLR} low	5.2		5.2		5.2		
t_{su}	Setup time	SER before SRCLK \uparrow	3		3		3		ns
		SRCLK \uparrow before RCLK \uparrow ⁽¹⁾	5		5		5		
		SRCLR low before SRCLK \uparrow	5		5		5		
		SRCLR high (inactive) before SRCLK \uparrow	2.9		3.3		3.3		
		RCLR high (inactive) before RCLK \uparrow	3.2		3.7		3.7		
t_h	Hold time, data after CLK \uparrow	SER after SRCLK \uparrow	2		2		2		ns

(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

(2) Product Preview

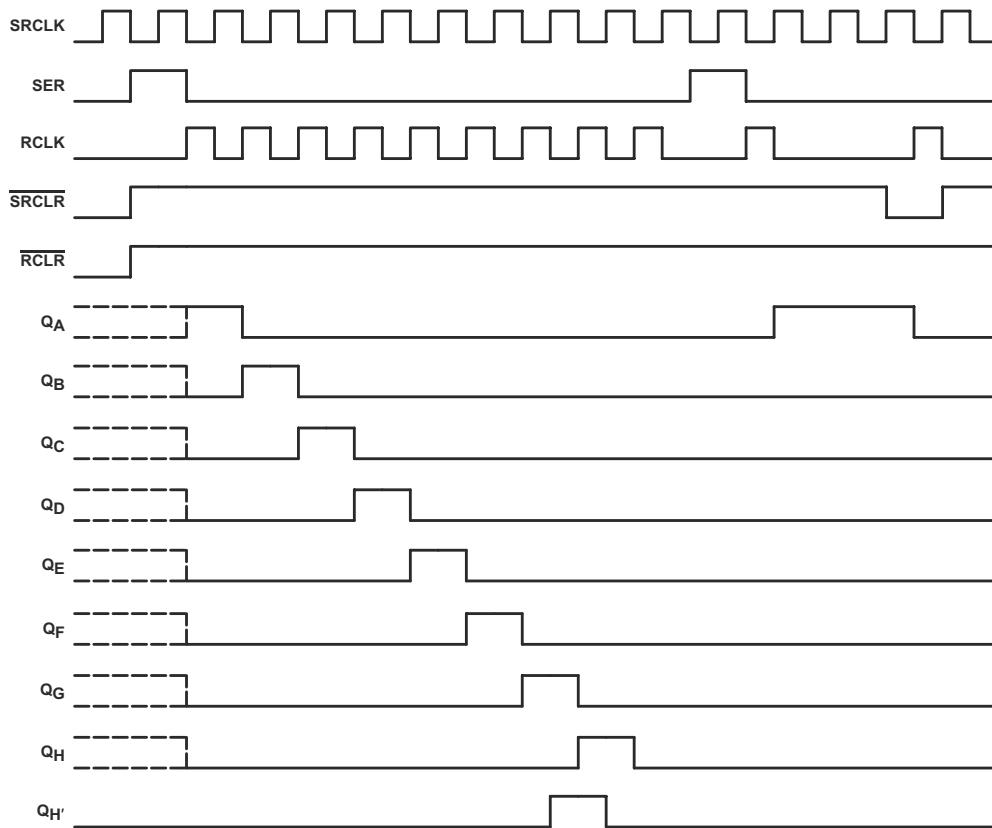


Figure 5-1. Timing Diagram

5.8 Switching Characteristics, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC594 ⁽²⁾		SN74AHC594		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15 \text{ pF}$	80 ⁽¹⁾	120 ⁽²⁾		70 ⁽¹⁾		70		MHz
			$C_L = 50 \text{ pF}$	55	105		50		50		
t_{PLH}	RCLK	$Q_A - Q_H$	$C_L = 15 \text{ pF}$	4.6 ⁽¹⁾	8 ⁽¹⁾		1 ⁽¹⁾	8.5 ⁽¹⁾	1	8.5	ns
				4.9 ⁽¹⁾	8.2 ⁽¹⁾		1 ⁽¹⁾	8.8 ⁽¹⁾	1	8.8	
t_{PLH}	SRCLK	$Q_{H'}$	$C_L = 15 \text{ pF}$	5.4 ⁽¹⁾	9.1 ⁽¹⁾		1 ⁽¹⁾	9.7 ⁽¹⁾	1	9.7	ns
				5.5 ⁽¹⁾	9.2 ⁽¹⁾		1 ⁽¹⁾	9.9 ⁽¹⁾	1	9.9	
t_{PHL}	RCLR	$Q_A - Q_H$	$C_L = 15 \text{ pF}$	6 ⁽¹⁾	9.8 ⁽¹⁾		1 ⁽¹⁾	10.6 ⁽¹⁾	1	10.6	ns
t_{PHL}	SRCLR	$Q_{H'}$	$C_L = 15 \text{ pF}$	5.6 ⁽¹⁾	9.2 ⁽¹⁾		1 ⁽¹⁾	10 ⁽¹⁾	1	10	ns
t_{PLH}	RCLK	$Q_A - Q_H$	$C_L = 50 \text{ pF}$	6.9	10.5		1	11.1	1	11.1	ns
				8.1	11.9		1	13.1	1	13.1	
t_{PLH}	SRCLK	$Q_{H'}$	$C_L = 50 \text{ pF}$	7.7	11.7		1	12.4	1	12.4	ns
				8.4	12.5		1	13.9	1	13.9	
t_{PHL}	RCLR	$Q_A - Q_H$	$C_L = 50 \text{ pF}$	9.1	13.1		1	14.4	1	14.4	ns
t_{PHL}	SRCLR	$Q_{H'}$	$C_L = 50 \text{ pF}$	8.5	12.4		1	14	1	14	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) Product Preview

5.9 Switching Characteristics, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC594 ⁽²⁾		SN74AHC594		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15 \text{ pF}$	135 ⁽¹⁾	170 ⁽¹⁾		115 ⁽¹⁾		115		MHz
			$C_L = 50 \text{ pF}$	120	140		95		95		
t_{PLH}	RCLK	$Q_A - Q_H$	$C_L = 15 \text{ pF}$		3.3 ⁽¹⁾	6.2 ⁽¹⁾	1 ⁽¹⁾	6.5 ⁽¹⁾	1	6.5	ns
t_{PHL}					3.7 ⁽¹⁾	6.5 ⁽¹⁾	1 ⁽¹⁾	6.9 ⁽¹⁾	1	6.9	
t_{PLH}	SRCLK	Q_H'	$C_L = 15 \text{ pF}$		3.7 ⁽¹⁾	6.8 ⁽¹⁾	1 ⁽²⁾	7.2 ⁽¹⁾	1	7.2	ns
t_{PHL}					4.1 ⁽¹⁾	7.2 ⁽¹⁾	1 ⁽¹⁾	7.6 ⁽¹⁾	1	7.6	
t_{PHL}	$\overline{\text{RCLR}}$	$Q_A - Q_H$	$C_L = 15 \text{ pF}$		4.5 ⁽¹⁾	7.6 ⁽¹⁾	1 ⁽¹⁾	8.2 ⁽¹⁾	1	8.2	ns
t_{PHL}	$\overline{\text{SRCLR}}$	Q_H'	$C_L = 15 \text{ pF}$		4.1 ⁽¹⁾	7.1 ⁽¹⁾	1 ⁽¹⁾	7.6 ⁽¹⁾	1	7.6	ns
t_{PLH}	RCLK	$Q_A - Q_H$	$C_L = 50 \text{ pF}$		4.9	7.8	1	8.3	1	8.3	ns
t_{PHL}					5.8	8.9	1	9.7	1	9.7	
t_{PLH}	SRCLK	Q_H'	$C_L = 50 \text{ pF}$		5.5	8.6	1	9.1	1	9.1	ns
t_{PHL}					6	9.2	1	10.1	1	10.1	
t_{PHL}	$\overline{\text{RCLR}}$	$Q_A - Q_H$	$C_L = 50 \text{ pF}$		6.6	10	1	10.7	1	10.7	ns
t_{PHL}	$\overline{\text{SRCLR}}$	Q_H'	$C_L = 50 \text{ pF}$		6	9.2	1	10.1	1	10.1	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) Product Preview

5.10 Noise Characteristics

$V_{CC} = 5 \text{ V}$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$ ⁽¹⁾

PARAMETER	SN74AHC594			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		1	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.6	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.8	V
$V_{IH(D)}$	High-level dynamic input voltage		3.5	V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

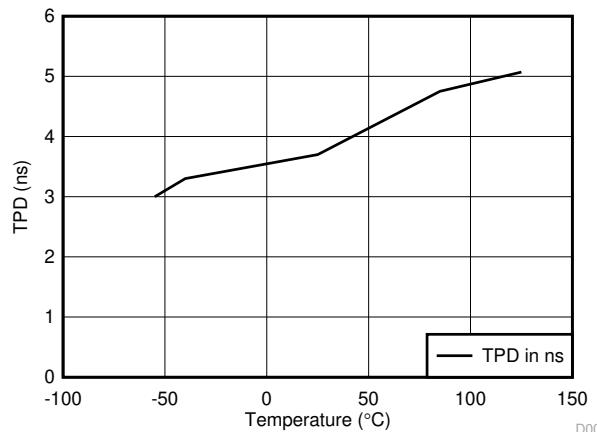
(1) Characteristics are for surface-mount packages only.

5.11 Operating Characteristics

$V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1 \text{ MHz}$	112	pF

5.12 Typical Characteristics



**Figure 5-2. SN74AHC594 TPD vs Temperature, 15
pF Load
RCLK to Q**

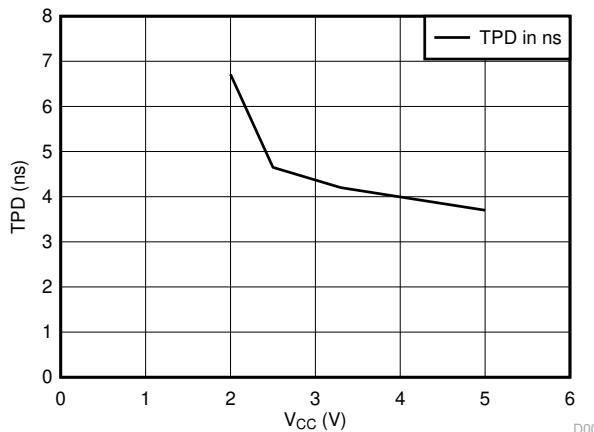
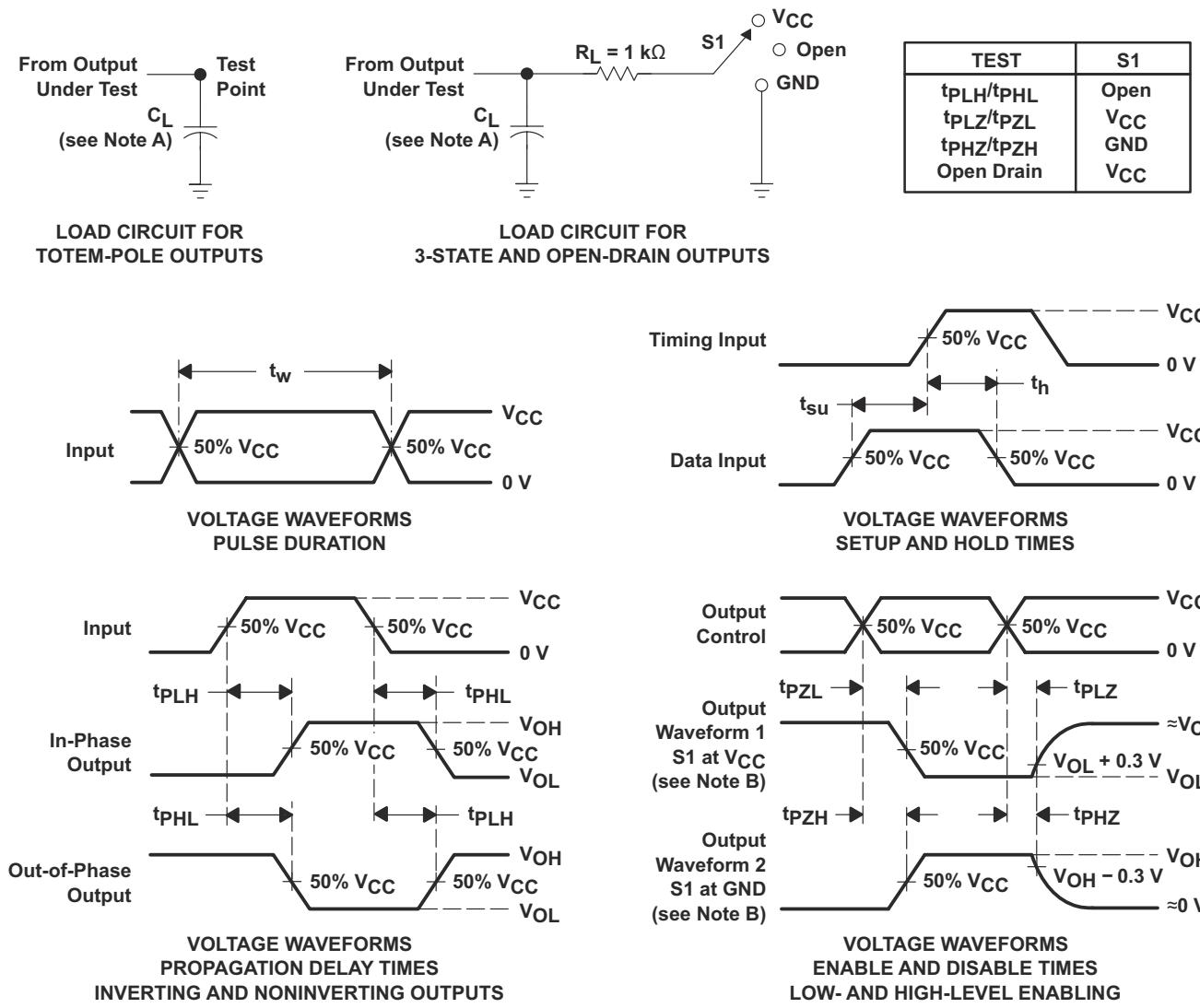


Figure 5-3. TPD vs V_{CC}

6 Parameter Measurement Information



NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
- The outputs are measured one at a time with one input transition per measurement.

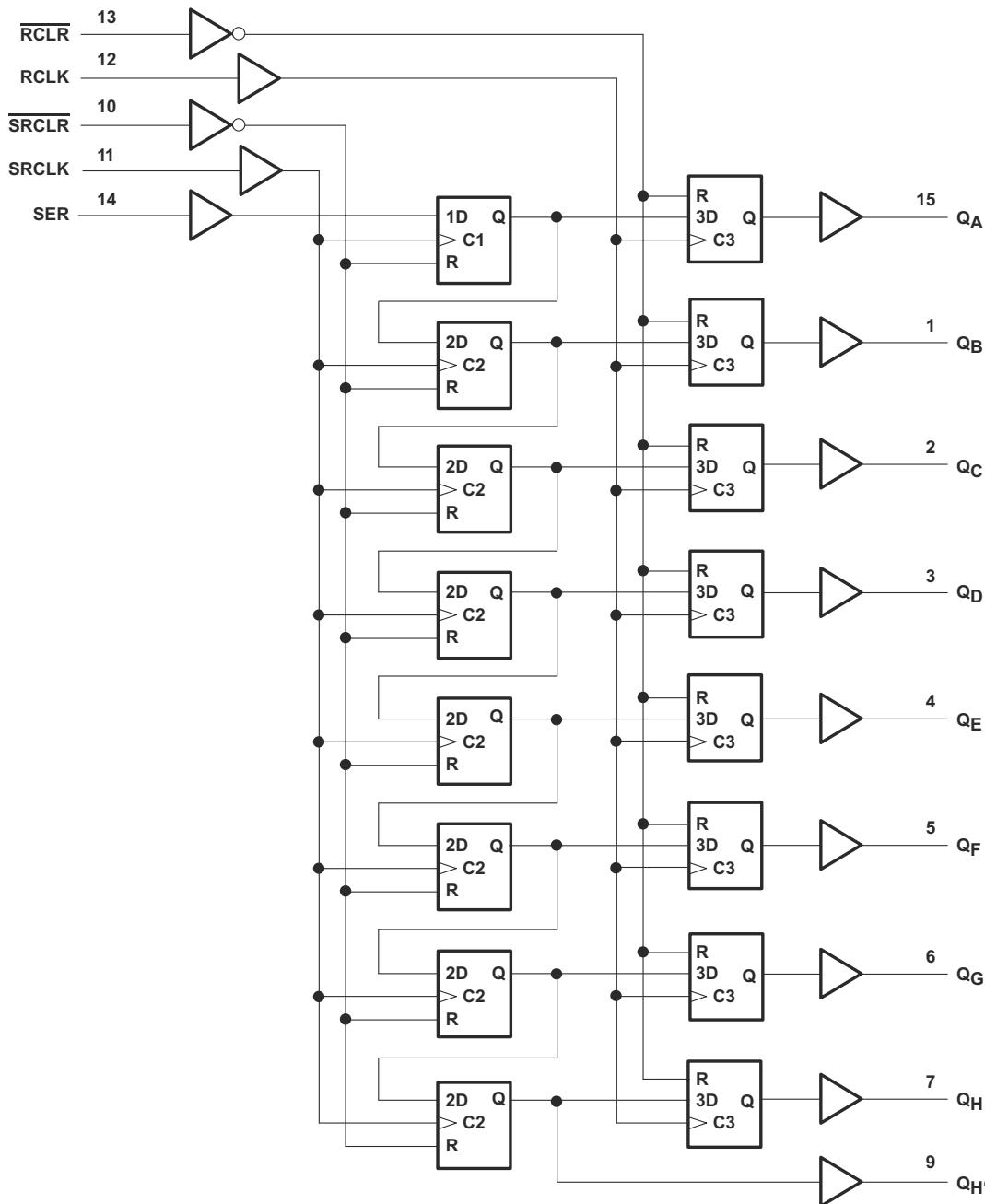
Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SNx4AHC594 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clear ($\overline{\text{SRCLR}}$, $\overline{\text{RCLR}}$) inputs are provided on the shift and storage registers. A serial (Q_H') output is provided for cascading purposes. The shift register (SRCLK) and storage register (RCLK) clocks are positive-edge triggered. If the clocks are tied together, the shift register always is one clock pulse ahead of the storage register.

7.2 Functional Block Diagram



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

7.3 Feature Description

- Allows for down translation
 - Inputs are tolerant up to 5.5 V
- Slow edges for reduced noise
- Low power

7.4 Device Functional Modes

Table 7-1. Function Table

INPUTS					FUNCTION
SER	SRCLK	SRCLR	RCLK	RCLR	
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of shift register goes high. Other stages store the data of previous stage, respectively.
L	↓	H	X	X	Shift register state is not changed.
X	X	X	X	L	Storage register is cleared.
X	X	X	↑	H	Shift register data is stored in the storage register.
X	X	X	↓	H	Storage register state is not changed.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74AHC594 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs accept voltages up to 5.5 V allowing down translation to the V_{CC} level. [Figure 8-2](#) shows how the slower edges can reduce ringing on the output compared to higher drive parts like AC.

8.2 Typical Application

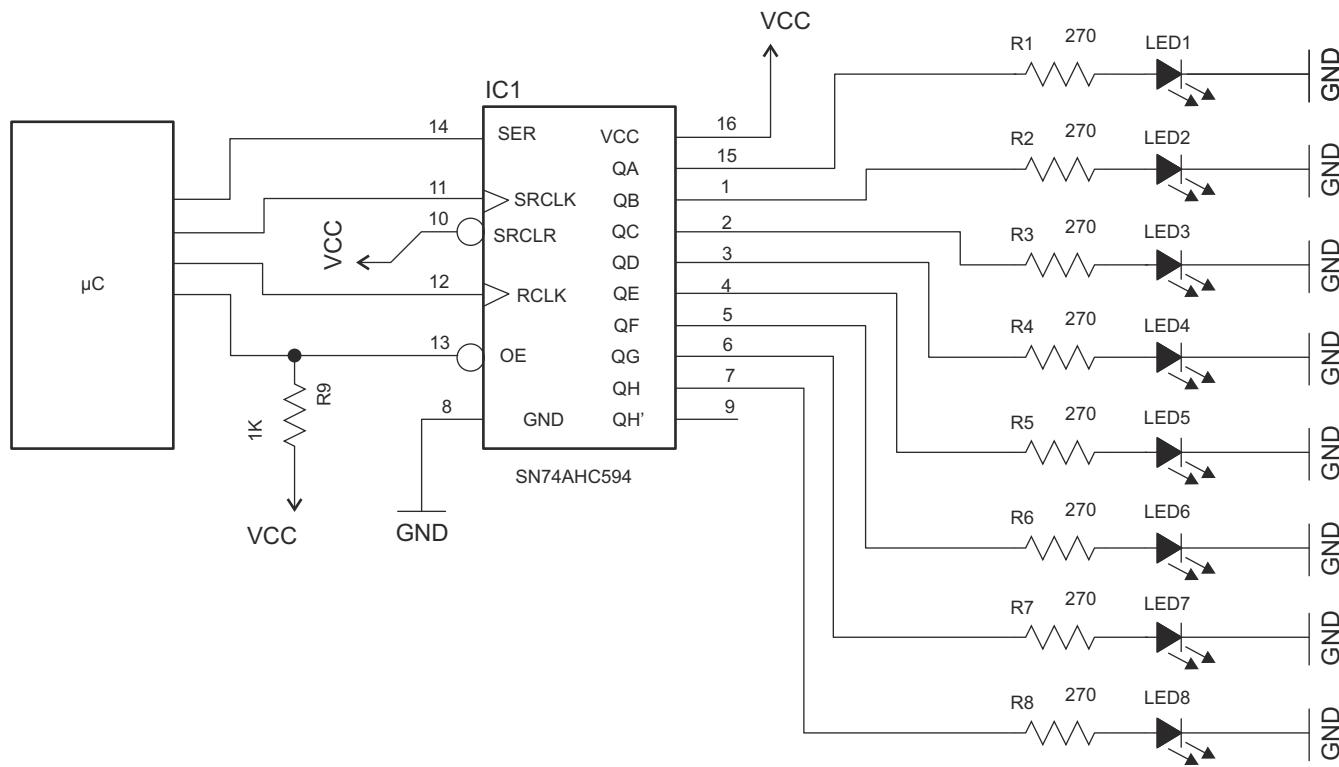


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive but the high drive will also create faster edges into light loads, so routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions

- Rise time and fall time specs: See ($\Delta t/\Delta V$) in the [Recommended Operating Conditions](#) table.
- Specified high and low levels: See (V_{IH} and V_{IL}) in the [Recommended Operating Conditions](#) table.

- Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .

2. Recommend Output Conditions

- Load currents should not exceed 25 mA per output and 75 mA total for the part.
- Outputs should not be pulled above V_{CC} .

8.2.3 Application Curves

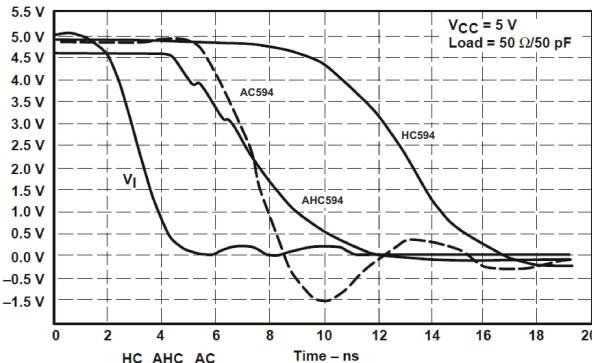


Figure 8-2. Switching Characteristics Comparison

8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ F is recommended; if there are multiple V_{CC} pins, then 0.01 μ F or 0.022 μ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μ F and a 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Figure 8-3](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the IOs, so they cannot float when disabled.

8.4.2 Layout Example

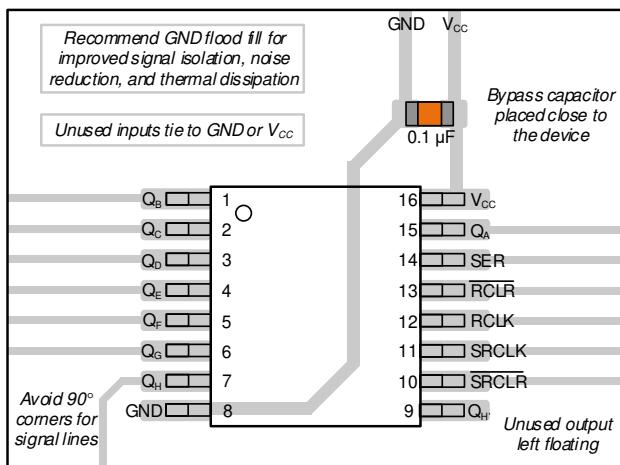


Figure 8-3. Example Layout for the SN74AHC594

9 Device and Documentation Support

9.1 Documentation Support (Analog)

9.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHC594	Click here				
SN74AHC594	Click here				

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (July 2014) to Revision H (April 2024)	Page
• Added package size to <i>Device Information</i> table, removed references to machine model, and updated layout structure to meet current data sheet standards	1
• Updated thermal values for PW package from R _{θJA} = 105.7 to 135.9, R _{θJC(top)} = 40.4 to 70.3, R _{θJB} = 50.7 to 81.3, Ψ _{JT} = 3.7 to 22.5 Ψ _{JB} = 50.1 to 80.8, all values in °C/W.....	5

Changes from Revision F (September 2003) to Revision G (July 2014)	Page
• Updated document to new TI data sheet standards.....	1
• Deleted Ordering Information table.....	1

• Added Applications.....	1
• Added Pin Functions table.	3
• Added Handling Ratings table.....	4
• Changed MAX operating temperature from 85°C to 125°C in Recommended Operating Conditions table.	4
• Added Typical Characteristics section.	9
• Added Detailed Description section.....	11
• Added Application and Implementation section.	13
• Added Power Supply Recommendations and Layout sections.....	14

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AHC594D	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-40 to 125	AHC594
SN74AHC594DBR	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA594
SN74AHC594DBR.A	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA594
SN74AHC594DR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC594
SN74AHC594DR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC594
SN74AHC594DRG4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC594
SN74AHC594N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC594N
SN74AHC594N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC594N
SN74AHC594NSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC594
SN74AHC594NSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC594
SN74AHC594PW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-40 to 125	HA594
SN74AHC594PWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	HA594
SN74AHC594PWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA594

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

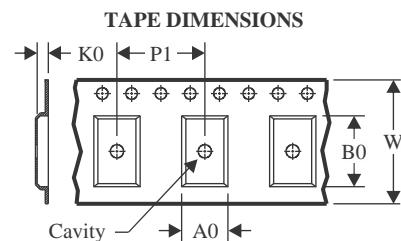
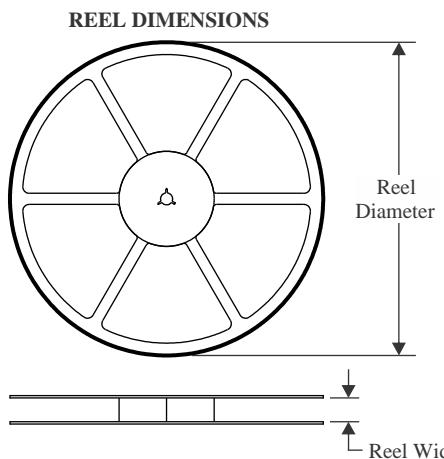
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AHC594 :

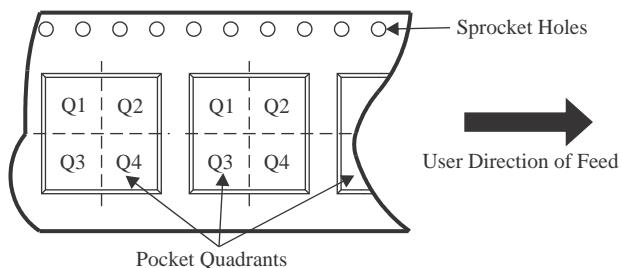
- Automotive : [SN74AHC594-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

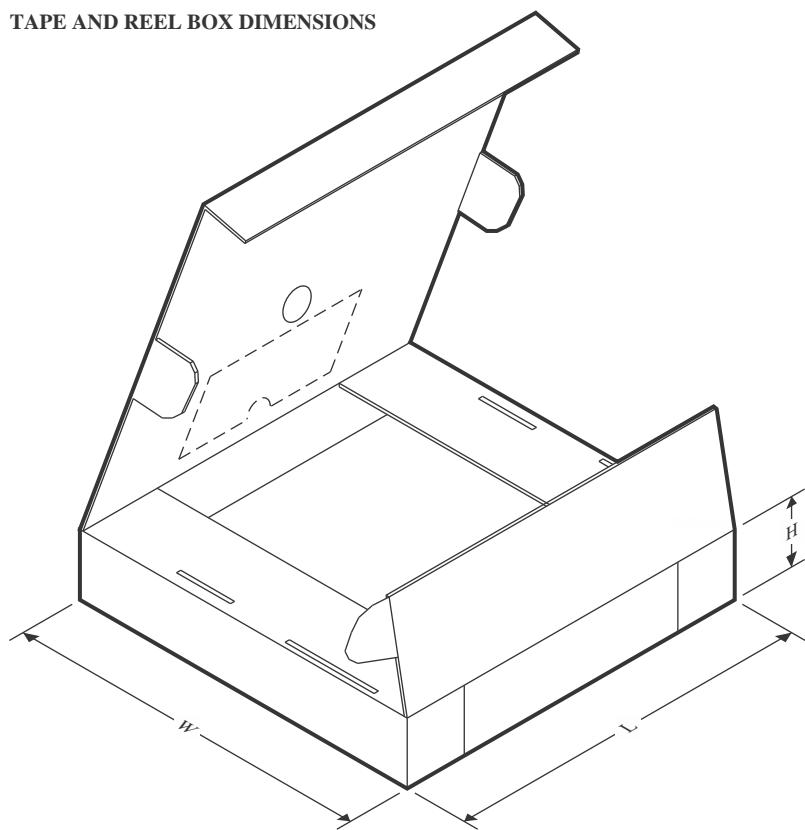
TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


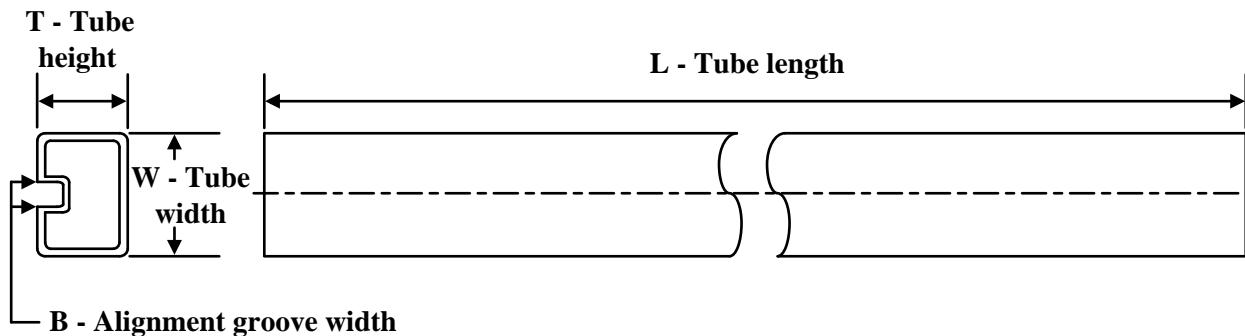
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC594DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC594DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHC594NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74AHC594PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC594PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC594DBR	SSOP	DB	16	2000	353.0	353.0	32.0
SN74AHC594DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74AHC594NSR	SOP	NS	16	2000	353.0	353.0	32.0
SN74AHC594PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74AHC594PWR	TSSOP	PW	16	2000	353.0	353.0	32.0

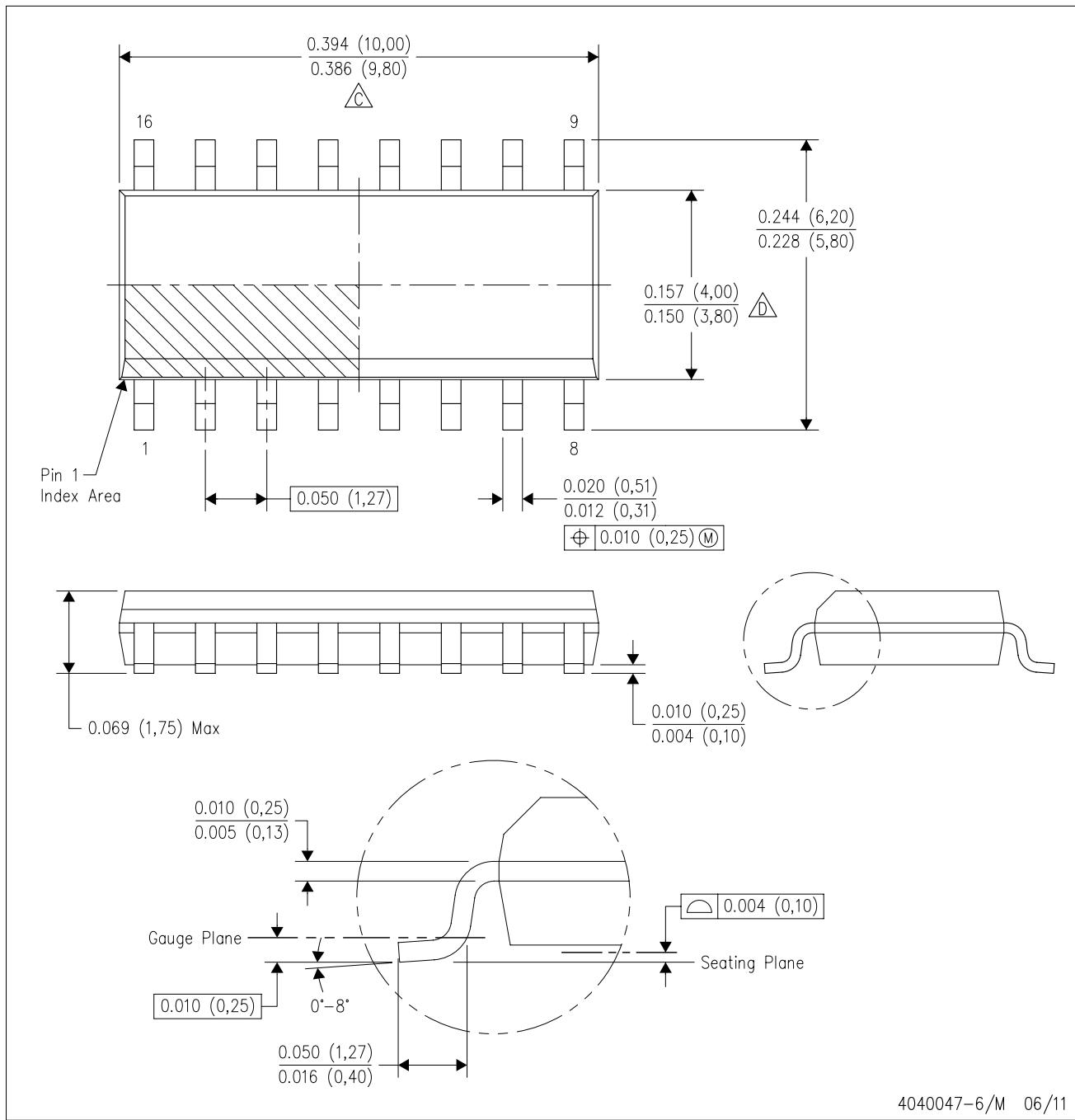
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
SN74AHC594N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHC594N	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHC594N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74AHC594N.A	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

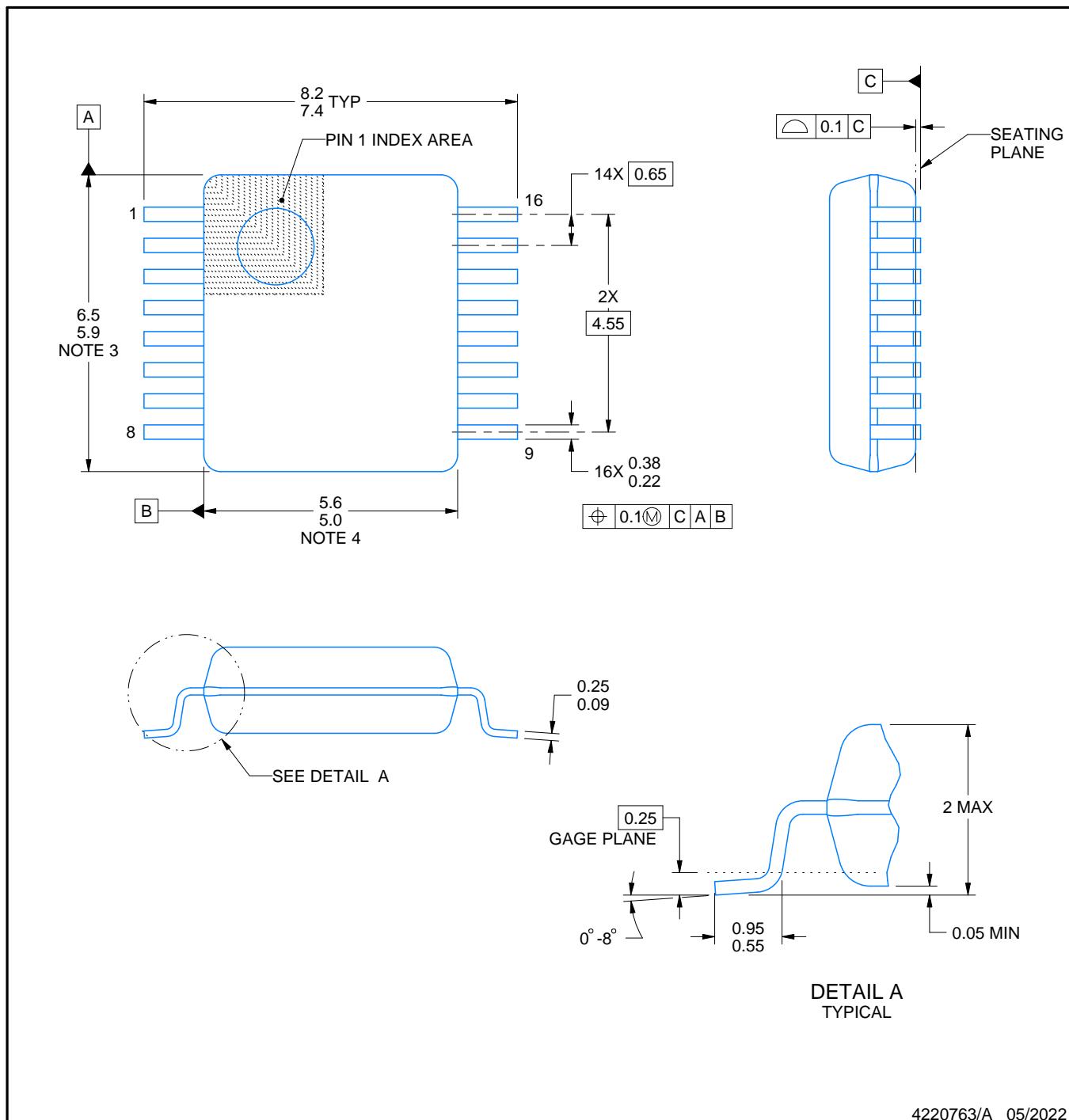
PACKAGE OUTLINE

DB0016A



SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

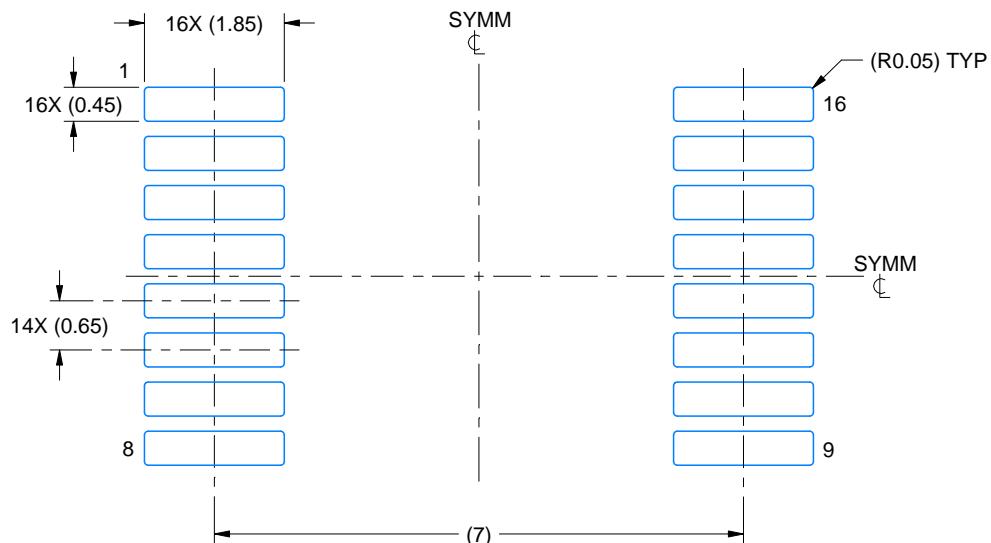
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

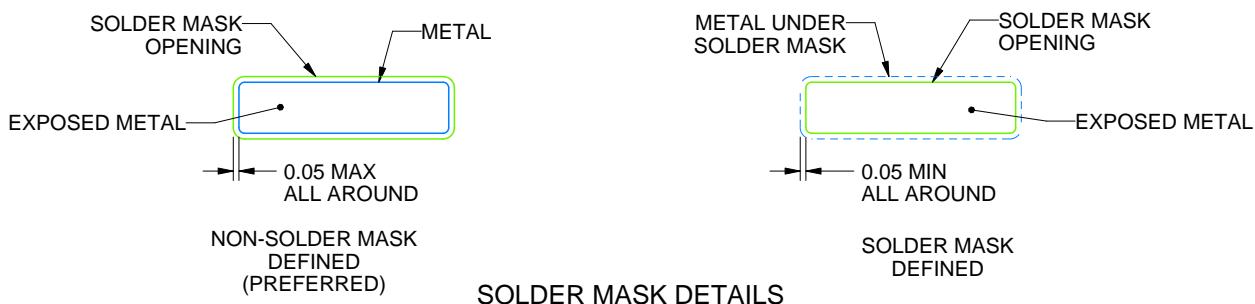
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

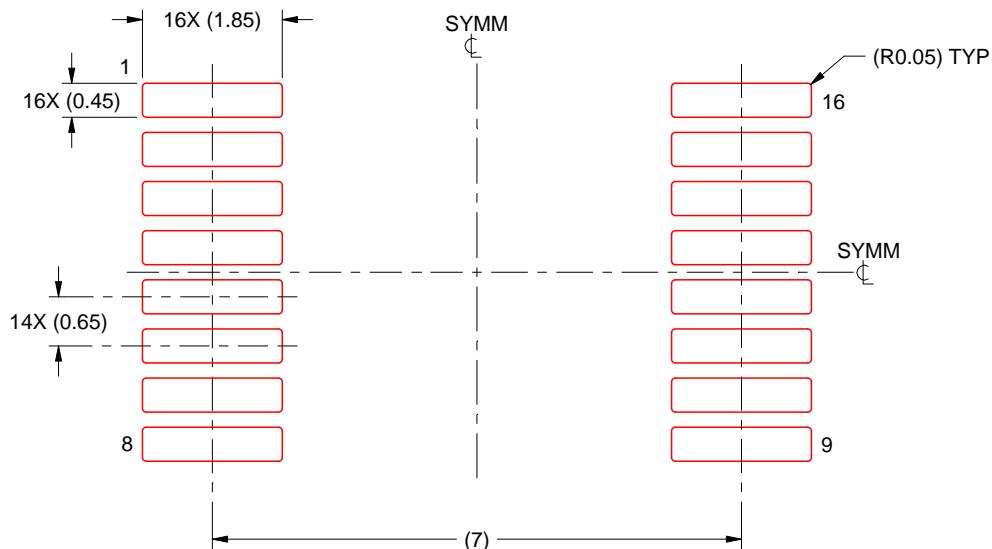
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

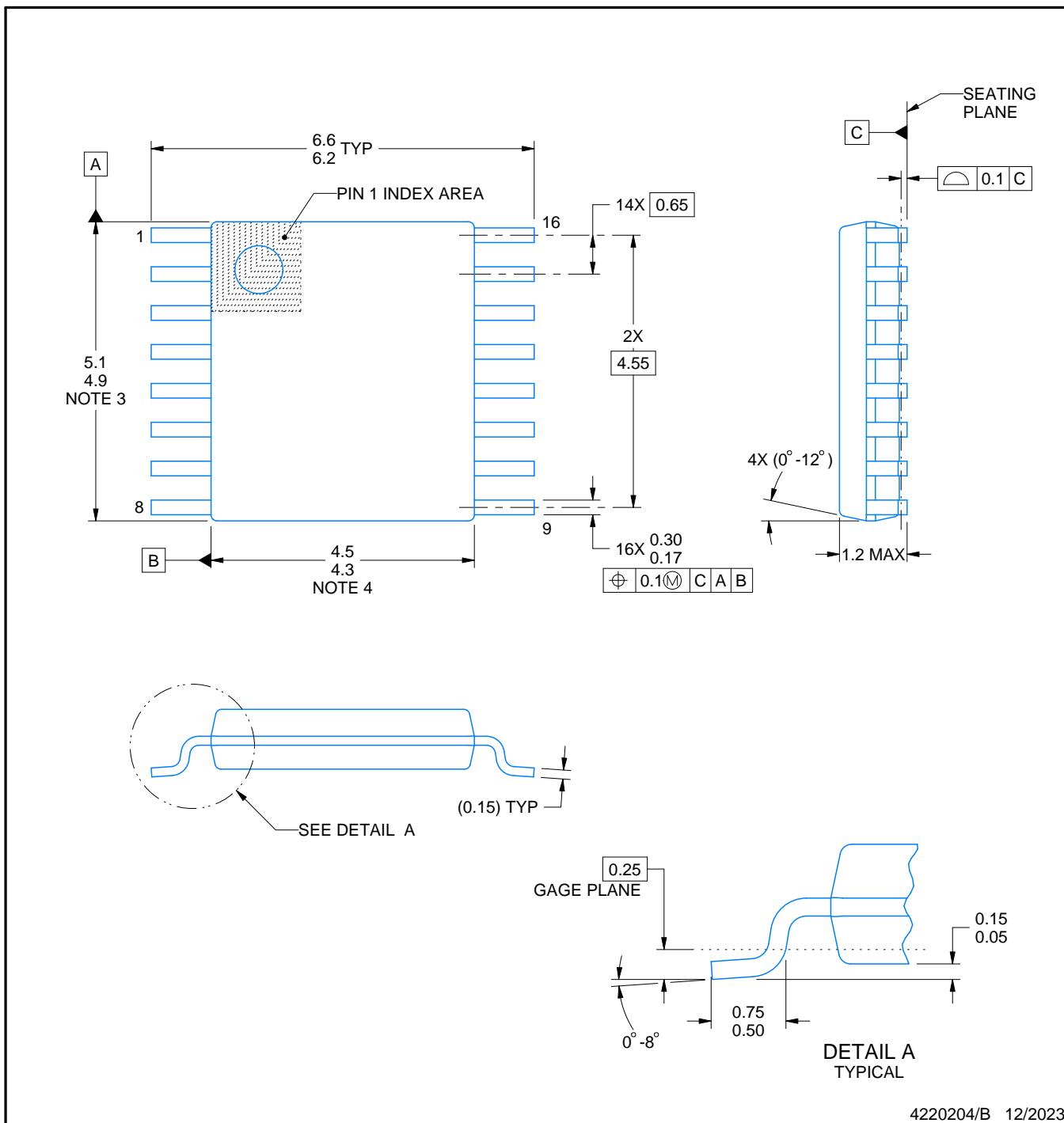
PACKAGE OUTLINE

PW0016A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

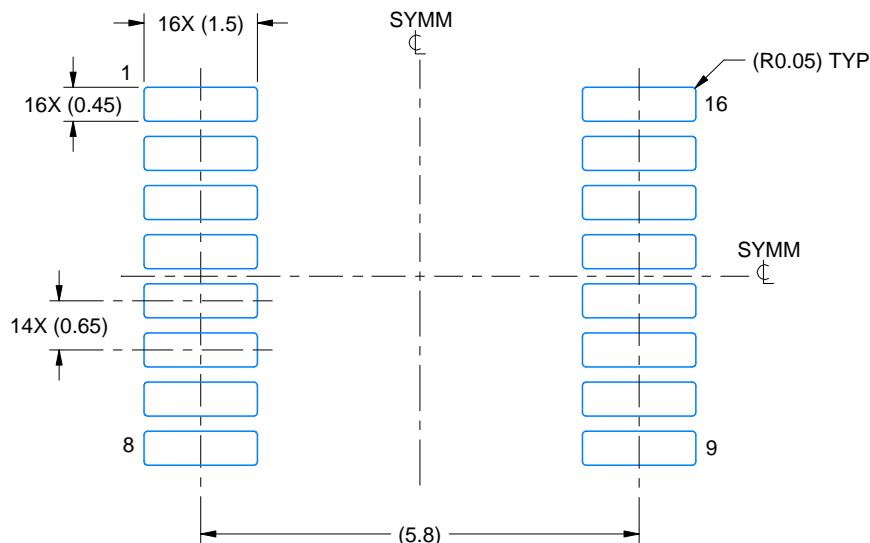
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

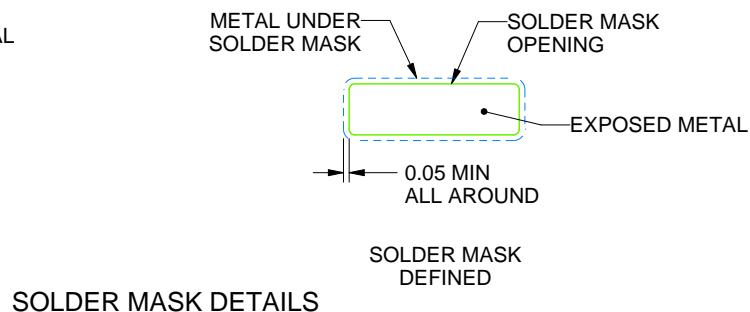
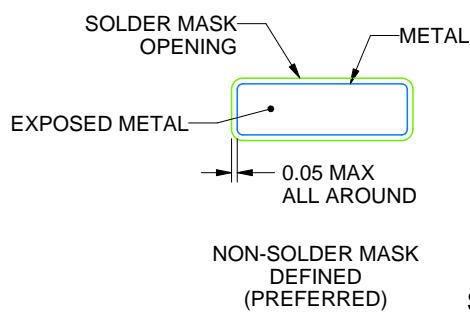
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

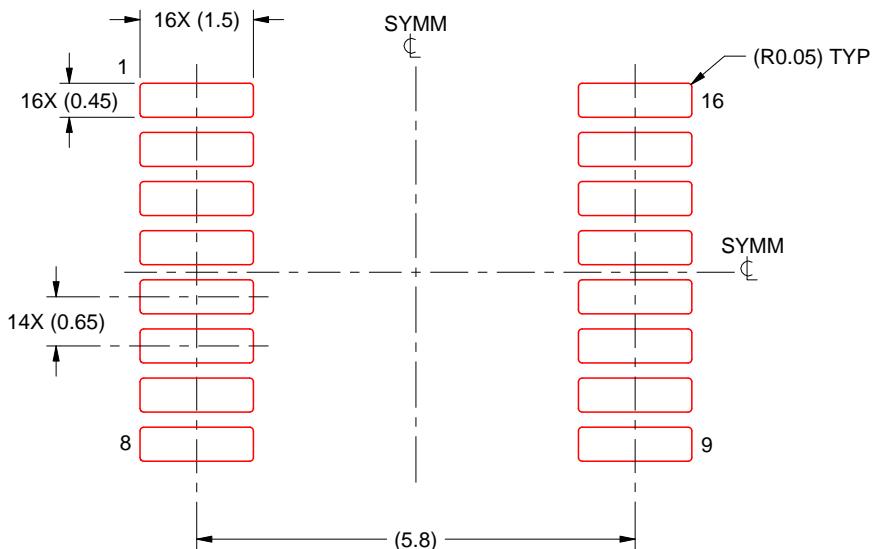
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

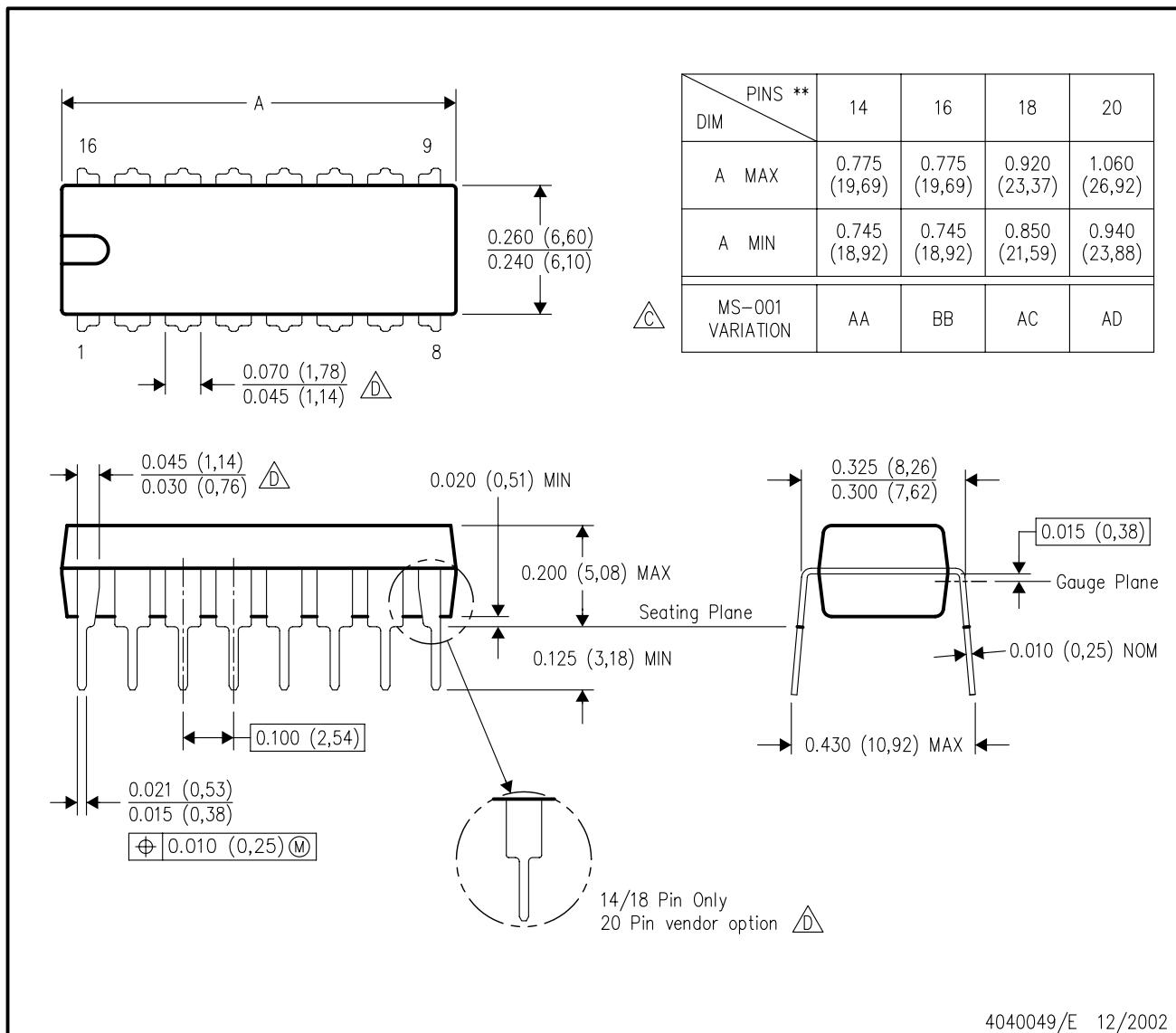
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

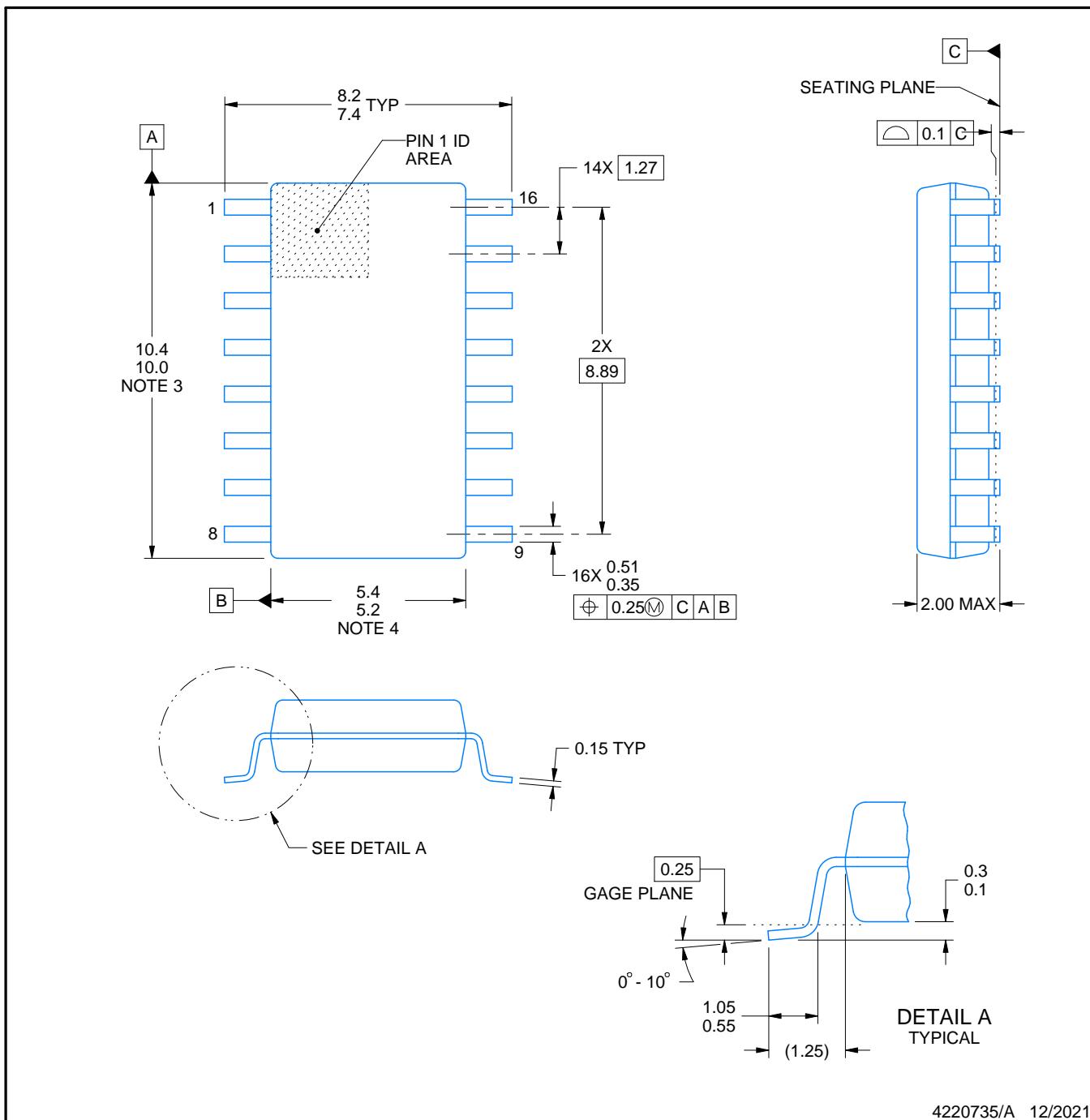
△ The 20 pin end lead shoulder width is a vendor option, either half or full width.



PACKAGE OUTLINE

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

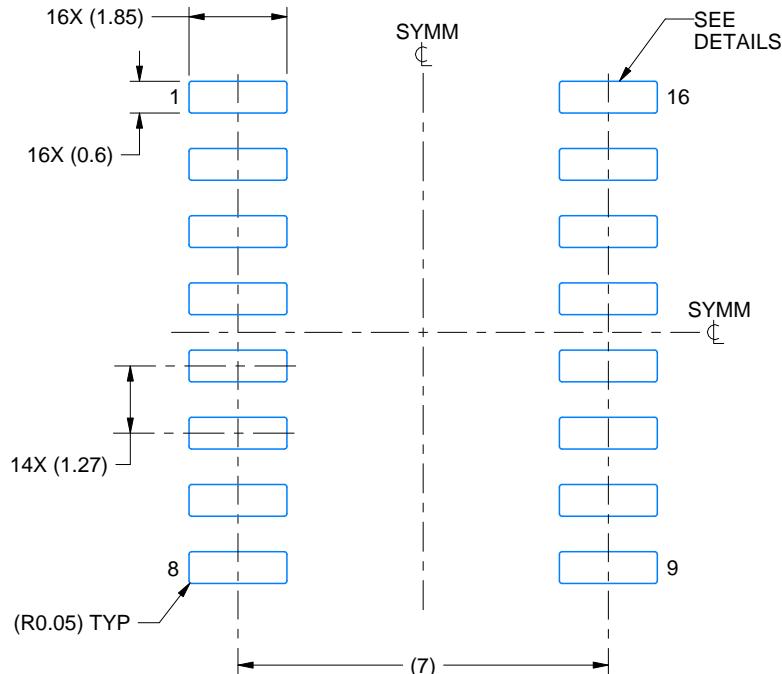
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

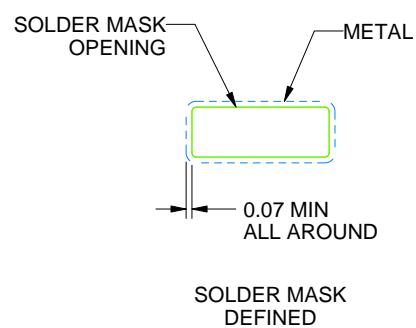
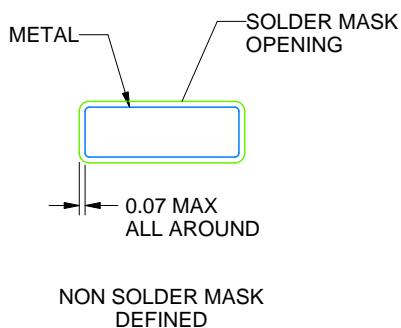
NS0016A

SOP - 2.00 mm max height

SOP



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

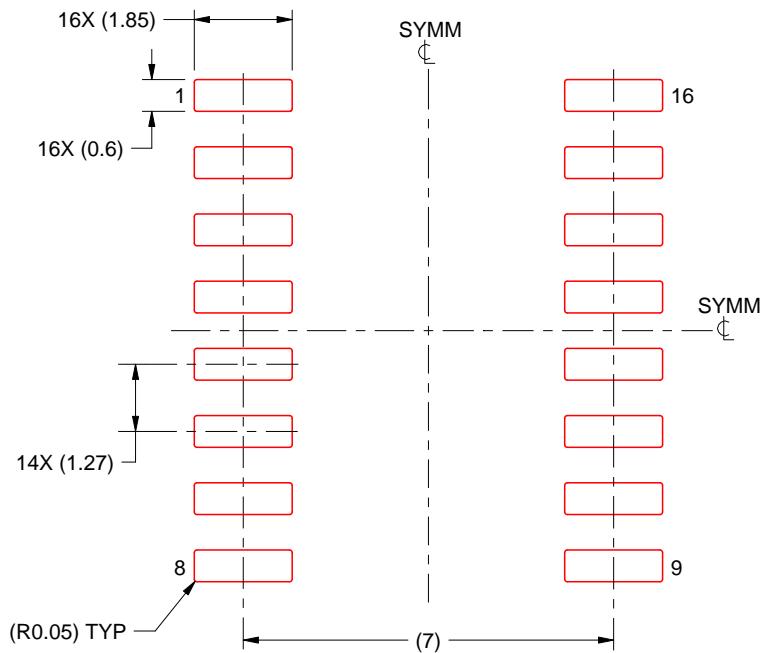
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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