

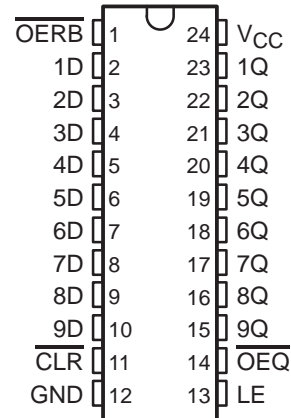
# SN74ALS992

## 9-BIT D-TYPE TRANSPARENT READ-BACK LATCH WITH 3-STATE OUTPUTS

SDAS028B – APRIL 1984 – REVISED JANUARY 1995

- 3-State I/O-Type Read-Back Inputs
- Bus-Structured Pinout
- True Logic Outputs
- Designed With Nine Bits for Parity Applications
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs

DW OR NT PACKAGE  
(TOP VIEW)



### description

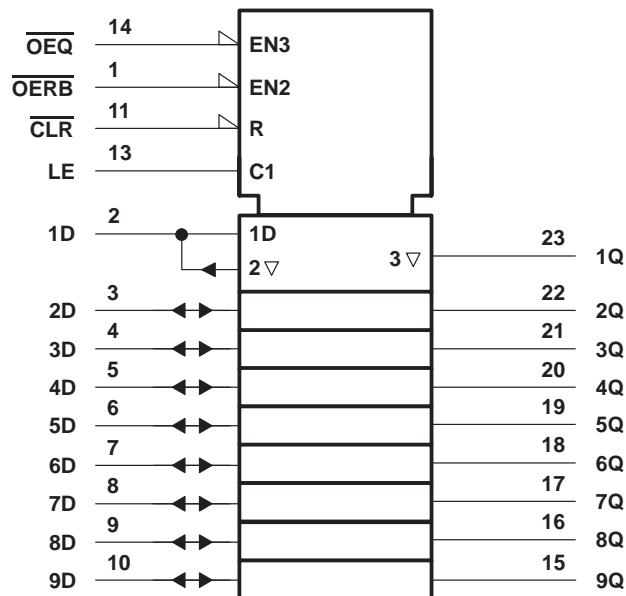
This 9-bit latch is designed specifically for storing the contents of the input data bus and providing the capability of reading back the stored data onto the input data bus. In addition, this device provides a 3-state buffer-type output and is easily implemented in parity applications.

The nine latches are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. The Q outputs are in the 3-state condition when the output-enable ( $\overline{\text{OEQ}}$ ) input is high.

Read back is provided through the output-enable ( $\overline{\text{OERB}}$ ) input. When  $\overline{\text{OERB}}$  is taken low, the data present at the output of the data latches is allowed to pass back onto the input data bus. When  $\overline{\text{OERB}}$  is taken high, the output of the data latches is isolated from the D inputs.  $\overline{\text{OERB}}$  does not affect the internal operation of the latches; however, precautions should be taken not to create a bus conflict.

The SN74ALS992 is characterized for operation from 0°C to 70°C.

### logic symbol†



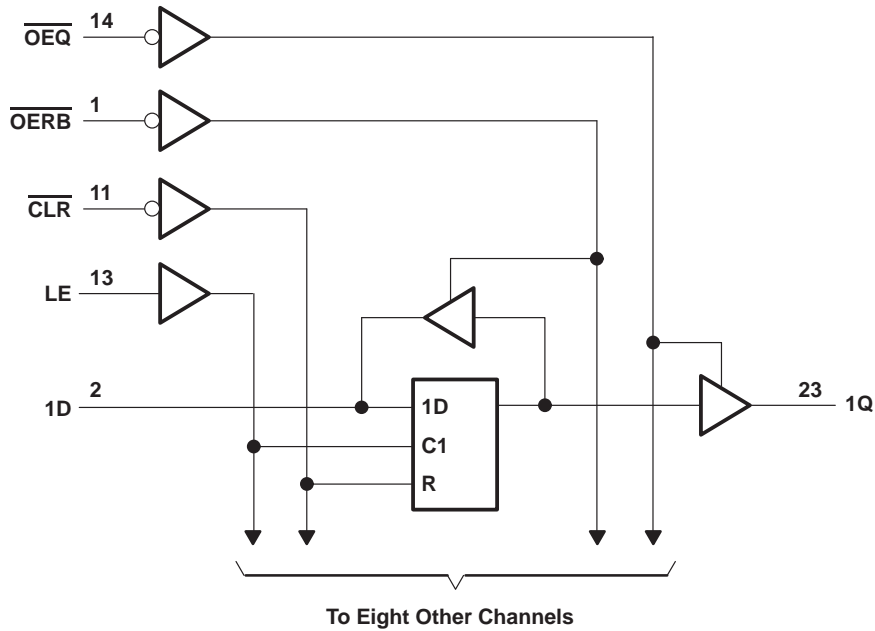
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# SN74ALS992

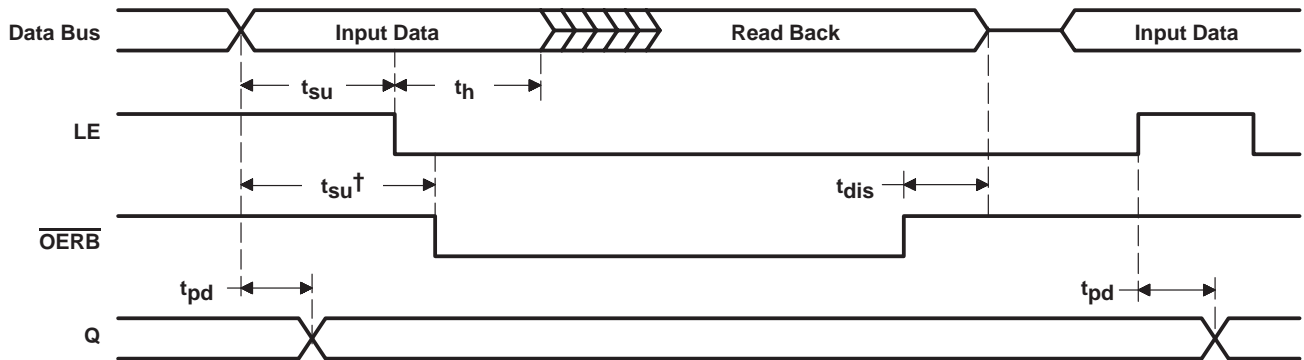
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### logic diagram (positive logic)



### timing diagram



$\overline{\text{CLR}} = \text{H}$ ,  $\overline{\text{OEQ}} = \text{L}$

$^\dagger$  This setup time ensures that the read-back circuit will not create a conflict on the input data bus.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted) $^\ddagger$

Supply voltage, $V_{CC}$ .....	7 V
Input voltage, $V_I$ ( $\overline{\text{OERB}}$ , $\overline{\text{OEQ}}$ , $\overline{\text{CLR}}$ , and LE) .....	7 V
Voltage applied to D inputs and to disabled 3-state outputs .....	5.5 V
Operating free-air temperature range, $T_A$ .....	0°C to 70°C
Storage temperature range .....	-65°C to 150°C

$^\ddagger$  Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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### recommended operating conditions

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{OH}$	High-level output current	Q		-2.6	mA
		D		-0.4	
$I_{OL}$	Low-level output current	Q		24	mA
		D		8	
$t_w$	Pulse duration	LE high	10		ns
		CLR low	10		
$t_{su}$	Setup time	Data before LE↓	10		ns
		Data before $\overline{OERB}$ ↓	10		
$t_h$	Hold time, data after LE↓	5			ns
$T_A$	Operating free-air temperature	0		70	°C

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2	V
$V_{OH}$	All outputs	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ ,	$I_{OH} = -0.4\text{ mA}$	$V_{CC} - 2$			V
	Q	$V_{CC} = 4.5\text{ V}$ ,	$I_{OH} = -2.6\text{ mA}$	2.4	3.2		
$V_{OL}$	D	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 4\text{ mA}$	0.25	0.4	V	
			$I_{OL} = 8\text{ mA}$	0.35	0.5		
	Q	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 12\text{ mA}$	0.25	0.4		
			$I_{OL} = 24\text{ mA}$	0.35	0.5		
$I_{OZH}$	Q	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.7\text{ V}$			20	μA
$I_{OZL}$	Q	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0.4\text{ V}$			-20	μA
$I_I$	D inputs	$V_{CC} = 5.5\text{ V}$	$V_I = 5.5\text{ V}$			0.1	mA
	All others		$V_I = 7\text{ V}$			0.1	
$I_{IH}$	D inputs‡	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$			20	μA
	All others					20	
$I_{IL}$	D inputs‡	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.4\text{ V}$			-0.1	mA
	All others					-0.1	
$I_{OS}§$		$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.25\text{ V}$	-30		-112	mA
$I_{CC}$		$V_{CC} = 5.5\text{ V}$ , OERB high	Outputs high		30	50	mA
			Outputs low		50	80	
			Outputs disabled		35	55	

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports ( $Q_A$  thru  $Q_H$ ), the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}$ .



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## 9-BIT D-TYPE TRANSPARENT READ-BACK LATCH WITH 3-STATE OUTPUTS

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### switching characteristics (see Figure 1)

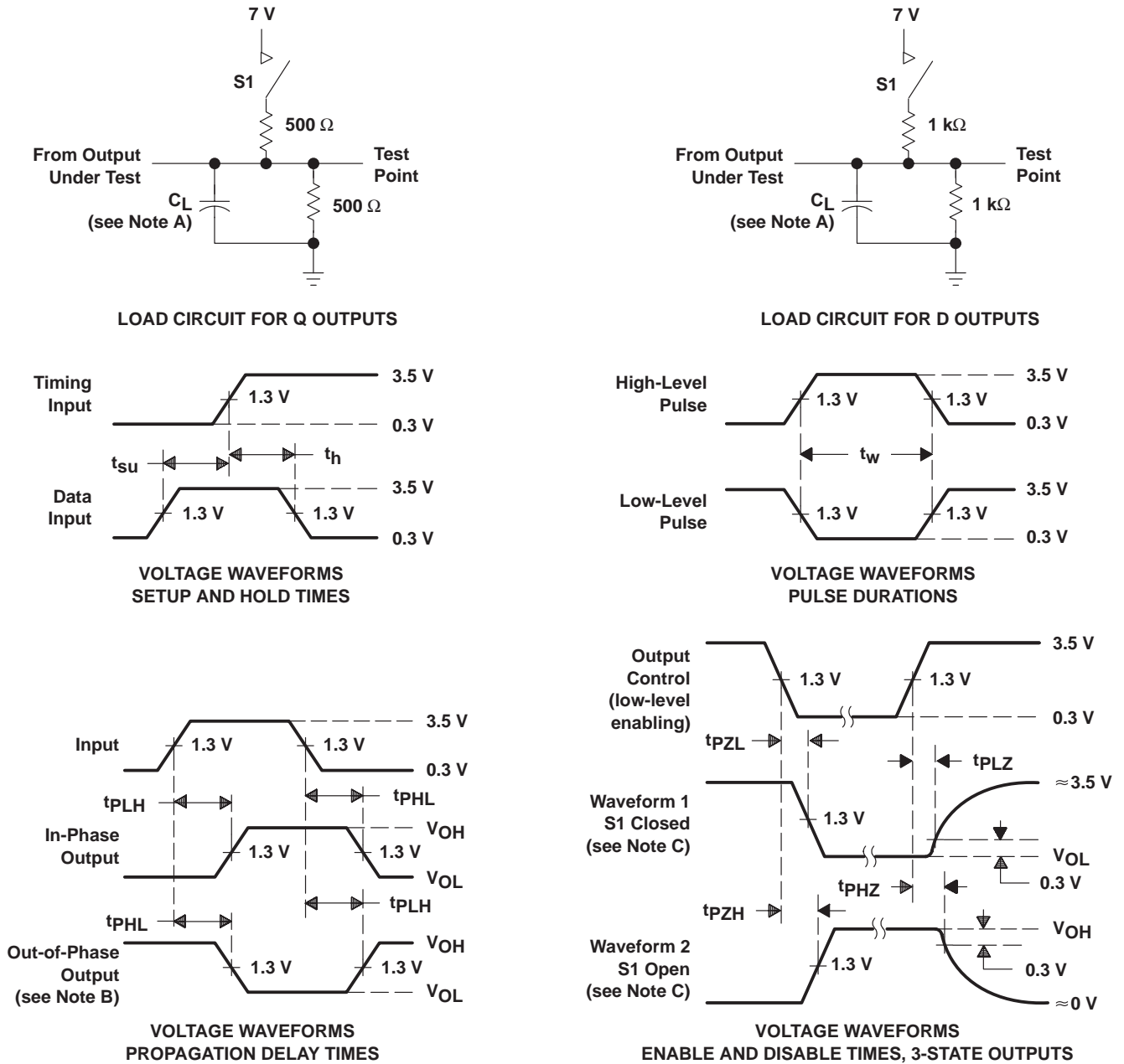
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, T <sub>A</sub> = MIN to MAX†		UNIT
			MIN	MAX	
t <sub>PLH</sub>	D	Q	3	14	ns
t <sub>PHL</sub>			4	16	
t <sub>PLH</sub>	LE	Q	6	20	ns
t <sub>PHL</sub>			8	25	
t <sub>PHL</sub>	$\overline{\text{CLR}}$	Q	6	20	ns
		D	8	26	
t <sub>en</sub> ‡	$\overline{\text{OERB}}$	D	4	21	ns
t <sub>dis</sub> §			2	14	
t <sub>en</sub> ‡	$\overline{\text{OEQ}}$	Q	4	18	ns
t <sub>dis</sub> §			1	14	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ t<sub>en</sub> = t<sub>PZH</sub> or t<sub>PZL</sub>

§ t<sub>dis</sub> = t<sub>PHZ</sub> or t<sub>PLZ</sub>

**PARAMETER MEASUREMENT INFORMATION**



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. When measuring propagation delay times of 3-state outputs, switch S1 is open.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.

**Figure 1. Load Circuits and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74ALS992DW</a>	Active	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS992
SN74ALS992DW.A	Active	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS992

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ALS992DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74ALS992DW.A	DW	SOIC	24	25	506.98	12.7	4826	6.6

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AD.



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