SN74AVC4T774 4-Bit Dual-Supply Bus Transceiver With Configurable Voltage-Level Shifting and 3-State Outputs With Independent Direction Control Inputs

1 Features

- Each channel has an independent DIR control input
- Control inputs V_{IH}/V_{IL} levels are referenced to V_{CCA} voltage
- Fully configurable dual-rail design allows each port to operate over the full 1.1V to 3.6V power-supply range
- I/Os are 4.6V tolerant
- I_{off} Supports partial power-down-mode operation
- Typical data rates
  - 380Mbps (1.8V to 3.3V translation)
  - 200Mbps (<1.8V to 3.3V translation)
  - 200Mbps (translate to 2.5V or 1.8V)
  - 150Mbps (translate to 1.5V)
  - 100Mbps (translate to 1.2V)
- Latch-up performance exceeds 100mA Per JESD 78, class II
- ESD Protection exceeds the following levels (tested per JESD 22)
  - ±8000V Human-body model (A114-A)
  - 250V Machine model (A115-A)
  - ±1500V Charged-device model (C101)

2 Applications

- Personal electronic
- Industrial
- Enterprise
- Telecom

3 Description

This 4-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.1V to 3.6V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.1 to 3.6V. The SN74AVC4T774 is optimized to operate with V_{CCA}/V_{CCB} set at 1.4V to 3.6V. It is operational with V_{CCA}/V_{CCB} as low as 1.2V. This allows for universal low-voltage bi-directional translation between any of the 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V voltage nodes.

The SN74AVC4T774 is designed for asynchronous communication between data buses. The logic levels of the direction-control (DIR) input and the output-enable ($\overline{OE}$) input activate either the B-port outputs or the A-port outputs or place both output ports in the high-impedance mode. The device transmits data from the A bus to the B bus when the B outputs are activated, and from the B bus to the A bus when the A outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ}.

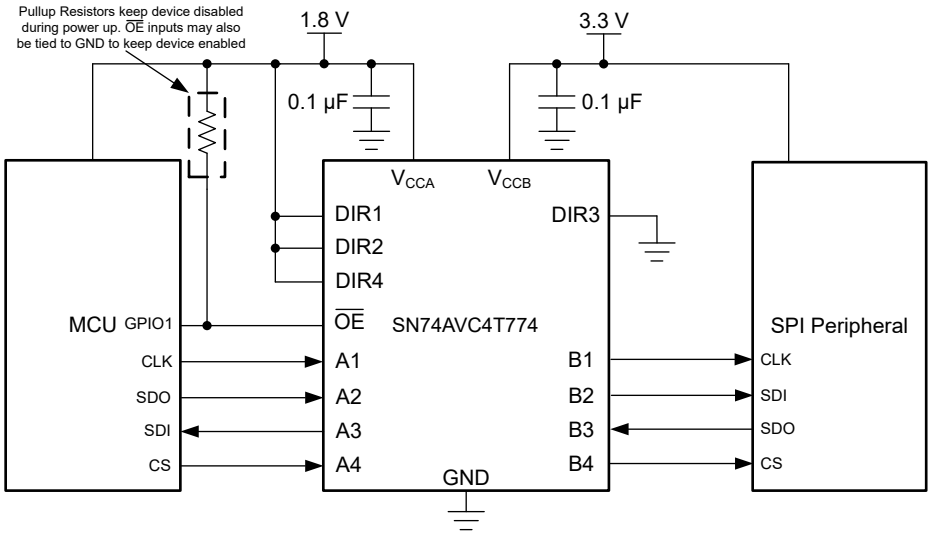
The SN74AVC4T774 is designed so that the control pins (DIR1, DIR2, DIR3, DIR4, and $\overline{OE}$) are supplied by V_{CCA}. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, then both ports are in the high-impedance state.

For a high-impedance state during power-up or power-down, $\overline{OE}$ should be tied to V_{CCA} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. Since this device has CMOS inputs, it is very important to not allow them to float. If the inputs are not driven to either a high V_{CC} state, or a low-GND state, an undesirable larger than expected I_{CC} current may result. Since the input voltage settlement is governed by many factors (for example, capacitance, board-layout, package inductance, surrounding conditions, and so forth), ensuring that they these inputs are kept out of erroneous switching states and tying them to either a high or a low level minimizes the leakage-current.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN74AVC4T774	PW (TSSOP, 16)	5mm × 6.4mm
	RGY (VQFN, 16)	4mm × 3.5mm
	RSV, (UQFN, 16)	2.6mm × 1.8mm
	BQB (WQFN, 16)	3.5mm × 2.5mm
	DYY (SOT, 16)	4.2mm × 2mm

(1) For more information, Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Schematic

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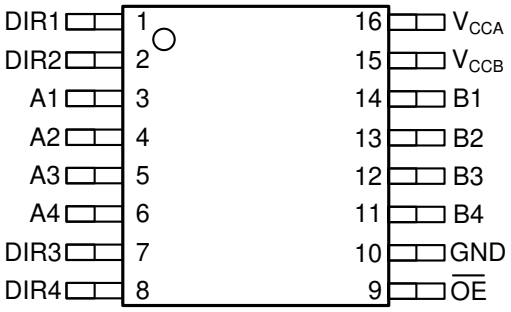
4 Pin Configuration and Functions



A. Shown for a single channel

Figure 4-1. PW Package, 16-Pin TSSOP (Top View)

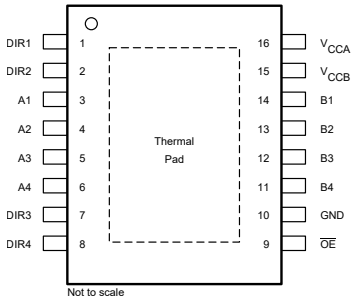


Figure 4-2. DYY Package, 16-Pin SOT (Top View)

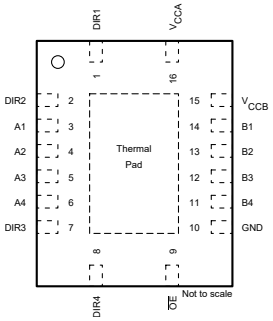


Figure 4-3. RGY Package, 16-Pin VQFN (Top View)

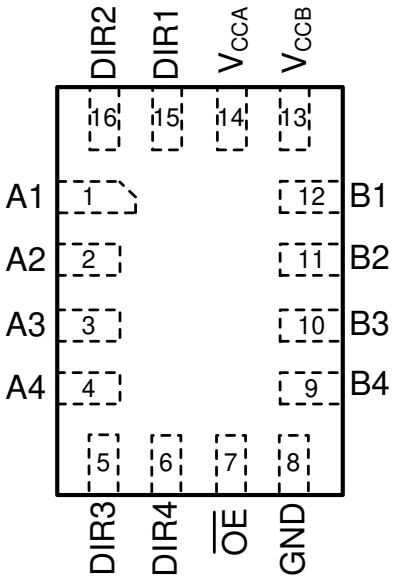


Figure 4-4. RSV Package, 16-Pin UQFN (Top View)

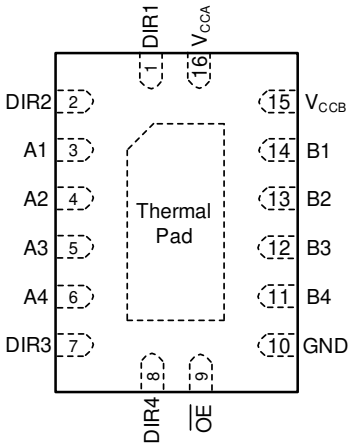


Figure 4-5. BQB Package, 16-Pin WQFN, Transparent (Top View)

Table 4-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	PW, RGY BQB, DYY	RSV		
DIR1	1	15	I	Direction-control input referenced to V_{CCA}, controls signal flow for the first (A1/B1) I/O channels.
DIR2	2	16	I	Direction-control input referenced to V_{CCA} , controls signal flow for the second (A2/B2) I/O channels.
A1	3	1	I/O	Input/output A1. Referenced to V_{CCA}.
A2	4	2	I/O	Input/output A2. Referenced to V_{CCA}.
A3	5	3	I/O	Input/output A3. Referenced to V_{CCA}.
A4	6	4	I/O	Input/output A4. Referenced to V_{CCA}.
DIR3	7	5	I	Direction-control input referenced to V_{CCA} , controls signal flow for the third (A3/B3) I/O channels.
DIR4	8	6	I	Direction-control input referenced to V_{CCA} , controls signal flow for the fourth (A4/B4) I/O channels.
$\overline{OE}$	9	7	I	3-state output-mode enables. Pull $\overline{OE}$ high to place all outputs in 3-state mode. Referenced to V_{CCA}.
GND	10	8	—	Ground.
B4	11	9	I/O	Input/output B4. Referenced to V_{CCB}.
B3	12	10	I/O	Input/output B3. Referenced to V_{CCB}.
B2	13	11	I/O	Input/output B2. Referenced to V_{CCB}.
B1	14	12	I/O	Input/output B1. Referenced to V_{CCB}.
V_{CCB}	15	13	—	B-port supply voltage. 1.1V ≤ V_{CCB} ≤ 3.6V.
V_{CCA}	16	14	—	A-port supply voltage. 1.1V ≤ V_{CCA} ≤ 3.6V.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
VCCA VCCB	Supply voltage		–0.5	4.6	V
VI	Input voltage range(2)	I/O ports (A port)	–0.5	4.6	V
		I/O ports (B port)	–0.5	4.6	
		Control inputs	–0.5	4.6	
VO	Voltage range applied to any output in the high-impedance or power-off state(2)	A port	–0.5	4.6	V
		B port	–0.5	4.6	
VO	Voltage range applied to any output in the high or low state(2) (3)	A port	–0.5	VCCA + 0.5	V
		B port	–0.5	VCCB + 0.5	
IIK	Input clamp current	VI< 0		–50	mA
IOK	Output clamp current	VO < 0		–50	mA
IO	Continuous output current			±50	mA
	Continuous current through VCCA, VCCB, or GND			±100	mA
TJ	Junction temperature			150	°C
Tstg	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6V maximum if the output current rating is observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±8000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	
		Machine model (A115-A)	250	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.1	3.6	V
V_{CCB}	Supply voltage				1.1	3.6	V
V_{IH}	High-level input voltage	Data inputs(4)	1.1V to 1.95V		V_{CCI} × 0.65		V
			1.95V to 2.7V		1.6		
			2.7V to 3.6V		2		
V_{IL}	Low-level input voltage	Data inputs(4)	1.1V to 1.95V			V_{CCI} × 0.35	V
			1.95V to 2.7V			0.7	
			2.7V to 3.6V			0.8	
V_{IH}	High-level input voltage	Control Inputs (referenced to V_{CCA}) (5) (DIRx, $\overline{OE}$)	1.1V to 1.95V		V_{CCA} × 0.65		V
			1.95V to 2.7V		1.6		
			2.7V to 3.6V		2		

5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{IL}	Low-level input voltage	Control Inputs (referenced to V_{CCA}) (5) (DIRx, $\overline{OE}$)	1.1V to 1.95V			V_{CCA} × 0.35	V
			1.95V to 2.7V			0.7	
			2.7V to 3.6V			0.8	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.1V to 1.3V		–3	mA
				1.4V to 1.6V		–6	
				1.65V to 1.95V		–8	
				2.3V to 2.7V		–9	
				3V to 3.6V		–12	
I_{OL}	Low-level output current			1.1V to 1.3V		3	mA
				1.4V to 1.6V		6	
				1.65V to 1.95V		8	
				2.3V to 2.7V		9	
				3V to 3.6V		12	
Δt/Δv	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				–40	85	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the Implications of Slow or Floating CMOS Inputs application report.
(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7V, V_{IL} max = V_{CCI} × 0.3V
(5) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7V, V_{IL} max = V_{CCA} × 0.3V

5.4 Thermal Information

THERMAL METRIC(1)		SN74AVC4T774					UNIT
		RGY (VQFN)	RSV (UQFN)	DYY (SOT)	BQB (WQFN)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.8	139.2	163.4	79.1	102.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.6	64.9	90.0	77.5	35.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45	67.7	93.1	49.0	57.5	°C/W
Y_{JT}	Junction-to-top characterization parameter	11.9	1.7	10.9	7.3	1.6	°C/W
Y_{JB}	Junction-to-board characterization parameter	44.7	67.4	92.1	48.9	56.9	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	28.2	N/A	N/A	26.4	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)(1) (2) (3)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	TA = 25°C			–40°C to 85°C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}		I_{OH} = –100µA	$V_I = V_{IH}$	1.1V to 3.6V	1.1V to 3.6V				V_{CCO} – 0.2			V
		I_{OH} = –3mA		1.2V	1.2V		0.95					
		I_{OH} = –6mA		1.4V	1.4V				1.05			
		I_{OH} = –8mA		1.65V	1.65V				1.2			
		I_{OH} = –9mA		2.3V	2.3V				1.75			
		I_{OH} = –12mA		3V	3V				2.3			
V_{OL}		I_{OL} = 100µA	$V_I = V_{IL}$	1.1V to 3.6V	1.1V to 3.6V						0.2	V
		I_{OL} = 3mA		1.2V	1.2V		0.25					
		I_{OL} = 6mA		1.4V	1.4V						0.35	
		I_{OL} = 8mA		1.65V	1.65V						0.45	
		I_{OL} = 9mA		2.3V	2.3V						0.55	
		I_{OL} = 12mA		3V	3V						0.7	
I_I	Control inputs	$V_I = V_{CCA}$ or GND		1.1V to 3.6V	1.1V to 3.6V		±0.025	±0.25			±1	µA
I_{off}	A or B port	V_I or V_O = 0 to 3.6V		0V	0V to 3.6V		±0.1	±1			±5	µA
				0V to 3.6V	0V		±0.1	±1			±5	
I_{OZ}	A or B port	$V_O = V_{CCO}$ or GND, VI = V_{CCI} or GND, $\overline{OE}$ = V_{IH}		3.6V	3.6V		±0.5	±2.5			±5	µA
I_{CCA}		$V_I = V_{CCI}$ or GND, I_O = 0		1.1V to 3.6V	1.1V to 3.6V						8	µA
				0V	0V to 3.6V				–2			
				0V to 3.6V	0V						8	
I_{CCB}		$V_I = V_{CCI}$ or GND, I_O = 0		1.1V to 3.6V	1.1V to 3.6V						8	µA
				0V	0V to 3.6V						8	
				0V to 3.6V	0V				–2			
I_{CCA} + I_{CCB}		$V_I = V_{CCI}$ or GND, I_O = 0		1.1V to 3.6V	1.1V to 3.6V						16	µA
C_i	Control inputs	V_I = 3.3V or GND		3.3V	3.3V		2.5				4.5	pF
C_{io}	A or B port	V_O = 3.3V or GND		3.3V	3.3V		5				7	pF

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the Implications of Slow or Floating CMOS Inputs application report.

5.6 Switching Characteristics: VCCA = 1.2V ± 0.1V

See Figure 8-1 and Table 8-1 for test circuit and loading. See Figure 8-2, Figure 8-3, and Figure 8-4 for measurement waveforms.

PARAMETER	PARAMETER	FROM	TO	Test Conditions	V_{CCB} = 1.2V ± 0.1V		V_{CCB} = 1.5V ± 0.1V		V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	t_{PLH}	A	B	-40°C to 85°C	2	7.5	1.5	5.5	1	4.5	1	4	0.5	4	ns
t_{PHL}	t_{PHL}				1.5	5.5	1	4	1	4	0.5	4.5	0.5	6	
t_{PLH}	t_{PLH}	B	A		2	7	1.5	6.5	1	6	1	6	1	6	
t_{PHL}	t_{PHL}				1.5	5.5	1	5	1	4.5	0.5	4	0.5	4	
t_{PZH}	t_{PZH}	$\overline{OE}$	A		2.5	8	2	8	1	8	1	8	1	8.5	
t_{PZL}	t_{PZL}				2.5	9	2	9	1.5	9	1	9	1	9	
t_{PZH}	t_{PZH}	$\overline{OE}$	B		2	7.5	1.5	5.5	1	6.5	1	9.5	0.5	30	
t_{PZL}	t_{PZL}				2.5	8.5	1.5	6.5	1	7	1	8.5	0.5	24	
t_{PHZ}	t_{PHZ}	$\overline{OE}$	A		3	6.5	2	6.5	2	6.5	1.5	6.5	2	6.5	
t_{PLZ}	t_{PLZ}				3	6.5	2.5	6.5	2.5	6.5	2	6.5	2	6.5	
t_{PHZ}	t_{PHZ}	$\overline{OE}$	B		3	6	2.5	5.5	2	6	1.5	5	2	6.5	
t_{PLZ}	t_{PLZ}				3	6	2.5	5.5	2.5	5.5	1.5	5	2	6	

5.7 Switching Characteristics: VCCA = 1.5V ± 0.1V

See Figure 8-1 and Table 8-1 for test circuit and loading. See Figure 8-2, Figure 8-3, and Figure 8-4 for measurement waveforms.

PARAMETER	PARAMETER	FROM	TO	V_{CCB} = 1.2V ± 0.1V		V_{CCB} = 1.5V ± 0.1V		V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	t_{PLH}	A	B	1.5	6.5	0.3	6.3	0.3	5.2	0.4	4.2	0.4	4.2	ns
t_{PHL}	t_{PHL}			1.5	4.5	0.3	6.3	0.3	5.2	0.4	4.2	0.4	4.2	
t_{PLH}	t_{PLH}	B	A	1.5	5	0.7	6.3	0.5	6	0.4	5.7	0.3	5.6	ns
t_{PHL}	t_{PHL}			1.5	4	0.7	6.3	0.5	6	0.4	5.7	0.3	5.6	
t_{PZH}	t_{PZH}	$\overline{OE}$	A	1.5	5	1.4	9.6	1.1	9.5	0.7	9.4	0.4	9.4	ns
t_{PZL}	t_{PZL}			2	5.5	1.4	9.6	1.1	9.5	0.7	9.4	0.4	9.4	
t_{PZH}	t_{PZH}	$\overline{OE}$	B	2	6.5	1.4	9.6	1.1	7.7	0.9	5.8	0.9	5.6	ns
t_{PZL}	t_{PZL}			2	7.5	1.4	9.6	1.1	7.7	0.9	5.8	0.9	5.6	
t_{PHZ}	t_{PHZ}	$\overline{OE}$	A	2	5	1.8	10.2	1.5	10.2	1.3	10.2	1.6	10.2	ns
t_{PLZ}	t_{PLZ}			2.5	4.5	1.8	10.2	1.5	10.2	1.3	10.2	1.6	10.2	
t_{PHZ}	t_{PHZ}	$\overline{OE}$	B	3	5.5	1.9	10.3	1.9	9.1	1.4	7.4	1.2	7.6	ns
t_{PLZ}	t_{PLZ}			3	5.5	1.9	10.3	1.9	9.1	1.4	7.4	1.2	7.6	

5.8 Switching Characteristics: VCCA = 1.8V ± 0.15V

See Figure 8-1 and Table 8-1 for test circuit and loading. See Figure 8-2, Figure 8-3, and Figure 8-4 for measurement waveforms.

PARAMETER	PARAMETER	FROM	TO	Test Conditions	V_{CCB} = 1.2V ± 0.1V		V_{CCB} = 1.5V ± 0.1V		V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	t_{PLH}	A	B	-40°C to 85°C	1.5	6.5	0.3	6.3	0.3	5.2	0.4	4.2	0.4	4.2	ns
t_{PHL}	t_{PHL}				1	4.5	0.3	6.3	0.3	5.2	0.4	4.2	0.4	4.2	
t_{PLH}	t_{PLH}	B	A		1.5	6	0.7	6.3	0.5	6	0.4	5.7	0.3	5.6	
t_{PHL}	t_{PHL}				1	4.5	0.7	6.3	0.5	6	0.4	5.7	0.3	5.6	
t_{PZH}	t_{PZH}	$\overline{OE}$	A		1	6.5	1.4	9.6	1.1	9.5	0.7	9.4	0.4	9.4	
t_{PZL}	t_{PZL}				1.5	7.5	1.4	9.6	1.1	9.5	0.7	9.4	0.4	9.4	
t_{PZH}	t_{PZH}	$\overline{OE}$	B		2	6	1.4	9.6	1.1	7.7	0.9	5.8	0.9	5.6	
t_{PZL}	t_{PZL}				2	7	1.4	9.6	1.1	7.7	0.9	5.8	0.9	5.6	
t_{PHZ}	t_{PHZ}	$\overline{OE}$	A		2	6	1.8	10.2	1.5	10.2	1.3	10.2	1.6	10.2	
t_{PLZ}	t_{PLZ}				2.5	5.5	1.8	10.2	1.5	10.2	1.3	10.2	1.6	10.2	
t_{PHZ}	t_{PHZ}	$\overline{OE}$	B		2.5	5	1.9	10.3	1.9	9.1	1.4	7.4	1.2	7.6	
t_{PLZ}	t_{PLZ}				2.5	5	1.9	10.3	1.9	9.1	1.4	7.4	1.2	7.6	

5.9 Switching Characteristics: VCCA = 2.5V ± 0.2V

See Figure 8-1 and Table 8-1 for test circuit and loading. See Figure 8-2, Figure 8-3, and Figure 8-4 for measurement waveforms.

PARAMETER	PARAMETER	FROM	TO	V_{CCB} = 1.2V ± 0.1V		V_{CCB} = 1.5V ± 0.1V		V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	t_{PLH}	A	B	1.5	6.5	0.1	5.7	0.1	4.6	0.2	3.5	0.1	3.6	ns
t_{PHL}	t_{PHL}			1	4.5	0.1	5.7	0.1	4.6	0.2	3.5	0.1	3.6	
t_{PLH}	t_{PLH}	B	A	1.5	4	0.6	4.2	0.4	3.9	0.2	3.4	0.2	3.3	ns
t_{PHL}	t_{PHL}			1	5	0.6	4.2	0.4	3.9	0.2	3.4	0.2	3.3	
t_{PZH}	t_{PZH}	$\overline{OE}$	A	1	2.5	0.7	6.5	0.7	5.2	0.6	4.8	0.4	4.8	ns
t_{PZL}	t_{PZL}			1	3	0.7	6.5	0.7	5.2	0.6	4.8	0.4	4.8	
t_{PZH}	t_{PZH}	$\overline{OE}$	B	1.5	6	0.9	8.8	0.8	7	0.6	4.8	0.6	4	ns
t_{PZL}	t_{PZL}			2	7	0.9	8.8	0.8	7	0.6	4.8	0.6	4	
t_{PHZ}	t_{PHZ}	$\overline{OE}$	A	1.5	3.5	1	8.4	1	8.4	1	6.2	1	6.6	ns
t_{PLZ}	t_{PLZ}			2	3.5	1	8.4	1	8.4	1	6.2	1	6.6	
t_{PHZ}	t_{PHZ}	$\overline{OE}$	B	2	5	1.5	9.4	1.3	8.2	1.1	6.2	0.9	5.2	ns
t_{PLZ}	t_{PLZ}			2.5	5	1.5	9.4	1.3	8.2	1.1	6.2	0.9	5.2	

5.10 Switching Characteristics: VCCA = 3.3V ± 0.3V

See Figure 8-1 and Table 8-1 for test circuit and loading. See Figure 8-2, Figure 8-3, and Figure 8-4 for measurement waveforms.

PARAMETER	PARAMETER	FROM	TO	V_{CCB} = 1.2V ± 0.1V		V_{CCB} = 1.5V ± 0.1V		V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	t_{PLH}	A	B	1.5	6	0.1	5.6	0.1	4.5	0.1	3.3	0.1	2.9	ns
t_{PHL}	t_{PHL}			1	4	0.1	5.6	0.1	4.5	0.1	3.3	0.1	2.9	
t_{PLH}	t_{PLH}	B	A	1.5	4	0.6	4.2	0.4	3.4	0.2	3	0.1	2.8	ns
t_{PHL}	t_{PHL}			1.5	7.5	0.6	4.2	0.4	3.4	0.2	3	0.1	2.8	
t_{PZH}	t_{PZH}	$\overline{OE}$	A	1	2.5	0.6	8.7	0.6	5.2	0.6	3.8	0.4	3.8	ns
t_{PZL}	t_{PZL}			1	2.5	0.6	8.7	0.6	5.2	0.6	3.8	0.4	3.8	
t_{PZH}	t_{PZH}	$\overline{OE}$	B	1.5	6	0.8	8.7	0.6	6.8	0.5	4.7	0.5	3.8	ns
t_{PZL}	t_{PZL}			1.5	7	0.8	8.7	0.6	6.8	0.5	4.7	0.5	3.8	
t_{PHZ}	t_{PHZ}	$\overline{OE}$	A	2	4	0.7	9.3	0.7	8.3	0.7	5.6	0.7	6.6	ns
t_{PLZ}	t_{PLZ}			2	4	0.7	9.3	0.7	8.3	0.7	5.6	0.7	6.6	
t_{PHZ}	t_{PHZ}	$\overline{OE}$	B	2	5	1.4	9.3	1.2	8.1	1	6.4	0.8	6.2	ns
t_{PLZ}	t_{PLZ}			2	4.5	1.4	9.3	1.2	8.1	1	6.4	0.8	6.2	

5.11 Typical Characteristics

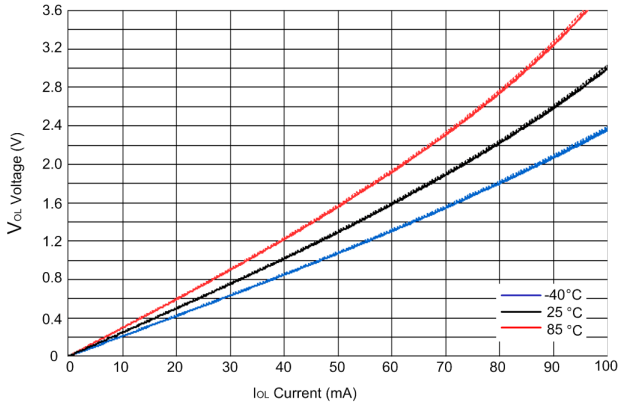


Figure 5-1. Low-Level Output Voltage (V_{OL}) vs Low-Level Current (I_{OL}) at V_{CCA} = V_{CCB} = 3.6V

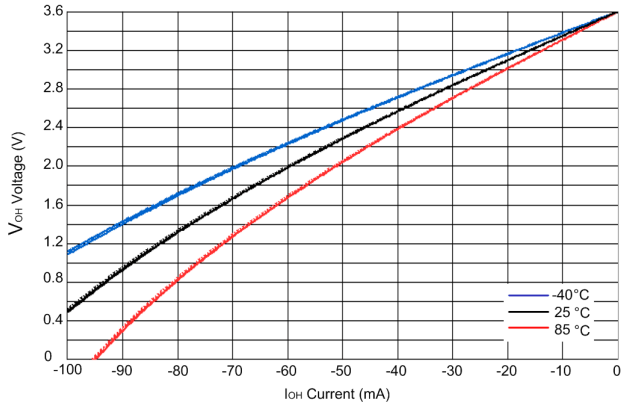


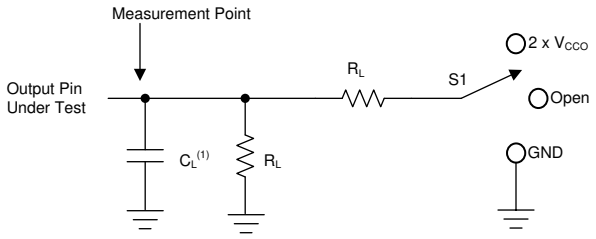
Figure 5-2. High-Level Output Voltage (V_{OH}) vs High-Level Current (I_{OH}) at V_{CCA} = V_{CCB} = 3.6V

6 Parameter Measurement Information

6.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- f = 10MHz
- Z_O = 50Ω
- Δt/ΔV ≤ 1ns/V



A. C_L includes probe and jig capacitance.

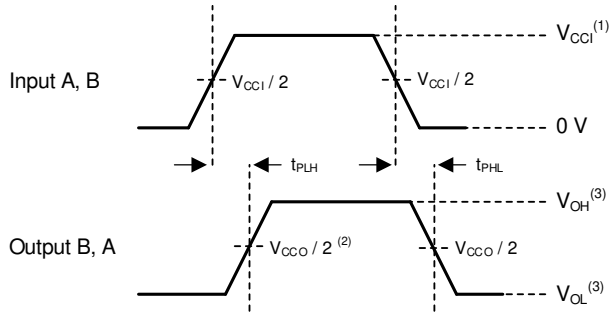
Figure 6-1. Load Circuit

Table 6-1. Load Circuit Parameters

Test Parameter		S_1
t_{pd}	Propagation (delay) time	Open
t_{PZL}, t_{PLZ}	Enable time, disable time	2 × V_{CCO}
t_{PZH}, t_{PHZ}	Enable time, disable time	GND

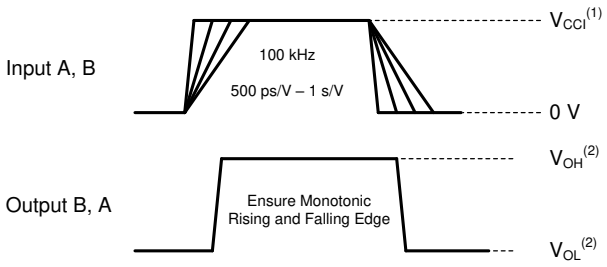
Table 6-2. Load Circuit Conditions

V_{CCO}	R_L	C_L	V_{TP}
1.2V ± 0.1V	2kΩ	15pF	0.1V
1.5V ± 0.1V	2kΩ	15pF	0.1V
1.8V ± 0.15V	2kΩ	15pF	0.15V
2.5V ± 0.2V	2kΩ	15pF	0.15V
3.3V ± 0.3V	2kΩ	15pF	0.3V



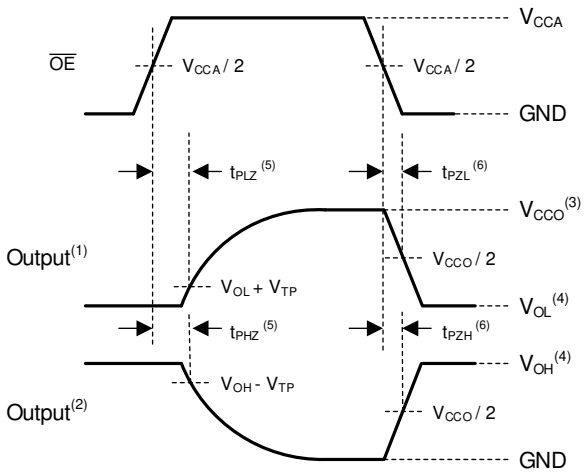
1. V_{CCI} is the V_{CC} associated with the input port.
2. V_{CCO} is the V_{CC} associated with the output port.
3. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1.
4. t_{PLH} and t_{PHL} are the same as t_{pd}.
5. The outputs are measured one at a time, with one transition per measurement.

Figure 6-2. Propagation Delay



1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1.

Figure 6-3. Input Transition Rise and Fall Rate



A. Output waveform on the condition that input is driven to a valid Logic Low.
B. Output waveform on the condition that input is driven to a valid Logic High.
C. V_{CCO} is the supply pin associated with the output port.
D. V_{OH} and V_{OL} are typical output voltage levels with specified R_L, C_L, and S_1.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 6-4. Enable Time And Disable Time

7 Detailed Description

7.1 Overview

The SN74AVC4T774 is a 4-bit, dual-supply, noninverting, bi-directional voltage level translation. Pins An and control pins (DIR1, DIR2, DIR3, DIR4 and $\overline{OE}$) are support by V_{CCA} and pins Bn are support by V_{CCB}. The A port is able to accept I/O voltages ranging from 1.1V to 3.6V, while the B port can accept I/O voltages from 1.1V to 3.6V. A high on DIR allows data transmission from An to Bn and a low on DIR allows data transmission from B to A when $\overline{OE}$ is set to low. When $\overline{OE}$ is set to high, both An and Bn are in the high-impedance state.

7.2 Functional Block Diagram

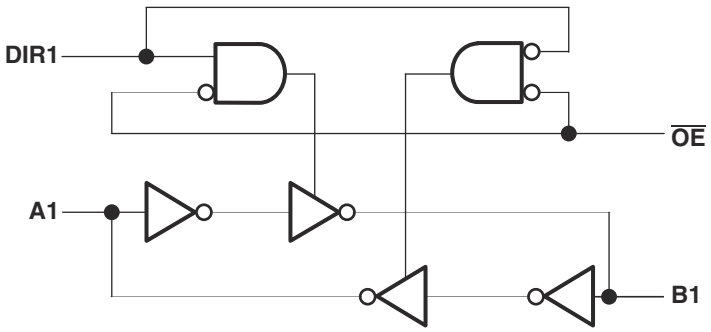


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

7.3.1 Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.1V to 3.6V Power-Supply Range

Both V_{CCA} and V_{CCB} can be supplied at any voltage between 1.1V and 3.6V making the device suitable for translating between any of the low-voltage nodes (1.2V, 1.8V, 2.5V and 3.3V).

7.3.2 Support High-Speed Translation

SN74AVC4T774 can support high data rate application. The translated signal data rate can be up to 380Mbps when signal is translated from 1.8V to 3.3V.

7.3.3 I_{off} Supports Partial-Power-Down Mode Operation

I_{off} prevents backflow current by disabling I/O output circuits when device is in partial-power-down mode.

7.4 Device Functional Modes

Table 7-1. Function Table (Each Bit)

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A data
L	H	Hi-Z	Enabled	A data to B data
H	X	Hi-Z	Hi-Z	Isolation

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74AVC4T774 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The device is designed for use in applications where a push-pull driver is connected to the data I/Os. The max data rate can be up to 380Mbps when the device translate signal is from 1.8V to 3.3V.

8.2 Typical Application

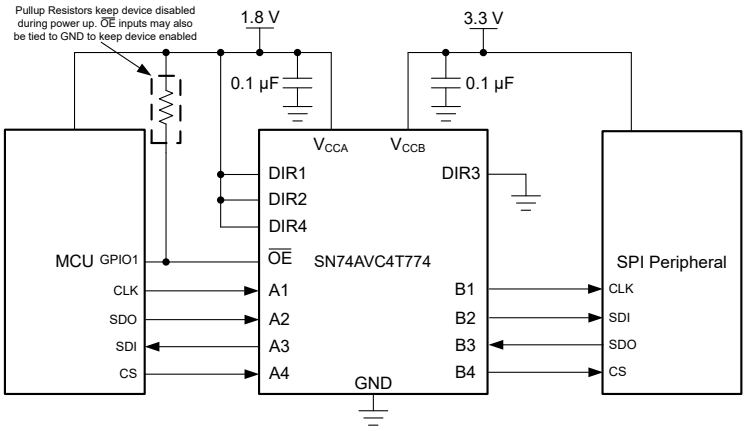


Figure 8-1. Typical Application of the SN74AVC4T774

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1.

Table 8-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input Voltage Range	1.1V to 3.6V
Output Voltage Range	1.1V to 3.6V

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AVC4T774 device to determine the input voltage range. For a valid logic high, the value must exceed the V_{IH} of the input port. For a valid logic low, the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AVC4T774 device is driving to determine the output voltage range.

8.2.3 Application Curve

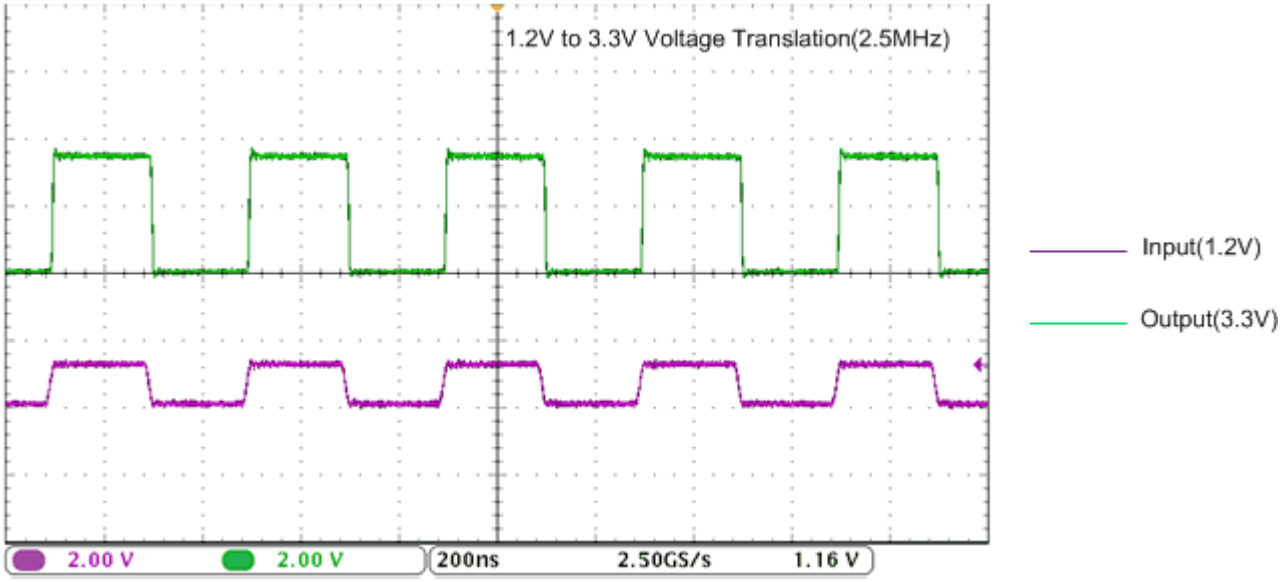


Figure 8-2. Translation Up (1.2 V to 3.3 V) at 2.5 MHz

8.3 Power Supply Recommendations

The SN74AVC4T774 device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. V_{CCA} accepts any supply voltage from 1.1V to 3.6V and V_{CCB} accepts any supply voltage from 1.1V to 3.6V. The A port and B port are designed to track V_{CCA} and V_{CCB} respectively allowing for low-voltage, bi-directional translation between any of the 1.2V, 1.5V, 1.8V, 2.5V and 3.3V voltage nodes.

The output-enable $\overline{OE}$ input circuit is designed so that it is supplied by V_{CCA} and when the $\overline{OE}$ input is high, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power-up or power-down, the $\overline{OE}$ input pin must be tied to V_{CCA} through a pullup resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pullup resistor to V_{CCA} is determined by the current-sinking capability of the driver.

8.4 Layout

8.4.1 Layout Guidelines

For reliability of the device, following common printed-circuit board layout guidelines are recommended:

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements

8.4.2 Layout Example

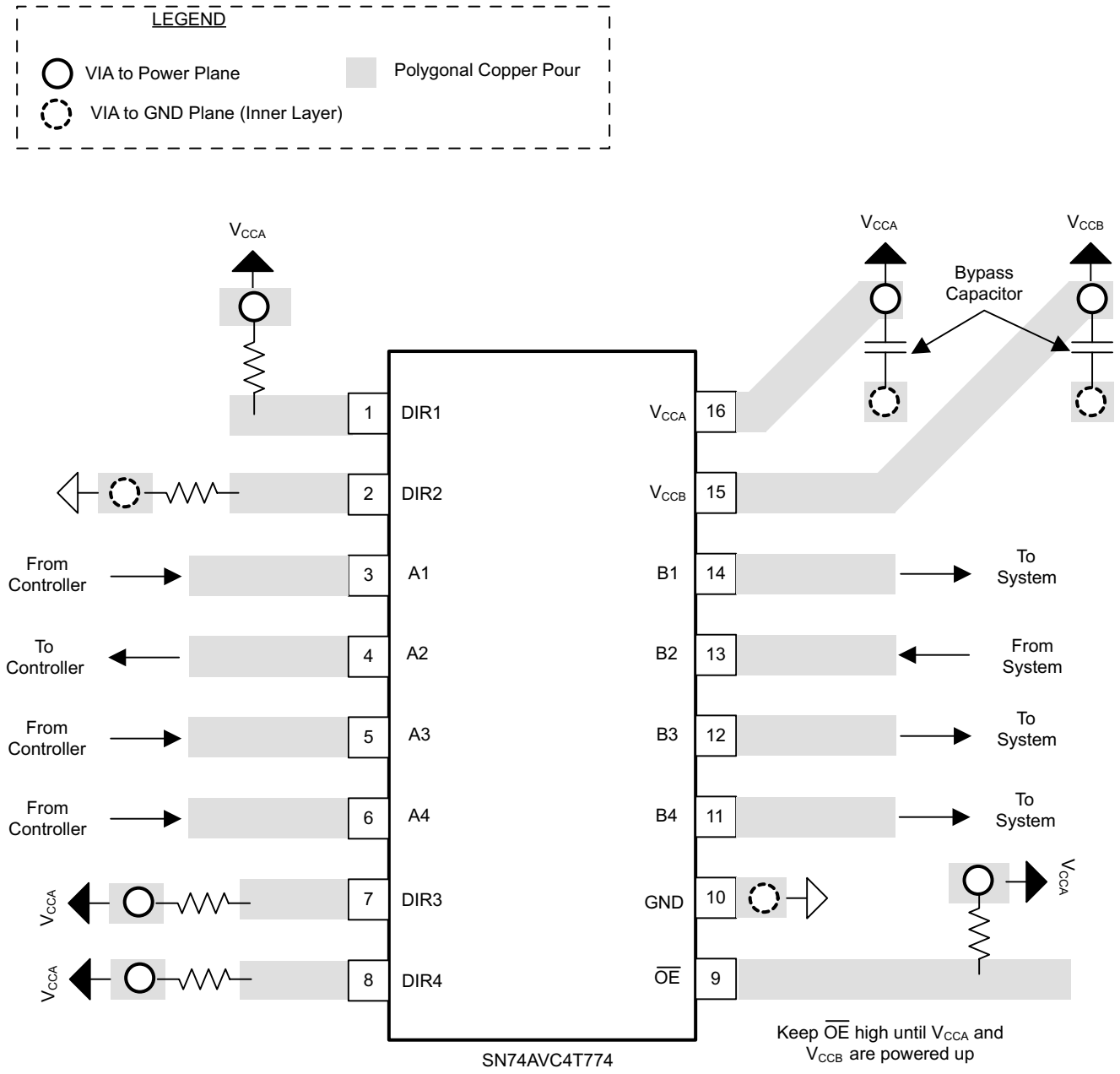


Figure 8-3. PCB Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *16-Bit Widebus Logic Families in 56-Ball, 0.65-mm Pitch Very Thin Fine-Pitch BGA* application report
- Texas Instruments, *AVC Logic Family Technology and Applications* application report
- Texas Instruments, *AVC Advanced Very-Low-Voltage CMOS Logic Data Book, March 2000* data book
- Texas Instruments, *Dynamic Output Control (DOC) Circuitry Technology And Applications (Rev. B)* application report
- Texas Instruments, *Introduction to Logic* application report
- Texas Instruments, *LCD Module Interface Application Clip* brochure
- Texas Instruments, *Logic Cross-Reference* application note
- Texas Instruments, *Logic Guide* marketing selection guide
- Texas Instruments, *LOGIC Pocket Data Book* data book
- Texas Instruments, *Selecting the Right Level Translation Solution* application report
- Texas Instruments, *Semiconductor Packing Material Electrostatic Discharge (ESD) Protection* application report
- Texas Instruments, *Solving CMOS Transition Rate Issues Using Schmitt Trigger Solution* white paper
- Texas Instruments, *Standard Linear & Logic for PCs, Servers & Motherboards* brochure
- Texas Instruments, *TI Tablet Solutions* solution guide
- Texas Instruments, *Understanding and Interpreting Standard-Logic Data Sheets* application report
- Texas Instruments, *Voltage Translation Between 3.3-V, 2.5-V, 1.8-V, and 1.5-V Logic Standards* application report

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (May 2024) to Revision I (February 2025)	Page
• Updated RGY and PW thermal information	7

Changes from Revision G (May 2021) to Revision H (March 2024)	Page
• Added the BQB and DYY packages to the datasheet	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74AVC4T774RSVR-NT	Active	Production	UQFN (RSV) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZVK
74AVC4T774RSVR-NT.A	Active	Production	UQFN (RSV) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZVK
74AVC4T774RSVR-NT.B	Active	Production	UQFN (RSV) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZVK
74AVC4T774RSVRG4	Active	Production	UQFN (RSV) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZVK
SN74AVC4T774BQBR	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT774
SN74AVC4T774BQBR.A	Active	Production	WQFN (BQB) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT774
SN74AVC4T774DYYR	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT774
SN74AVC4T774DYYR.A	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT774
SN74AVC4T774PW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT774
SN74AVC4T774PW.B	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT774
SN74AVC4T774PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	WT774
SN74AVC4T774PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT774
SN74AVC4T774PWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT774
SN74AVC4T774PWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT774
SN74AVC4T774PWRG4.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT774
SN74AVC4T774PWRG4.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT774
SN74AVC4T774RGYR	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	WT774
SN74AVC4T774RGYR.A	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	WT774
SN74AVC4T774RGYR.B	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	WT774
SN74AVC4T774RGYRG4	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	WT774
SN74AVC4T774RGYRG4.A	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	WT774
SN74AVC4T774RGYRG4.B	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	WT774
SN74AVC4T774RSVR	Active	Production	UQFN (RSV) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZVK
SN74AVC4T774RSVR.A	Active	Production	UQFN (RSV) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZVK
SN74AVC4T774RSVR.B	Active	Production	UQFN (RSV) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZVK

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AVC4T774 :

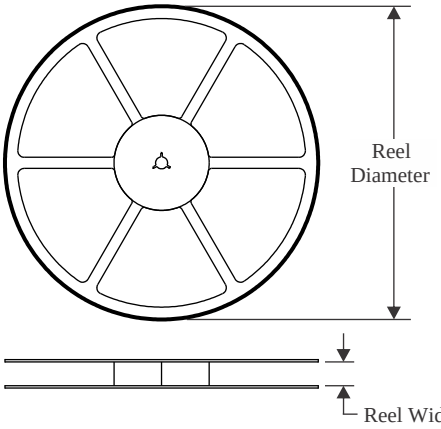
- Automotive : SN74AVC4T774-Q1

NOTE: Qualified Version Definitions:

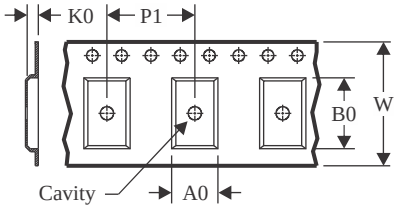
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

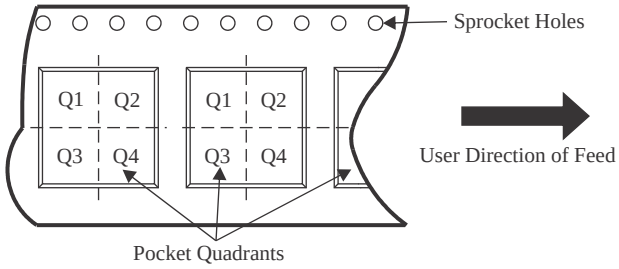


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

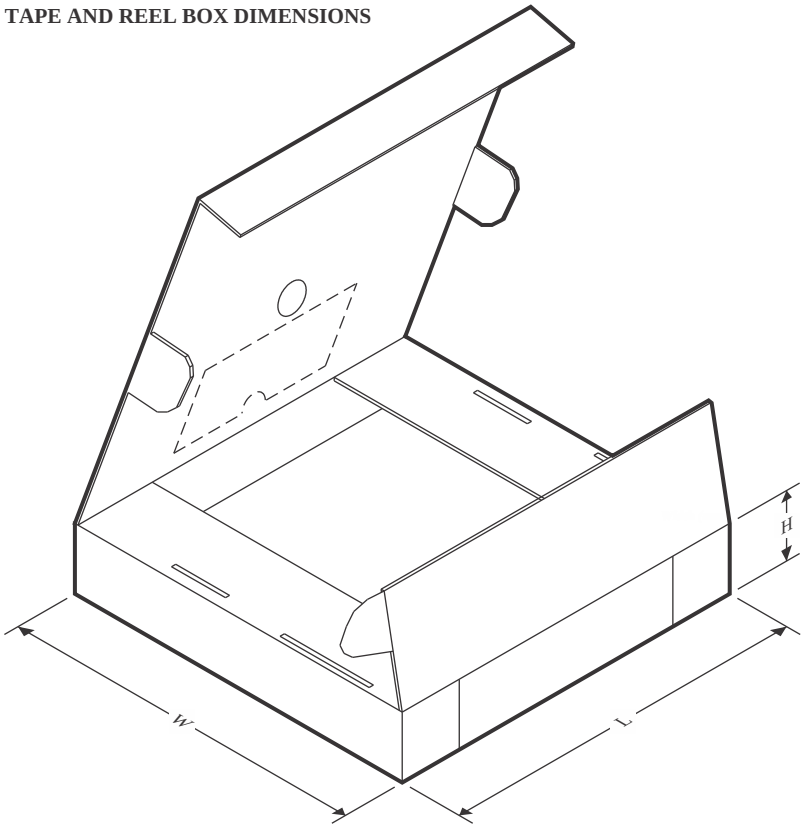
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AVC4T774RSVR-NT	UQFN	RSV	16	3000	180.0	9.5	2.1	2.9	0.75	4.0	8.0	Q1
SN74AVC4T774BQBR	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
SN74AVC4T774DYYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
SN74AVC4T774PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AVC4T774PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AVC4T774PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AVC4T774RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN74AVC4T774RGYRG4	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN74AVC4T774RSVR	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1

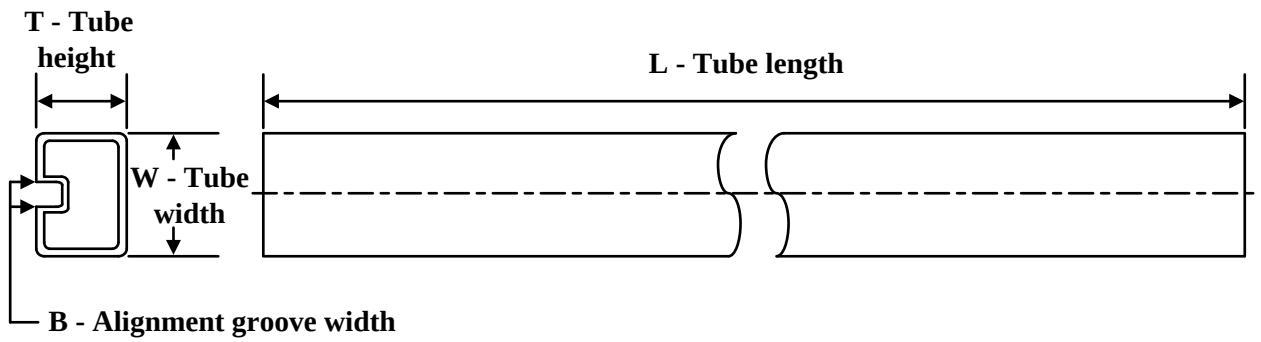
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AVC4T774RSVR-NT	UQFN	RSV	16	3000	189.0	185.0	36.0
SN74AVC4T774BQBR	WQFN	BQB	16	3000	210.0	185.0	35.0
SN74AVC4T774DYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
SN74AVC4T774PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74AVC4T774PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74AVC4T774PWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74AVC4T774RGYR	VQFN	RGY	16	3000	353.0	353.0	32.0
SN74AVC4T774RGYRG4	VQFN	RGY	16	3000	353.0	353.0	32.0
SN74AVC4T774RSVR	UQFN	RSV	16	3000	189.0	185.0	36.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74AVC4T774PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN74AVC4T774PW.B	PW	TSSOP	16	90	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

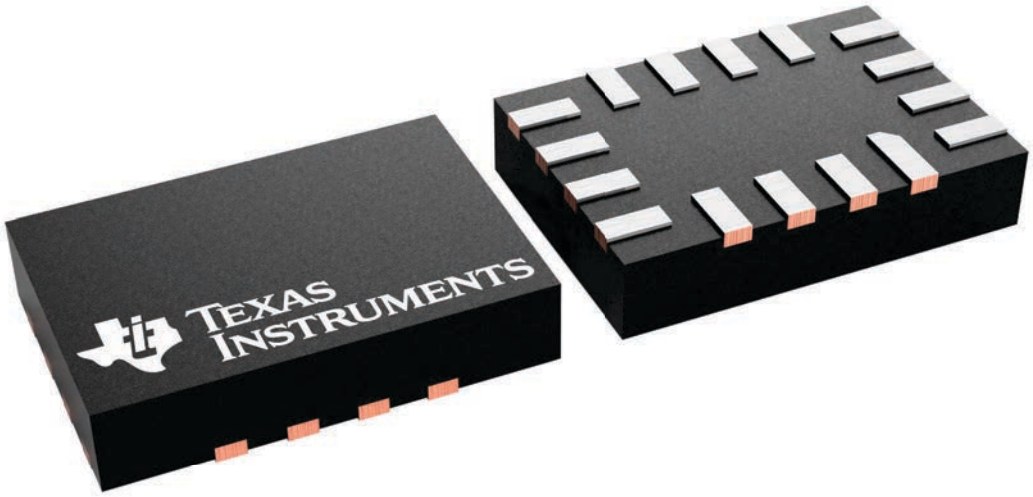
RSV 16

UQFN - 0.55 mm max height

1.8 x 2.6, 0.4 mm pitch

ULTRA THIN QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



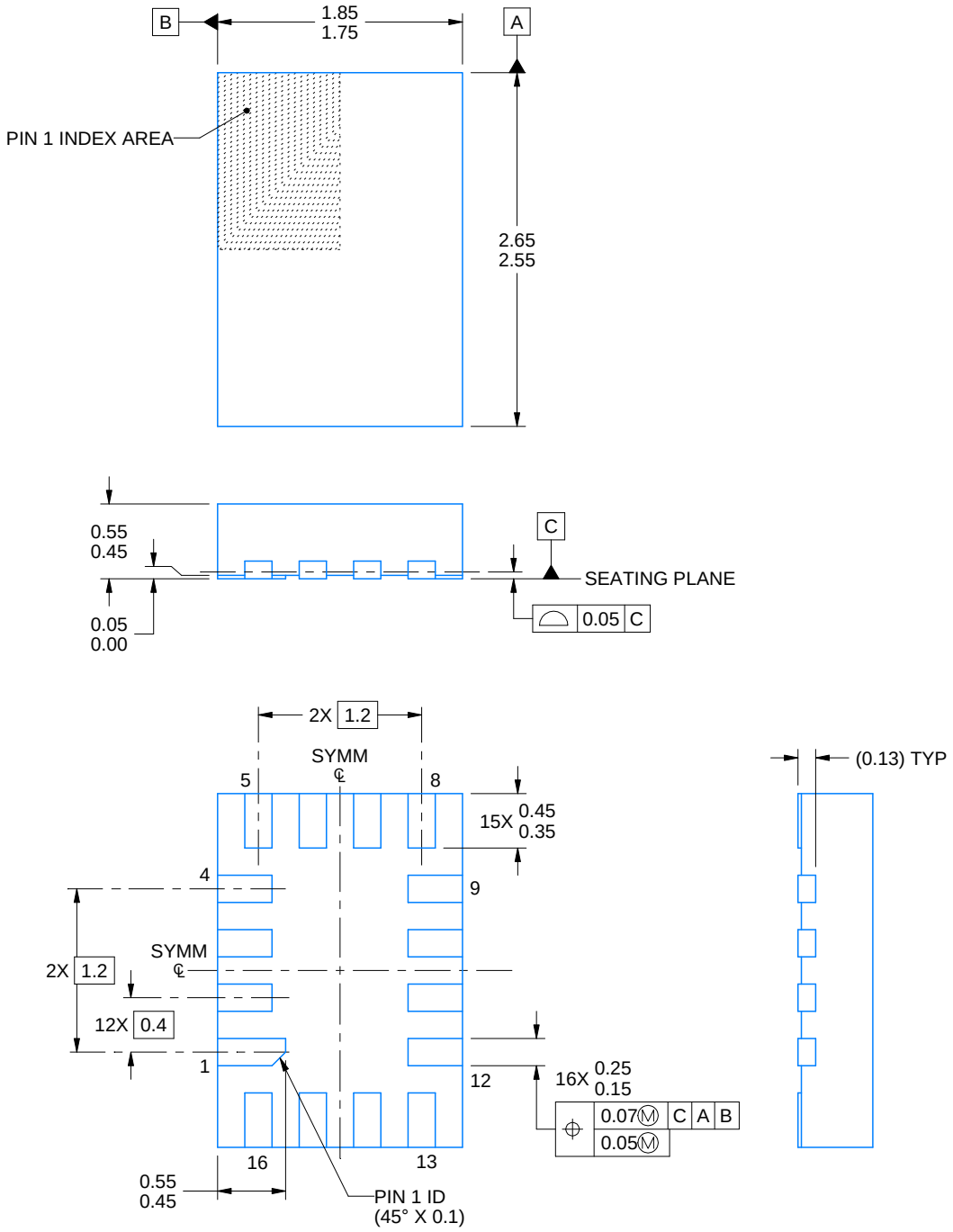
4231225/A

RSV0016A

PACKAGE OUTLINE

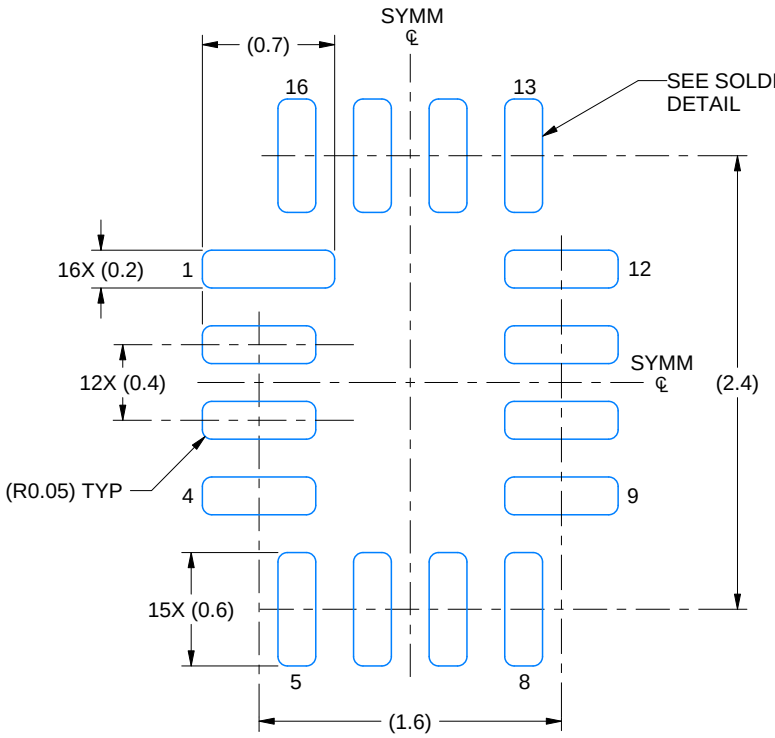
UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD

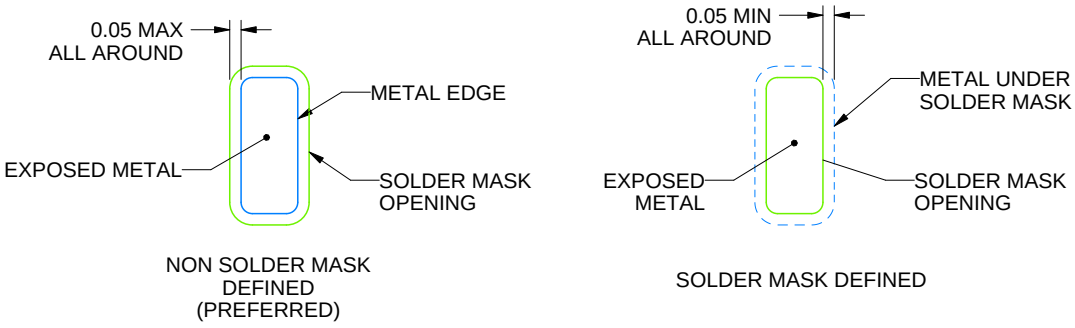


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

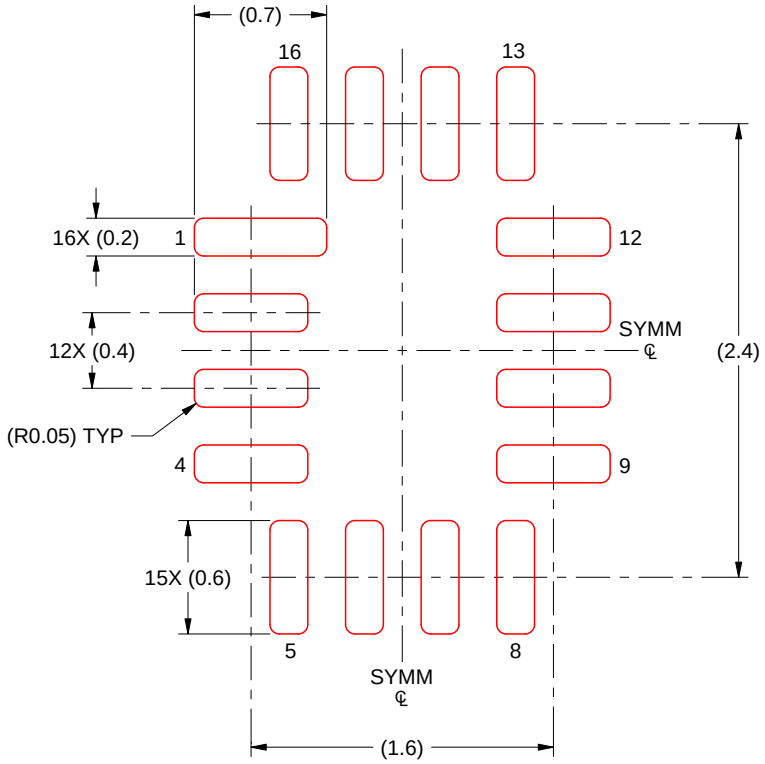


SOLDER MASK DETAILS

4220314/C 02/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

4220314/C 02/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

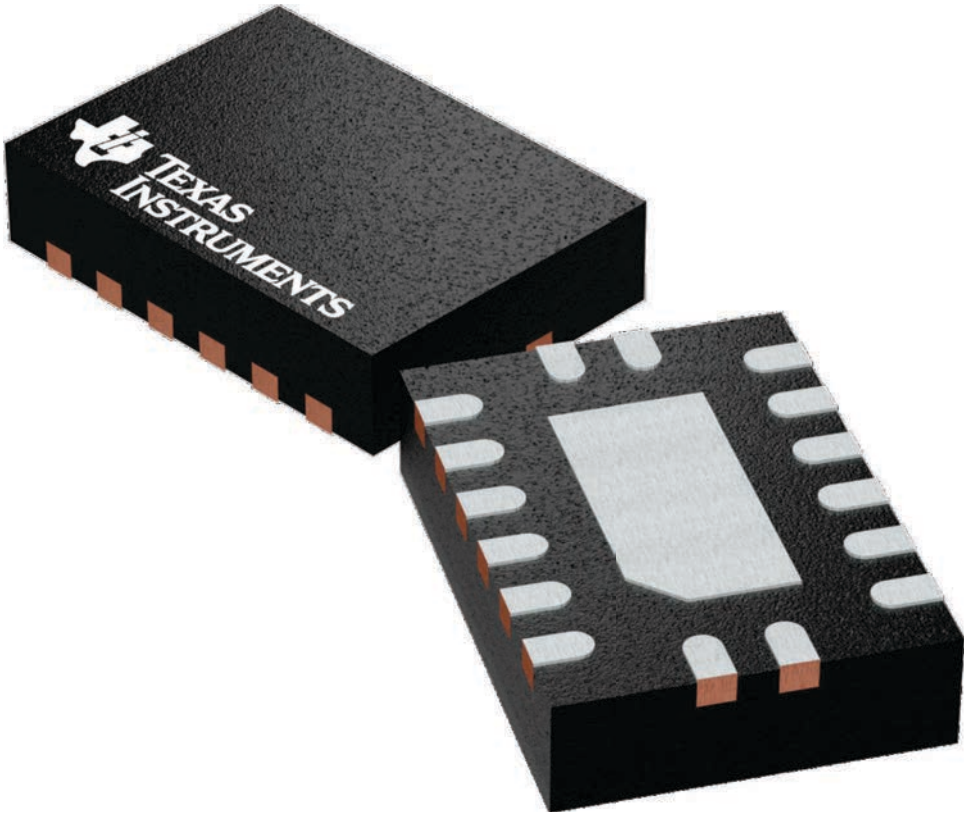
BQB 16

WQFN - 0.8 mm max height

2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



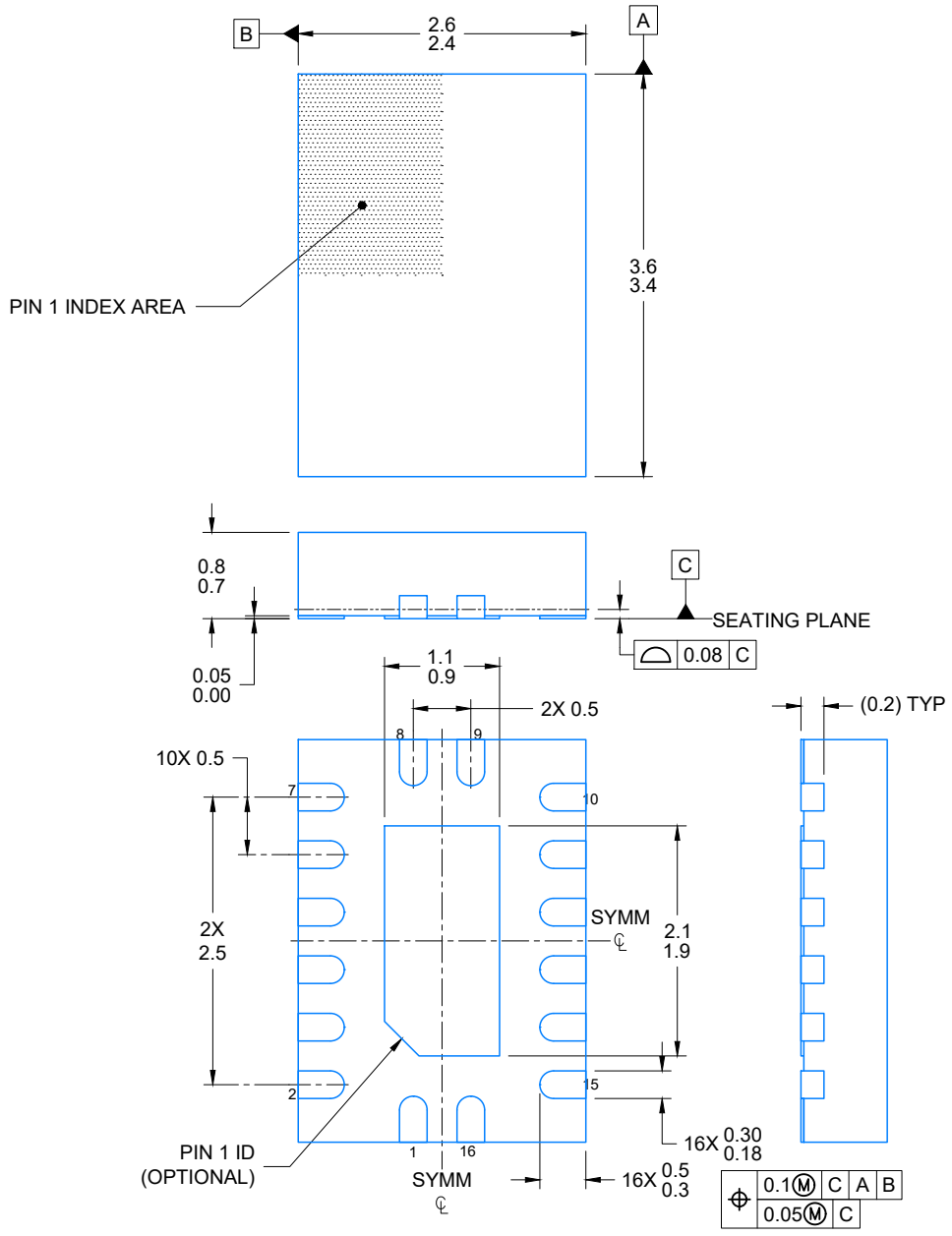
4226161/A

PACKAGE OUTLINE

BQB0016A

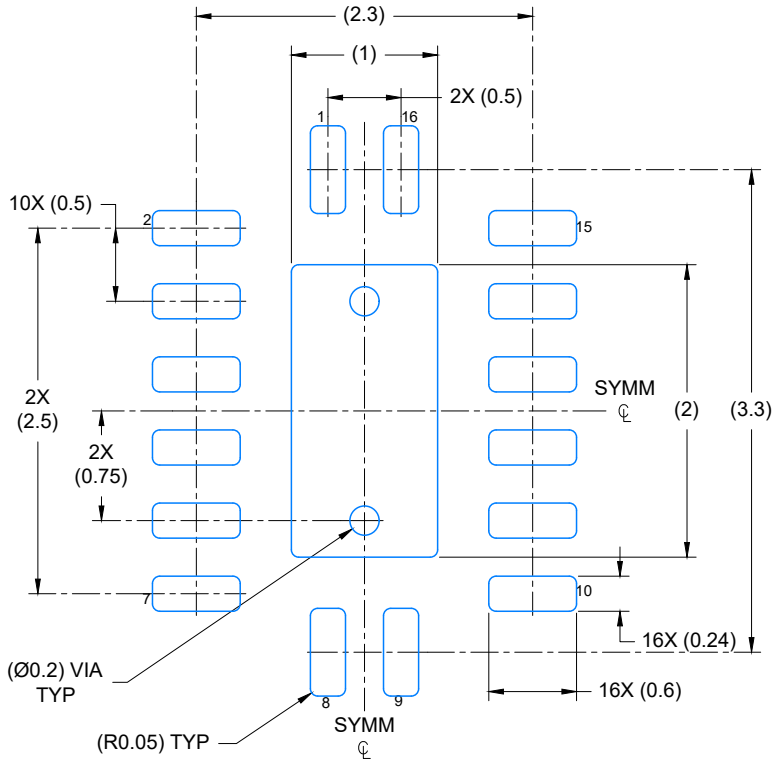
WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

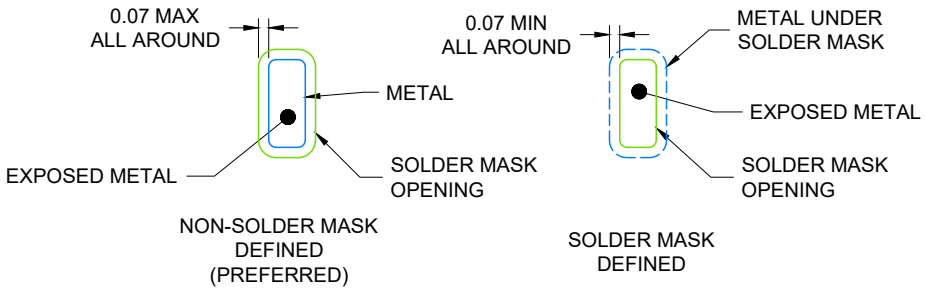


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



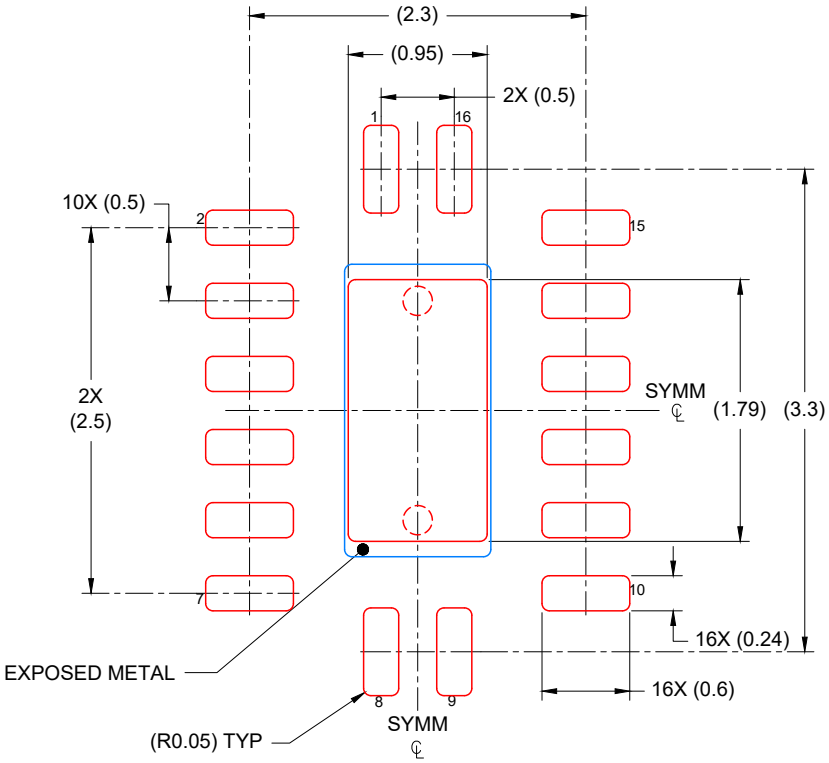
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224640/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4224640/A 11/2018

NOTES: (continued)

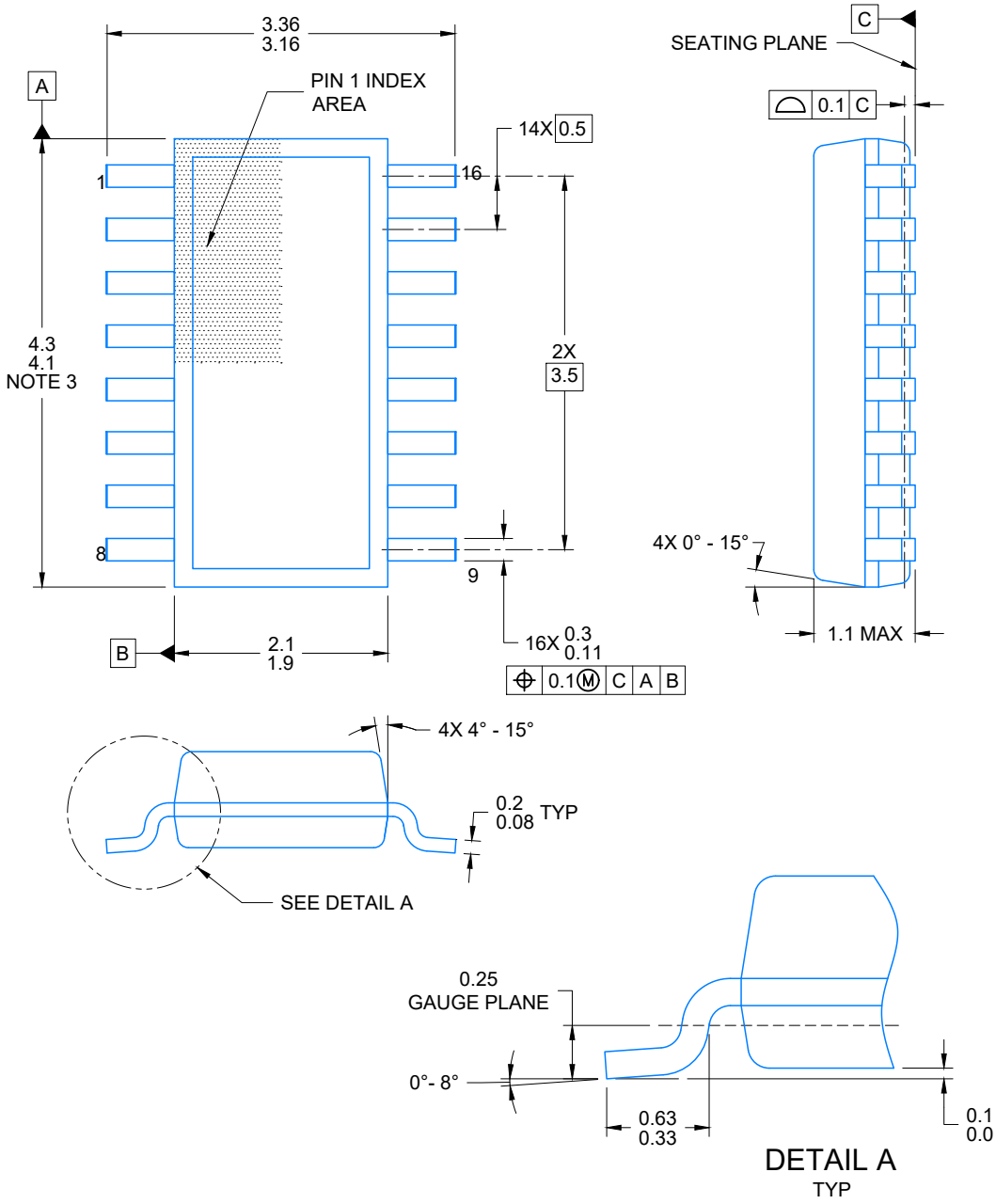
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DYY0016A

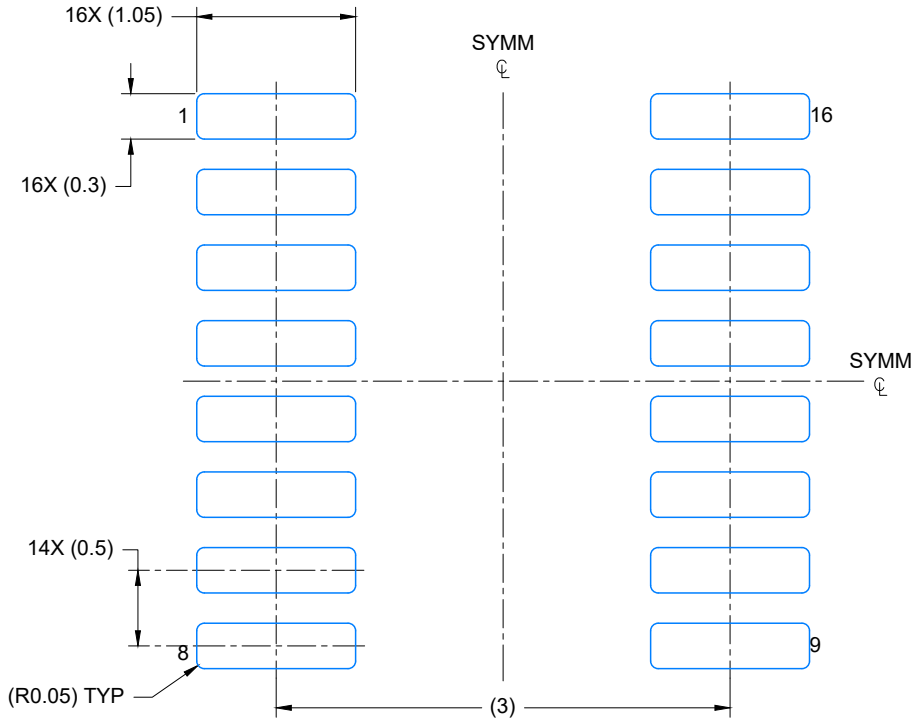
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

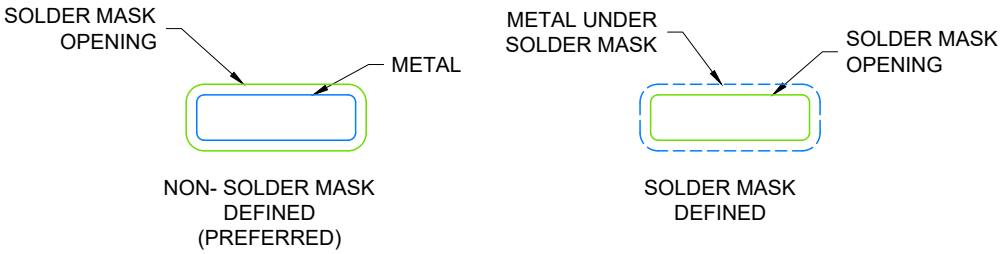


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224642/D 07/2024

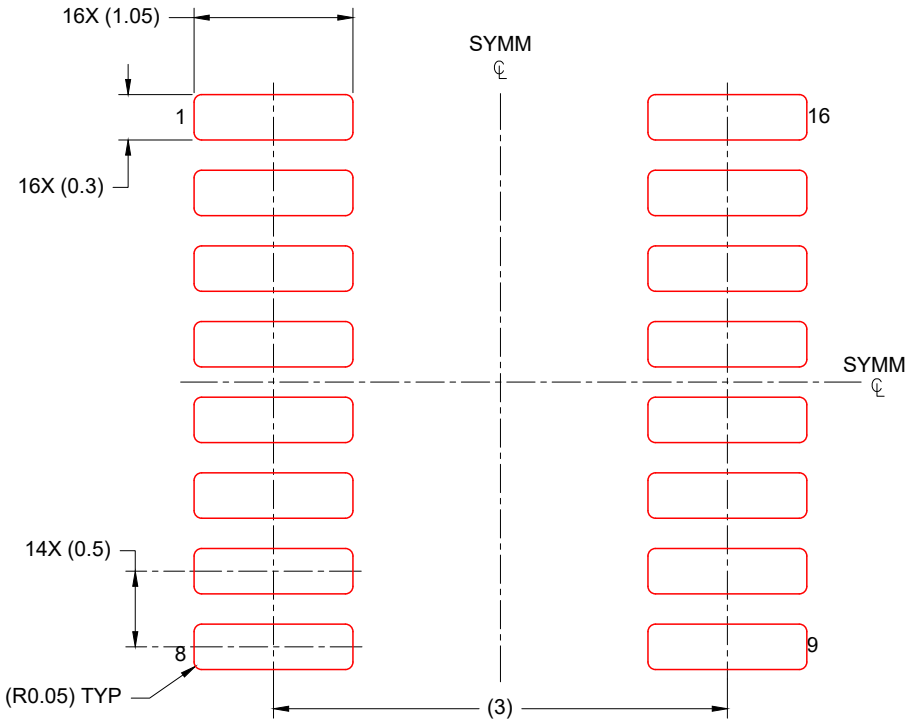
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

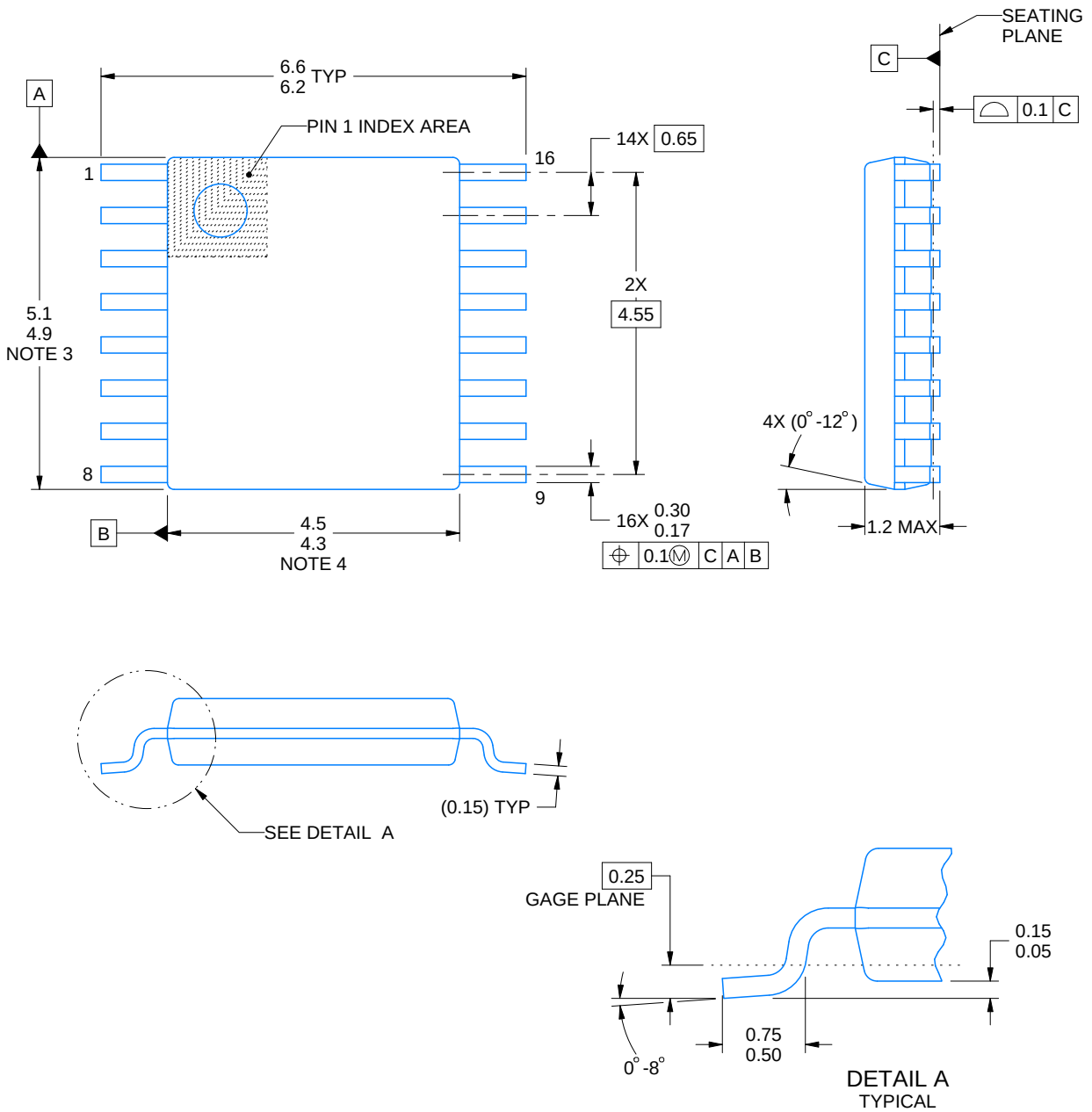
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0016A

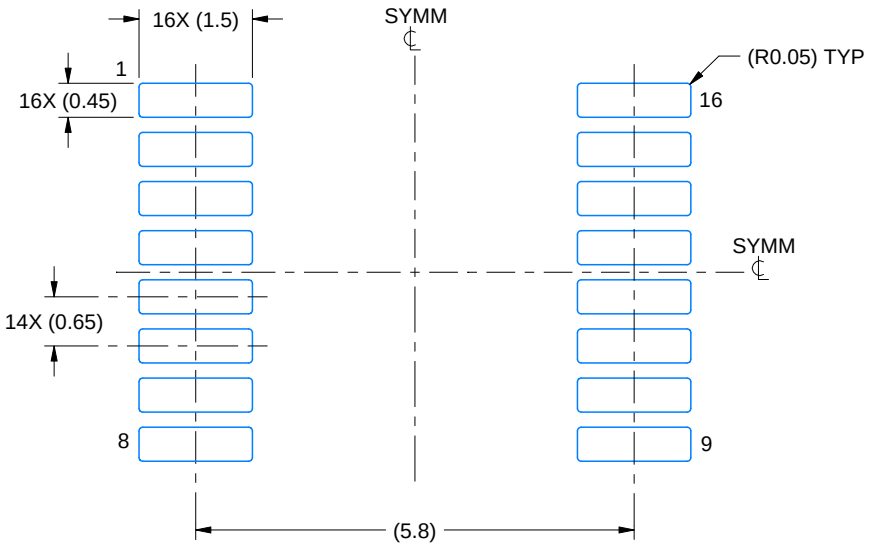
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



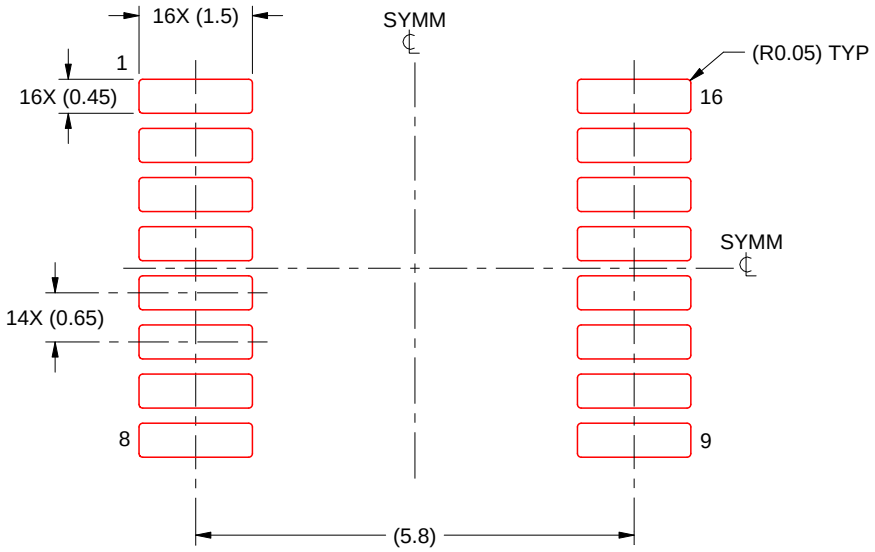
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



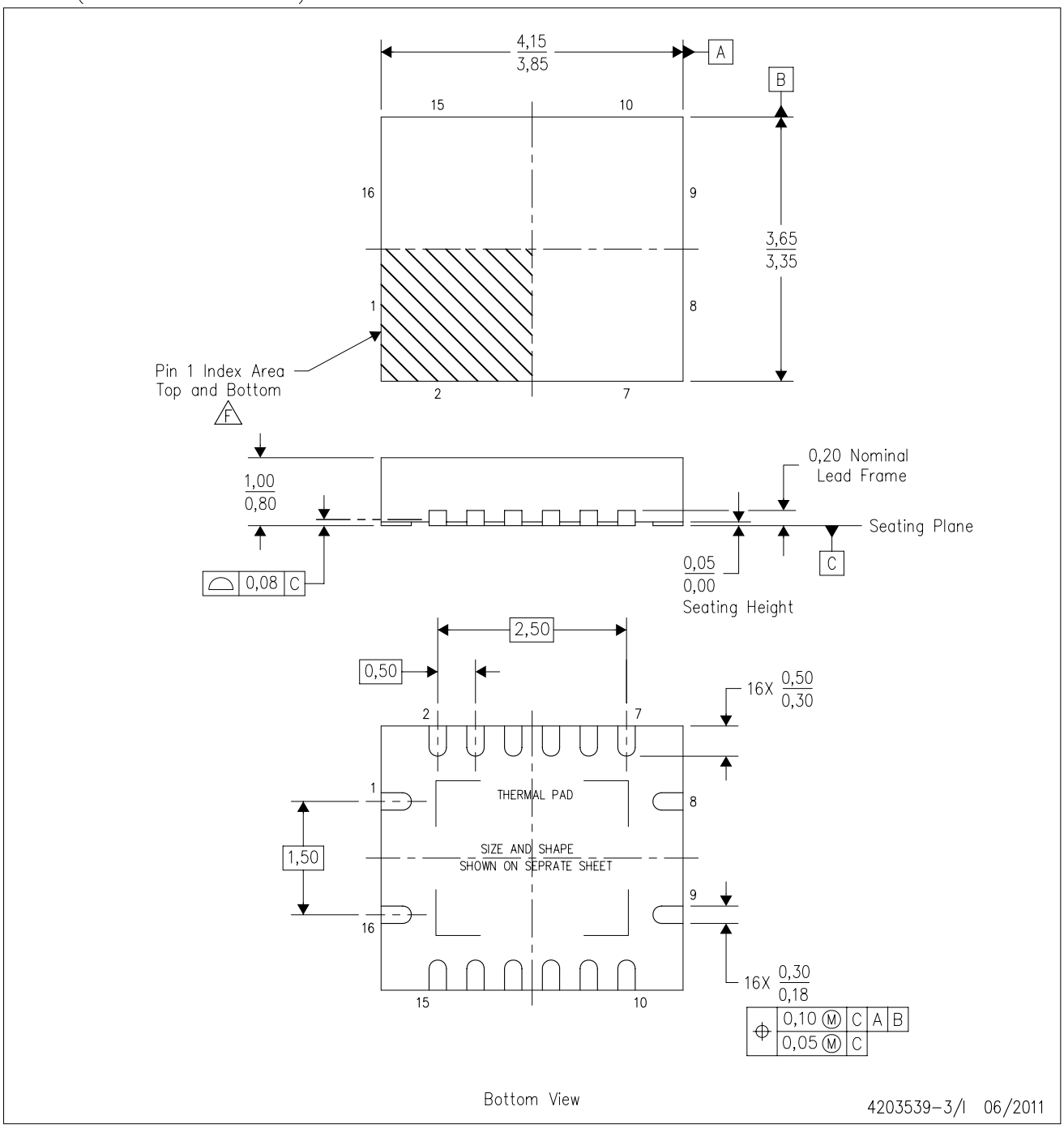
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

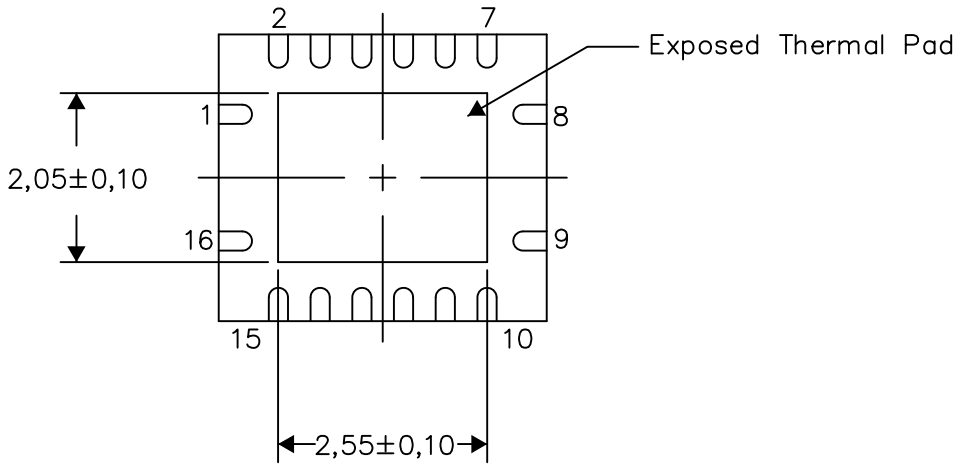
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



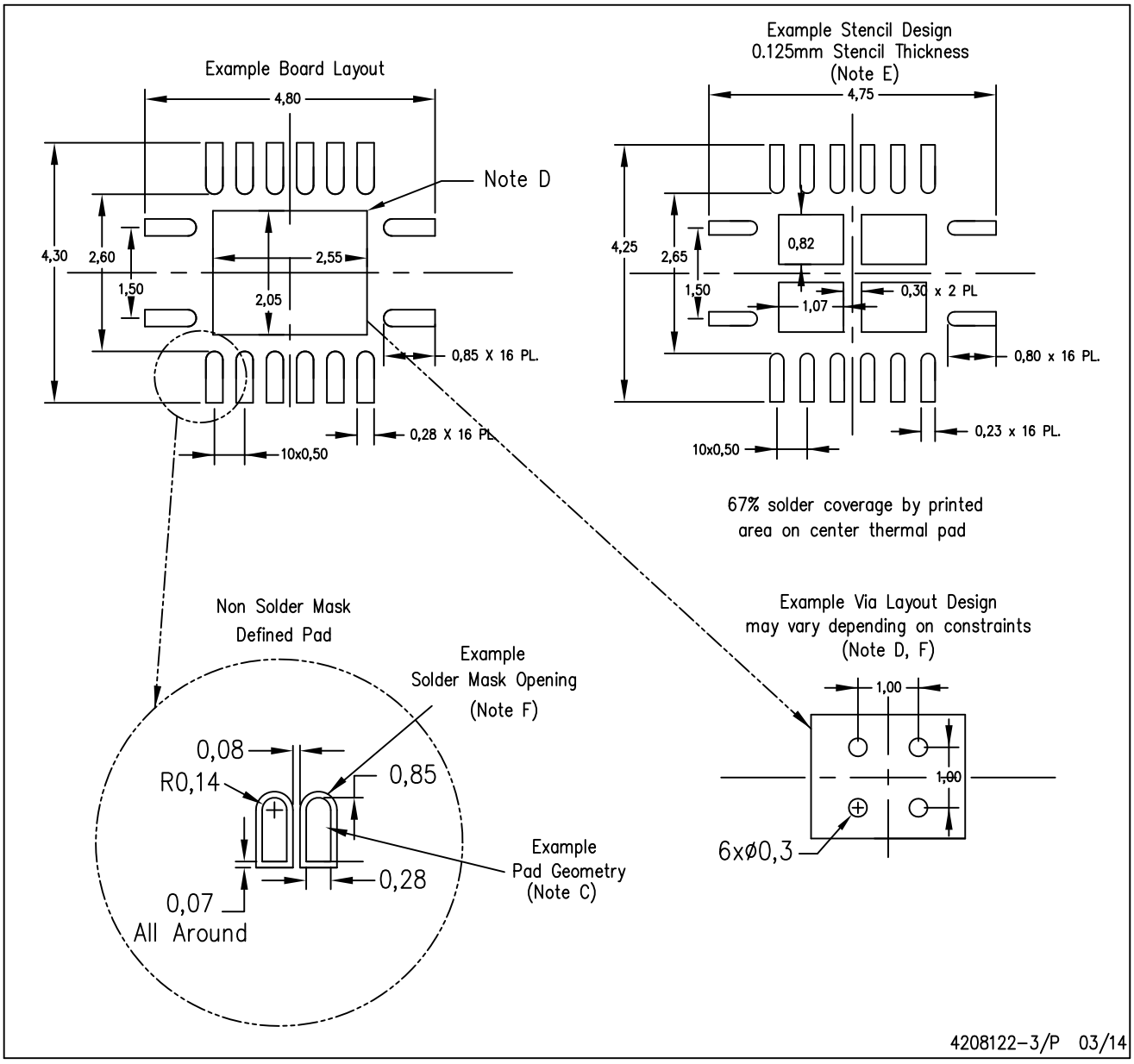
Bottom View

Exposed Thermal Pad Dimensions

4206353–3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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Last updated 10/2025