

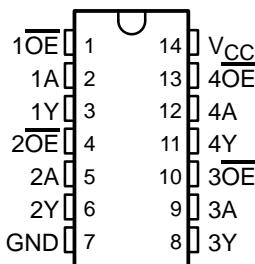
# SN54BCT125A, SN74BCT125A QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCBS032F – SEPTEMBER 1988 – REVISED MARCH 2003

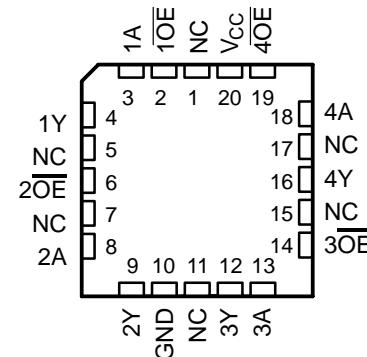
- Operating Voltage Range of 4.5 V to 5.5 V
- State-of-the-Art BiCMOS Design  
Significantly Reduces  $I_{CCZ}$

- 3-State Outputs Drive Bus Lines or Buffer  
Memory Address Registers

SN54BCT125A . . . J OR W PACKAGE  
SN74BCT125A . . . D, N, OR NS PACKAGE  
(TOP VIEW)



SN54BCT125A . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The 'BCT125A bus buffers feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ( $\overline{OE}$ ) input is high.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74BCT125AN	SN74BCT125AN
	SOIC – D	Tube	SN74BCT125AD	BCT125A
	SOP – NS	Tape and reel	SN74BCT125ADR	
-55°C to 125°C	SOP – NS	Tape and reel	SN74BCT125ANSR	BCT125A
	CDIP – J	Tube	SNJ54BCT125AJ	SNJ54BCT125AJ
	CFP – W	Tube	SNJ54BCT125AW	SNJ54BCT125AW
	LCCC – FK	Tube	SNJ54BCT125AFK	SNJ54BCT125AFK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## FUNCTION TABLE (each buffer)

INPUTS		OUTPUT Y
$\overline{OE}$	A	
L	H	H
L	L	L
H	X	Z



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



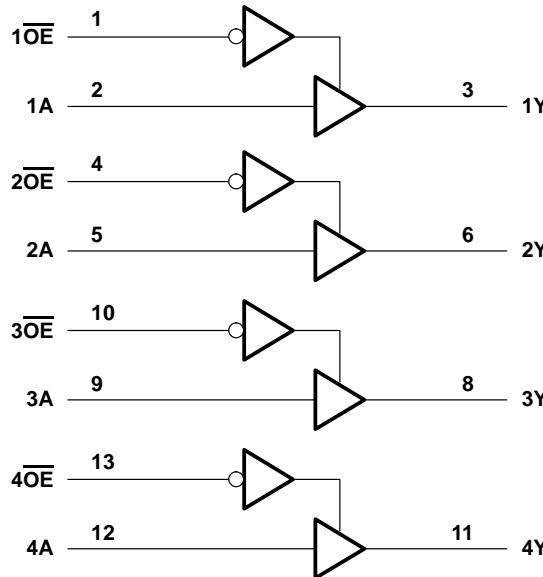
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# **SN54BCT125A, SN74BCT125A QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS**

SCBS032F – SEPTEMBER 1988 – REVISED MARCH 2003

## logic diagram (positive logic)



Pin numbers shown are for the D, J, N, NS, and W packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, $V_O$ .....	-0.5 V to 5.5 V
Voltage range applied to any output in the high state, $V_O$ .....	-0.5 V to $V_{CC}$
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-30 mA
Current into any output in the low state, $I_O$ :	
SN54BCT125A .....	96 mA
SN74BCT125A .....	128 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2):	
D package .....	86°C/W
N package .....	80°C/W
NS package .....	76°C/W
Storage temperature range, $T_{STG}$ .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

**SN54BCT125A, SN74BCT125A  
QUADRUPLE BUS BUFFER GATES  
WITH 3-STATE OUTPUTS**

SCBS032F – SEPTEMBER 1988 – REVISED MARCH 2003

**recommended operating conditions (see Note 3)**

		SN54BCT125A			SN74BCT125A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
I <sub>IK</sub>	Input clamp current			-18			-18	mA
I <sub>OH</sub>	High-level output current			-12			-15	mA
I <sub>OL</sub>	Low-level output current			48			64	mA
T <sub>A</sub>	Operating free-air temperature	-55	125		0		70	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	SN54BCT125A			SN74BCT125A			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2			-1.2	V
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -3 mA	2.4	3.3	2.4	3.3		V
		I <sub>OH</sub> = -12 mA	2	3.2				
		I <sub>OH</sub> = -15 mA			2	3.1		
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 48 mA	0.38	0.55				V
		I <sub>OL</sub> = 64 mA			0.42	0.55		
I <sub>I</sub>	V <sub>CC</sub> = 0, V <sub>I</sub> = 7 V		0.1		0.1		0.1	mA
I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V			35			25	µA
I <sub>IL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.5 V			-20			-20	µA
I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.7 V		50		50		50	µA
I <sub>OZL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0.5 V			-50			-50	µA
I <sub>OS</sub> ‡	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0	-100	-225	-100	-225			mA
I <sub>CCH</sub>	V <sub>CC</sub> = 5.5 V, Outputs open	19	31		19	31		mA
I <sub>CCL</sub>	V <sub>CC</sub> = 5.5 V, Outputs open	46	49		46	49		mA
I <sub>CCZ</sub>	V <sub>CC</sub> = 5.5 V, Outputs open	6	14		6	14		mA
C <sub>i</sub>	V <sub>CC</sub> = 5 V, V <sub>I</sub> = 2.5 V or 0.5 V	4			4			pF
C <sub>o</sub>	V <sub>CC</sub> = 5 V, V <sub>O</sub> = 2.5 V or 0.5 V	9			9			pF

† All typical values are at V<sub>CC</sub> = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

**SN54BCT125A, SN74BCT125A  
QUADRUPLE BUS BUFFER GATES  
WITH 3-STATE OUTPUTS**

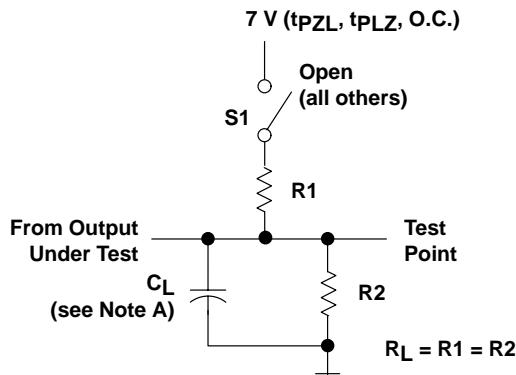
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**switching characteristics (see Figure 1)**

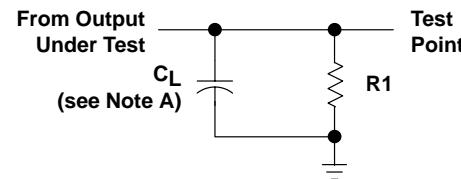
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, C <sub>L</sub> = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T <sub>A</sub> = 25°C			V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T <sub>A</sub> = MIN to MAX\$			UNIT	
			'BCT125A			SN54BCT125A		SN74BCT125A		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	Y	1.6	3.5	5.2	1.6	6	1.6	5.7	ns
t <sub>PHL</sub>			2.7	5	6.9	2.7	8	2.7	7.7	
t <sub>PZH</sub>	OE	Y	3.4	6.7	9	3.4	11.1	3.4	10.3	ns
t <sub>PZL</sub>			5	8.2	10.4	5	12.8	5	11.7	
t <sub>PHZ</sub>	OE	Y	3	5.8	7.4	3	9.4	3	8.9	ns
t <sub>PLZ</sub>			2.8	5.5	7.3	2.8	9.9	2.8	8.6	

\$ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

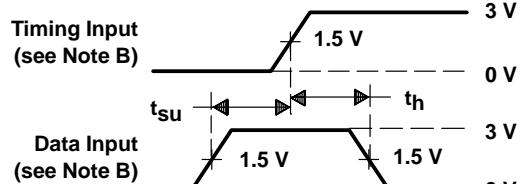
PARAMETER MEASUREMENT INFORMATION



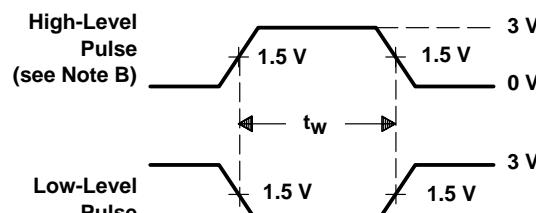
LOAD CIRCUIT FOR  
3-STATE AND OPEN-COLLECTOR OUTPUTS



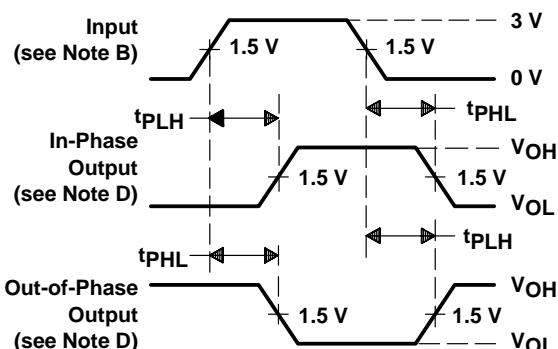
LOAD CIRCUIT FOR  
TOTEM-POLE OUTPUTS



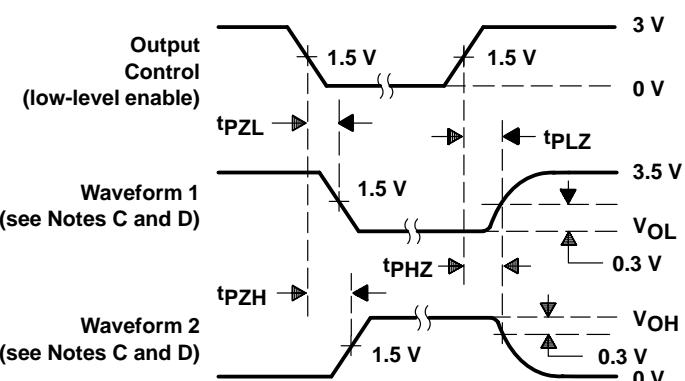
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES (see Note D)



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES:

- C<sub>L</sub> includes probe and jig capacitance.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, t<sub>r</sub> = t<sub>f</sub>  $\leq$  2.5 ns, duty cycle = 50%.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- The outputs are measured one at a time with one transition per measurement.
- When measuring propagation delay times of 3-state outputs, switch S1 is open.
- All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9093701M2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9093701M2A SNJ54BCT125AFK
5962-9093701MCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9093701MC A SNJ54BCT125AJ
5962-9093701MDA	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9093701MD A SNJ54BCT125AW
SN54BCT125AJ	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54BCT125AJ
SN54BCT125AJ.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54BCT125AJ
SN74BCT125AD	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	0 to 70	BCT125A
SN74BCT125ADR	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT125A
SN74BCT125ADR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT125A
SN74BCT125AN	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74BCT125AN
SN74BCT125AN.A	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74BCT125AN
SN74BCT125ANSR	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT125A
SN74BCT125ANSR.A	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCT125A
SNJ54BCT125AFK	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9093701M2A SNJ54BCT125AFK
SNJ54BCT125AFK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9093701M2A SNJ54BCT125AFK
SNJ54BCT125AJ	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9093701MC A SNJ54BCT125AJ
SNJ54BCT125AJ.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9093701MC A SNJ54BCT125AJ

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54BCT125AW	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9093701MD A SNJ54BCT125AW
SNJ54BCT125AW.A	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9093701MD A SNJ54BCT125AW

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN54BCT125A, SN74BCT125A :**

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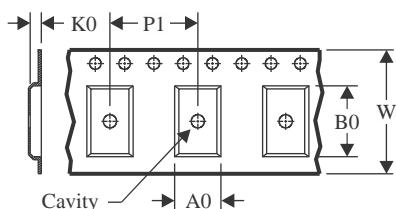
- Catalog : [SN74BCT125A](#)

- Military : [SN54BCT125A](#)

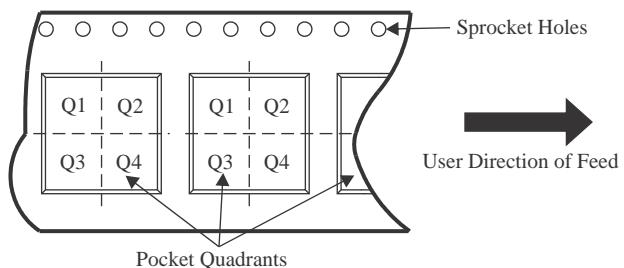
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

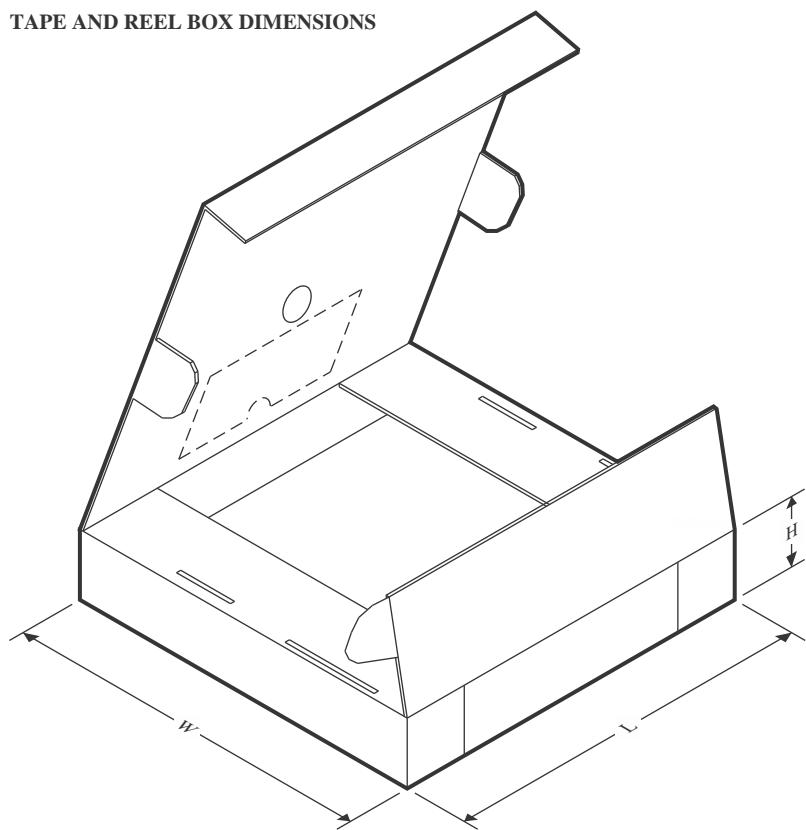
**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


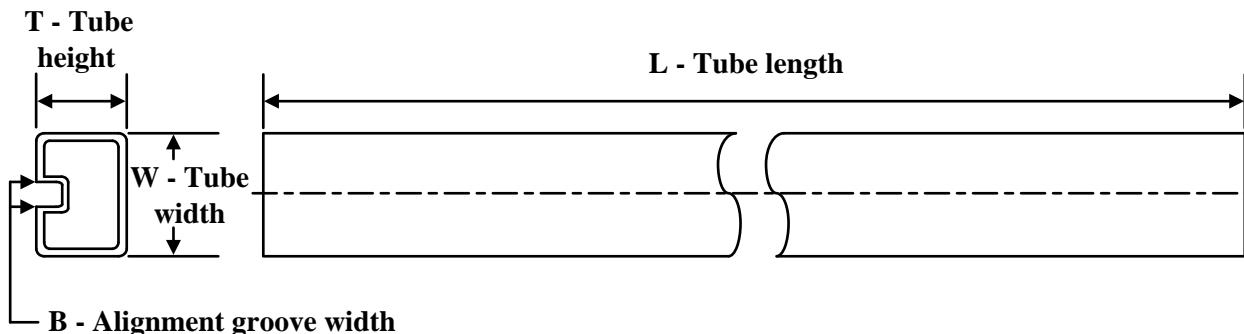
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74BCT125ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74BCT125ADR	SOIC	D	14	2500	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

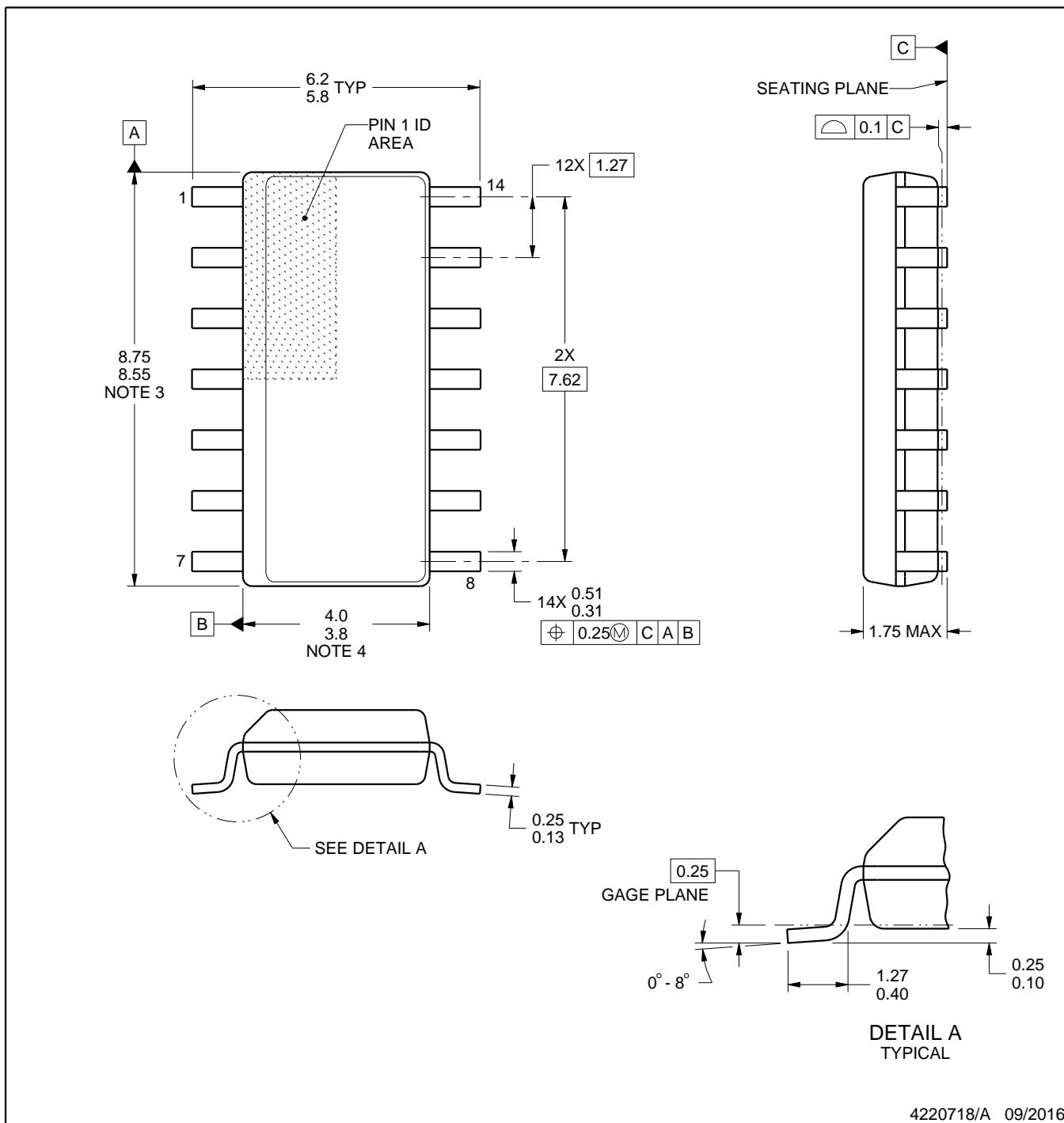
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T ( $\mu$ m)	B (mm)
5962-9093701M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9093701MDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74BCT125AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74BCT125AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74BCT125AN.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74BCT125AN.A	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54BCT125AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54BCT125AFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54BCT125AW	W	CFP	14	25	506.98	26.16	6220	NA
SNJ54BCT125AW.A	W	CFP	14	25	506.98	26.16	6220	NA

# PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

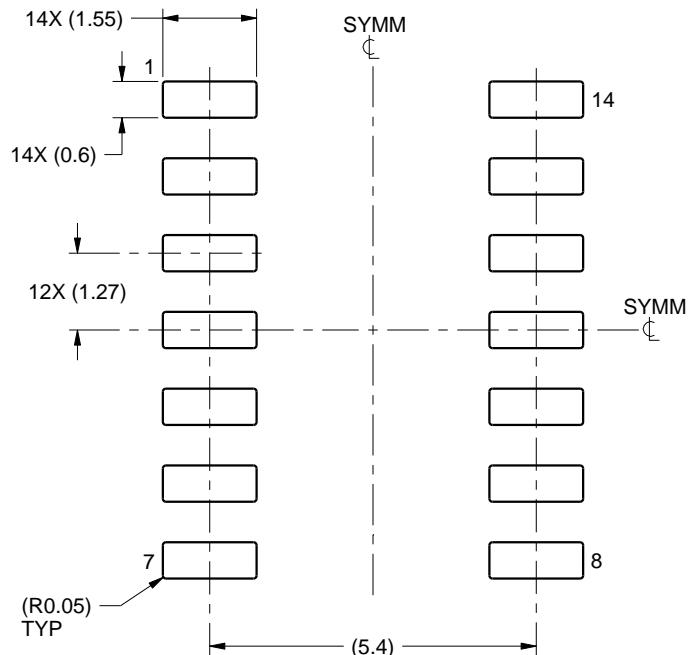
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

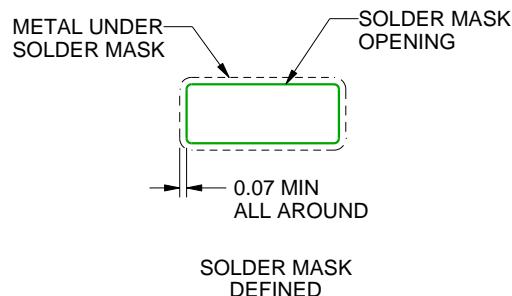
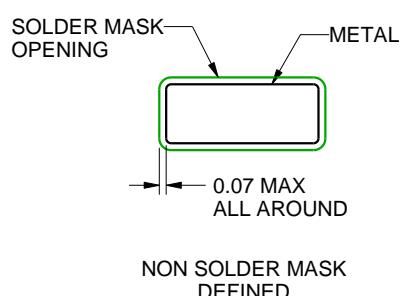
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

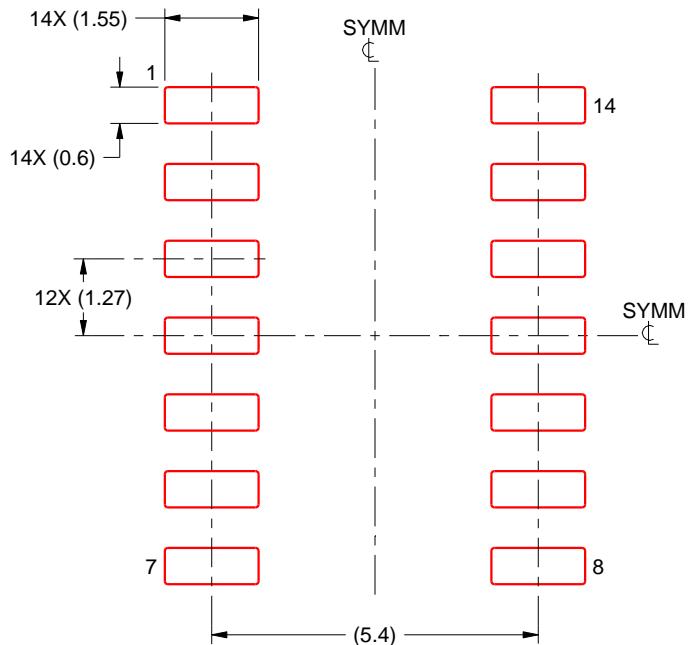
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

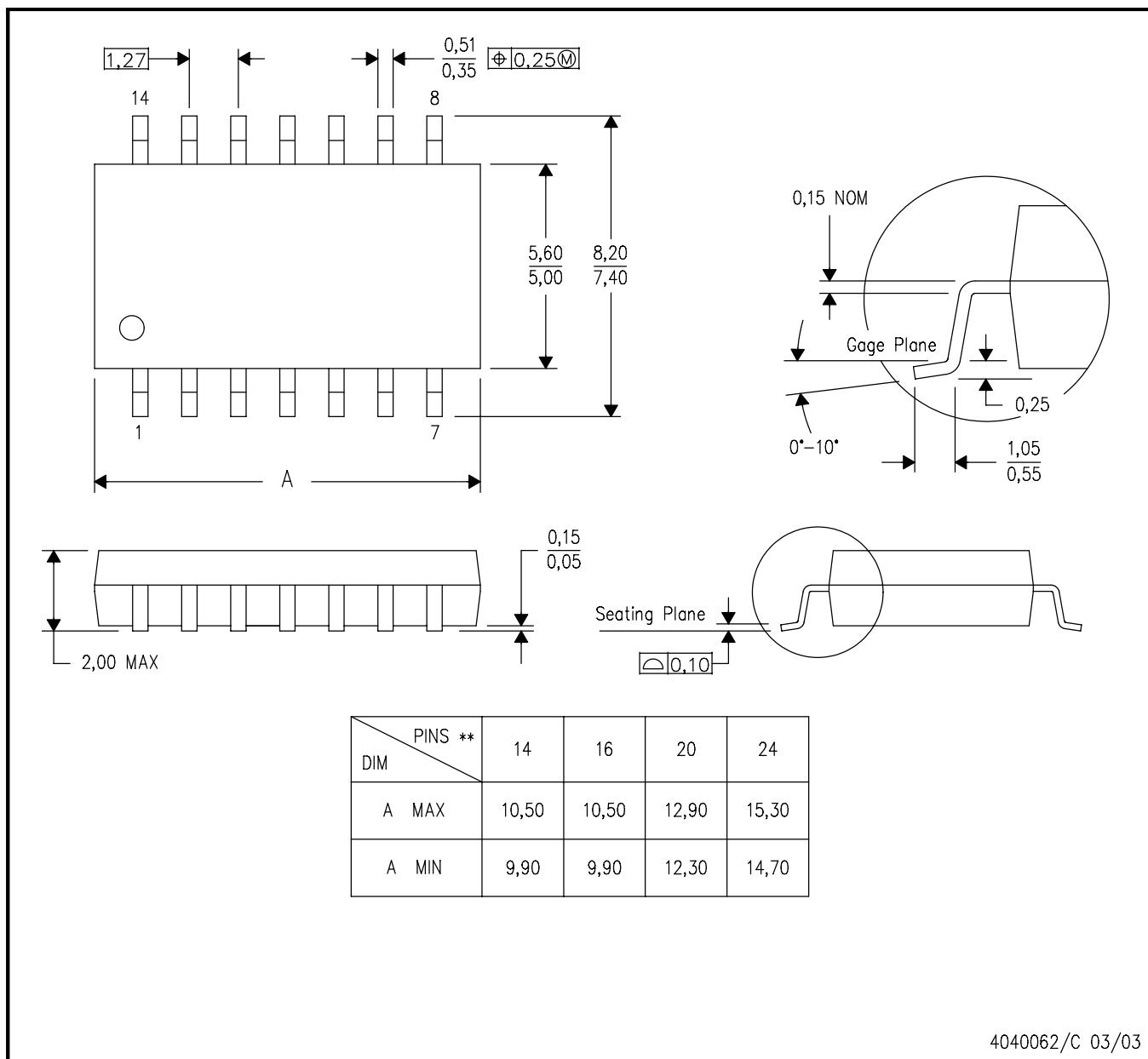
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE

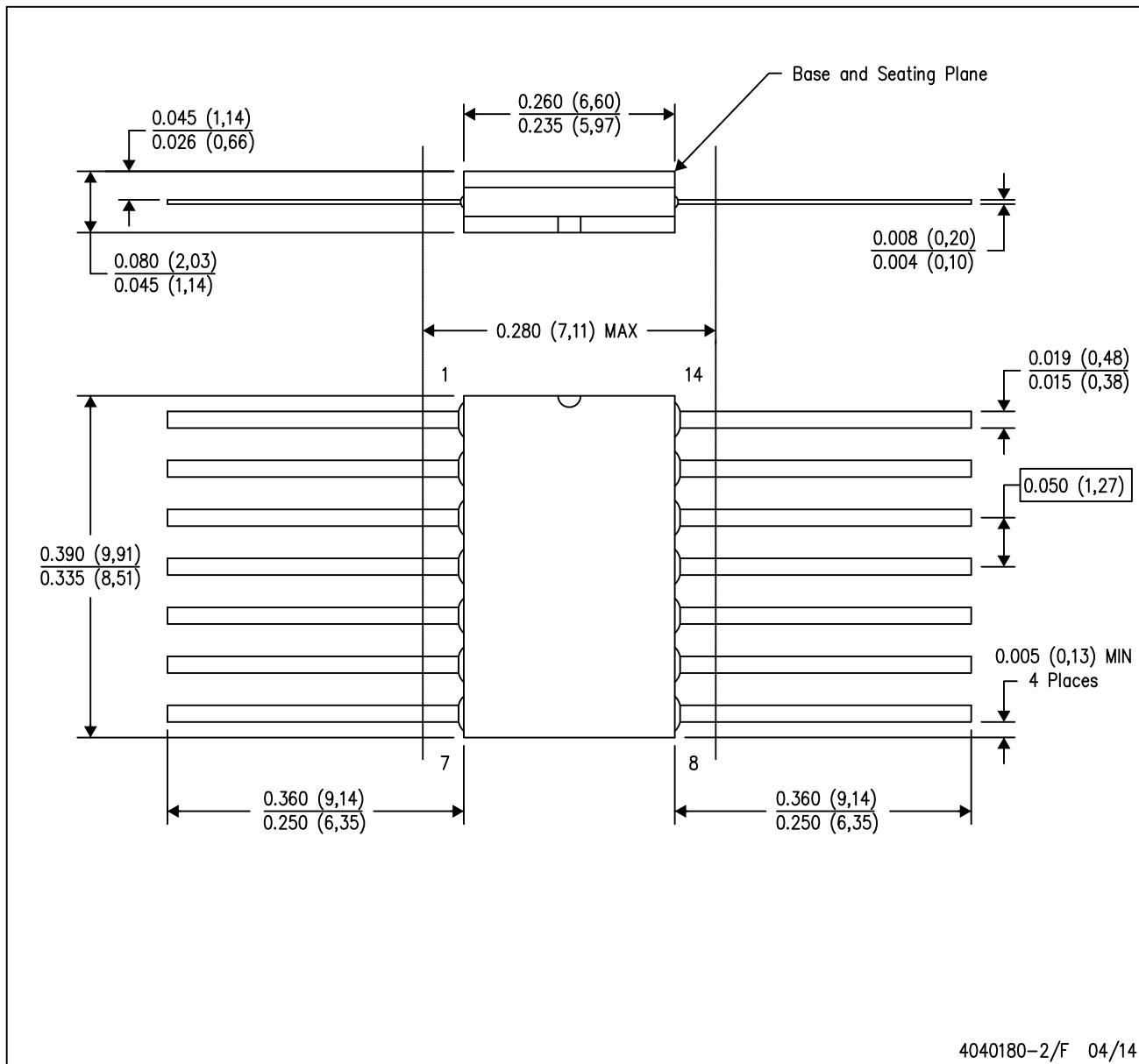


4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



4040180-2/F 04/14

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL-STD 1835 GDFP1-F14

# GENERIC PACKAGE VIEW

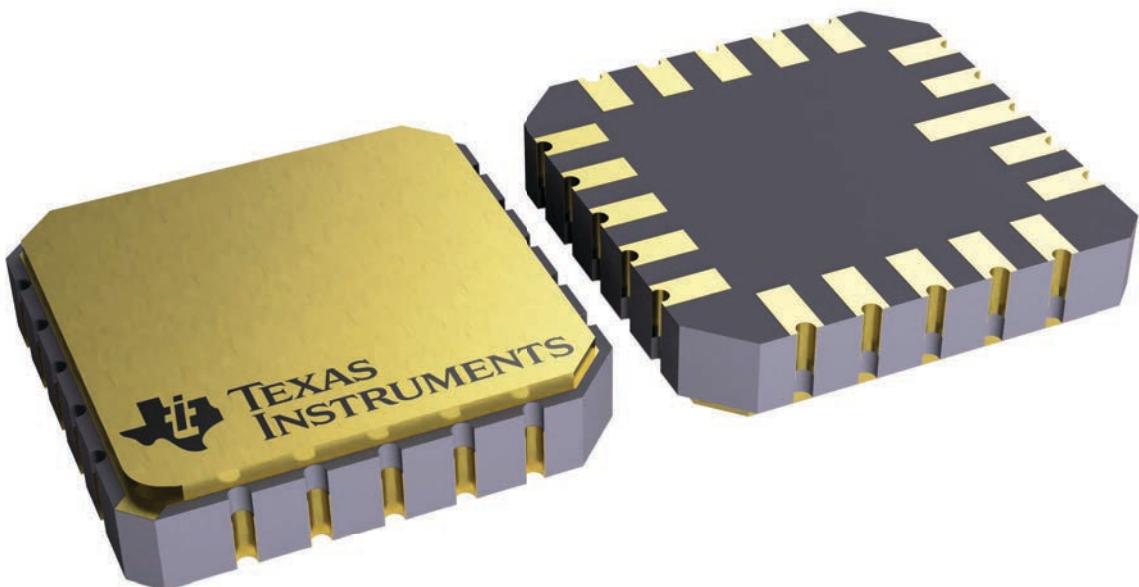
**FK 20**

**LCCC - 2.03 mm max height**

**8.89 x 8.89, 1.27 mm pitch**

**LEADLESS CERAMIC CHIP CARRIER**

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



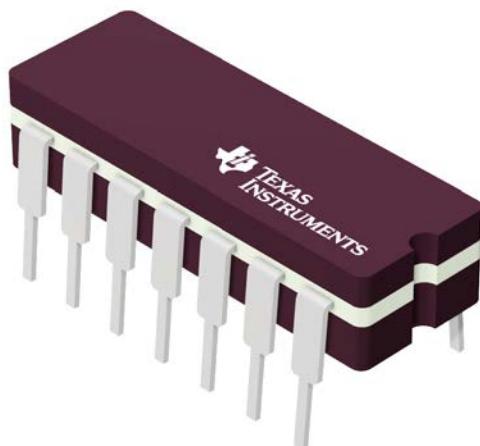
4229370VA\

# GENERIC PACKAGE VIEW

**J 14**

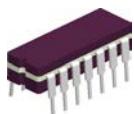
**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

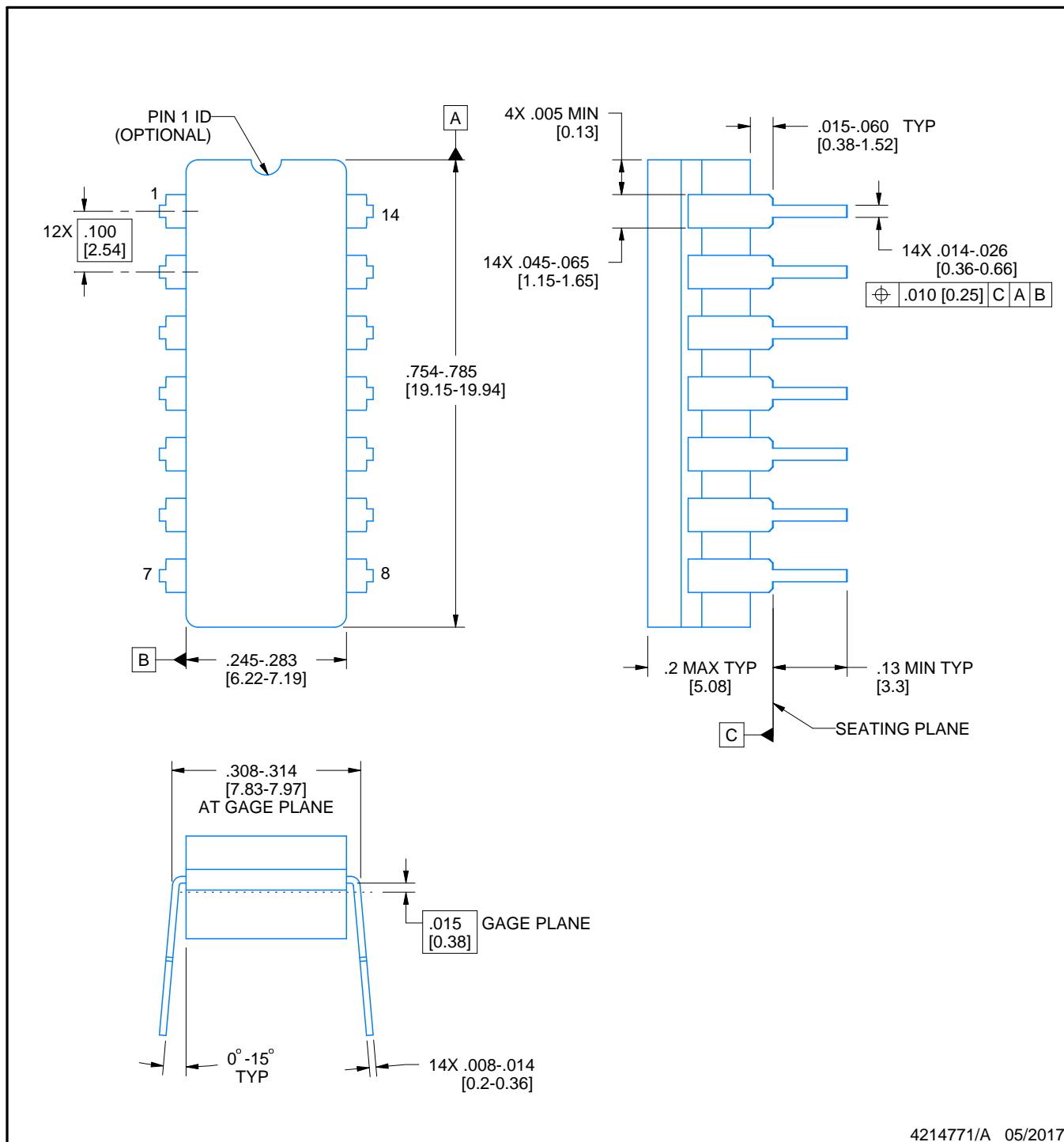


# PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

## NOTES:

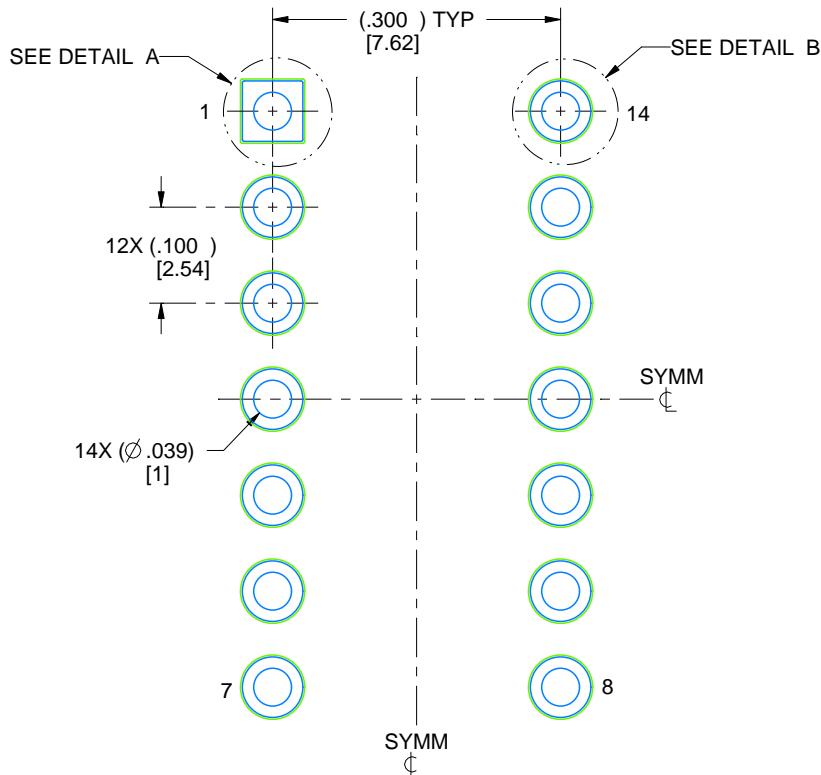
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

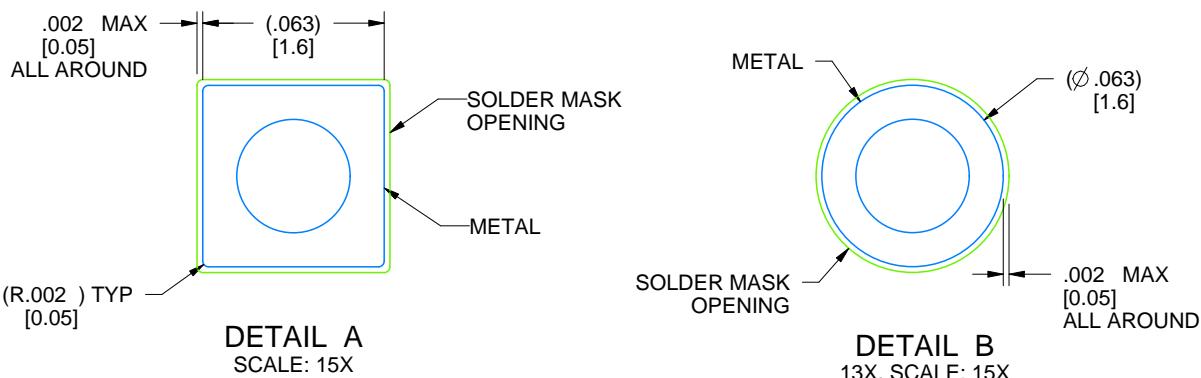
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



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