

## SNx4HC153 Dual 4-Line To 1-Line Data Selectors/Multiplexers

### 1 Features

- Wide operating voltage range of 2 V to 6 V
- Outputs can drive up to 15 LSTTL loads
- Low power consumption, 80- $\mu$ A max  $I_{CC}$
- Typical  $t_{pd} = 9$  ns
- $\pm 6$ -mA output drive at 5 V
- Low input current of 1  $\mu$ A max
- Permit multiplexing from n lines to one line
- Perform parallel-to-serial conversion
- Strobe (enable) line provided for cascading (N lines to n lines)

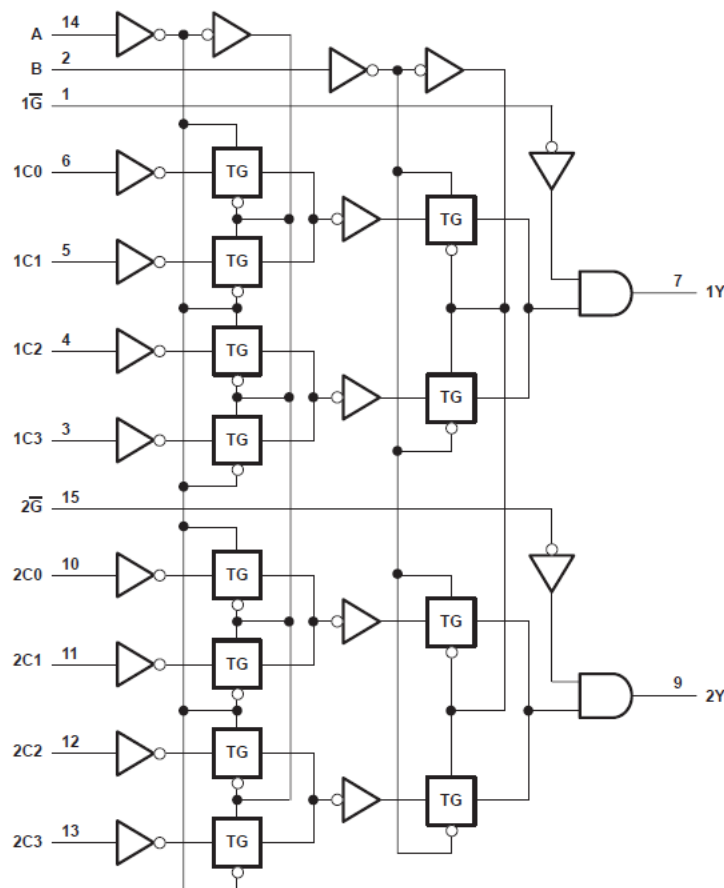
### 2 Description

The SNx4HC153 is a dual data selector/multiplexer containing full binary decoding to select one of four data sources. Both channels are controlled by the same address select inputs, and each channel includes its own strobe ( $\overline{G}$ ) input. A high level at the strobe terminal forces the respective output low.

#### Device Information

| PART NUMBER  | PACKAGE <sup>(1)</sup> | BODY SIZE (NOM)           |
|--------------|------------------------|---------------------------|
| SN74HC153D   | SOIC (16)              | 9.90 mm $\times$ 3.90 mm  |
| SN74HC153N   | PDIP (16)              | 19.31 mm $\times$ 6.35 mm |
| SN74HC153NS  | SO (16)                | 6.20 mm $\times$ 5.30 mm  |
| SN74HC153PW  | TSSOP (16)             | 5.00 mm $\times$ 4.40 mm  |
| SN54HC153J   | CDIP (16)              | 24.38 mm $\times$ 6.92 mm |
| SNJ54HC153FK | LCCC (20)              | 8.89 mm $\times$ 8.45 mm  |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Pin numbers are for the D, J, N, NS, PW, and W packages.

#### Functional Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

## Table of Contents

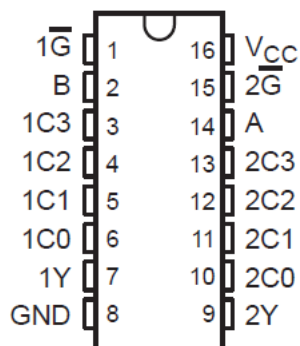
|                                                           |          |                                                                  |           |
|-----------------------------------------------------------|----------|------------------------------------------------------------------|-----------|
| <b>1 Features</b> .....                                   | <b>1</b> | 7.1 Overview.....                                                | <b>8</b>  |
| <b>2 Description</b> .....                                | <b>1</b> | 7.2 Functional Block Diagram.....                                | <b>8</b>  |
| <b>3 Revision History</b> .....                           | <b>2</b> | 7.3 Device Functional Modes.....                                 | <b>9</b>  |
| <b>4 Pin Configuration and Functions</b> .....            | <b>3</b> | <b>8 Power Supply Recommendations</b> .....                      | <b>10</b> |
| <b>5 Specifications</b> .....                             | <b>4</b> | <b>9 Layout</b> .....                                            | <b>10</b> |
| 5.1 Absolute Maximum Ratings.....                         | <b>4</b> | 9.1 Layout Guidelines.....                                       | <b>10</b> |
| 5.2 Recommended Operating Conditions <sup>(1)</sup> ..... | <b>4</b> | <b>10 Device and Documentation Support</b> .....                 | <b>11</b> |
| 5.3 Thermal Information.....                              | <b>4</b> | 10.1 Receiving Notification of Documentation Updates..           | <b>11</b> |
| 5.4 Electrical Characteristics.....                       | <b>5</b> | 10.2 Support Resources.....                                      | <b>11</b> |
| 5.5 Switching Characteristics.....                        | <b>5</b> | 10.3 Trademarks.....                                             | <b>11</b> |
| 5.6 Switching Characteristics.....                        | <b>6</b> | 10.4 Electrostatic Discharge Caution.....                        | <b>11</b> |
| 5.7 Operating Characteristics.....                        | <b>6</b> | 10.5 Glossary.....                                               | <b>11</b> |
| <b>6 Parameter Measurement Information</b> .....          | <b>7</b> | <b>11 Mechanical, Packaging, and Orderable Information</b> ..... | <b>11</b> |
| <b>7 Detailed Description</b> .....                       | <b>8</b> |                                                                  |           |

## 3 Revision History

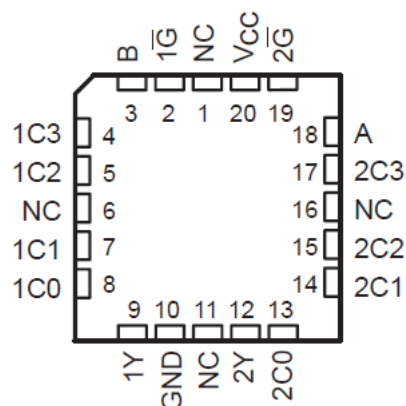
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision D (October 2003) to Revision E (February 2022)</b>                                                                                                                    | <b>Page</b> |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| <ul style="list-style-type: none"> <li>Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards.....</li> </ul> | <b>1</b>    |

## 4 Pin Configuration and Functions



**J, W, D, N, NS, or PW Package**  
**16-Pin CDIP, CFP, SOIC, PDIP, SO, or TSSOP**  
**Top View**



NC - No internal connection

**FK Package**  
**20-Pin LCCC**  
**Top View**

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                                   |                                                        | MIN  | MAX | UNIT |
|------------------|---------------------------------------------------|--------------------------------------------------------|------|-----|------|
| V <sub>CC</sub>  | Supply voltage range                              |                                                        | –0.5 | 7   | V    |
| I <sub>IK</sub>  | Input clamp current <sup>(2)</sup>                | V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub> |      | ±20 | mA   |
| I <sub>OK</sub>  | Output clamp current <sup>(2)</sup>               | V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> |      | ±20 | mA   |
| I <sub>O</sub>   | Continuous output current                         | V <sub>O</sub> = 0 to V <sub>CC</sub>                  |      | ±35 | mA   |
|                  | Continuous current through V <sub>CC</sub> or GND |                                                        |      | ±70 | mA   |
| T <sub>J</sub>   | Junction temperature                              |                                                        |      | 150 | °C   |
| T <sub>stg</sub> | Storage temperature                               |                                                        | –65  | 150 | °C   |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under [Section 5.2](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 Recommended Operating Conditions<sup>(1)</sup>

|                 |                                 |                         | SN54HC153 |     |                 | SN74HC153 |     |                 | UNIT |
|-----------------|---------------------------------|-------------------------|-----------|-----|-----------------|-----------|-----|-----------------|------|
|                 |                                 |                         | MIN       | NOM | MAX             | MIN       | NOM | MAX             |      |
| V <sub>CC</sub> | Supply voltage                  |                         | 2         | 5   | 6               | 2         | 5   | 6               | V    |
| V <sub>IH</sub> | High-level input voltage        | V <sub>CC</sub> = 2 V   | 1.5       |     |                 | 1.5       |     |                 | V    |
|                 |                                 | V <sub>CC</sub> = 4.5 V | 3.15      |     |                 | 3.15      |     |                 |      |
|                 |                                 | V <sub>CC</sub> = 6 V   | 4.2       |     |                 | 4.2       |     |                 |      |
| V <sub>IL</sub> | Low-level input voltage         | V <sub>CC</sub> = 2 V   |           |     | 0.5             |           |     | 0.5             | V    |
|                 |                                 | V <sub>CC</sub> = 4.5 V |           |     | 1.35            |           |     | 1.35            |      |
|                 |                                 | V <sub>CC</sub> = 6 V   |           |     | 1.8             |           |     | 1.8             |      |
| V <sub>I</sub>  | Input voltage                   |                         | 0         |     | V <sub>CC</sub> | 0         |     | V <sub>CC</sub> | V    |
| V <sub>O</sub>  | Output voltage                  |                         | 0         |     | V <sub>CC</sub> | 0         |     | V <sub>CC</sub> | V    |
| Δt/Δv           | Input transition rise/fall time | V <sub>CC</sub> = 2 V   |           |     | 1000            |           |     | 1000            | ns   |
|                 |                                 | V <sub>CC</sub> = 4.5 V |           |     | 500             |           |     | 500             |      |
|                 |                                 | V <sub>CC</sub> = 6 V   |           |     | 400             |           |     | 400             |      |
| T <sub>A</sub>  | Operating free-air temperature  |                         | –55       |     | 125             | –40       |     | 85              | °C   |

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

### 5.3 Thermal Information

|                               |                                        | D (SOIC) | N (PDIP) | NS (SO) | PW (TSSOP) | UNIT |
|-------------------------------|----------------------------------------|----------|----------|---------|------------|------|
| THERMAL METRIC <sup>(1)</sup> |                                        | 16 PINS  | 16 PINS  | 16 PINS | 16 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance | 73       | 67       | 64      | 108        | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

## 5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER       | TEST CONDITIONS <sup>(1)</sup>                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> = 25°C |       |      | SN54HC153 |       | SN74HC153 |       | UNIT |
|-----------------|-----------------------------------------------------------|------------------------|-----------------------|-------|------|-----------|-------|-----------|-------|------|
|                 |                                                           |                        | MIN                   | TYP   | MAX  | MIN       | MAX   | MIN       | MAX   |      |
| V <sub>OH</sub> | I <sub>OH</sub> = -20 µA                                  | 2                      | 1.9                   | 1.998 |      | 1.9       |       | 1.9       |       | V    |
|                 |                                                           | 4.5                    | 4.4                   | 4.499 |      | 4.4       |       | 4.4       |       |      |
|                 |                                                           | 6                      | 5.9                   | 5.999 |      | 5.9       |       | 5.9       |       |      |
|                 | I <sub>OH</sub> = -6 mA                                   | 4.5                    | 3.98                  | 4.3   |      | 3.7       |       | 3.84      |       |      |
|                 | I <sub>OH</sub> = -7.8 mA                                 | 6                      | 5.48                  | 5.8   |      | 5.2       |       | 5.34      |       |      |
| V <sub>OL</sub> | I <sub>OL</sub> = 20 µA                                   | 2                      |                       | 0.002 | 0.1  |           | 0.1   |           | 0.1   | V    |
|                 |                                                           | 4.5                    |                       | 0.001 | 0.1  |           | 0.1   |           | 0.1   |      |
|                 |                                                           | 6                      |                       | 0.001 | 0.1  |           | 0.1   |           | 0.1   |      |
|                 | I <sub>OL</sub> = 6 mA                                    | 4.5                    |                       | 0.17  | 0.26 |           | 0.4   |           | 0.33  |      |
|                 | I <sub>OL</sub> = 7.8 mA                                  | 6                      |                       | 0.15  | 0.26 |           | 0.4   |           | 0.33  |      |
| I <sub>I</sub>  | V <sub>I</sub> = V <sub>CC</sub> or 0                     | 6                      |                       | ±0.1  | ±100 |           | ±1000 |           | ±1000 | nA   |
| I <sub>CC</sub> | V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0 | 6                      |                       |       | 8    |           | 160   |           | 80    | µA   |
| C <sub>i</sub>  |                                                           | 2 to 6                 |                       | 3     | 10   |           | 10    |           | 10    | pF   |

(1) V<sub>I</sub> = V<sub>IH</sub> or V<sub>IL</sub>, unless otherwise noted.

## 5.5 Switching Characteristics

over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see [Figure 6](#))

| PARAMETER       | FROM<br>(INPUT) | TO<br>(OUTPUT) | V <sub>CC</sub> (V) | T <sub>A</sub> = 25°C |     |     | SN54HC153 |     | SN74HC153 |     | UNIT |
|-----------------|-----------------|----------------|---------------------|-----------------------|-----|-----|-----------|-----|-----------|-----|------|
|                 |                 |                |                     | MIN                   | TYP | MAX | MIN       | MAX | MIN       | MAX |      |
| t <sub>pd</sub> | A or B          | Y              | 2                   |                       | 90  | 150 |           | 225 |           | 190 | ns   |
|                 |                 |                | 4.5                 |                       | 21  | 30  |           | 45  |           | 38  |      |
|                 |                 |                | 6                   |                       | 17  | 26  |           | 38  |           | 32  |      |
|                 | Data<br>(Any C) | Y              | 2                   |                       | 73  | 126 |           | 189 |           | 158 |      |
|                 |                 |                | 4.5                 |                       | 17  | 28  |           | 42  |           | 35  |      |
|                 |                 |                | 6                   |                       | 14  | 23  |           | 35  |           | 29  |      |
|                 | $\overline{G}$  | Y              | 2                   |                       | 38  | 95  |           | 150 |           | 125 |      |
|                 |                 |                | 4.5                 |                       | 11  | 19  |           | 28  |           | 24  |      |
|                 |                 |                | 6                   |                       | 9   | 16  |           | 24  |           | 20  |      |
| t <sub>t</sub>  |                 | Y              | 2                   |                       | 20  | 60  |           | 90  |           | 75  | ns   |
|                 |                 |                | 4.5                 |                       | 8   | 12  |           | 18  |           | 15  |      |
|                 |                 |                | 6                   |                       | 6   | 10  |           | 15  |           | 13  |      |

## 5.6 Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 150$  pF (unless otherwise noted) (see [Figure 6](#))

| PARAMETER | FROM<br>(INPUT) | TO<br>(OUTPUT) | $V_{CC}$ (V) | $T_A = 25^\circ\text{C}$ |     |     | SN54HC153 |     | SN74HC153 |     | UNIT |
|-----------|-----------------|----------------|--------------|--------------------------|-----|-----|-----------|-----|-----------|-----|------|
|           |                 |                |              | MIN                      | TYP | MAX | MIN       | MAX | MIN       | MAX |      |
| $t_{pd}$  | A or B          | Y              | 2            |                          | 105 | 235 |           | 355 |           | 295 | ns   |
|           |                 |                | 4.5          |                          | 27  | 47  |           | 71  |           | 59  |      |
|           |                 |                | 6            |                          | 21  | 41  |           | 60  |           | 51  |      |
|           | Data<br>(Any C) | Y              | 2            |                          | 93  | 220 |           | 335 |           | 274 |      |
|           |                 |                | 4.5          |                          | 23  | 44  |           | 67  |           | 55  |      |
|           |                 |                | 6            |                          | 19  | 38  |           | 57  |           | 48  |      |
|           | $\overline{G}$  | Y              | 2            |                          | 60  | 185 |           | 280 |           | 230 |      |
|           |                 |                | 4.5          |                          | 17  | 37  |           | 56  |           | 46  |      |
|           |                 |                | 6            |                          | 14  | 32  |           | 48  |           | 40  |      |
| $t_t$     |                 | Y              | 2            |                          | 45  | 210 |           | 315 |           | 265 | ns   |
|           |                 |                | 4.5          |                          | 17  | 42  |           | 63  |           | 53  |      |
|           |                 |                | 6            |                          | 13  | 36  |           | 53  |           | 45  |      |

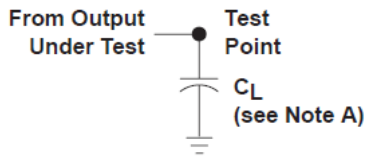
## 5.7 Operating Characteristics

$T_A = 25^\circ\text{C}$

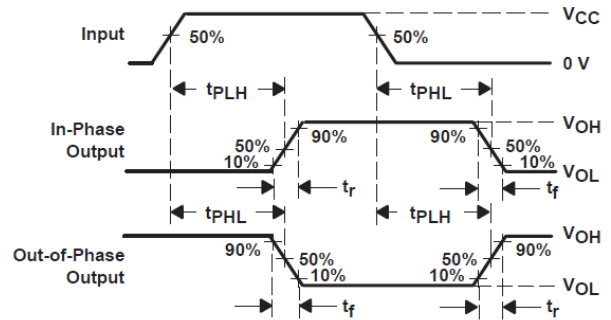
| PARAMETER |                                               | TEST CONDITIONS | TYP | UNIT |
|-----------|-----------------------------------------------|-----------------|-----|------|
| $C_{pd}$  | Power dissipation capacitance per multiplexer | No load         | 40  | pF   |

## 6 Parameter Measurement Information

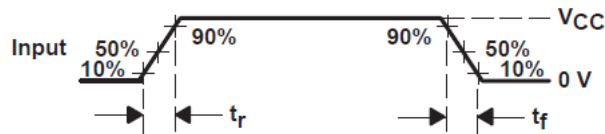
$t_{pd}$  is the maximum between  $t_{PLH}$  and  $t_{PHL}$



**Figure 6-1. Load Circuit**



**Figure 6-2. Voltage Waveforms**  
Propagation Delay and Output Transition Times



**Figure 6-3. Voltage Waveform**  
Input Rise and Fall Times

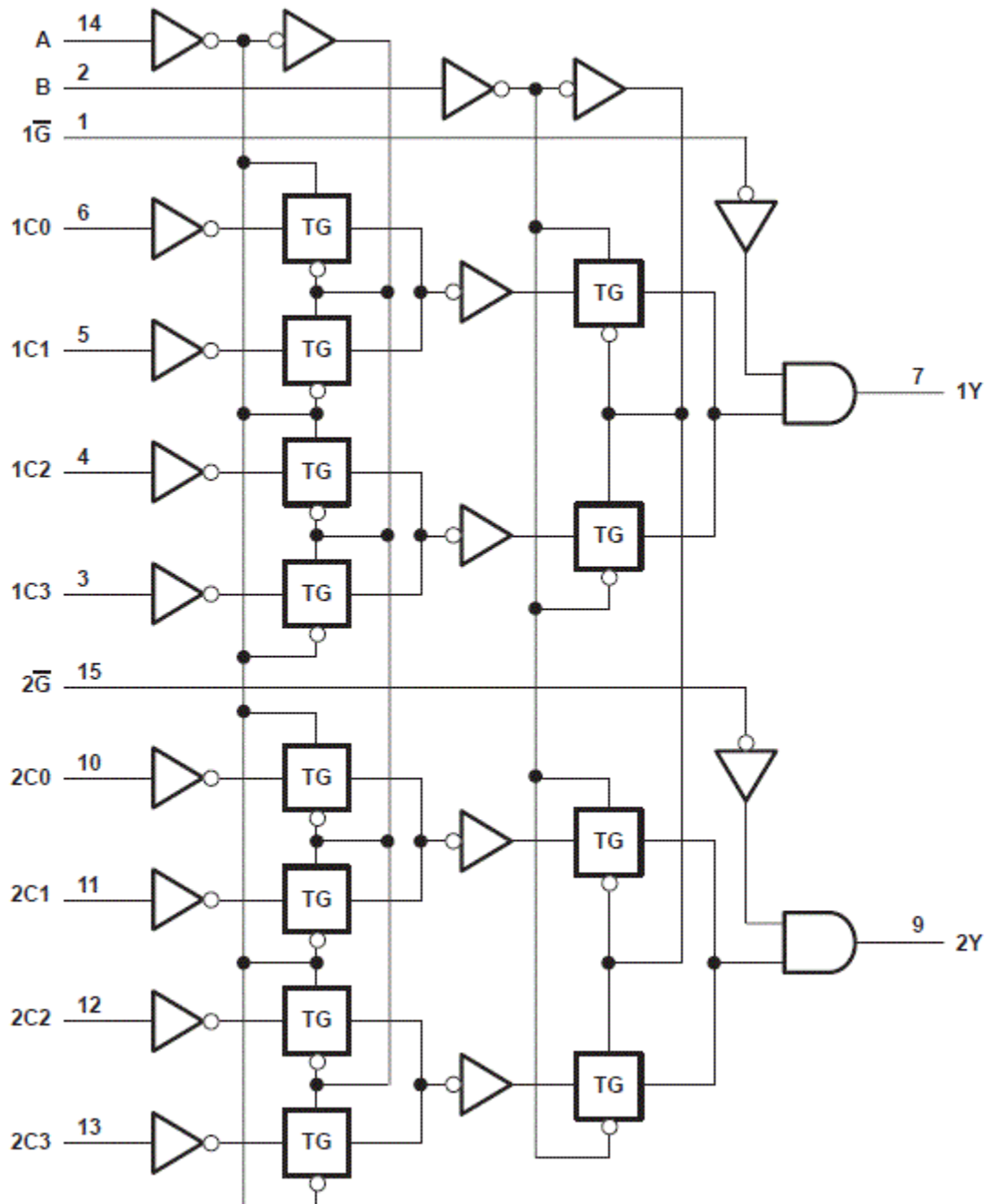
- A.  $C_L$  includes probe and jig capacitance.
- B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
- C. The outputs are measured one at a time with one input transition per measurement.

## 7 Detailed Description

### 7.1 Overview

Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate strobe ( $\overline{G}$ ) inputs are provided for each of the two 4-line sections.

### 7.2 Functional Block Diagram



Pin numbers are for the D, J, N, NS, PW, and W packages.



## 7.3 Device Functional Modes

| INPUTS                |   |      |    |    |    |                | OUTPUT Y |
|-----------------------|---|------|----|----|----|----------------|----------|
| SELECT <sup>(1)</sup> |   | DATA |    |    |    | $\overline{G}$ |          |
| B                     | A | C0   | C1 | C2 | C3 |                |          |
| X                     | X | X    | X  | X  | X  | H              | L        |
| L                     | L | L    | X  | X  | X  | L              | L        |
| L                     | L | H    | X  | X  | X  | L              | H        |
| L                     | H | X    | L  | X  | X  | L              | L        |
| L                     | H | X    | H  | X  | X  | L              | H        |
| H                     | L | X    | X  | L  | X  | L              | L        |
| H                     | L | X    | X  | H  | X  | L              | H        |
| H                     | H | X    | X  | X  | L  | L              | L        |
| H                     | H | X    | X  | X  | H  | L              | H        |

(1) Select inputs A and B are common to both sections.

## 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 9 Layout

### 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)                |
|---------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|------------------------------------|
| <a href="#">5962-8409301VEA</a> | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8409301VE<br>A<br>SNV54HC153J |
| 5962-8409301VEA.A               | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8409301VE<br>A<br>SNV54HC153J |
| <a href="#">5962-8409301VFA</a> | Active        | Production           | CFP (W)   16    | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8409301VF<br>A<br>SNV54HC153W |
| 5962-8409301VFA.A               | Active        | Production           | CFP (W)   16    | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-8409301VF<br>A<br>SNV54HC153W |
| <a href="#">84093012A</a>       | Active        | Production           | LCCC (FK)   20  | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 84093012A<br>SNJ54HC<br>153FK      |
| <a href="#">8409301EA</a>       | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8409301EA<br>SNJ54HC153J           |
| <a href="#">SN54HC153J</a>      | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | SN54HC153J                         |
| SN54HC153J.A                    | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | SN54HC153J                         |
| <a href="#">SN74HC153D</a>      | Obsolete      | Production           | SOIC (D)   16   | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | HC153                              |
| <a href="#">SN74HC153DR</a>     | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 85    | HC153                              |
| SN74HC153DR.A                   | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HC153                              |
| SN74HC153DR1G4                  | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HC153                              |
| SN74HC153DR1G4.A                | Active        | Production           | SOIC (D)   16   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HC153                              |
| <a href="#">SN74HC153N</a>      | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN74HC153N                         |
| SN74HC153N.A                    | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN74HC153N                         |
| SN74HC153NE4                    | Active        | Production           | PDIP (N)   16   | 25   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN74HC153N                         |
| <a href="#">SN74HC153NSR</a>    | Active        | Production           | SOP (NS)   16   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HC153                              |
| SN74HC153NSR.A                  | Active        | Production           | SOP (NS)   16   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HC153                              |
| <a href="#">SN74HC153PW</a>     | Obsolete      | Production           | TSSOP (PW)   16 | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | HC153                              |
| <a href="#">SN74HC153PWR</a>    | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 85    | HC153                              |
| SN74HC153PWR.A                  | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HC153                              |

| Orderable part number          | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)           |
|--------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-------------------------------|
| <a href="#">SN74HC153PWRG4</a> | Active        | Production           | TSSOP (PW)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | HC153                         |
| <a href="#">SNJ54HC153FK</a>   | Active        | Production           | LCCC (FK)   20  | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 84093012A<br>SNJ54HC<br>153FK |
| SNJ54HC153FK.A                 | Active        | Production           | LCCC (FK)   20  | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 84093012A<br>SNJ54HC<br>153FK |
| <a href="#">SNJ54HC153J</a>    | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8409301EA<br>SNJ54HC153J      |
| SNJ54HC153J.A                  | Active        | Production           | CDIP (J)   16   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 8409301EA<br>SNJ54HC153J      |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

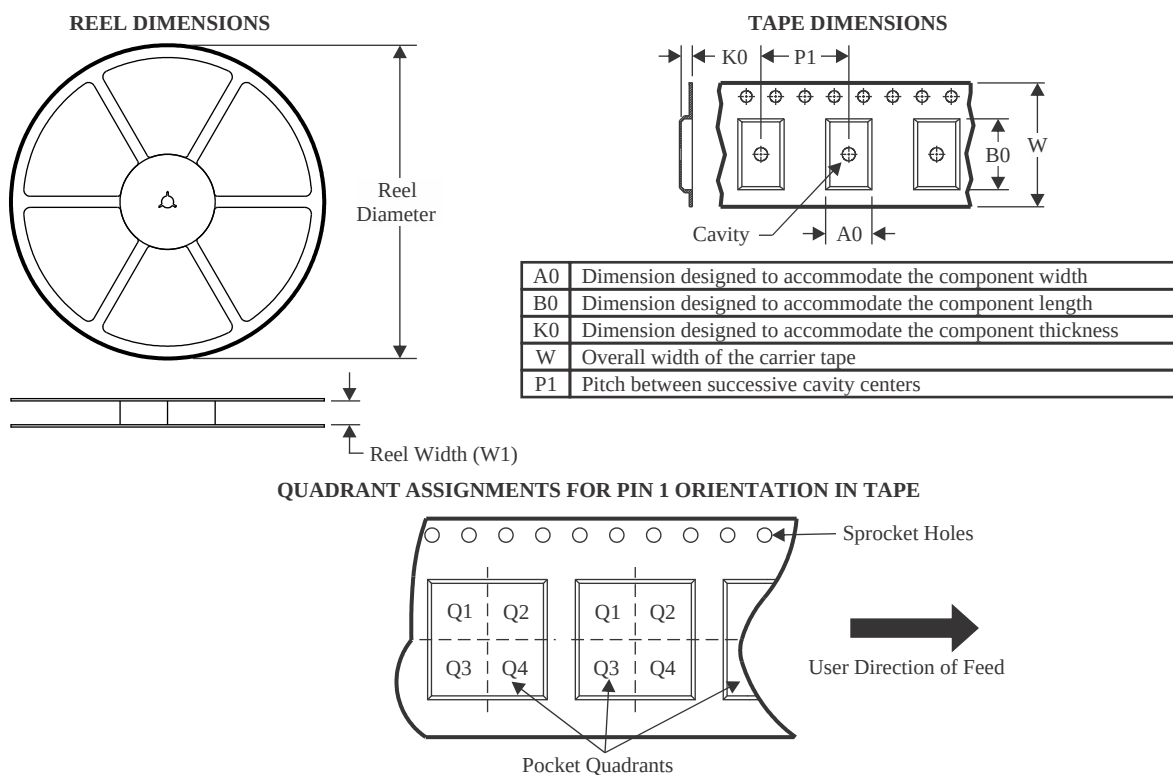
**OTHER QUALIFIED VERSIONS OF SN54HC153, SN54HC153-SP, SN74HC153 :**

- Catalog : [SN74HC153, SN54HC153](#)
- Military : [SN54HC153](#)
- Space : [SN54HC153-SP](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

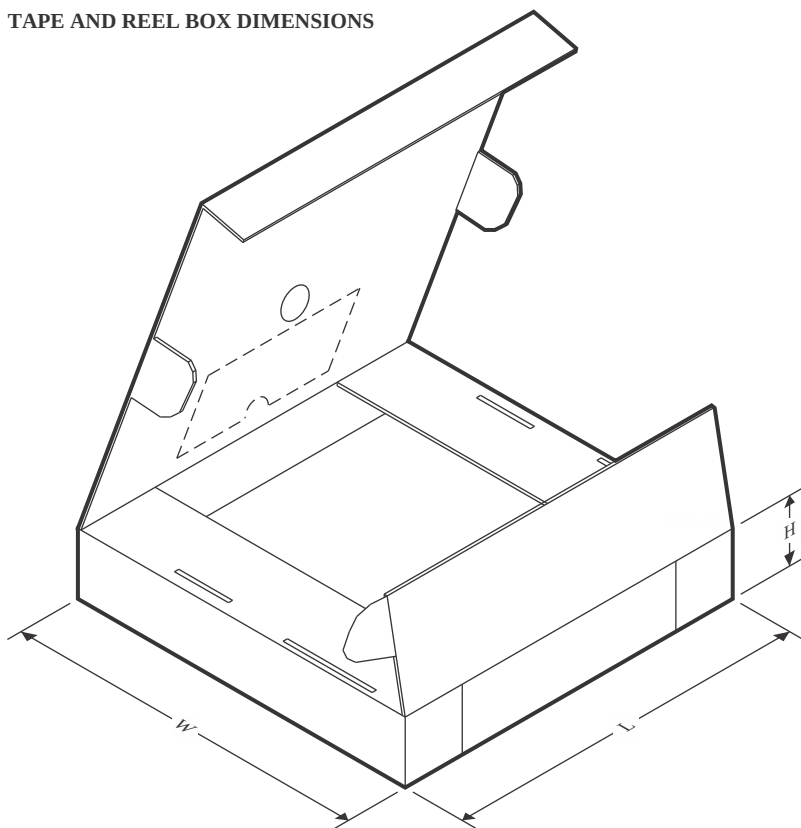
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC153DR    | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| SN74HC153DR1G4 | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| SN74HC153NSR   | SOP          | NS              | 16   | 2000 | 330.0              | 16.4               | 8.1     | 10.4    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74HC153PWR   | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74HC153PWR   | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74HC153PWRG4 | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS

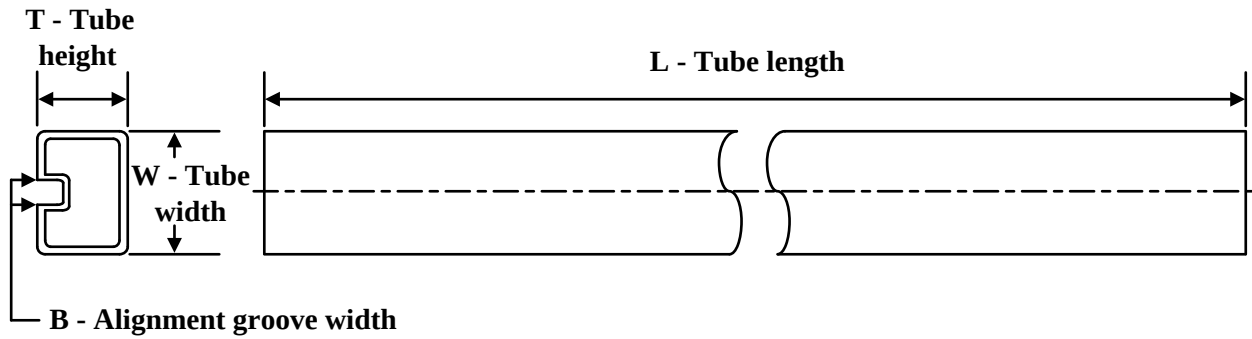


\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC153DR    | SOIC         | D               | 16   | 2500 | 353.0       | 353.0      | 32.0        |
| SN74HC153DR1G4 | SOIC         | D               | 16   | 2500 | 353.0       | 353.0      | 32.0        |
| SN74HC153NSR   | SOP          | NS              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74HC153PWR   | TSSOP        | PW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74HC153PWR   | TSSOP        | PW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |
| SN74HC153PWRG4 | TSSOP        | PW              | 16   | 2000 | 356.0       | 356.0      | 35.0        |

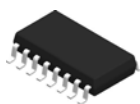


## TUBE



\*All dimensions are nominal

| Device            | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-8409301VFA   | W            | CFP          | 16   | 25  | 506.98 | 26.16  | 6220   | NA     |
| 5962-8409301VFA.A | W            | CFP          | 16   | 25  | 506.98 | 26.16  | 6220   | NA     |
| 84093012A         | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| SN74HC153N        | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74HC153N        | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74HC153N.A      | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74HC153N.A      | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74HC153NE4      | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SN74HC153NE4      | N            | PDIP         | 16   | 25  | 506    | 13.97  | 11230  | 4.32   |
| SNJ54HC153FK      | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| SNJ54HC153FK.A    | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |

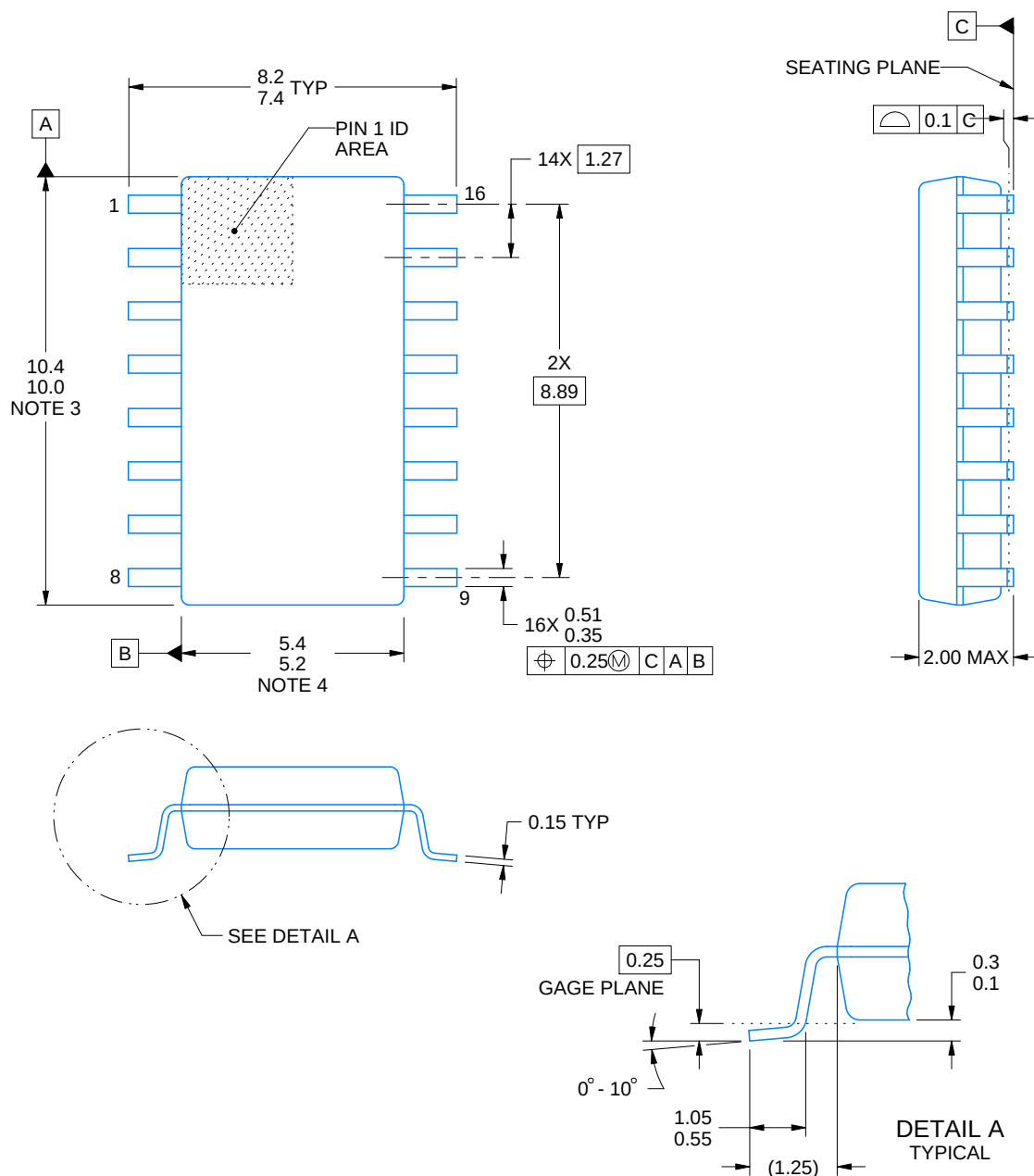


# PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP

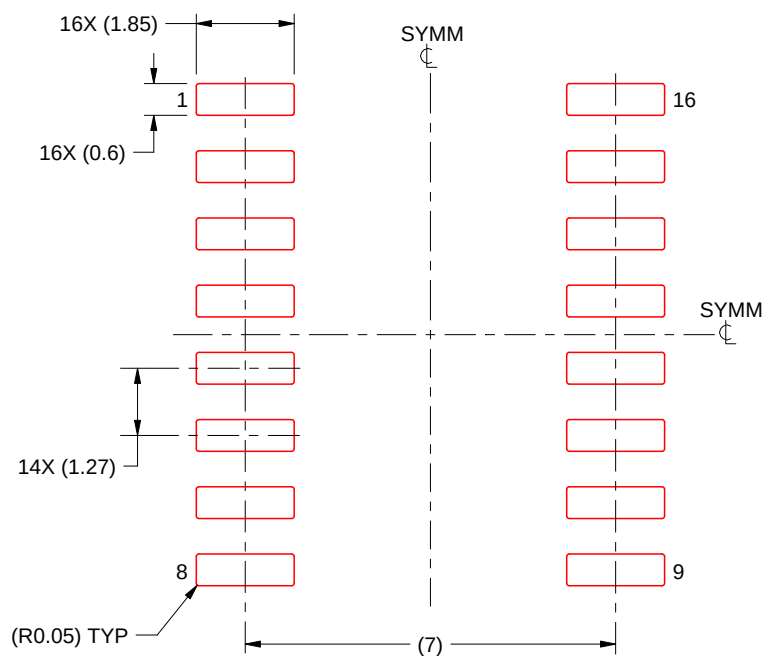


4220735/A 12/2021

## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.





SOLDER PASTE EXAMPLE  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE:7X

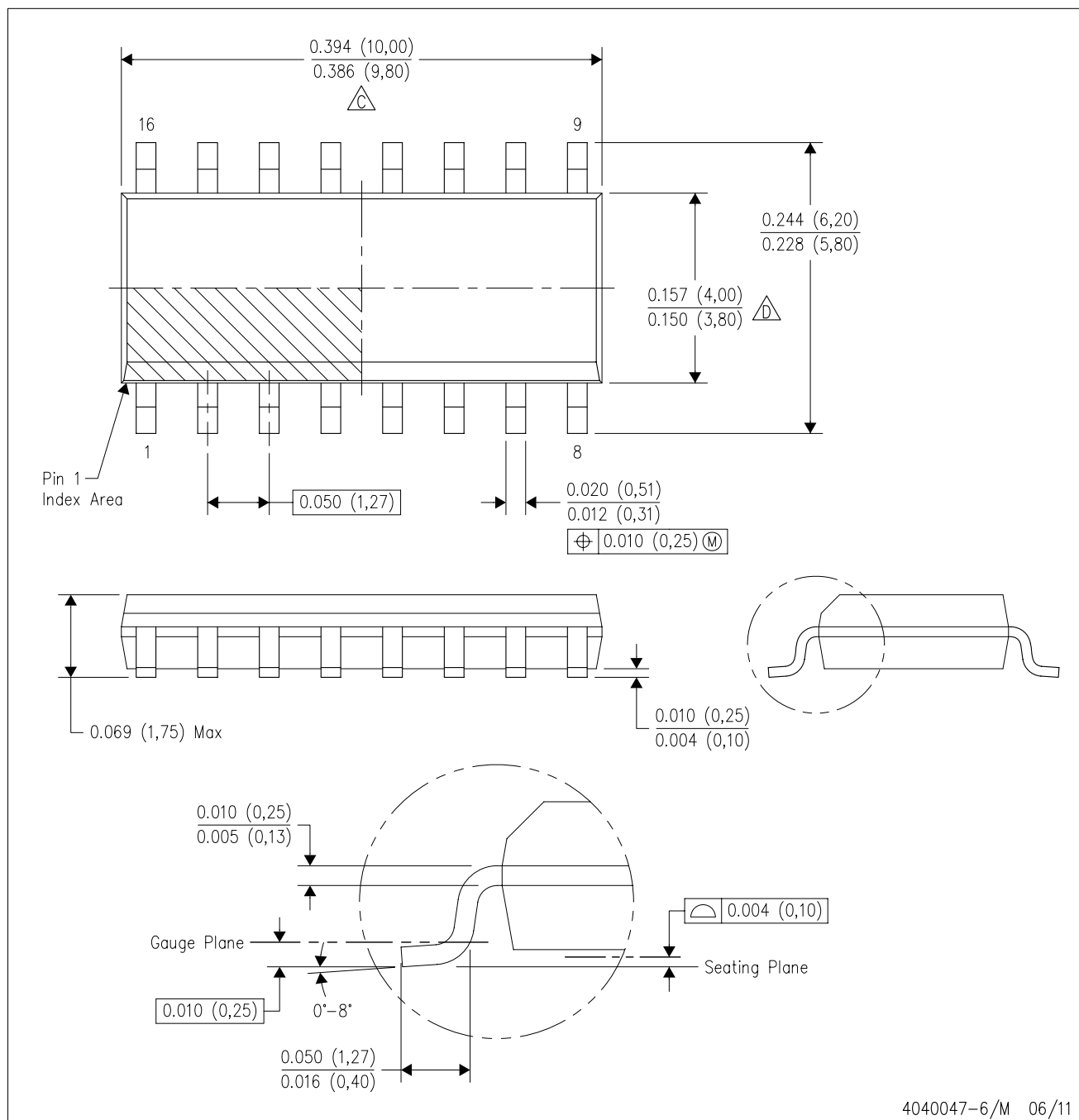
4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

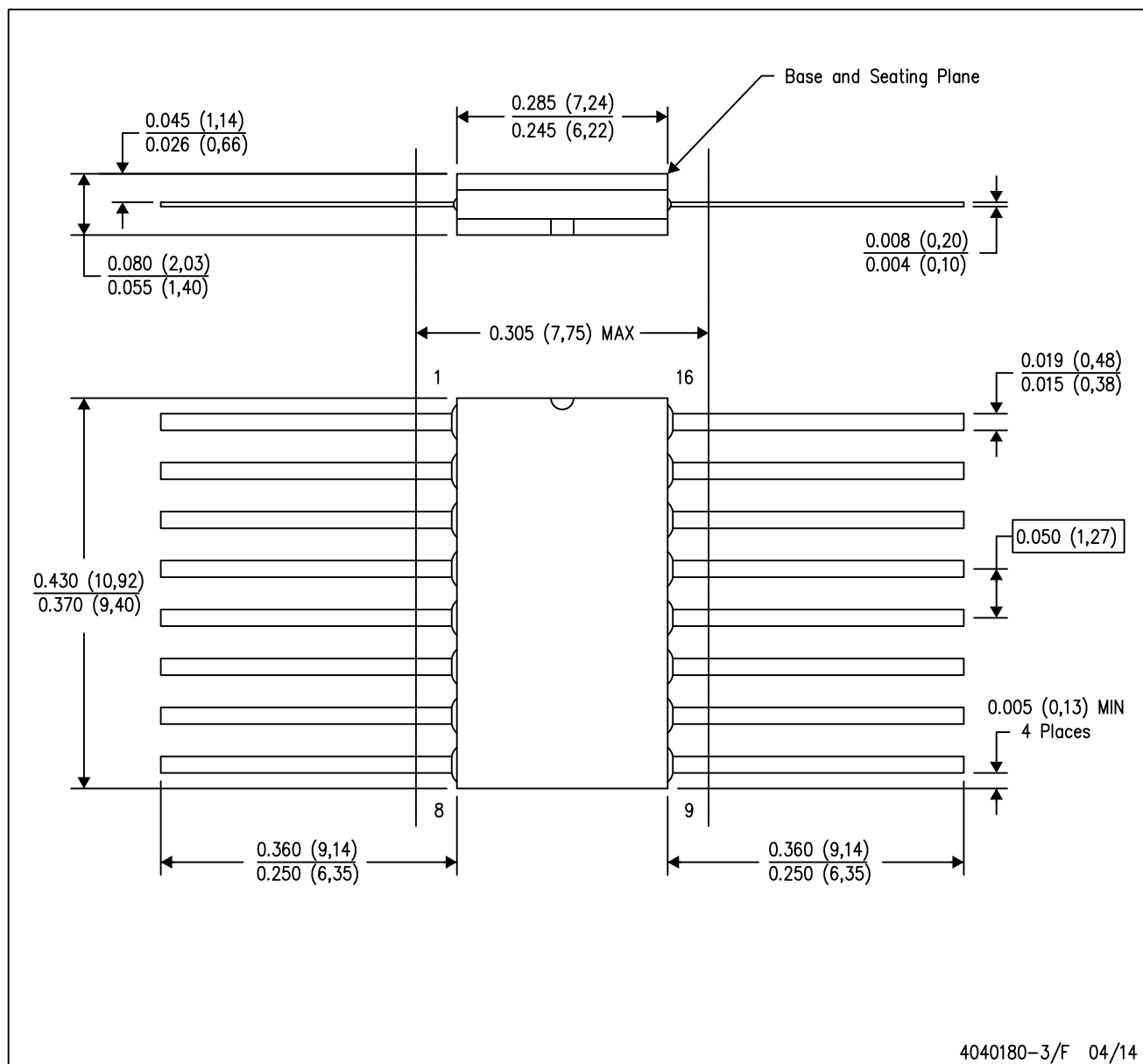
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within MIL STD 1835 GDFP2-F16

## GENERIC PACKAGE VIEW

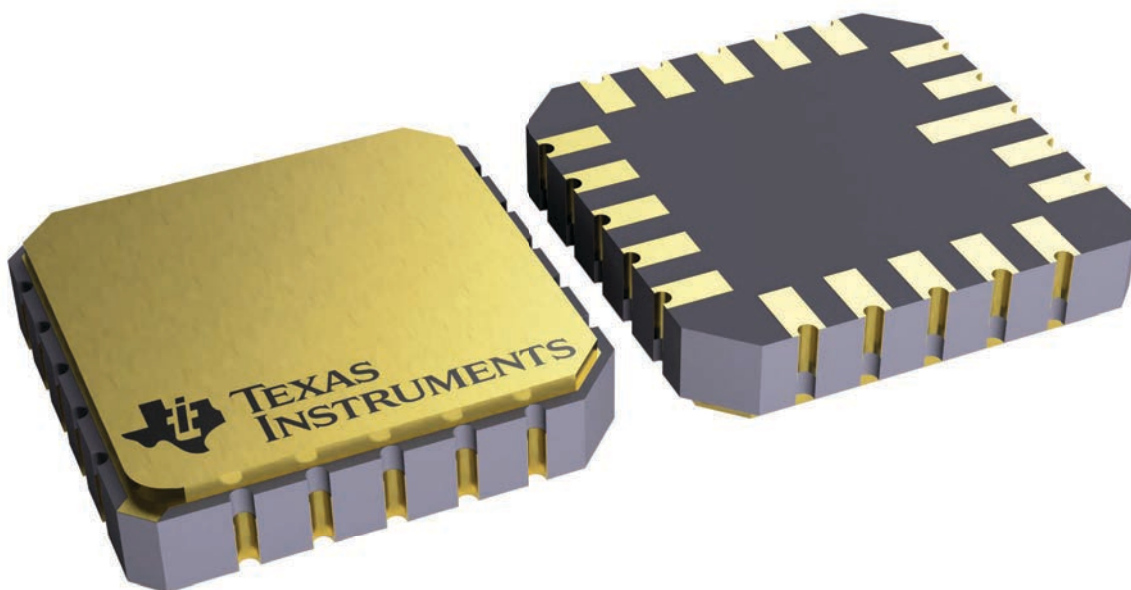
**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

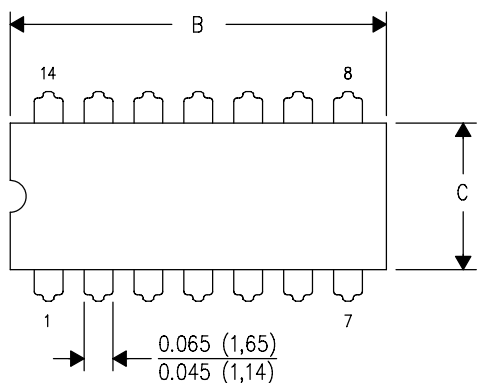


4229370VA\

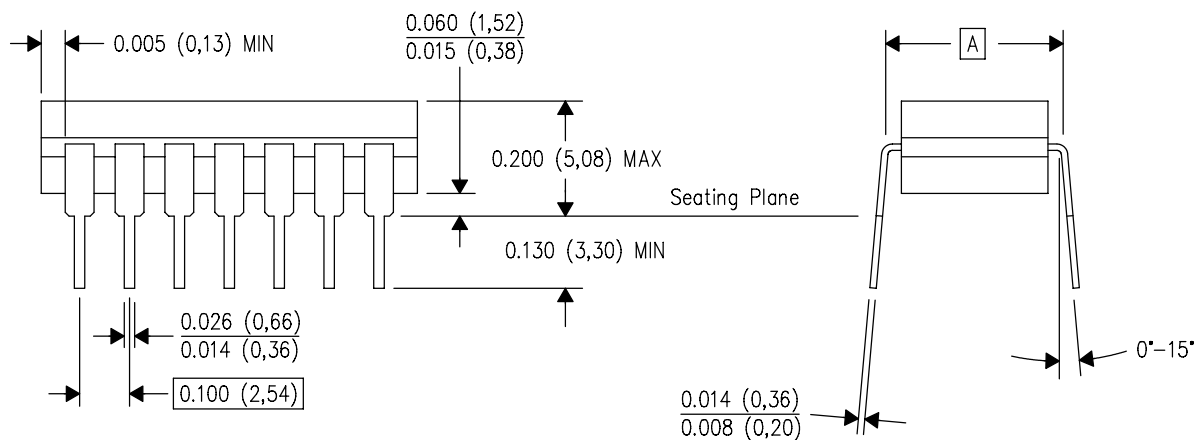
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



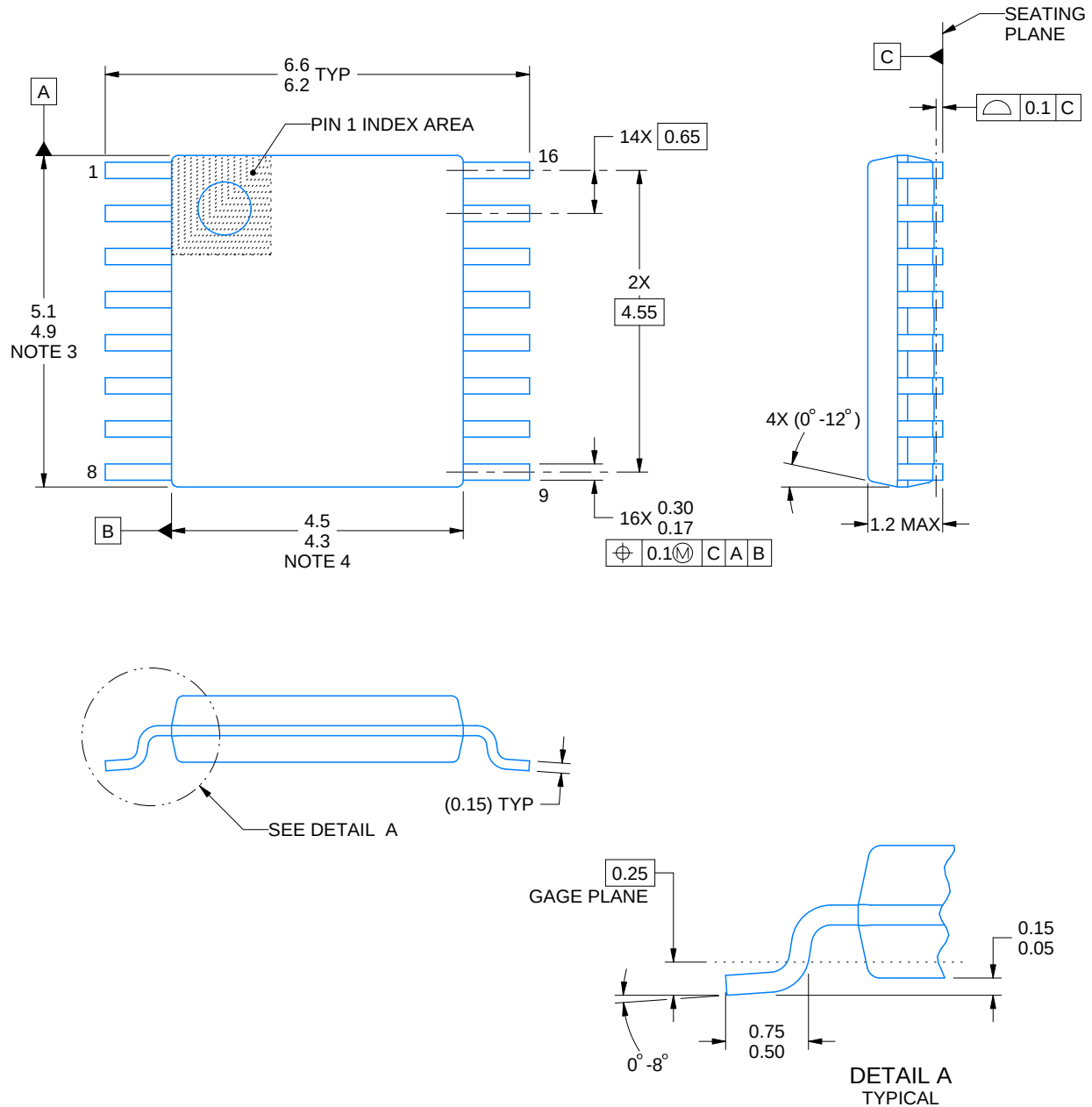
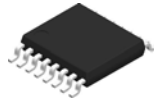
| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.





4220204/B 12/2023

## NOTES:

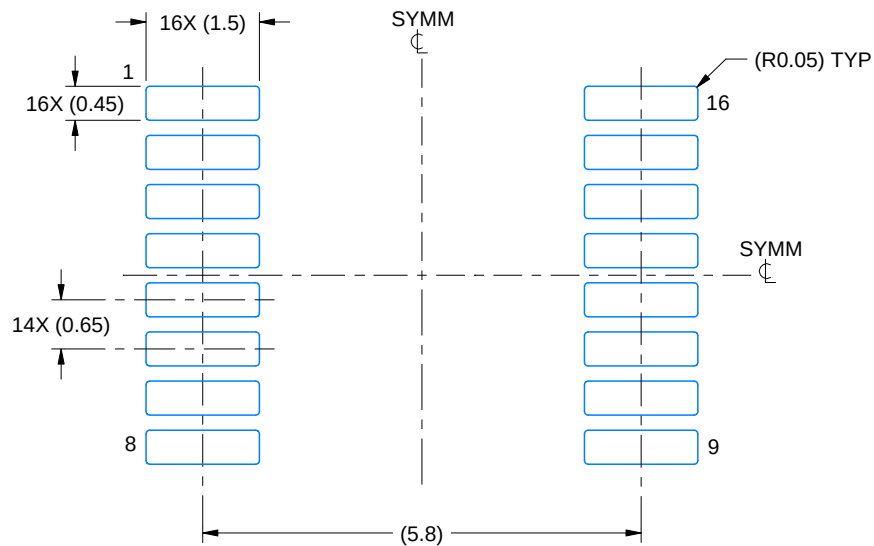
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

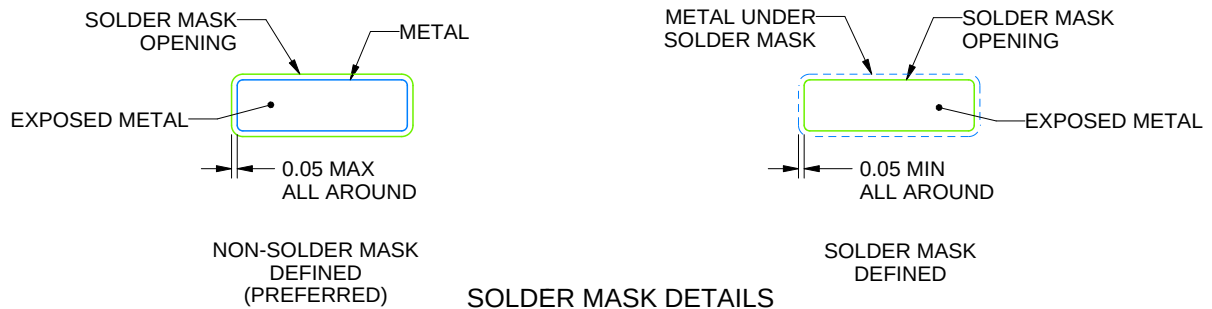
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

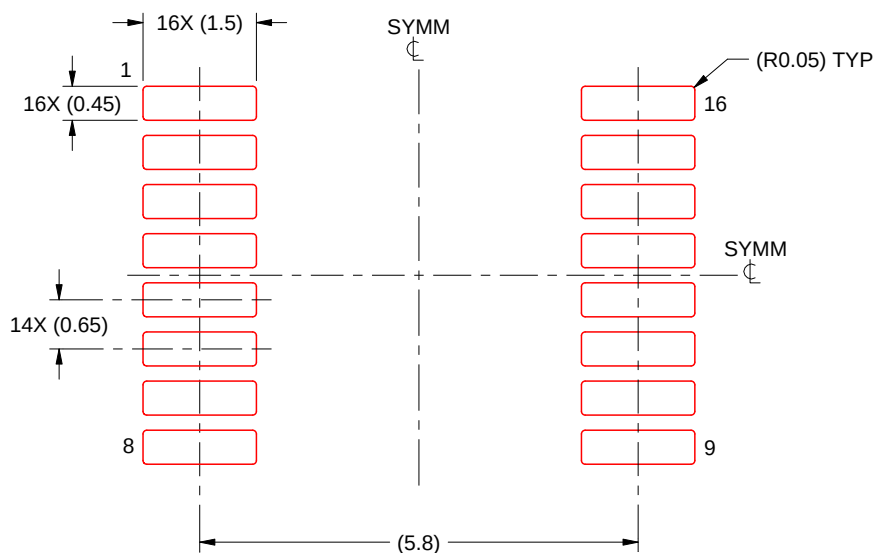
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/B 12/2023

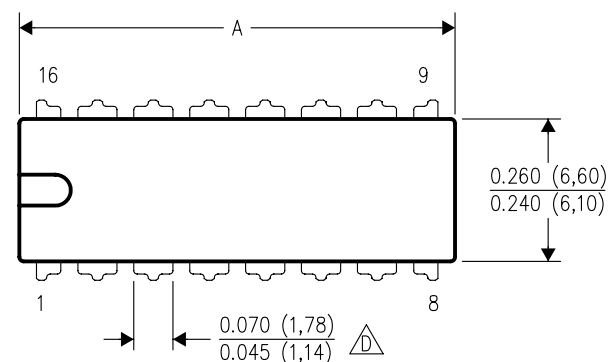
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

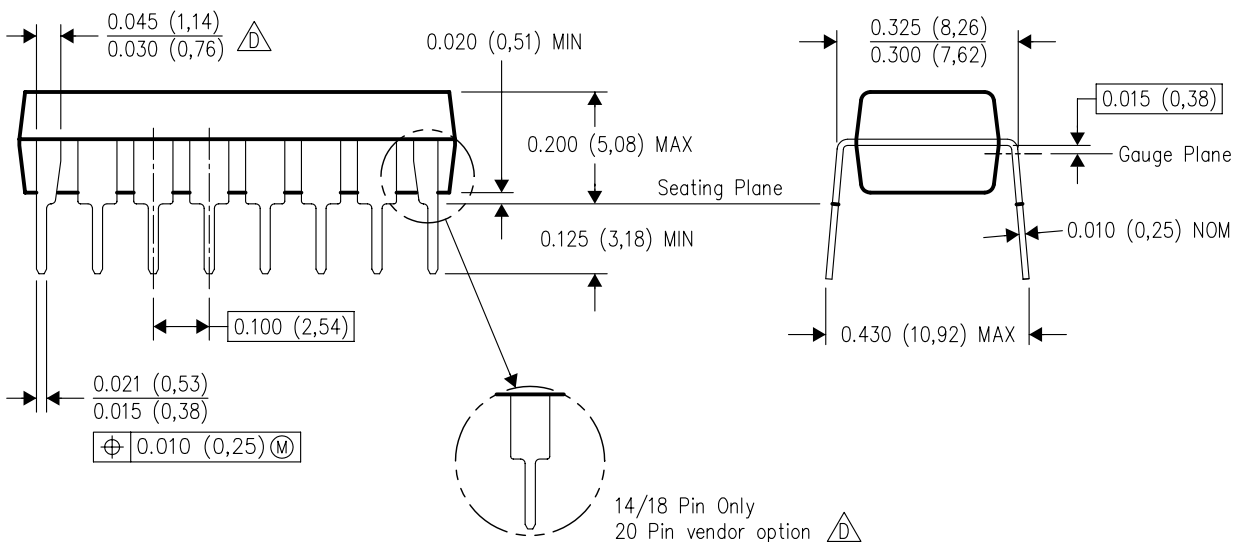
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| DIM \ PINS **       | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025