SN75157 Dual Differential Line Receiver

1 Features

- Meets or exceeds the requirements of ANSI standards EIA/TIA-422-B and EIA/TIA-423-B and ITU recommendation V.10 and V.11
- Operates from single 5V power supply
- Wide common-mode voltage range
- High input impedance
- TTL-compatible outputs
- High-speed schottky circuitry
- 8-Pin dual-in-line package

2 Applications

- Factory automation
- AC and servo motor drives

3 Description

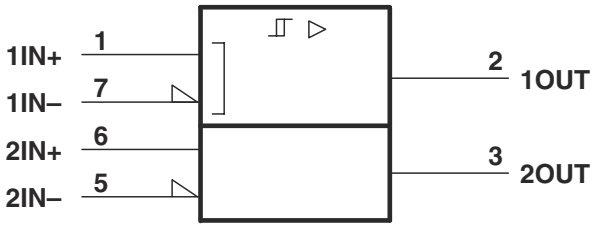
The SN75157 is a dual differential line receiver designed to meet standards EIA/TIA-422-B and EIA/TIA-423-B and ITU V.10 and V.11. The device uses Schottky circuitry, and has TTL-compatible outputs. The inputs are compatible with either a single-ended or a differential-line system. The device operates from a single 5V power supply and is supplied in 8-pin dual-in-line and small-outline packages.

The SN75157 is characterized for operation from 0°C to 70°C.

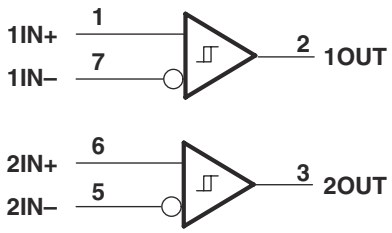
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN75157	SOIC (D, 8)	4.9mm × 6mm
	PDIP (P, 8)	9.81mm × 9.43mm
	SOP (PS, 8)	6.2mm × 7.8mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Symbol†



Logic Diagram (Positive Logic)

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Table of Contents

4 Pin Configuration and Functions

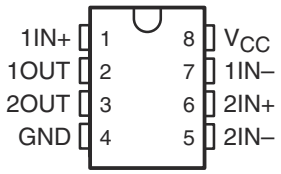


Figure 4-1. D, P, OR PS Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1IN+	1	I	Non-Inverting Differential Input for Channel 1's Differential Receiver
1OUT	2	O	Single Ended Output for Channel 1 Differential Receiver
2OUT	3	O	Single Ended Output for Channel 2 Differential Receiver
GND	4	GND	Device Ground
2IN-	5	I	Inverting Differential Input for Channel 2's Differential Receiver
2IN+	6	I	Non-Inverting Differential Input for Channel 2's Differential Receiver
1IN-	7	I	Inverting Differential Input for Channel 1's Differential Receiver
V_{CC}	8	POW	5V (+/-5%) Positive Supply Connection Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, POW = Power, GND = Ground.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)	–0.5	7	V
V_I	Input voltage range		±15	V
V_{ID}	Differential input voltage(3)		±15	v
V_O	Output voltage range(2)	–0.5	5.5	V
I_{OL}	Low-level output current		50	mA
	Continuous total dissipation		See Dissipation Ratings	
T_J	Operating free-air temperature range	0	70	°C
T_{stg}	Storage temperature range	–65	150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 s		260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential input voltage, are with respect to the network ground terminal.
(3) Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

5.2 Dissipation Ratings

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A \le 70°C$ POWER RATING
D	725mW	5.8mW/°C	464mW
P	1000mW	8.0mW/°C	640mW
PS	450mW	3.6mW/°C	288mW

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IC}	Common-mode input voltage			±7	V
T_A	Operating free-air temperature	0	25	70	°C

5.4 Thermal Resistance Characteristics

THERMAL METRIC(1)		D (SOIC)	P (PIDP)	PS (SOP)	UNIT
		8 Pins	8 Pins	8 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	84.3	89.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	65.4	46.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	62.1	50.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	31.3	23.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.6	60.4	60.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Electrical Characteristics

over recommended ranges of supply voltage,common-mode input voltage, and operating free-air temperature (unless otherwise noted)(4)

PARAMETER		TEST CONDITIONS		MIN	TYP(5)	MAX	UNIT
V_{IT}	Input threshold voltage (V_{IT+} and $V_{IT–}$)(2)			–0.2		0.2	V
				–0.4		0.4	
V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT–}$)				70		mV
V_{OH}	High-level output voltage	V_{ID} = 0.2V,	I_O = –1mA	2.5	3.5		V
V_{OL}	Low-level output voltage	V_{ID} = –0.2V,	I_O = 20mA		0.35	0.5	V
I_I	Input current(3)	V_{CC} = 0 to 5.5V,	V_I = 10V		1.1	3.25	mA
			V_I = –1 V		–1.6	–3.25	
I_{OS}	Short-circuit output current(1)	V_O = 0V,	V_{ID} = 0.2V	–40	–75	–100	mA
I_{CC}	Supply current	V_{ID} = –0.5V,	No load		35	50	mA

(1) Only one output should be shorted at a time and duration of the short circuit should not exceed one second.
(2) The expanded threshold parameter is tested with a 500-W resistor in series with each input.
(3) The input not under test is grounded.
(4) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
(5) All typical values are at V_{CC} = 5 V, T_A = 25°C.

5.6 Switching Characteristics

V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 15pF, see Figure 6-1		15	25	ns
t_{PHL}	Propagation delay time,high- to low-level output			13	25	ns

5.7 Typical Characteristics

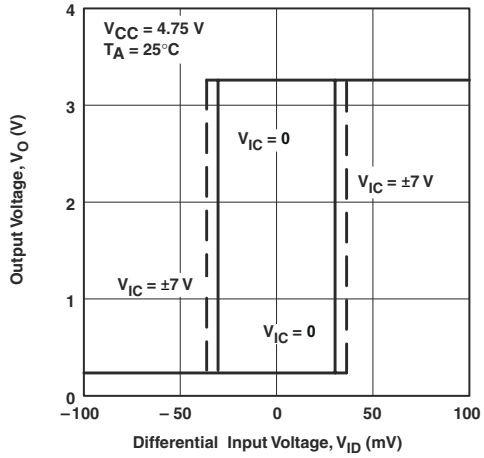


Figure 5-1. Output Voltage vs Differential Input Voltage

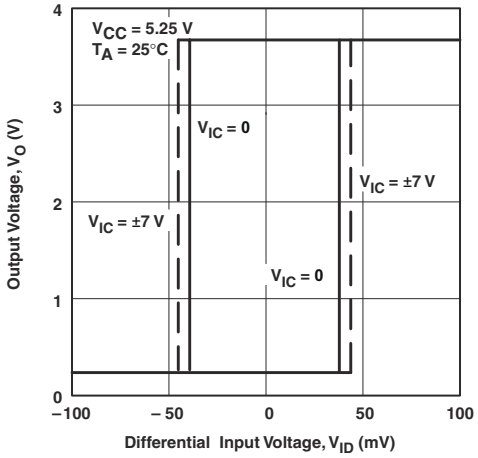


Figure 5-2. Output Voltage vs Differential Input Voltage

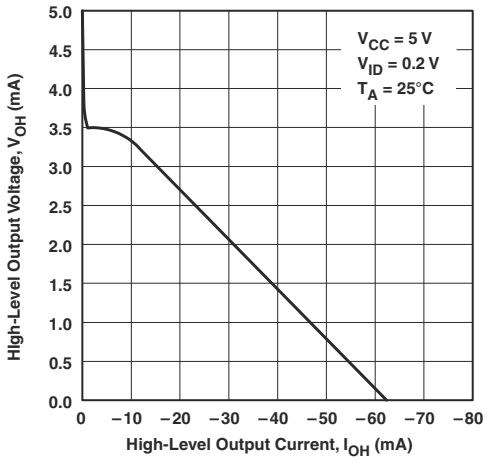


Figure 5-3. High-Level Output Voltage vs High-Level Output Current

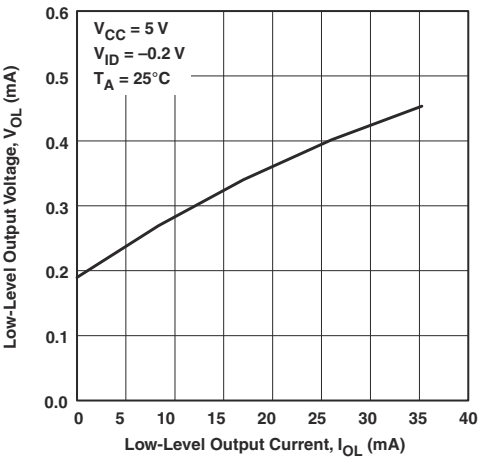


Figure 5-4. Low-Level Output Voltage vs Low-Level Output Current

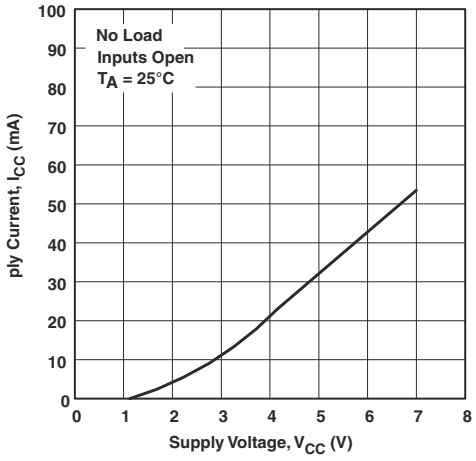
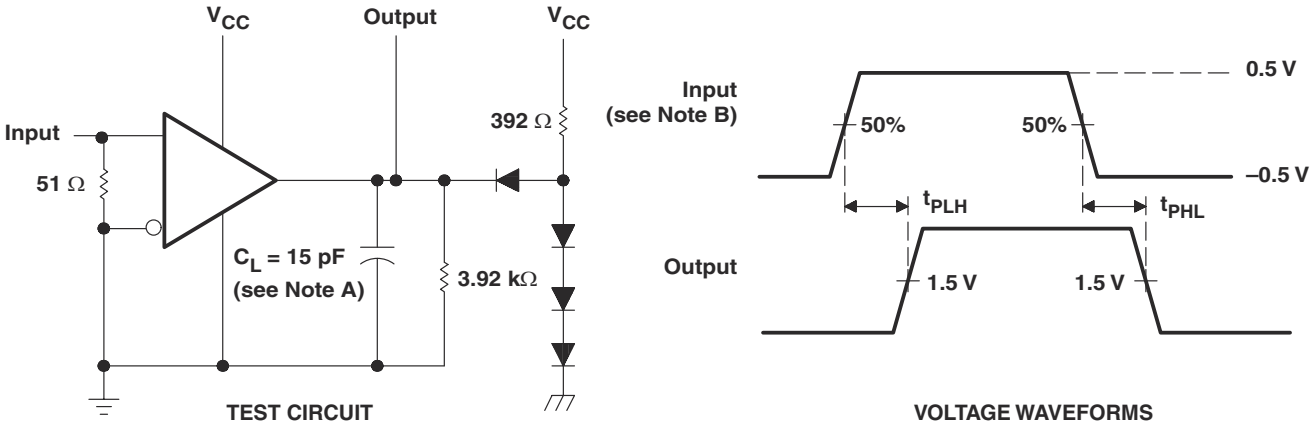


Figure 5-5. Supply Current vs Supply Voltage

Parameter Measurement Information



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR ≤ 5 MHz, duty cycle = 50%.

Figure 6-1. Test Circuit and Voltage Waveforms

6 Detailed Description

6.1 Device Functional Modes

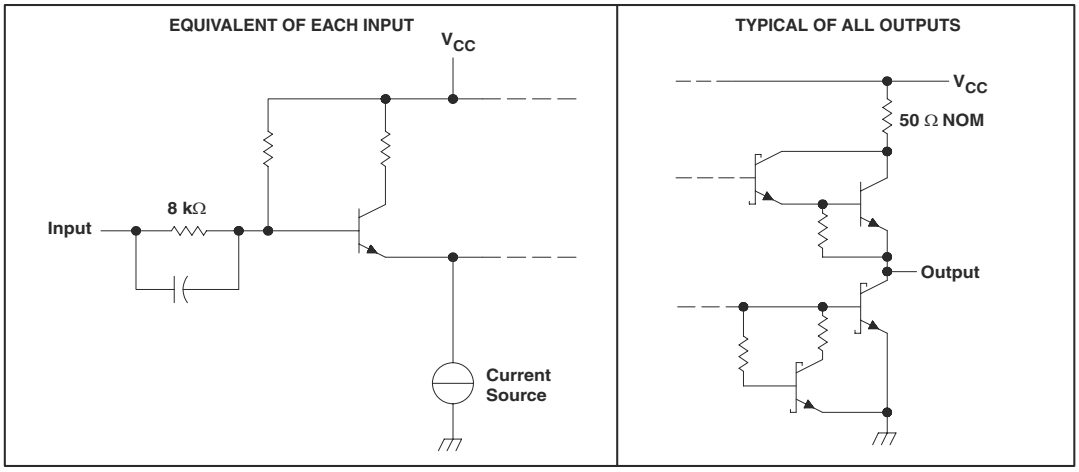


Figure 6-1. Schematics of Inputs and Outputs

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Typical Application

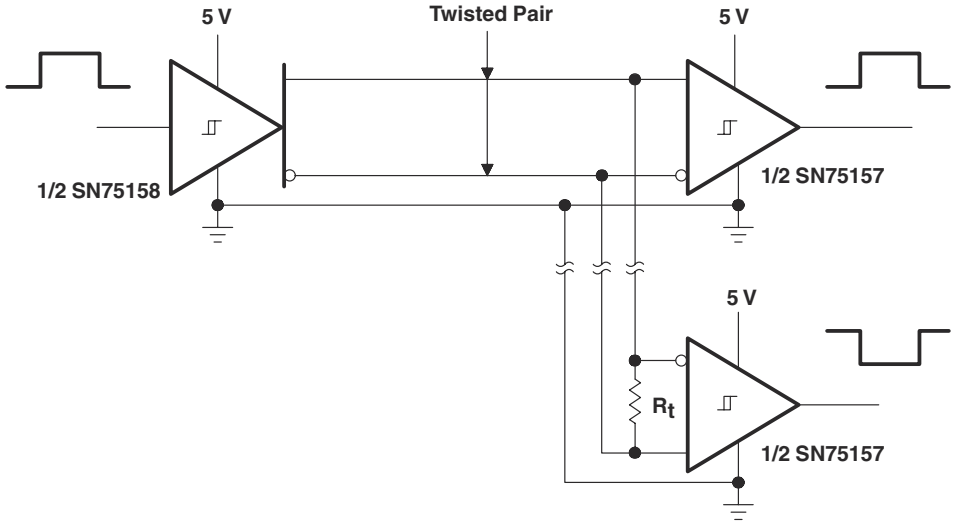


Figure 7-1. EIA/TIA-422-B System Application

8 Device and Documentation Support

8.1 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.2 Trademarks

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All trademarks are the property of their respective owners.

8.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.4 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 1997) to Revision D (January 2024)	Page
• Changed the numbering format for tables, figures, and cross-references throughout the document	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75157D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	75157
SN75157DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	75157
SN75157DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75157
SN75157P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75157P
SN75157P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75157P
SN75157PSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	A157
SN75157PSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	A157

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

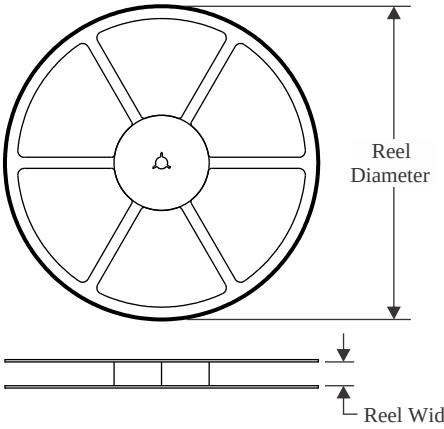
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

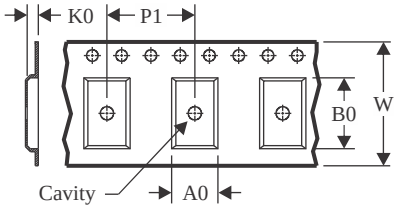
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

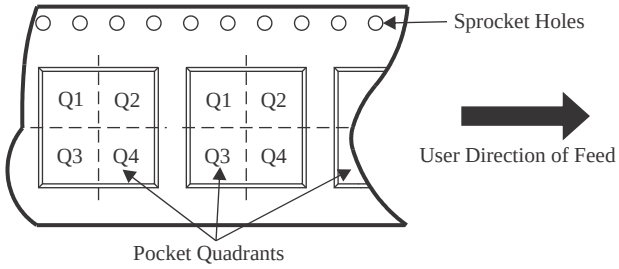


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

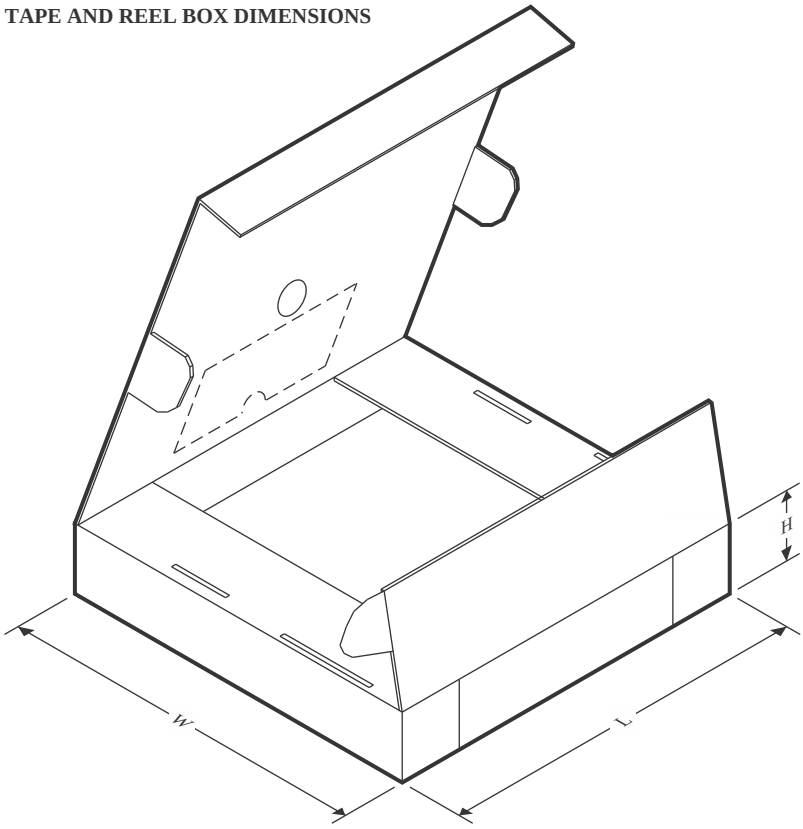
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75157DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75157DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75157PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

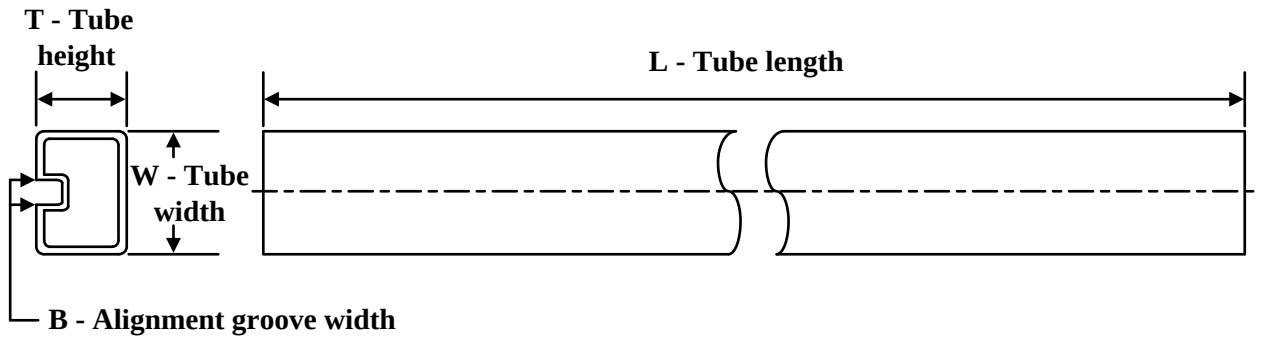
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

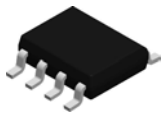
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75157DR	SOIC	D	8	2500	340.5	336.1	25.0
SN75157DR	SOIC	D	8	2500	340.5	336.1	25.0
SN75157PSR	SO	PS	8	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75157P	P	PDIP	8	50	506	13.97	11230	4.32
SN75157P.A	P	PDIP	8	50	506	13.97	11230	4.32

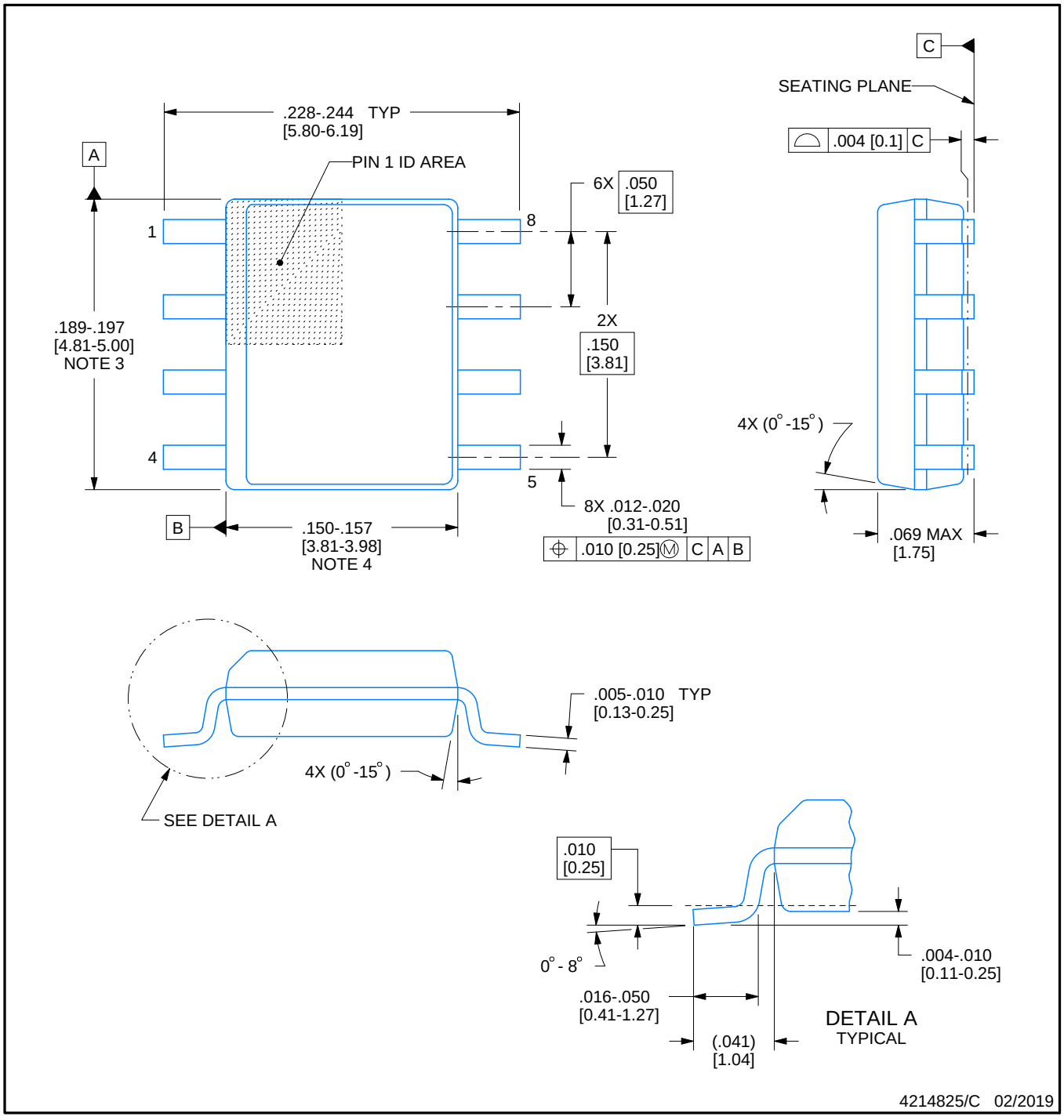


PACKAGE OUTLINE

D0008A

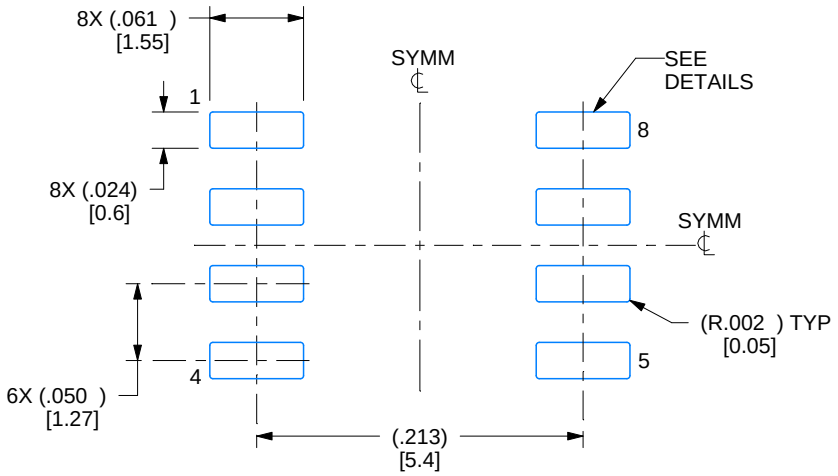
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

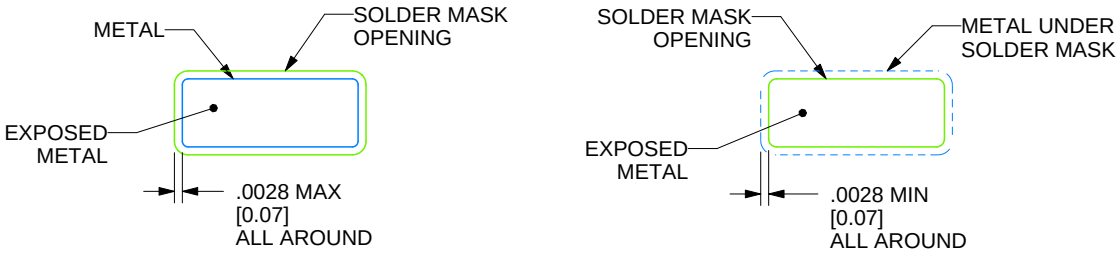


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

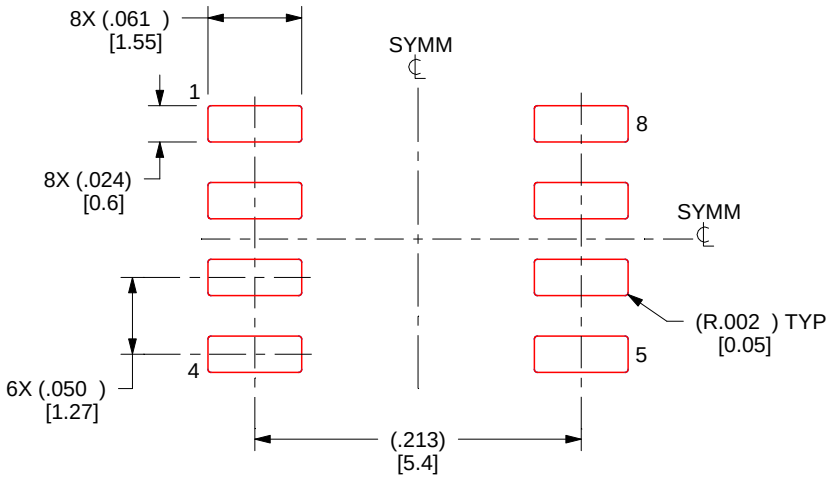
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

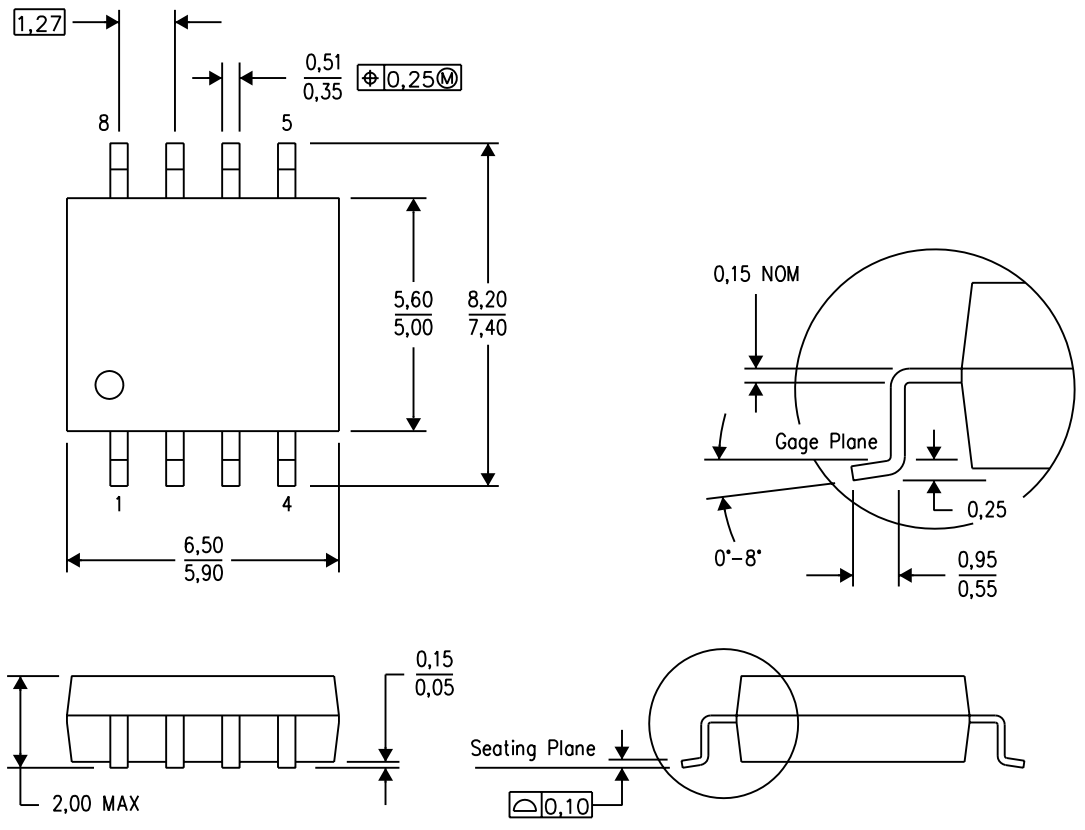
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

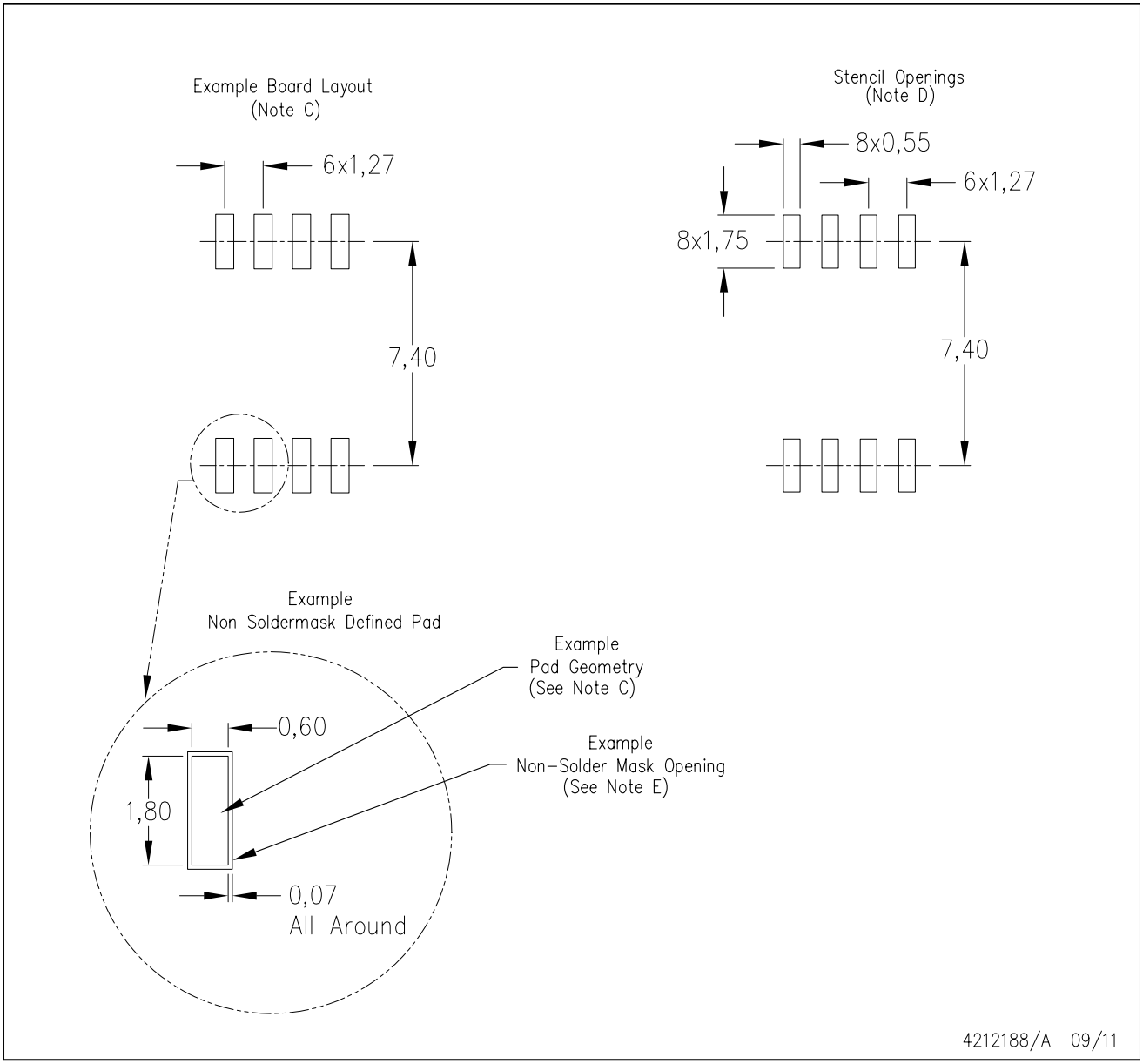
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

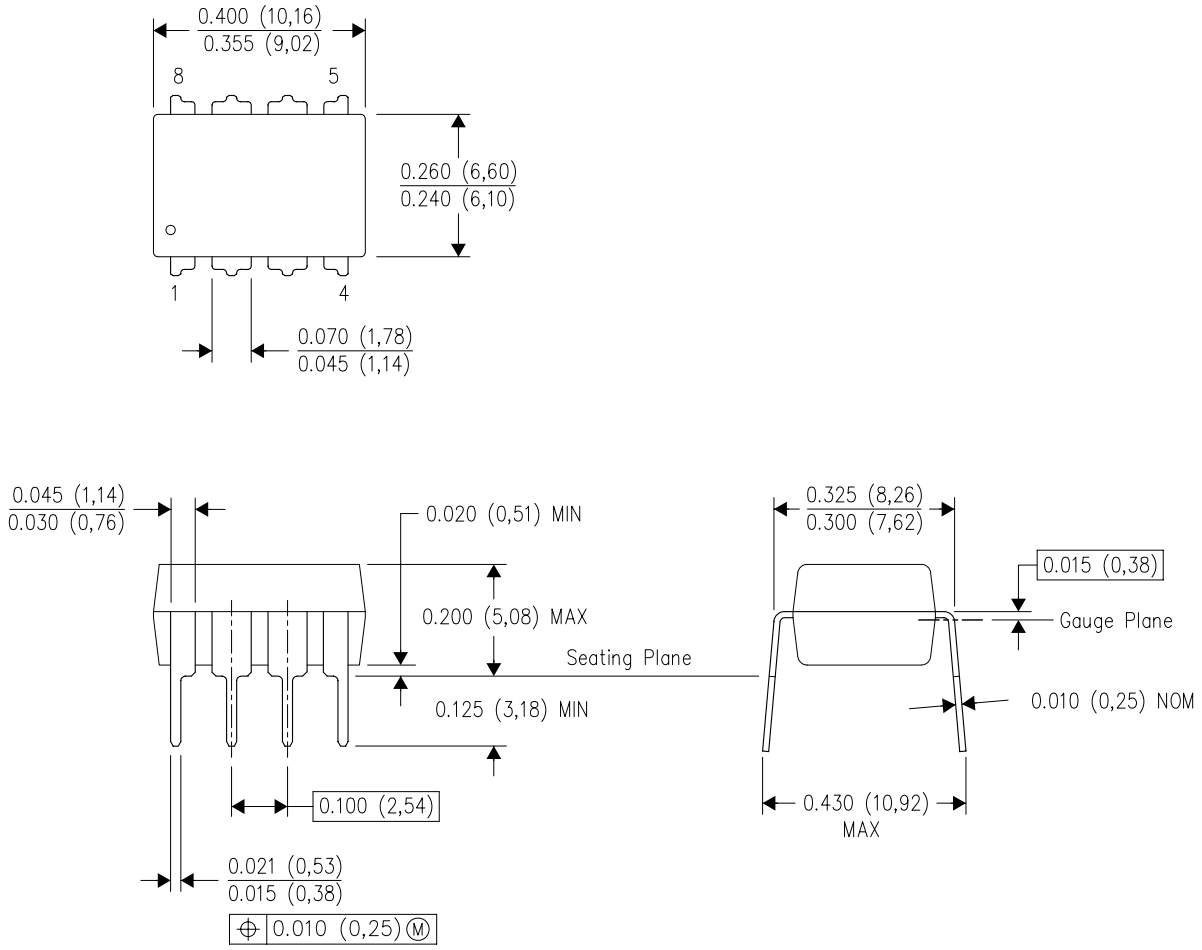
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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