TAS5822M 35-W, Digital Input, Stereo, Closed-Loop Class-D Audio Amplifier with 96kHz Enhanced Processing

1 Features

- Flexible audio I/O:
  - Supports 32, 44.1, 48, 88.2, 96 kHz sample rates
  - I^2S, LJ, RJ, TDM
  - SDOUT for audio monitoring, sub-channel or echo cancellation
  - PLL integrated, supports 3-Wire digital audio interface (no MCLK required)
  - Supports stereo bridge-tied or mono parallel bridge-tied loads (BTL and PBTL)
- Efficient class-D operation:
  - > 90% power efficiency, 90 mΩ R_{DS}on
- Supports multiple output configurations
  - 2 × 35 W in 2.0 Mode (8-Ω, 24 V, THD+N=1%)
  - 2 × 22 W in 2.0 Mode (6-Ω, 18 V, THD+N=1%)
- Excellent audio performance:
  - THD+N ≤ 0.06% at 1 W, 1 kHz, PVDD = 24 V
  - SNR ≥ 110 dB (A-weighted), ICN ≤ 40 μVRMS
- Enhanced audio processing:
  - Sample rate convertor
  - 96-kHz processor sampling
  - DC blocking, 2 ×14 BQs, THD manager
  - DPEQ, Volume Control
  - Input Mixer, Output Crossbar
  - 4th order 2-Band DRC + AGL
  - Over temperature fold back
- Flexible power supply configurations
  - PVDD: 4.5 V to 26.4 V
  - DVDD and I/O: 1.8 V or 3.3 V
- Excellent Integrated self-protection:
  - Over-current error (OCE)
  - Over-temperature warning (OTW)
  - Over-temperature error (OTE)
  - Under/over-voltage lock-out (UVLO/OVLO)
- Easy system integration
  - I^2C Software Control
  - Reduced solution size
    - Less passives required compared with open loop devices
    - Ultra Low EMI with latest EMI technology
    - No large inductors required for most applications

2 Applications

- Sounds bars, PC audio
- Wireless, Bluetooth speakers
- DTV, HDTV, UHD and multi-purpose monitors

3 Description

The TAS5822M is a High Efficiency digital input Class-D audio amplifier for driving loudspeakers used in consumer, commercial, and industrial electronics. .

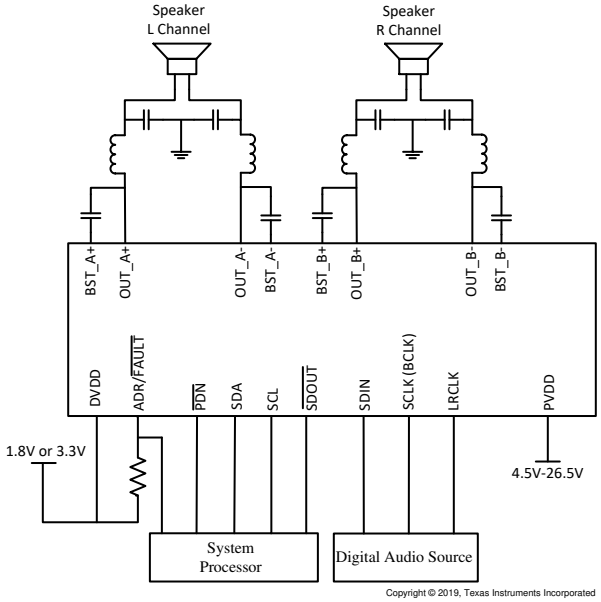
The high-performance closed loop architecture and wide-switching frequency range reduces the solution size by reducing passive components and minimize the inductor size in most applications. TAS5822M has an integrated audio processor with up to 96-kHz architecture support advanced process flow.

This device supports high efficiency 1SPW modulation with adjustable Class D loop bandwidth to achieve good audio performance.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TAS5822M	HTSSOP (38) DCP	9.7 mm × 4.4 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2020	*	Initial release.

Device Comparison Table

ORDERABLE PART NUMBER	RECOMMENDED PVDD RANGE	Typical Peak Current (speaker current)	$R_{DS(ON)}$ OPTION	Package
TAS5805M	4.5 V to 26.4 V	5A	180 mΩ	TSSOP 28
TAS5806M	4.5 V to 26.4 V	5A	180 mΩ	TSSOP 38 (Pin to Pin with TAS5822M)
TAS5822M	4.5 V to 26.4 V	7A	90 mΩ	TSSOP 38 (Pin to Pin with TAS5806M)

5 Pin Configuration and Functions

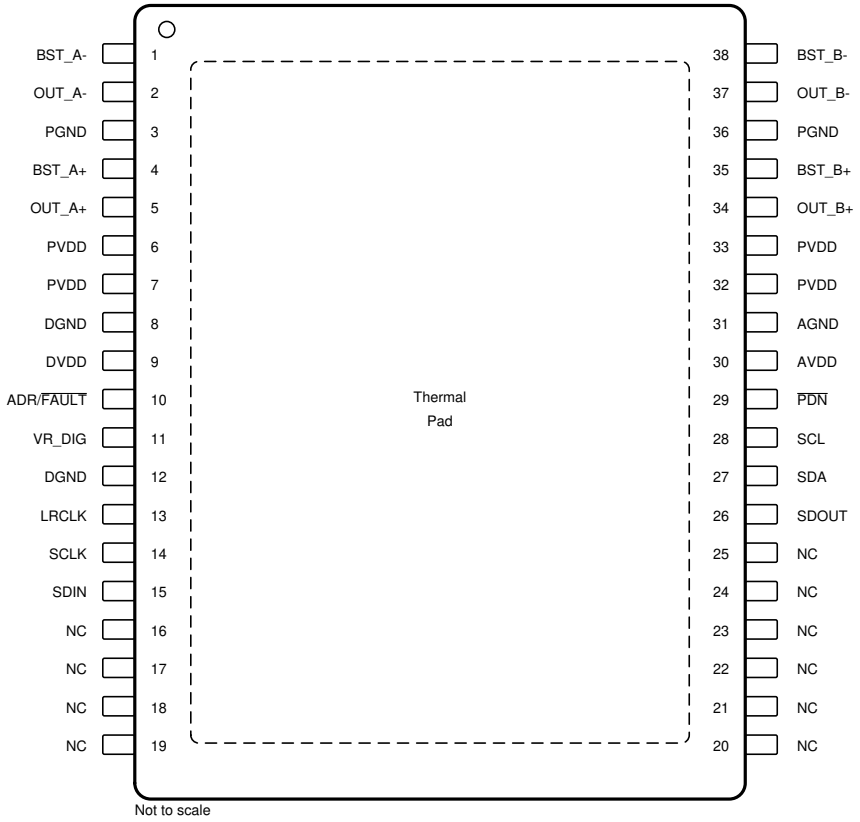


Figure 5-1. DCP Package, 38-Pin TSSOP, Top View

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
DGND	8,12	G	Digital ground
DVDD	9	P	3.3-V or 1.8-V digital power supply
VR_DIG	11	P	Internally regulated 1.5-V digital supply voltage. This pin must not be used to drive external devices
ADR/ $\overline{\text{FAULT}}$	10	DIO	Different I^2C device address can be set by selecting different pull up resistor to DVDD, see Table 4 for details. This pin can be programed by writing 1 to a register bit after Power up bit. In this mode, the ADR/ $\overline{\text{FAULT}}$ Is redefined as $\overline{\text{FAULT}}$,go to Page 0, Book 0, set register 0x61 = 0x0b first, then set register 0x60 = 0x01
LRCLK	13	DI	Word select clock for the digital signal that is active on the serial port's input data line. In I^2S, LJ and RJ, this corresponds to the left channel and right channel boundary. In TDM mode, this corresponds to the frame sync boundary.
SCLK	14	DI	Bit clock for the digital signal that is active on the input data line of the serial data port.
SDIN	15	DI	Data line to the serial data port
SDOUT	26	DO	Serial Audio data output, the source data can select as Pre-DSP or Post DSP

Table 5-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
SDA	27	DI/O	I²C serial control data interface input/output
SCL	28	DI	I²C serial control clock input
$\overline{PDN}$	29	DI	Power Down, active-low. $\overline{PDN}$ place the amplifier in Shutdown, turn off all internal regulators.
AVDD	30	P	Internally regulated 5-V analog supply voltage. This pin must not be used to drive external devices
AGND	31	G	Analog ground
PVDD	6	P	PVDD voltage input
	7	P	
	32	P	
	33	P	
PGND	3	G	Ground reference for power device circuitry. Connect this pin to system ground.
	36	G	
OUT_A+	5	O	Positive pin for differential speaker amplifier output A+
BST_A+	4	P	Connection point for the OUT_A+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A+
OUT_A-	2	O	Negative pin for differential speaker amplifier output A-
BST_A-	1	P	Connection point for the OUT_A- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_A-
BST_B-	38	P	Connection point for the OUT_B- bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B-
OUT_B-	37	O	Negative pin for differential speaker amplifier output B
BST_B+	35	P	Connection point for the OUT_B+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for OUT_B+
OUT_B+	34	O	Positive pin for differential speaker amplifier output B+
NC	18	-	No Connect Pin. Can be shorted to PVDD or shorted to GND or left open.
NC	19	-	No Connect Pin. Can be shorted to PVDD or shorted to GND or left open.
NC	20	-	No Connect Pin. Can be shorted to PVDD or shorted to GND or left open.
NC	21	-	No Connect Pin. Can be shorted to PVDD or shorted to GND or left open.
NC	17	-	No Connect Pin. Can be shorted to PVDD or shorted to GND or left open.
NC	16	-	No Connect Pin. Can be shorted to PVDD or shorted to GND or left open.
NC	22	-	No Connect Pin. Can be shorted to PVDD or shorted to GND or left open.
NC	25	-	No Connect Pin. Can be shorted to PVDD or shorted to GND or left open.
NC	23	-	No Connect Pin. Can be shorted to PVDD or shorted to GND or left open.
NC	24	-	No Connect Pin. Can be shorted to PVDD or shorted to GND or left open.
PowerPAD™		G	Connect to the system Ground

(1) AI = Analog input, AO = Analog output, DI = Digital Input, DO = Digital Output, DI/O = Digital Bi-directional (input and output), P = Power, G = Ground (0 V)

6 Specifications

6.1 Absolute Maximum Ratings

Free-air room temperature 25°C (unless otherwise noted) (1)

		MIN	MAX	UNIT
DVDD	Low-voltage digital supply	–0.3	3.9	V
PVDD	PVDD supply	–0.3	30	V
$V_{I(DigIn)}$	DVDD referenced digital inputs(2)	–0.5	V_{DVDD} + 0.5	V
$V_{I(SPK\_OUTxx)}$	Voltage at speaker output pins	–0.3	32	V
T_A	Ambient operating temperature,	–40	85	°C
T_J	Operating junction temperature	-40	160	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) DVDD referenced digital pins include: ADR/$\overline{\text{FAULT}}$, LRCLK, SCLK, SDIN, SDOUT, SCL, SDA, $\overline{\text{PDN}}$

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{(POWER)}$	Power supply inputs	DVDD	1.62		3.63	V
		PVDD	4.5		26.4	
	Recommended PVDD Range(1)	BTL mode, Speaker Load =4Ω (+/-20% Variation)	4.5		20.8	V
		BTL mode, Speaker Load =5Ω (+/-20% Variation)	4.5		26	V
		BTL mode, Speaker Load =6Ω (+/-20% Variation)	4.5		26.4	V
		BTL mode, Speaker Load =8Ω (+/-20% Variation)	4.5		26.4	V
		PBTL mode, Speaker Load =2Ω (+/-20% Variation)	4.5		21	V
		PBTL mode, Speaker Load =3Ω (+/-20% Variation)	4.5		26.4	V
		PBTL mode, Speaker Load =4Ω (+/-20% Variation)	4.5		26.4	V
$V_{IH(DigIn)}$	Input logic high for DVDD referenced digital inputs		0.9 × V_{DVDD}		DVDD	V
$V_{IL(DigIn)}$	Input logic low for DVDD referenced digital inputs				0.1 × V_{DVDD}	V
L_{OUT}	Minimum inductor value in LC filter under short-circuit condition		1			µH

(1) The Max Recommended PVDD value is limited by OCE_{THRES}, if the Class D amplifier's output peak current lower than OCE_{THRES}, 4Ω BTL load and 2Ω PBTL load also supports higher PVDD up to 26.4V

6.4 Thermal Information

THERMAL METRIC(1)		TAS5822M TSSOP (DCP) 38 PINS	UNIT
		JEDEC STANDARD 4-LAYER PCB	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	28.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Free-air room temperature 25°C, 1SPW Mode, LC filter=4.7uH+0.68uF, Fsw=768kHz, Class D Bandwidth=175kHz, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital I/O						
|IIH|	Input logic high current level for DVDD referenced digital input pins	$V_{IN(DigIn)} = V_{DVDD}$			10	uA
|IIL|	Input logic low current level for DVDD referenced digital input pins	$V_{IN(DigIn)}$ = 0 V			–10	uA
$V_{IH(Digin)}$	Input logic high threshold for DVDD referenced digital inputs		70%			V_{DVDD}
$V_{IL(Digin)}$	Input logic low threshold for DVDD referenced digital inputs				30%	V_{DVDD}
$V_{OH(Digin)}$	Output logic high voltage level	I_{OH} = 4 mA	80%			V_{DVDD}
$V_{OL(Digin)}$	Output logic low voltage level	I_{OH} = –4 mA			20%	V_{DVDD}
I^2C CONTROL PORT						
$C_{L(I2C)}$	Allowable load capacitance for each I^2C Line				400	pF
$f_{SCL(fast)}$	Support SCL frequency	No wait states, fast mode			400	kHz
$f_{SCL(slow)}$	Support SCL frequency	No wait states, slow mode			100	kHz
SERIAL AUDIO PORT						
t_{DLY}	Required LRCLK/FS to SCLK rising edge delay		5			ns
D_{SCLK}	Allowable SCLK duty cycle		40%		60%	
f_S	Supported input sample rates		32		96	kHz
f_{SCLK}	Supported SCLK frequencies		32		64	f_S
f_{SCLK}	SCLK frequency				24.576	MHz
AMPLIFIER OPERATING MODE AND DC PRAMETERS						
t_{off}	Turn-off Time	Excluding volume ramp			10	ms
$A_{V(SPK\_AMP)}$	Programmable Gain	Value represents the "peak voltage" disregarding clipping due to lower PVDD Measured at 0 dB input(1FS)	13.75		29.4	dBV
$\Delta A_{V(SPK\_AMP)}$	Amplifier gain error	Gain = 29.4dBV		0.5		dB
f_{SPK_AMP}	Switching frequency of the speaker amplifier			384		kHz
				480		kHz
				576		kHz
				768		kHz
				1024		kHz

6.5 Electrical Characteristics (continued)

Free-air room temperature 25°C, 1SPW Mode, LC filter=4.7uH+0.68uF, Fsw=768kHz, Class D Bandwidth=175kHz, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(on)}$	Drain-to-source on resistance of the individual output MOSFETs	FET + Metallization. V_{PVDD}=24V, $I_{(OUT)}$=500mA, T_J=25℃		90		mΩ
PROTECTION						
OCE_{THRES}	Over-Current Error Threshold	Speaker Output Current (Post LC filter), Speaker current	6	7		A
$UVE_{THRES(PVDD)}$	PVDD under voltage error threshold		3.7	4	4.2	V
$OVE_{THRES(PVDD)}$	PVDD over voltage error threshold		27	28.1	29.2	V
DCE_{THRES}	Output DC Error protection threshold	Class D Amplifier's output DC voltage cross speaker load to trigger Output DC Fault protection		1.9		V
T_{DCDET}	Output DC Detect time	Class D Amplifier's output remain at or above DCE_{THRES}		570		ms
OTE_{THRES}	Over temperature error threshold			160		℃
$OTE_{Hystersis}$	Over temperature error hysteresis			10		℃
OTW_{THRES}	Over temperature warning level	Read by register 0x73 bit3		135		°C
OL	Open Load Detection	Open Load Detection for ChA or ChB or both	40	70		Ω
SL	Short Load Detection	Short Load Detection for ChA or ChB or both		2		Ω
AUDIO PERFORMACNE (STEREO BTL)						
$\|V_{OS}\|$	Amplifier offset voltage	Measured differentially with zero input data, programmable gain configured with 29.4dBV analog gain, V_{PVDD} = 18 V, 1SPW Modulation	–6.5		6.5	mV
$P_{O(SPK)}$	Output Power (Per Channel)	V_{PVDD} = 13.5 V, R_{SPK} = 6 Ω, f = 1 KHz, THD +N =10%		15		W
		V_{PVDD} = 13.5 V, R_{SPK} = 6 Ω, f = 1 KHz, THD +N =1%		13		W
		V_{PVDD} = 18 V, R_{SPK} = 6 Ω, f = 1 KHz, THD +N =10%		27		W
		V_{PVDD} = 18 V, R_{SPK} = 6 Ω, f = 1 KHz, THD +N =1%		23		W
		V_{PVDD} = 24 V, R_{SPK} = 8 Ω, f = 1 KHz, THD+N =1%		35		W
$THD+N_{SPK}$	Total harmonic distortion and noise (P_O = 1 W, f = 1 KHz, R_{SPK} = 6 Ω)	V_{PVDD} = 13.5 V		0.03		%
		V_{PVDD} = 18 V		0.02		%
		V_{PVDD} = 24 V		0.02		%
$ICN_{(SPK)}$	Idle channel noise(Aweighted, AES17)	V_{PVDD} = 13.5 V, LC-filter, Load=6 Ω		35		μVrms
		V_{PVDD} = 18 V, LC-filter ,Load=6 Ω		35		μVrms
DR	Dynamic range	A-Weighted, -60 dBFS method. V_{PVDD} = 24 V, Analog Gain = 29.4dBV		111		dB

6.5 Electrical Characteristics (continued)

Free-air room temperature 25°C, 1SPW Mode, LC filter=4.7uH+0.68uF, Fsw=768kHz, Class D Bandwidth=175kHz, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio	A-Weighted, referenced to 1% THD+N Output Level, V_{PVDD}=24V		111		dB
		A-Weighted, referenced to 1% THD+N Output Level, V_{PVDD}=13.5V		106		dB
PSRR	Power supply rejection ratio	Injected Noise = 1 KHz, 1 Vrms, V_{PVDD} = 13.5 V, input audio signal = digital zero		72		dB
X-talk$_{SPK}$	Cross-talk (worst case between left-to-right and right-to-left coupling)	f = 1 KHz, based on Inductor (DFEG7030D-4R7) from Murata		100		dB
AUDIO PERFORMANCE (MONO PBTL)						
$\|V_{OS}\|$	Amplifier offset voltage	Measured differentially with zero input data, programmable gain configured with 29.4dBV Analog gain, V_{PVDD} = 18 V, 1SPW Modulation	–6.5		6.5	mV
$P_{O(SPK)}$	Output Power	V_{PVDD} = 24 V, R_{SPK} = 4 Ω, f = 1KHz, THD+N =1%		65		W
		V_{PVDD} = 18 V, R_{SPK} = 3 Ω, f = 1KHz, THD+N =1%		45		W
		V_{PVDD} = 18 V, R_{SPK} = 3 Ω, f = 1KHz, THD+N =10%		55		W
THD+N$_{SPK}$	Total harmonic distortion and noise (P_O = 1 W, f = 1 KHz)	V_{PVDD} = 18 V, LC-filter, R_{SPK} = 3 Ω		0.05		%
		V_{PVDD} = 24 V, LC-filter, R_{SPK} = 4 Ω		0.02		%
DR	Dynamic range	A-Weighted, -60 dBFS method, V_{PVDD}=24V, R_{SPK}= 3 Ω.		111		dB
SNR	Signal-to-noise ratio	A-Weighted, referenced to 1% THD+N Output Level, V_{PVDD}=18V, R_{SPK} = 3 Ω		108		dB
		A-Weighted,referenced to 1% THD+N Output Level, V_{PVDD}=13.5V, R_{SPK} = 2 Ω		106		dB
PSRR	Power supply rejection ratio	Injected Noise = 1 KHz, 1 Vrms,V_{PVDD} = 18 V, input audio signal = digital zero		72		dB

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
Serial Audio Port Timing - Slave Mode					
f_{SCLK}	SCLK frequency	1.024			MHz
t_{SCLK}	SCLK period	40			ns
t_{SCLKL}	SCLK pulse width, low	16			ns
t_{SCLKH}	SCLK pulse width, high	16			ns
t_{SL}	SCLK rising to LRCLK/FS edge	8			ns
t_{LS}	LRCK/FS Edge to SCLK rising edge	8			ns
t_{SU}	Data setup time, before SCLK rising edge	8			ns
t_{DH}	Data hold time, after SCLK rising edge	8			ns
t_{DFS}	Data delay time from SCLK falling edge			15	ns
I^2C Bus Timing – Standard					
f_{SCL}	SCL clock frequency			100	kHz
t_{BUF}	Bus free time between a STOP and START condition	4.7			µs
t_{LOW}	Low period of the SCL clock	4.7			µs
t_{HI}	High period of the SCL clock	4			µs
t_{RS-SU}	Setup time for (repeated) START condition	4.7			µs
t_{S-HD}	Hold time for (repeated) START condition	4			µs
t_{D-SU}	Data setup time	250			ns
t_{D-HD}	Data hold time	0		3450	ns
t_{SCL-R}	Rise time of SCL signal	$20 + 0.1C_B$		1000	ns
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20 + 0.1C_B$		1000	ns
t_{SCL-F}	Fall time of SCL signal	$20 + 0.1C_B$		1000	ns
t_{SDA-R}	Rise time of SDA signal	$20 + 0.1C_B$		1000	ns
t_{SDA-F}	Fall time of SDA signal	$20 + 0.1C_B$		1000	ns
t_{P-SU}	Setup time for STOP condition	4			µs
C_B	Capacitive load for each bus line			400	pf
I^2C Bus Timing – Fast					
f_{SCL}	SCL clock frequency			400	kHz
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs
t_{LOW}	Low period of the SCL clock	1.3			µs
t_{HI}	High period of the SCL clock	600			ns
t_{RS-SU}	Setup time for (repeated)START condition	600			ns
t_{RS-HD}	Hold time for (repeated)START condition	600			ns
t_{D-SU}	Data setup time	100			ns
t_{D-HD}	Data hold time	0		900	ns
t_{SCL-R}	Rise time of SCL signal	$20 + 0.1C_B$		300	ns
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20 + 0.1C_B$		300	ns
t_{SCL-F}	Fall time of SCL signal	$20 + 0.1C_B$		300	ns
t_{SDA-R}	Rise time of SDA signal	$20 + 0.1C_B$		300	ns
t_{SDA-F}	Fall time of SDA signal	$20 + 0.1C_B$		300	ns
t_{P-SU}	Setup time for STOP condition	600			ns
t_{SP}	Pulse width of spike suppressed			50	ns
C_B	Capacitive load for each bus line			400	pf

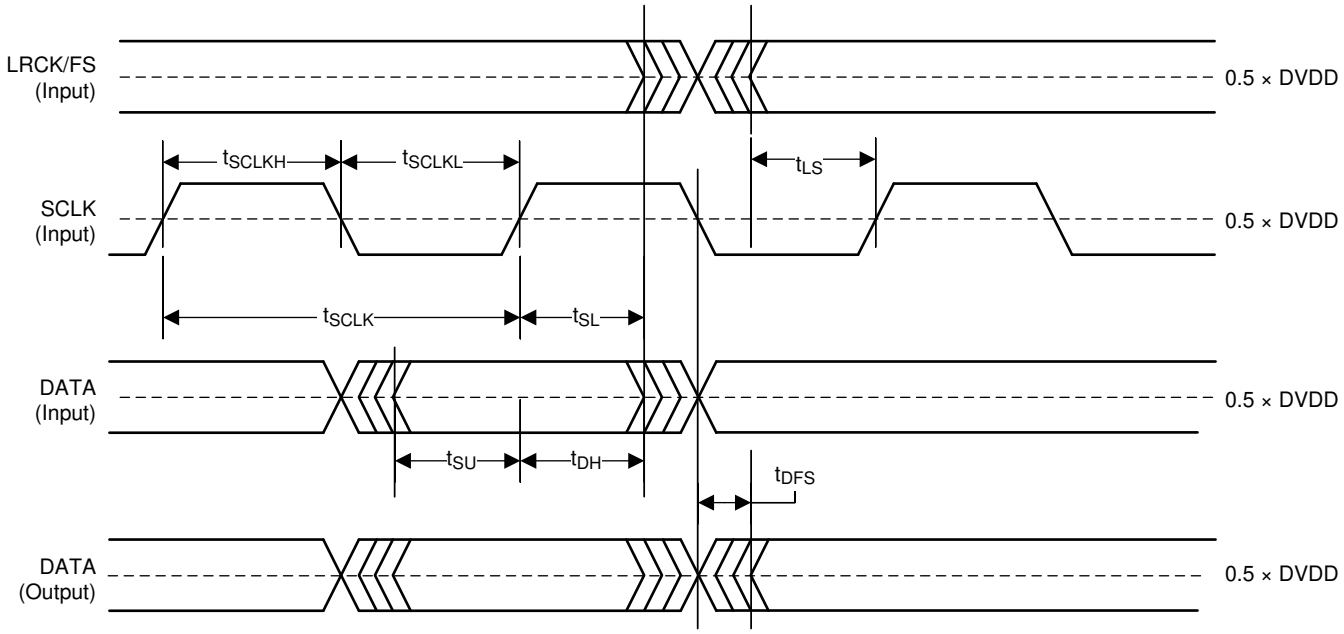


Figure 6-1. Serial Audio Port Timing in Slave Mode

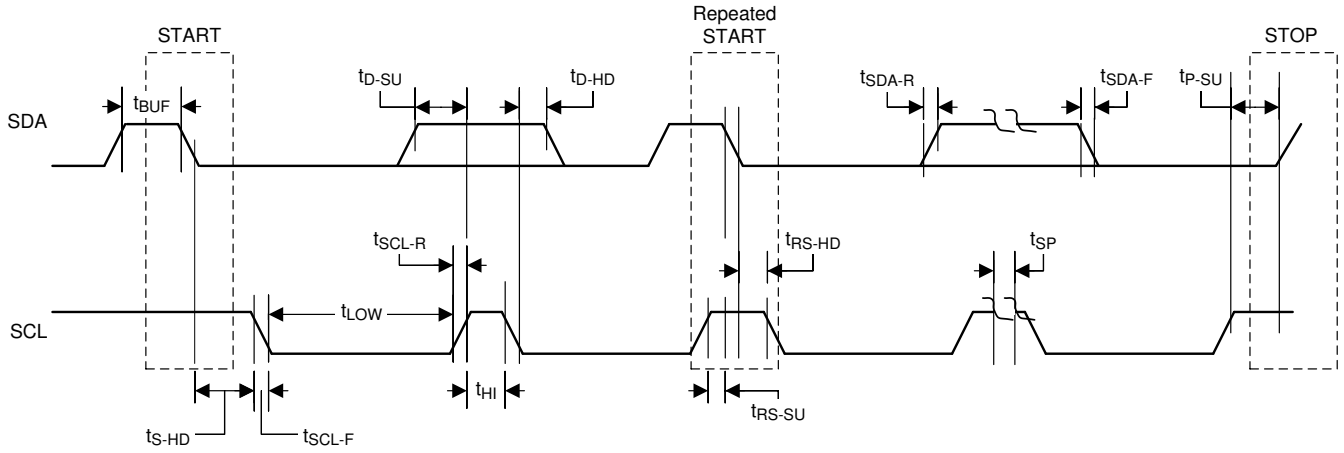
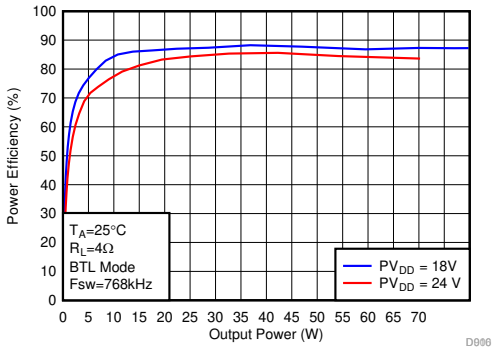


Figure 6-2. I²C Communication Port Timing Diagram

6.7 Typical Characteristics

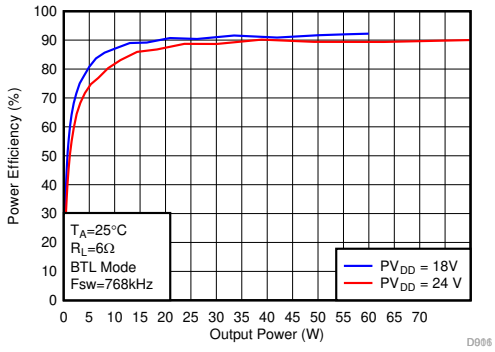
6.7.1 Bridge Tied Load (BTL) Configuration Curves with 1SPW Modulation, Fsw = 768kHz

Free-air room temperature 25°C (unless otherwise noted) Measurements were made using TAS5822MEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 768 kHz, 1SPW Mode, the LC filter used was 10µH / 0.68 µF, Class D bandwidth = 175 kHz, unless otherwise noted.



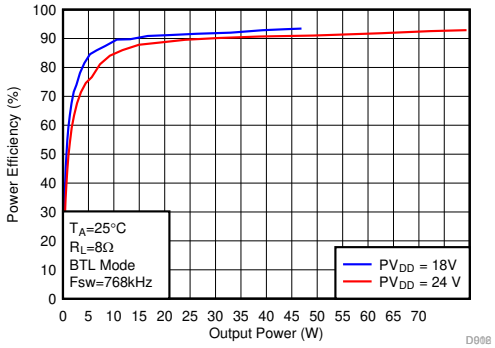
F_{SW} = 768 kHz Load=4Ω 1SPW Mode

Figure 6-3. Efficiency vs Output Power-BTL



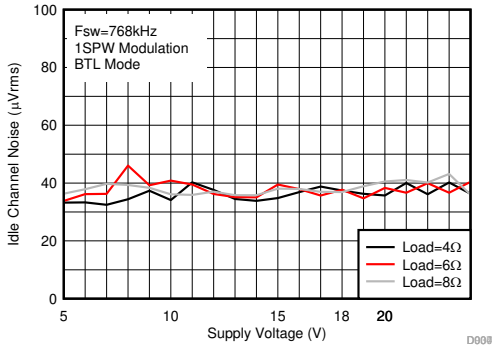
F_{SW} = 768 kHz Load=6Ω 1SPW Mode

Figure 6-4. Efficiency vs Output Power-BTL



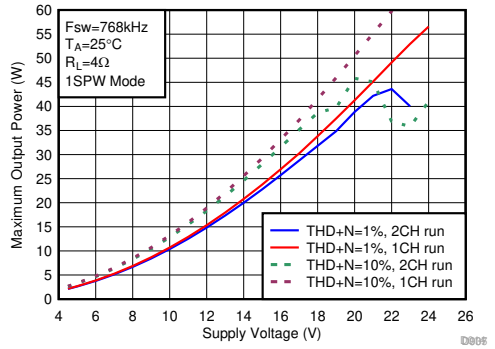
F_{SW} = 768 kHz Load=8Ω 1SPW Mode

Figure 6-5. Efficiency vs Output Power-BTL



F_{SW} = 768 kHz 1SPW Mode

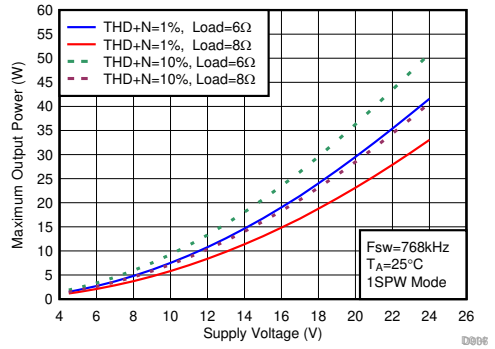
Figure 6-6. Idle Channel Noise vs Supply Voltage



Continuous Output Power, 2CH run, High PVDD, R_{DS}on increase due to die temperature increase.

F_{SW} = 768 kHz 1SPW Mode Load=4Ω

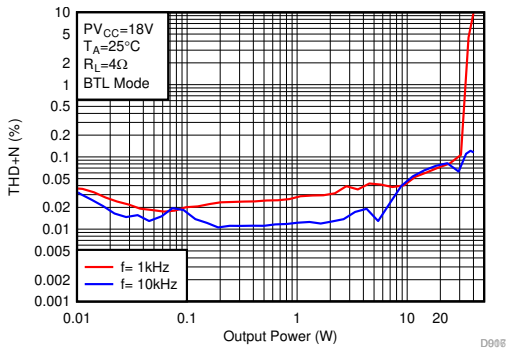
Figure 6-7. Output Power vs Supply Voltage



6Ω and 8Ω efficiency is higher than 4Ω, better thermal performance, 2CH and 1CH data almost same.

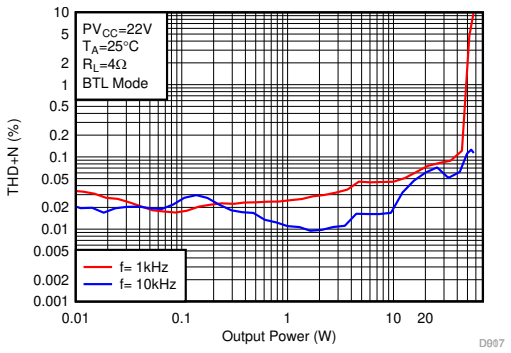
F_{SW} = 768 kHz 1SPW Mode Load=6Ω or 8Ω

Figure 6-8. Output Power vs Supply Voltage



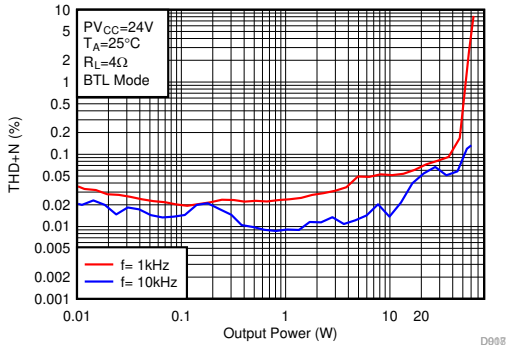
F_{SW} = 768 kHz Load=4Ω PVDD = 18V

Figure 6-9. THD+N vs Output Power-BTL



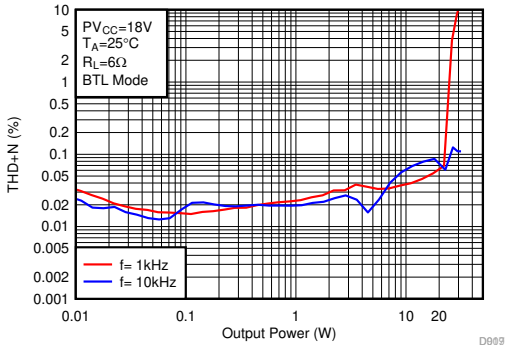
F_{SW} = 768 kHz Load=4Ω PVDD = 22V

Figure 6-10. THD+N vs Output Power-BTL



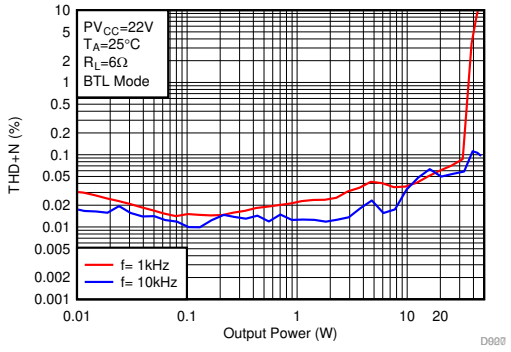
F_{SW} = 768 kHz Load=4Ω PVDD = 24V

Figure 6-11. THD+N vs Output Power-BTL



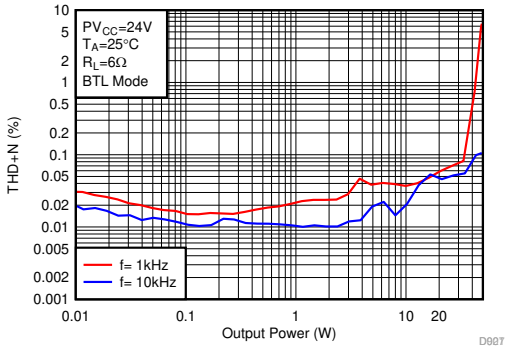
F_{SW} = 768 kHz Load=6Ω PVDD = 18V

Figure 6-12. THD+N vs Output Power-BTL



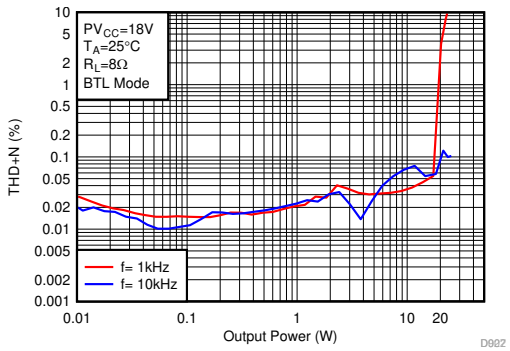
F_{SW} = 768 kHz Load=6Ω PVDD = 22V

Figure 6-13. THD+N vs Output Power-BTL



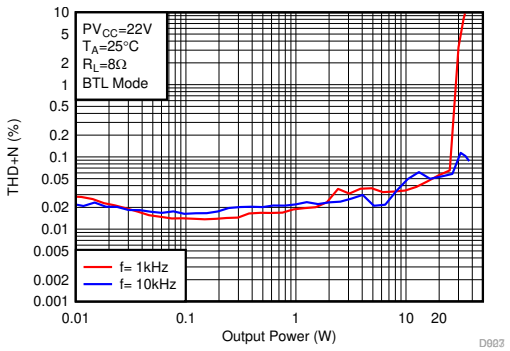
F_{SW} = 768 kHz Load=6Ω PVDD = 24V

Figure 6-14. THD+N vs Output Power-BTL



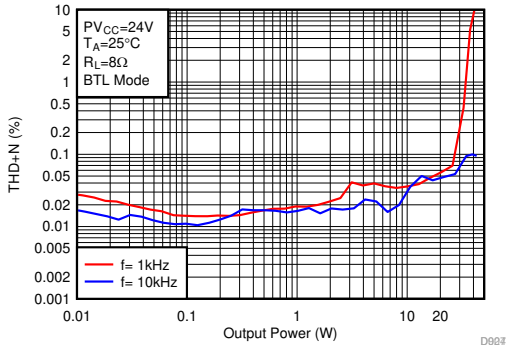
F_{SW} = 768 kHz Load=8Ω PVDD = 18V

Figure 6-15. THD+N vs Output Power-BTL



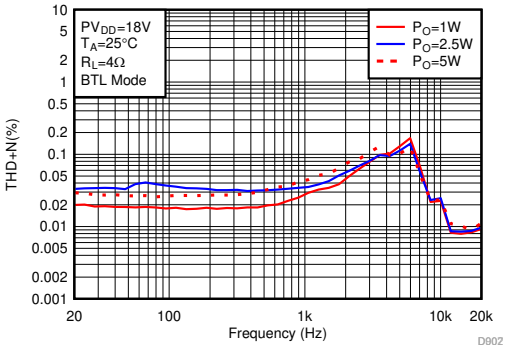
F_{SW} = 768 kHz Load=8Ω PVDD = 22V

Figure 6-16. THD+N vs Output Power-BTL



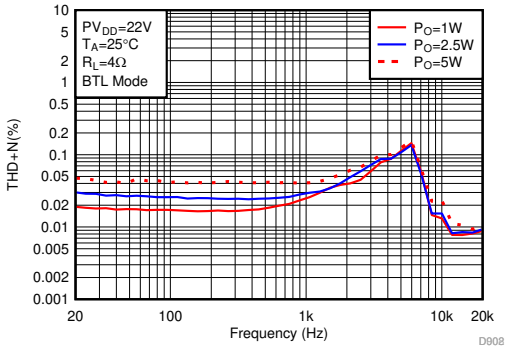
F_{SW} = 768 kHz Load=8Ω PVDD = 24V

Figure 6-17. THD+N vs Output Power-BTL



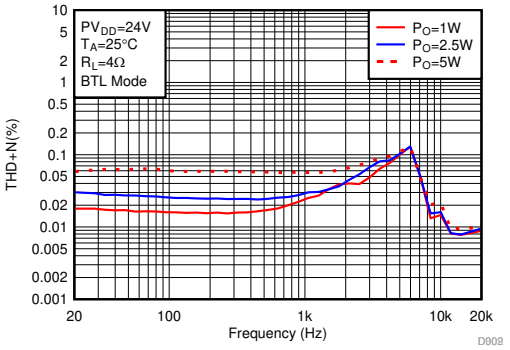
F_{SW} = 768 kHz Load=4Ω PVDD = 18V

Figure 6-18. THD+N vs Frequency-BTL



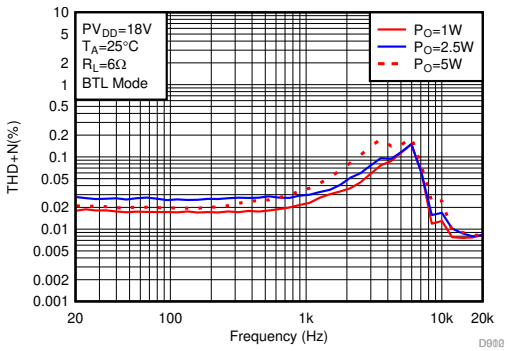
F_{SW} = 768 kHz Load=4Ω PVDD = 22V

Figure 6-19. THD+N vs Frequency-BTL



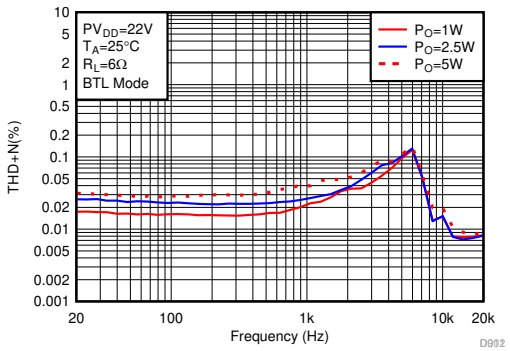
F_{SW} = 768 kHz Load=4Ω PVDD = 24V

Figure 6-20. THD+N vs Frequency-BTL



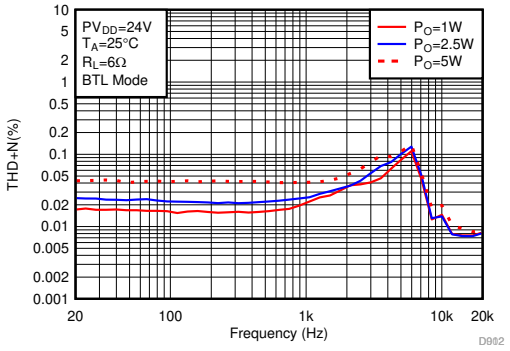
FSW = 768 kHz Load=6Ω PVDD = 18V

Figure 6-21. THD+N vs Frequency-BTL



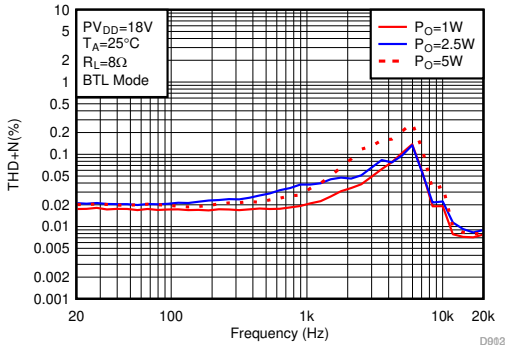
FSW = 768 kHz Load=6Ω PVDD = 22V

Figure 6-22. THD+N vs Frequency-BTL



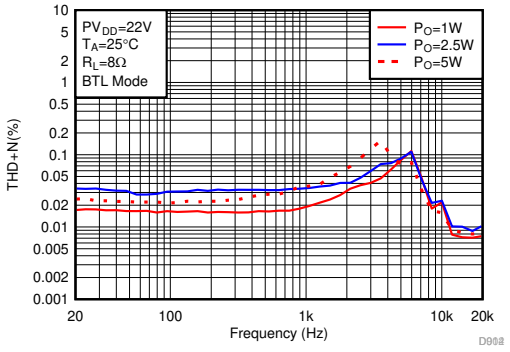
FSW = 768 kHz Load=6Ω PVDD = 24V

Figure 6-23. THD+N vs Frequency-BTL



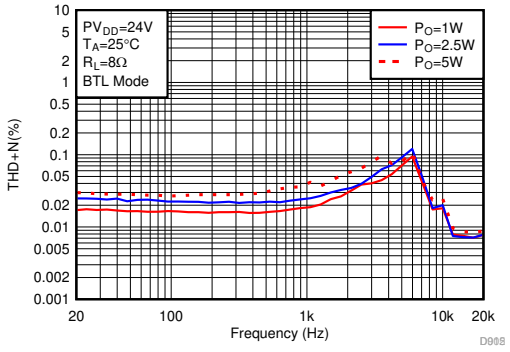
FSW = 768 kHz Load=8Ω PVDD = 18V

Figure 6-24. THD+N vs Frequency-BTL



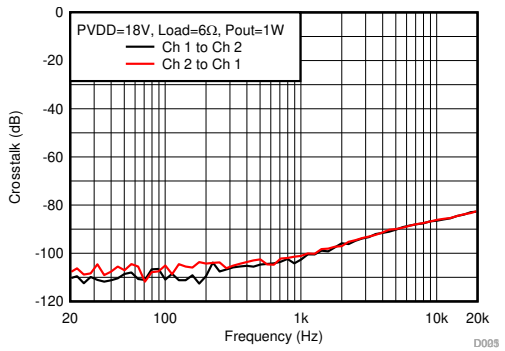
FSW = 768 kHz Load=8Ω PVDD = 22V

Figure 6-25. THD+N vs Frequency-BTL



FSW = 768 kHz Load=8Ω PVDD = 24V

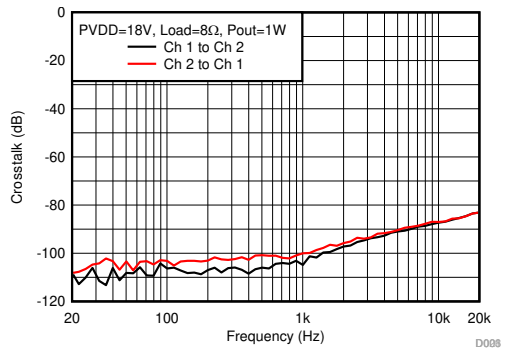
Figure 6-26. THD+N vs Frequency-BTL



Load = 6Ω

F_{SW} = 768 kHz 1SPW Mode PVDD = 18V

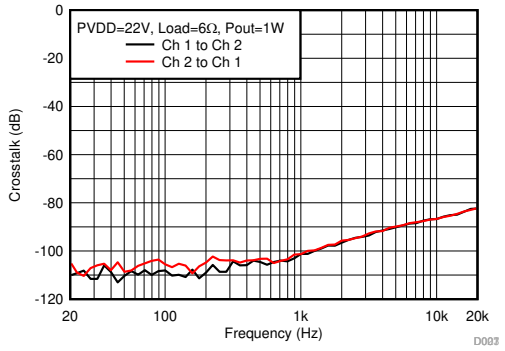
Figure 6-27. Crosstalk vs Frequency-BTL



Load = 8Ω

F_{SW} = 768 kHz 1SPW Mode PVDD = 18V

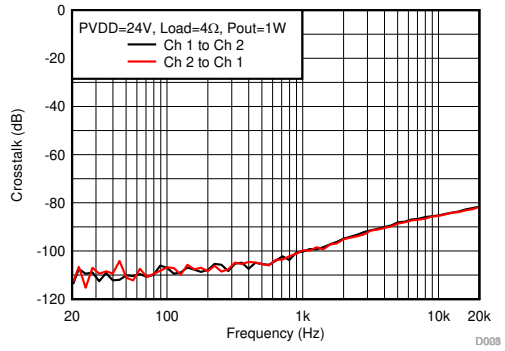
Figure 6-28. Crosstalk vs Frequency-BTL



Load = 6Ω

F_{SW} = 768 kHz 1SPW Mode PVDD = 22V

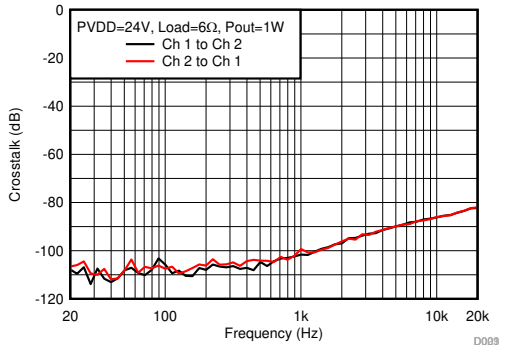
Figure 6-29. Crosstalk vs Frequency-BTL



Load = 4Ω

F_{SW} = 768 kHz 1SPW Mode PVDD = 24V

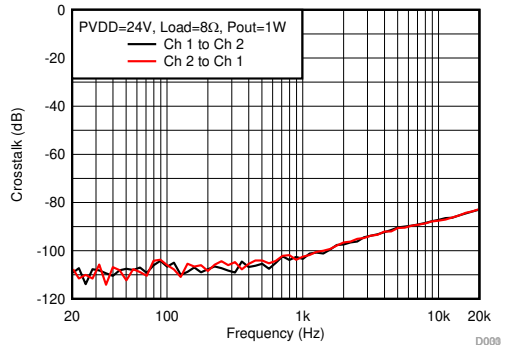
Figure 6-30. Crosstalk vs Frequency-BTL



Load = 6Ω

F_{SW} = 768 kHz 1SPW Mode PVDD = 24V

Figure 6-31. Crosstalk vs Frequency-BTL



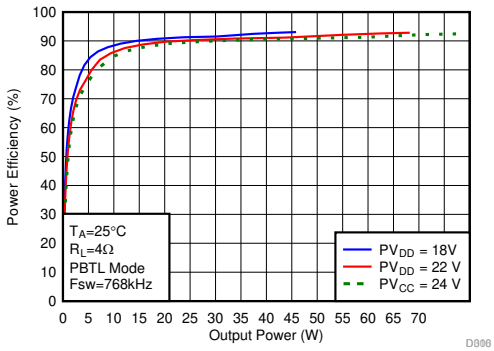
Load = 8Ω

F_{SW} = 768 kHz 1SPW Mode PVDD = 24V

Figure 6-32. Crosstalk vs Frequency-BTL

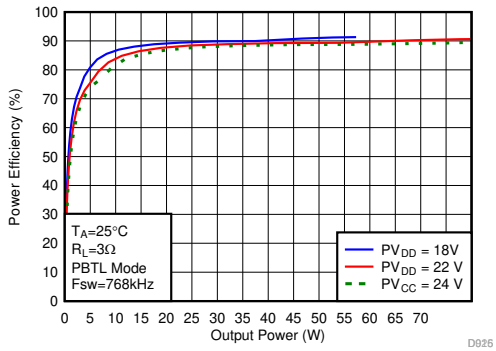
6.7.2 Parallel Bridge Tied Load (PBTL) Configuration Curves with 1SPW Modulation, Fsw = 768kHz

Free-air room temperature 25°C (unless otherwise noted).Measurements were made using TAS5822MEVM board and Audio Precision System 2722 with Analog Analyzer filter set to 20-kHz brickwall filter. All measurements taken with audio frequency set to 1 kHz and device PWM frequency set to 768 kHz, 1SPW Mode, the LC filter used was 10 µH / 0.68 µF, Class D bandwidth = 175 kHz, unless otherwise noted.



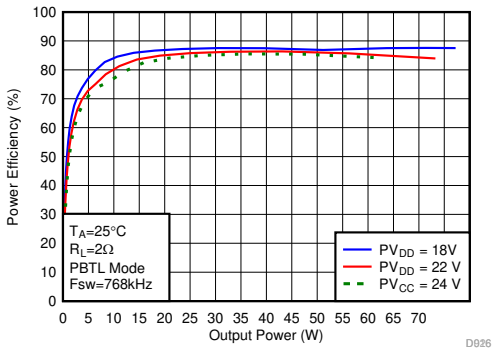
F_{SW} = 768 kHz Load = 4Ω PVDD = 18V/22V/24V

Figure 6-33. Efficiency vs Output Power



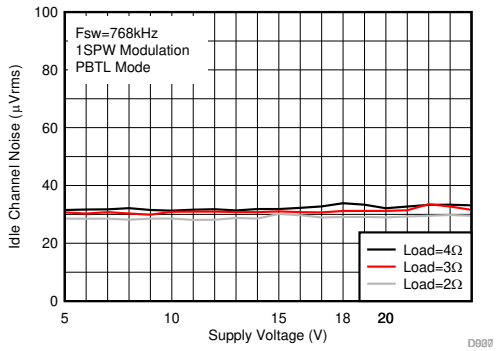
F_{SW} = 768 kHz Load = 3Ω PVDD = 18V/22V/24V

Figure 6-34. Efficiency vs Output Power



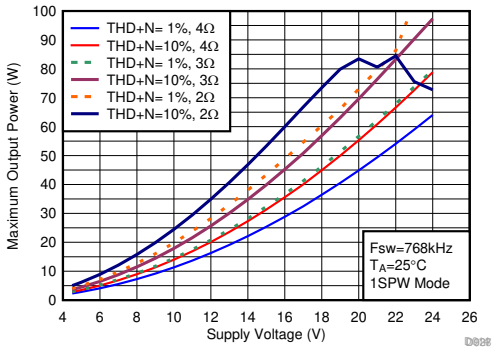
F_{SW} = 768 kHz Load = 2Ω PVDD = 18V/22V/24V

Figure 6-35. Efficiency vs Output Power



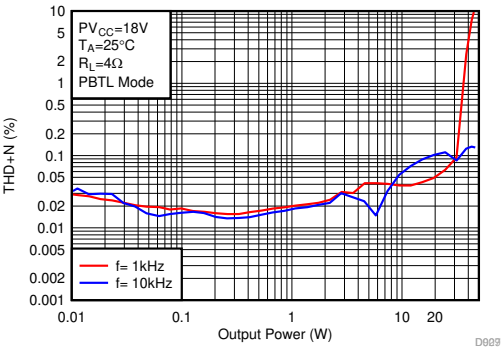
F_{SW} = 768 kHz Load = 2Ω/3Ω/4Ω 1SPW Mode

Figure 6-36. idle Channel Noise vs PVDD



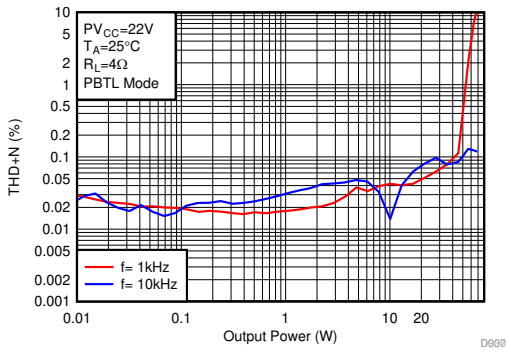
F_{SW} = 768 kHz Load = 2Ω/3Ω/4Ω 1SPW Mode

Figure 6-37. Output Power vs PVDD



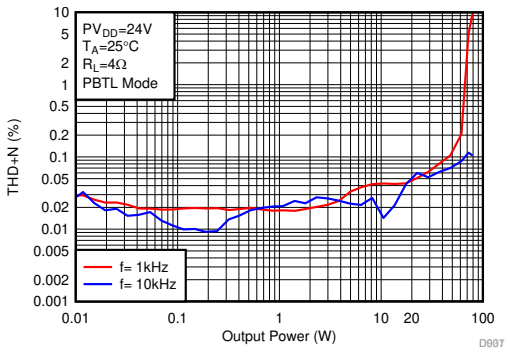
F_{SW} = 768 kHz Load = 4Ω PVDD = 18V

Figure 6-38. THD+N vs Output Power



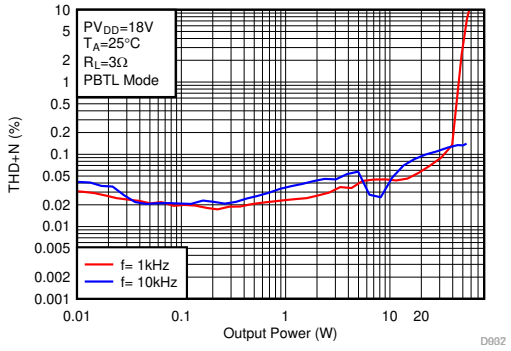
F_{SW} = 768 kHz Load = 4Ω PVDD=22V

Figure 6-39. THD+N vs Output Power



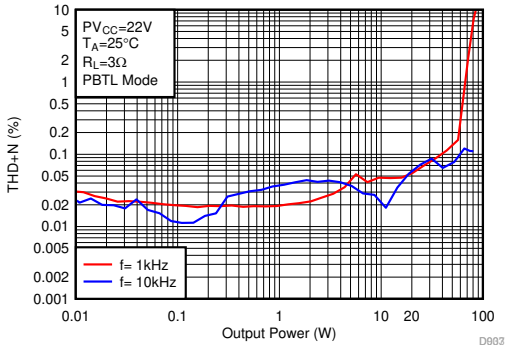
F_{SW} = 768 kHz Load = 4Ω PVDD = 24V

Figure 6-40. THD+N vs Output Power



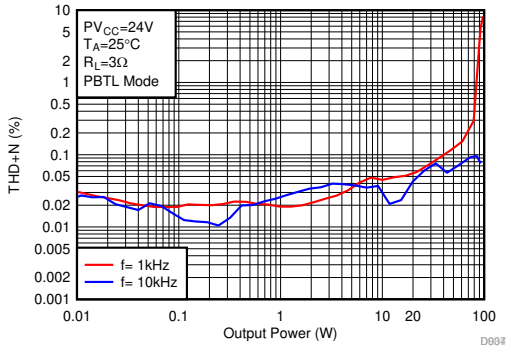
F_{SW} = 768 kHz Load = 3Ω PVDD = 18V

Figure 6-41. THD+N vs Output Power



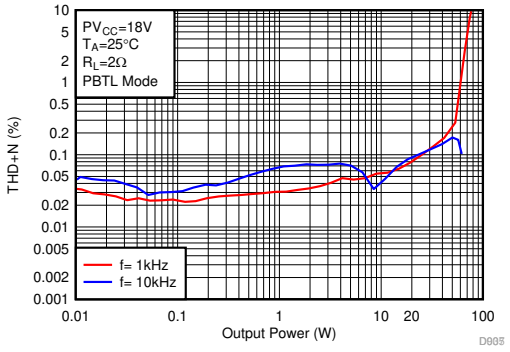
F_{SW} = 768 kHz Load = 3Ω PVDD = 22V

Figure 6-42. THD+N vs Output Power



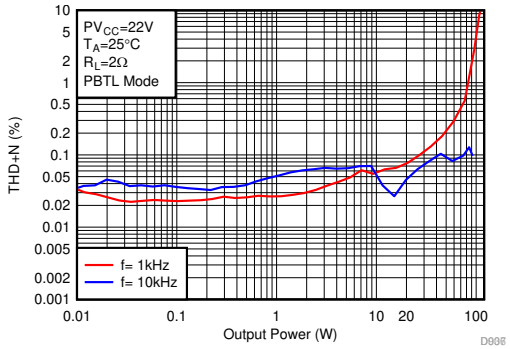
F_{SW} = 768 kHz Load = 3Ω PVDD = 24V

Figure 6-43. THD+N vs Output Power



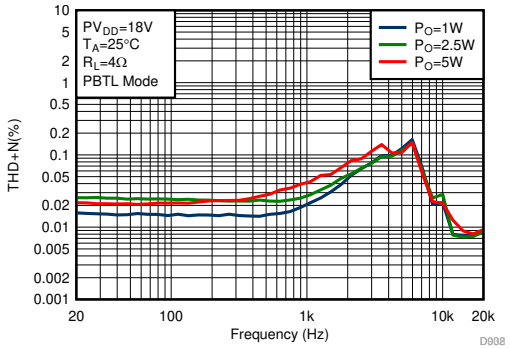
F_{SW} = 768 kHz Load = 2Ω PVDD = 18V

Figure 6-44. THD+N vs Output Power



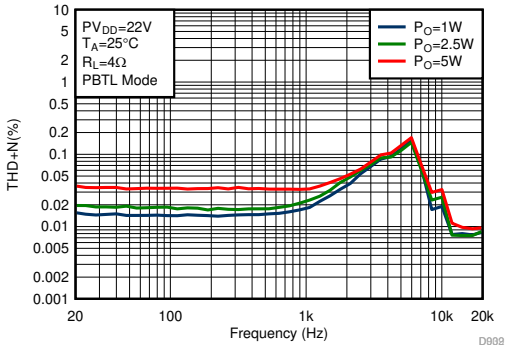
F_{SW} = 768 kHz Load = 2Ω PVDD = 22V

Figure 6-45. THD+N vs Output Power



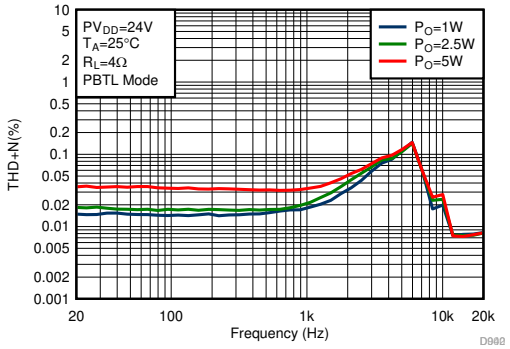
F_{SW} = 768 kHz Load = 4Ω PVDD = 18V

Figure 6-46. THD+N vs Frequency



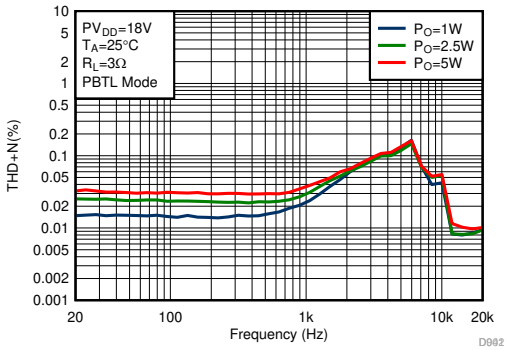
F_{SW} = 768 kHz Load = 4Ω PVDD = 22V

Figure 6-47. THD+N vs Frequency



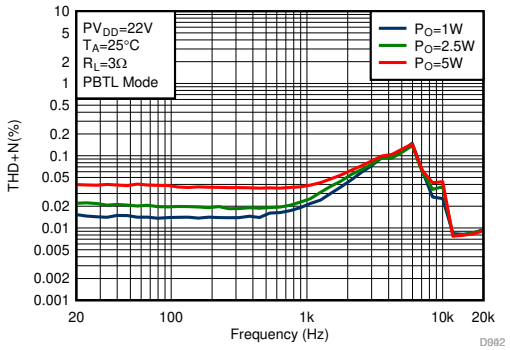
F_{SW} = 768 kHz Load = 4Ω PVDD = 24V

Figure 6-48. THD+N vs Frequency



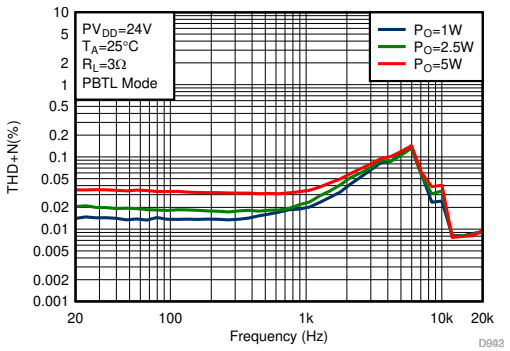
F_{SW} = 768 kHz Load = 3Ω PVDD = 18V

Figure 6-49. THD+N vs Frequency



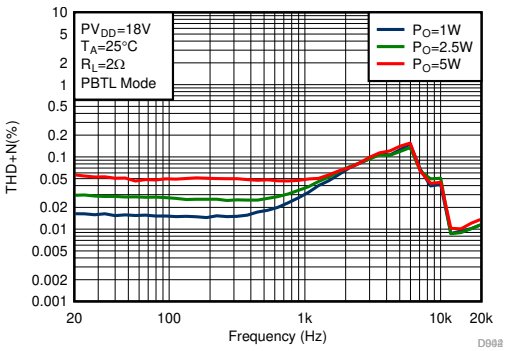
F_{SW} = 768 kHz Load = 3Ω PVDD = 22V

Figure 6-50. THD+N vs Frequency



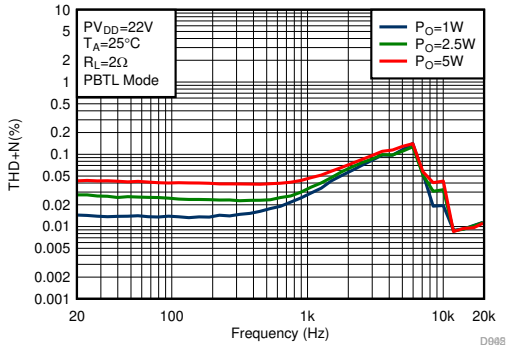
F_{SW} = 768 kHz Load = 3Ω PVDD = 24V

Figure 6-51. THD+N vs Frequency



F_{SW} = 768 kHz Load = 2Ω PVDD = 18V

Figure 6-52. THD+N vs Frequency



F_{SW} = 768 kHz Load = 2Ω PVDD = 22V

Figure 6-53. THD+N vs Frequency

6.8 Parametric Measurement Information

6.8.1 Power Consumption Summary

Free-air room temperature 25°C (unless others noted), LC filter = 10 µH + 0.68 µF, Enable DSP (96 kHz Process Flow), 1SPW Modulation, DVDD = 3.3 V, ADR/$\overline{\text{FAULT}}$ pin pull up resistor = 4.7 kΩ, $\overline{\text{PDN}}$ pin pull up resistor = 10 kΩ.

V_{PVDD} (V)	F_{SW}(kHz)	State of Operation	I_{PVDD} (mA)	I_{DVDD} (mA)	P_{DISS}(W)
18	384	**Play (Idle)**	**33.16**	**18.04**	**0.656**
		Hi-Z	10.15	17.84	0.242
		Sleep	7.01	0.76	0.129
		Deep Sleep	0.12	0.75	0.005
		Shutdown	0.009	0.33	0.001
	768	**Play (Idle)**	**28.66**	**18.04**	**0.575**
		Hi-Z	10.15	17.85	0.242
		Sleep	7.01	0.76	0.129
		Deep Sleep	0.12	0.75	0.005
		Shutdown	0.009	0.33	0.001
	1024	**Play (Idle)**	**29.75**	**18.06**	**0.595**
		Hi-Z	10.15	17.86	0.242
		Sleep	7.01	0.76	0.129
		Deep Sleep	0.12	0.75	0.005
		Shutdown	0.009	0.33	0.001
24	384	**Play (Idle)**	**41.01**	**18.1**	**1.044**
		Hi-Z	10.29	17.88	0.306
		Sleep	7.14	0.76	0.174
		Deep Sleep	0.13	0.76	0.006
		Shutdown	0.012	0.33	0.001
	768	**Play (Idle)**	**34.76**	**18.1**	**0.894**
		Hi-Z	10.29	17.87	0.306
		Sleep	7.14	0.76	0.174
		Deep Sleep	0.13	0.76	0.006
		Shutdown	0.011	0.33	0.001
	1024	**Play (Idle)**	**34.64**	**18.1**	**0.891**
		Hi-Z	10.29	17.86	0.306
		Sleep	7.15	0.76	0.174
		Deep Sleep	0.13	0.75	0.006
		Shutdown	0.012	0.33	0.001

7 Detailed Description

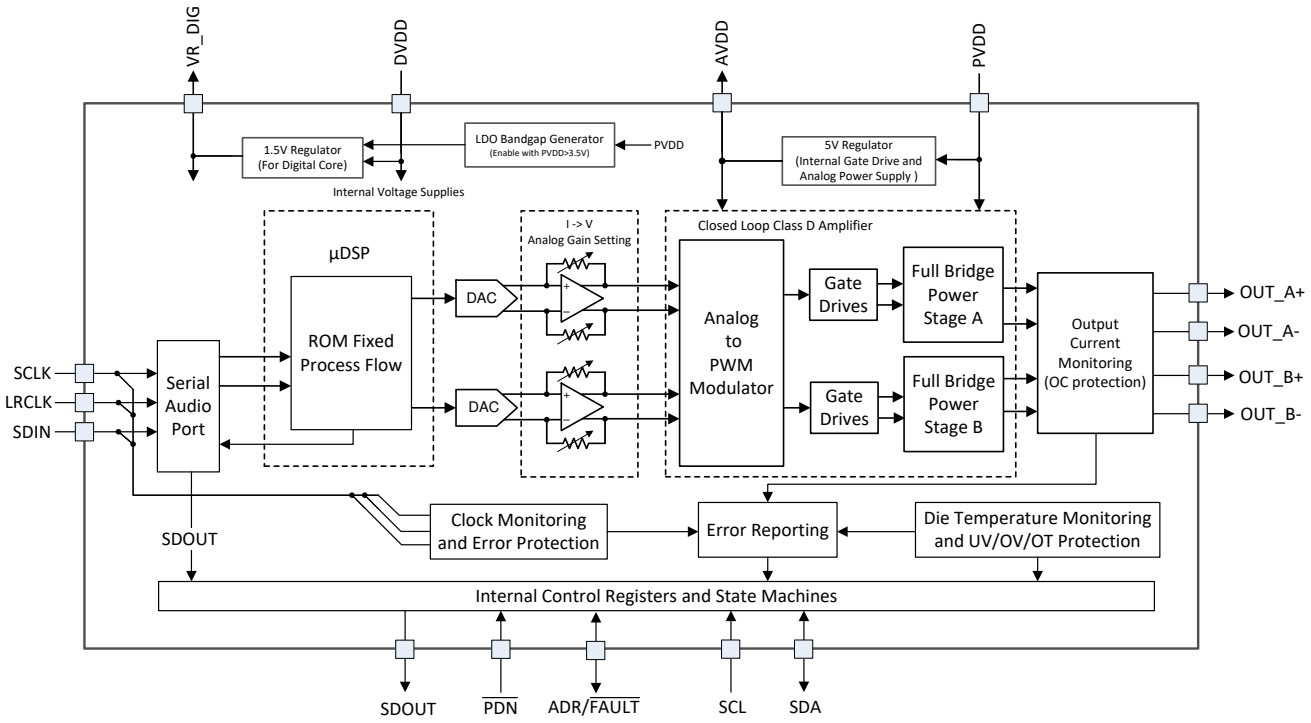
7.1 Overview

The TAS5822M device integrates 4 main building blocks together into a single cohesive device that maximizes sound quality, flexibility, and ease of use. The 4 main building blocks are listed as follows:

- A stereo Digital to PWM Coversion block.
- An Audio DSP subsystem.
- A flexible close-loop amplifier capable of operating in stereo or mono, at several different switching frequencies, and with a variety of output voltages and loads.
- An I^2C control port for communication with the device

The device requires only two power supplies for proper operation. A DVDD supply is required to power the low voltage digital circuitry. Another supply, called PVDD, is required to provide power to the output stage of the audio amplifier. One internal LDO converts PVDD to 5 V for GVDD and AVDD, another internal LDO converts DVDD to 1.5V VR_DIG for digital core.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Supplies

To facilitate system design, TAS5822M needs only a 3.3-V or 1.8-V supply in addition to the (typical) 12 V or 24 V power-stage supply. Two internal voltage regulators provide suitable voltage levels for the gate drive circuitry and internal circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors to filter the supply. Connecting external circuitry to these regulator outputs may result in reduced performance and damage to the device. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors. In order to provide good electrical and acoustical characteristics, the PWM signal path for the output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate bootstrap pins (BST_x). The gate drive voltages (AVDD) are derived from the PVDD voltage. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power-supply pins and decoupling capacitors must be avoided. For a properly functioning bootstrap circuit, a small ceramic

capacitor must be connected from each bootstrap pin (BST_x) to the power-stage output pin (OUT_x). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive regulator output pin (AVDD) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver.

7.3.2 Device Clocking

The TAS5822M devices have flexible systems for clocking. Internally, the device requires a number of clocks, mostly at related clock rates to function correctly. All of these clocks can be derived from the Serial Audio Interface.

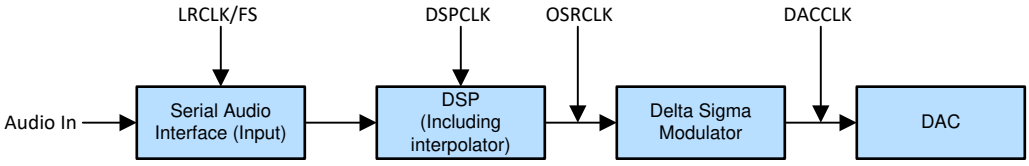


Figure 7-1. Audio Flow with Respective Clocks

Figure 7-1 shows the basic data flow and clock Distribution.

The Serial Audio Interface typically has 3 connection pins which are listed as follows:

- SCLK (Bit Clock)
- LRCLK/FS (Left Right Word Clock and Frame Sync)
- SDIN (Input Data)

The device has an internal PLL that is used to take SCLK and create the higher rate clocks required by the DSP and the DAC clock.

The device has an audio sampling rate detection circuit that automatically senses which frequency the sampling rate is operating. Common audio sampling frequencies of 32 kHz, 44.1kHz – 48 kHz, 88.2 kHz – 96 kHz are supported. The sampling frequency detector sets the clock for DAC and DSP automatically.

7.3.3 Serial Audio Port – Clock Rates

The serial audio interface port is a 3-wire serial port with the signals LRCLK/FS , SCLK and SDIN. SCLK is the serial audio bit clock, used to clock the serial data present on SDIN into the serial shift register of the audio interface. Serial data is clocked into the TAS5822M device on the rising edge of SCLK. The LRCK/FS pin is the serial audio left/right word clock or frame sync when the device is operated in TDM Mode.

Table 7-1. Audio Data Formats, Bit Depths and Clock Rates

FORMAT	DATA BITS	MAXIMUM LRCLK/FS FREQUENCY (kHz)	SCLK RATE (f_S)
I^2S/LJ/RJ	32, 24, 20, 16	32 to 96	64, 32
TDM	32, 24, 20, 16	32	128
		44.1,48	128,256,512
		96	128,256

Before DSP register initialize with I^2C during the startup , requires stable I^2S ready. When Clock halt, non-supported SCLK to LRCLK(FS) ratio is detected, the device reports Clock Error in Register 113 (Register Address 0x71).

7.3.4 Clock Halt Auto-recovery

As some of host processor will Halt the I^2S clock when there is no audio playing. When Clock halt, the device puts all channels into the Hi-Z state and reports Clock Error in Register 113 (Register Address 0x71). After audio clocks recovery, the device automatically returns to the previous state.

7.3.5 Sample Rate on the Fly Change

TAS5822M supports LRCLK(FS) rate on the fly change. For example, change LCRLK from 32kHz to 48kHz or 96kHz, Host processor needs to put the LRCLK(FS)/SCLK to Halt state at least 10ms before changing to the new sample rate.

7.3.6 Serial Audio Port - Data Formats and Bit Depths

The device supports industry-standard audio data formats, including standard I^2S, left-justified, right-justified and TDM/DSP data. Data formats are selected via Register (Register Address 0x33-D[5:4]). If the high width of LRCLK(FS) in TDM/DSP mode is less than 8 cycles of SCLK(BCLK), the register (Register Address 0x33-D[3:2]) should set to 01. All formats require binary two's complement, MSB-first audio data; up to 32-bit audio data is accepted. All the data formats, word length and clock rate supported by this device are shown in Table 1. The data formats are detailed in Figure 1 through Figure 6. The word length are selected via Register (Register Address 0x33-D[1:0]).Default setting is I^2S and 24 bit word length.

For TDM Mode, the offsets of data are selected via Register (Register Address 0x33-D[7-6]) and Register (Register Address 0x34-D[7:0]).

Table 7-2. TDM Slots vs FS

LRCLK(FS)	TDM Slots	Notes
48kHz	16	Each Slots's position (offset) can be set by Register 51 (Register address 0x33) and Register 52 (Register address 0x34).
96kHz	8	

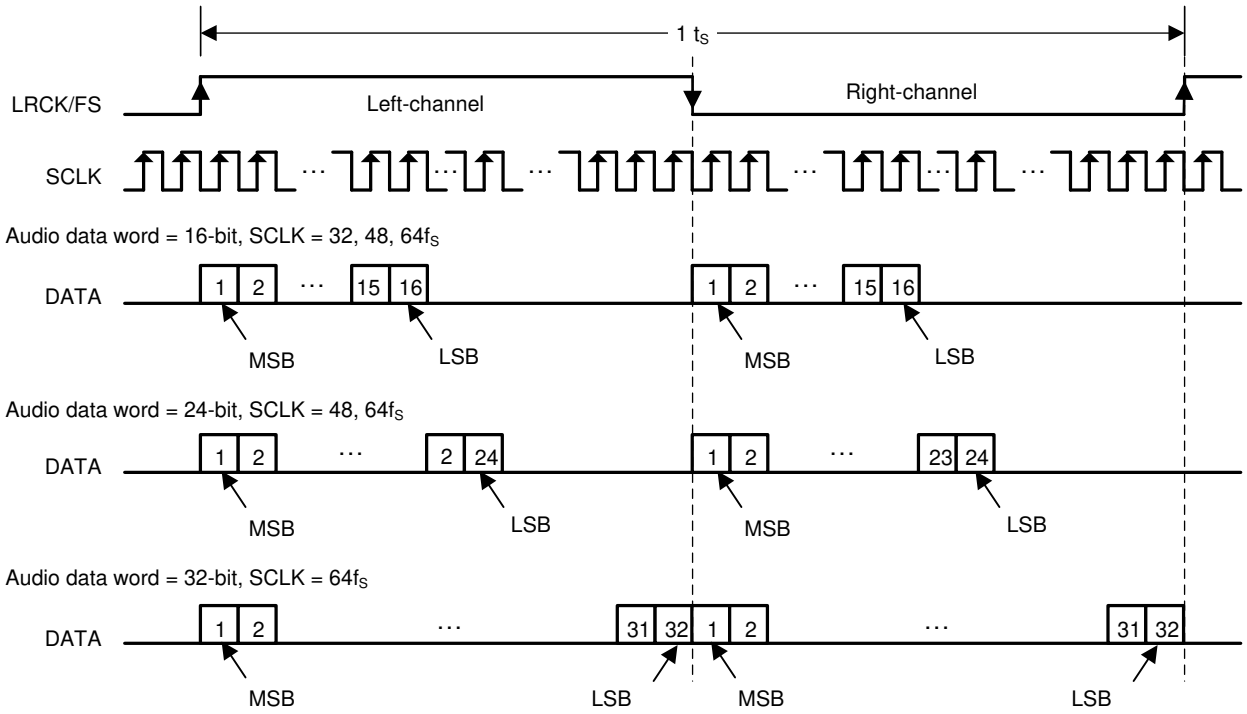
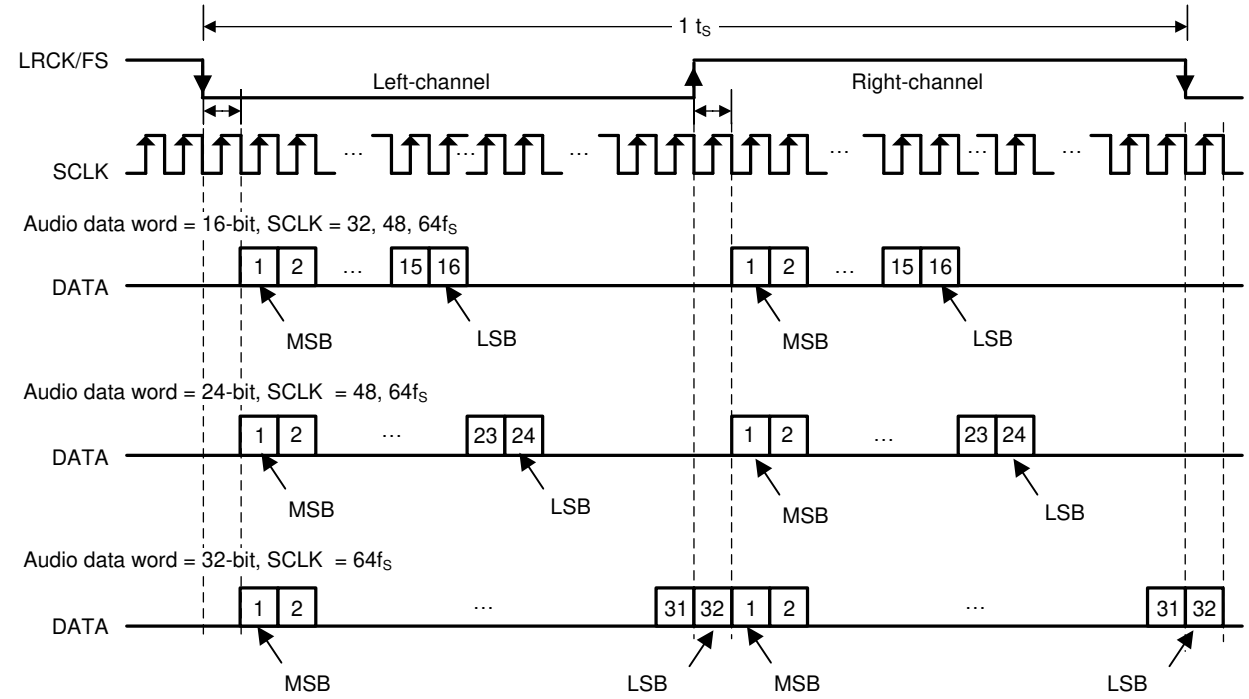
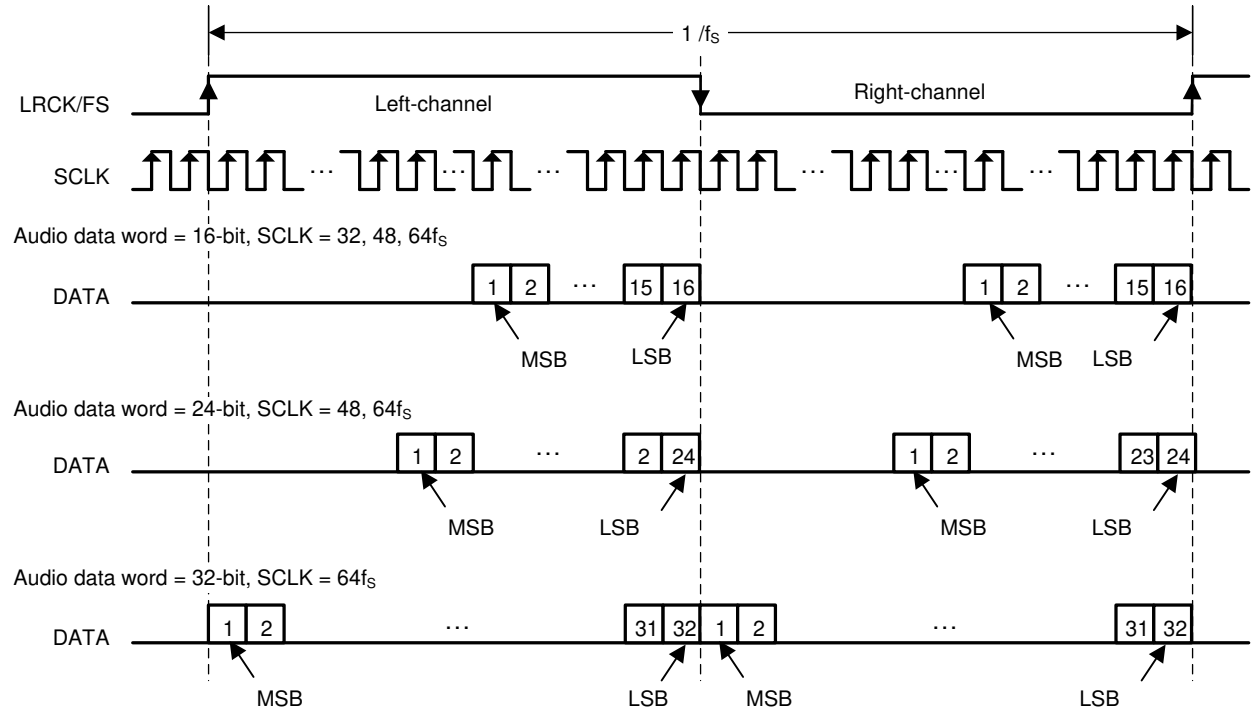


Figure 7-2. Left Justified Audio Data Format



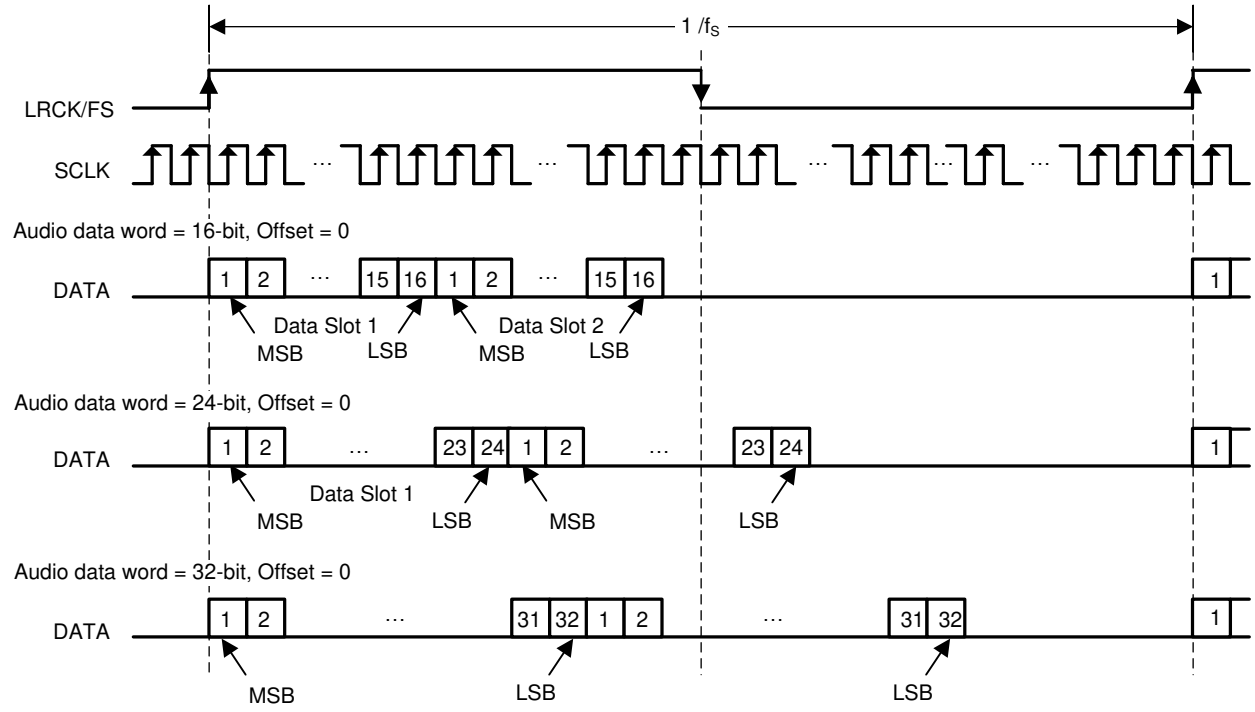
I²S Data Format; L-channel = LOW, R-channel = HIGH

Figure 7-3. I²S Audio Data Format



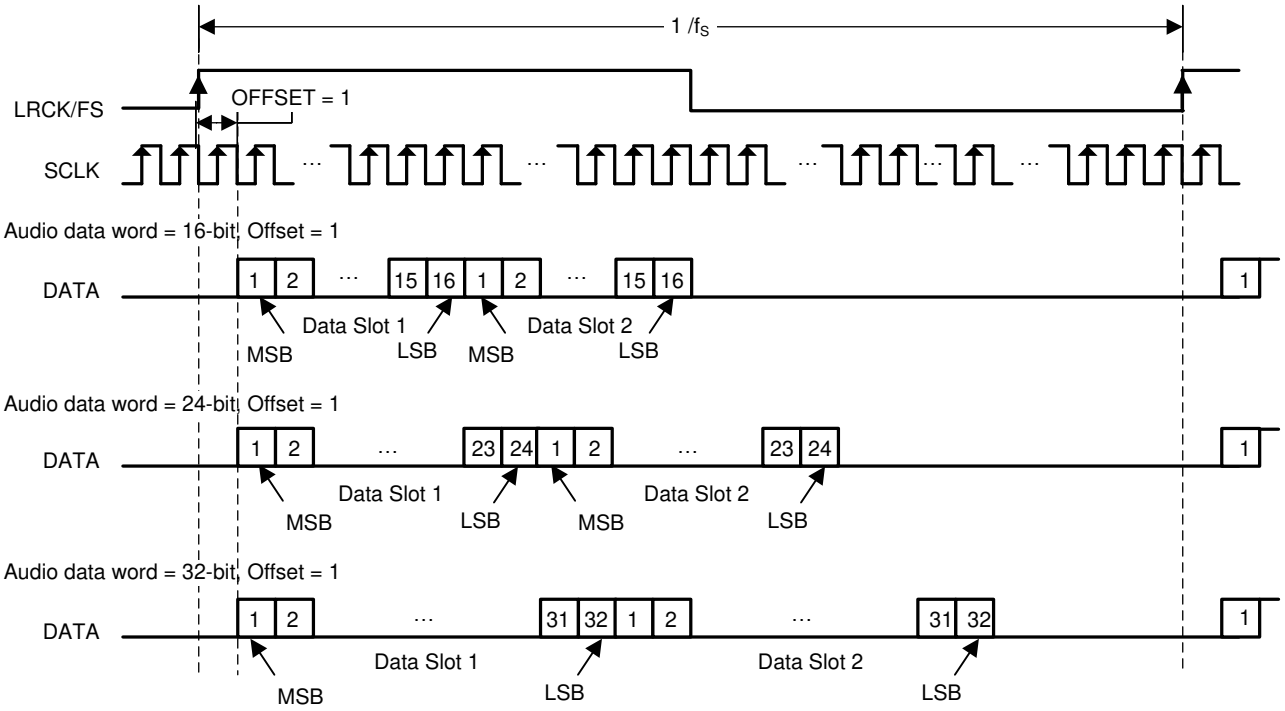
Right Justified Data Format; L-channel = HIGH, R-channel = LOW

Figure 7-4. Right Justified Audio Data Format



TDM Data Format with OFFSET = 0
In TDM Modes, Duty Cycle of LRCK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

Figure 7-5. TDM 1 Audio Data Format



TDM Data Format with OFFSET = 1
In TDM Modes, Duty Cycle of LRCLK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

Figure 7-6. TDM 2 Audio Data Format

7.3.7 Digital Audio Processing

TAS5822M DSP has a ROM fixed process flow which support 96kHz DSP sample rate. Request PPC3 tuning software for details.

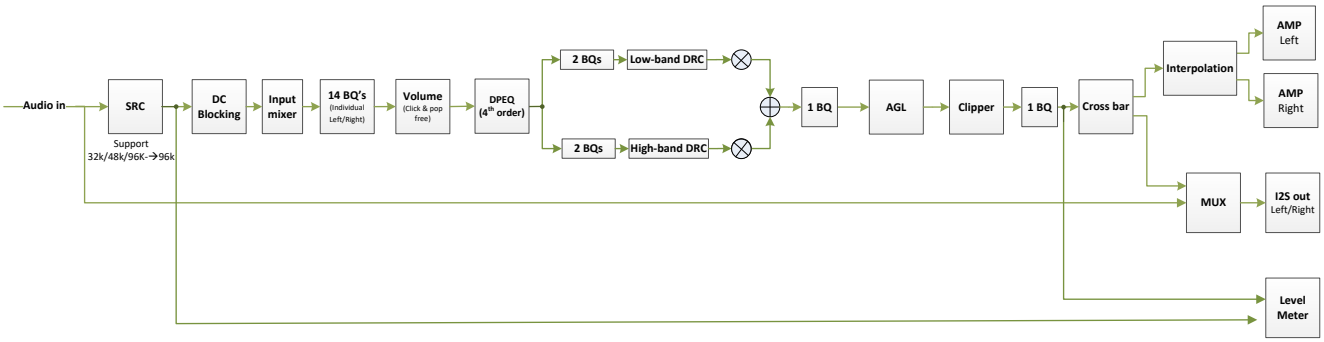


Figure 7-7. Audio Process Flow

7.3.8 Class D Audio Amplifier

Following the digital clipper, the interpolated audio data is next sent to the Closed Loop Class-D amplifier, whose first stage is Digital to PWM Conversion (DPC) block. In this block, the stereo audio data is translated into two pairs of complimentary pulse width modulated (PWM) signals which are used to drive the outputs of the speaker amplifier. Feedback loops around the DPC ensure constant gain across supply voltages, reduce distortion, and increase immunity to power supply injected noise and distortion. The analog gain is also applied in the Class-D amplifier section of the device.

7.3.8.1 Speaker Amplifier Gain Select

A combination of digital gain and analog gain is used to provide the overall gain of the speaker amplifier. As seen in Figure 7-8, the audio path of the device consists of a digital audio input port, a digital audio path, a stereo DAC, an analog to PWM modulator, a gate driver stage, a Class D power stage, and a feedback loop which feeds the output information back into the analog to PWM Modulator to correct for distortion sensed on the output pins. The total amplifier gain is comprised of digital gain, shown in the digital audio path and the analog gain from the input of the analog modulator to the output of the speaker amplifier power stage.

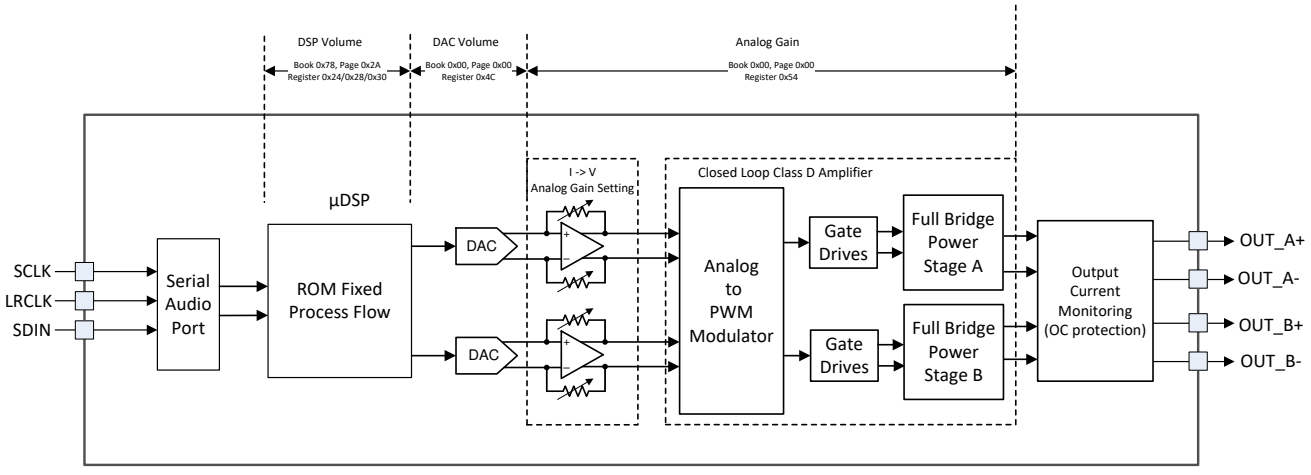


Figure 7-8. Speaker Amplifier Gain

As shown in Figure 7-8, the first gain stage for the speaker amplifier is present in the digital audio path. It consists of the DSP volume control and the DAC volume control. The volume control is set to 0dB by default. For all settings of the Register 0x54, AGAIN[4:0], the digital boost block remains at 0 dB. These gain settings ensure that the output signal is not clipping at different PVDD levels. 0dBFS output is 29.5-V peak output voltage

Table 7-3. Analog Gain Setting

AGAIN[4:0]	GAIN (dBFS)	AMPLIFIER OUTPUT PEAK VOLTAGE (V_P/FS)	AMPLIFIER OUTPUT PEAK VOLTAGE (dBV/FS)
00000 (Default Setting)	0 (Default Setting)	29.5V_P/FS (Default Setting)	29.4dBV
00001	-0.5	27.85V_P/FS	28.9dBV
00010	-1.0	26.29V_P/FS	28.4dBV
00011	-1.5	24.82V_P/FS	27.9dBV
…….	……..	…….	….
11111	-15.5	4.95V_P/FS	13.9dBV

Table 7-4. Example of Analog Gain Setting
(Based on 6Ω speaker Load, take 0.5Ω loss for PCB, Speaker wire, Inductor DCR and R_{DS}on)

DAC Input (µDSP Output) dBFS	Full Band AGL Threshold dBFS	PVDD V	Book0/Page0, Register 0x54, AGAIN[4:0]	Gain (dBFS)	Amplifier Output Peak Voltage V	Amplifier Output Peak Voltage dBV
0	0	24	00101	-2.5	22.5V (Without Clipping)	27dBV
		18	01010	-5	16.6V (Without Clipping)	24.35dBV
		13.5	01111	-7.5	12.46V (Without Clipping)	21.9dBV
-2.5	-2.5	24	00000	0	22.5V (Clipping or not, depends on AGL time constant tuning)	27dBV
-5	-5	18			16.6V (Clipping or not, depends on AGL time constant tuning)	24.35dBV
-7.5	-7.5	13.5			12.46V (Clipping or not, depends on AGL time constant tuning)	21.9dBV

7.4 Device Functional Modes

7.4.1 Software Control

The TAS5822M device is configured via an I^2C communication port.

The I^2C Communication Protocol is detailed in the I^2C Communication Port section. The I^2C timing requirements are described in the I^2C Bus Timing – Standard and I^2C Bus Timing – Fast sections.

7.4.2 Speaker Amplifier Operating Modes

The TAS5822M device can be used in two different amplifier configurations:

- BTL Mode
- PBTL Mode

7.4.2.1 BTL Mode

The familiar BTL mode of operation uses the TAS5822M device to amplify two independent signals, which represent the left and right portions of a stereo signal. The amplified left signal is presented on differential output pair shown as OUT_A+ and OUT_A-, the amplified right signal is presented on differential output pair shown as OUT_B+ and OUT_B-.

7.4.2.2 PBTL Mode

The PBTL mode of operation is used to describe operation in which the two outputs of the device are placed in parallel with one another to increase the power sourcing capabilities of the device. On the output side of the TAS5822M device, the summation of the devices can be done before the filter in a configuration called Pre-Filter Parallel Bridge Tied Load (PBTL). However, the two outputs can be required to merge together after the inductor portion of the output filter. Doing so does require two additional inductors, but allows smaller, less expensive

inductors to be used because the current is divided between the two inductors. The process is called Post-Filter PBTL. On the input side of the TAS5822M device, the input signal to the PBTL amplifier is left frame of I²S or TDM data.

7.4.3 Minimize EMI with Spread Spectrum

This device supports spread spectrum with triangle mode, Spread spectrum is used to minimize the EMI noise.

User need configure register SS_CTRL0 (0x6B) to Enable triangle mode and enable spread spectrum, and select spread spectrum frequency and range with SS_CTRL1 (0x6C). For 384kHz FSW which configured by DEVICE_CTRL1 (0x02), the spread spectrum frequency and range are described in Table 3.

Table 7-5. Spread Spectrum Setting

SS_TRI_CTRL[3:0]	0	1	2	3	4	5	6	7
Triangle Freq	24k				48k			
Spread Spectrum Range	5%	10%	20%	25%	5%	10%	20%	25%

User Application example-Central Switching Frequency is 384kHz, Triangle Frequency is 24kHz:

w 58 6b 03 //Enable Spread Spectrum

w 58 6c 03 //SS_TRI_CTRL[3:0]0011, Triangle Frequency = 24kHz, Spread Spectrum Range should be 25% (336kHz~432kHz)

7.4.4 Minimize EMI with channel to channel phase shift

This device support channel to channel 180 degree PWM phase shift to minimize the EMI. Bit 0 of Register 0x53 can be used to disable or enable the phase shift.

7.4.5 Minimize EMI with Multi-Devices PWM Phase Synchronization

This device support up to 4 phases selection for the multi devices application system. For example, when a system integrated 4 TAS5822M devices, user can select phase 0/1/2/3 for each device by register PHASE_CTRL (0x6A), which means there is a 45 degree phase shift between each device to minimize the EMI.

Recommend to do the Phase Synchronization with I²S clock during the Startup Phase.

1. Halt I²S clock.
2. Halt I²S clock.
3. Configure each device phase selection and enable the phase synchronization. For example: Register 0x6A = 0x03 for device 0; Register 0x6A = 0x07 for device 1; Register 0x6A = 0x0B for device 2; Register 0x6A = 0x0F for device 3. There should be a 45 degree PWM phase shift between each device to minimize the EMI.
4. Configure each device into Hi-Z mode.
5. Provide I²S to each device. Phase synchronization for all 4 devices will be automatically done by internal sequence.
6. Initialize the DSP code. (This step can be skipped if only need to do the PWM Phase Synchronization).
7. Device to Device PWM phase shift should be fixed with 45 degree.

7.4.6 Thermal Foldback

The Thermal Foldback (TFB) or Over temperature foldback, is designed to protect TAS5822M from excessive die temperature increases, in case the device operates beyond the recommended temperature/power limit, or with a weaker thermal system design than recommended. It allows the TAS5822M to play as loud as possible without triggering unexpected thermal shutdown. When the die temperature triggers the over-temperature warning (OTW) level (135C typ), an internal AGL (Automatic Gain Limiter) will reduce the digital gain automatically. Once the die temperature drops below the OTW, the device's digital gain gradually returns to the former setting. Both the attenuation gain and adjustable rate are programmable. The TFB gain regulation speed

(attack rate and release rate) settings are the same as a regular AGL, which is also configurable with TAS5822M tuning software.

7.4.7 Device State Control

TAS5822M has 5 states with different power dissipation which listed in the Electrical Characteristics Table.

- Shutdown Mode. With $\overline{\text{PDN}}$ pin pull down to GND. All internal LDOs (1.5V for digital core, 5V for analog) are disabled, all registers will be cleared to default value.

Note

Exit from Shutdown Mode and re-enter into Play mode, need follow up the start-up sequence and reload all register configurations (which generated by TAS5822M tuning software) again.

- Deep Sleep Mode. Deep Sleep Mode. Register 0x03h -D[1:0]=00, device stays in Deep Sleep Mode. In this mode, I2C block and 1.5V LDO for digital core still working, but internal 5V LDO (For AVDD and MOSFET gate driver) is disabled for low power dissipation. This mode can be used to extend the battery life in some portable speaker applications. If the host processor stops playing audio for a long time, can be set to Deep Sleep Mode to minimize power dissipation until host processor starts playing audio again. Unlike the Shutdown Mode (Pulling $\overline{\text{PDN}}$ Low), entering or exiting Deep Sleep Mode, the DSP keeps active.
- Sleep Mode. Register 0x03h -D[1:0]=01, device stays in Sleep Mode. In this mode, I^2C block, Digital core, DSP Memory , 5V Analog LDO are stilling working. Unlike the Shutdown Mode (Pull $\overline{\text{PDN}}$ Low), enter or exit Sleep Mode, DSP is kept active. Exit from this mode and re-enter into play mode, only need to set Register 0x03h -D[1:0]=11.
- Output Hiz Mode. Register 0x03h -D[1:0]=10, device stays in Hiz Mode. In this mode, only output driver is set to be Hi-Z state, all other block operate normally. Exit from this mode and re-enter into play mode, only need to set Register 0x03h -D[1:0]=11.
- Play Mode. Register 0x03h -D[1:0]=11, device stays in Play Mode.

7.4.8 Device Modulation

TAS5822M has 3 modulation schemes: BD Modulation, 1SPW modulation and Hybrid modulation. Select modulation schemes for with Register 0x02 [1:0]-DAMP_MOD.

7.4.8.1 BD Modulation

This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires. Each output is switching from 0 volts to the supply voltage. The OUTPx and OUTNx are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTPx is greater than 50% and OUTNx is less than 50% for positive output voltages. The duty cycle of OUTPx is less than 50% and OUTNx is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.

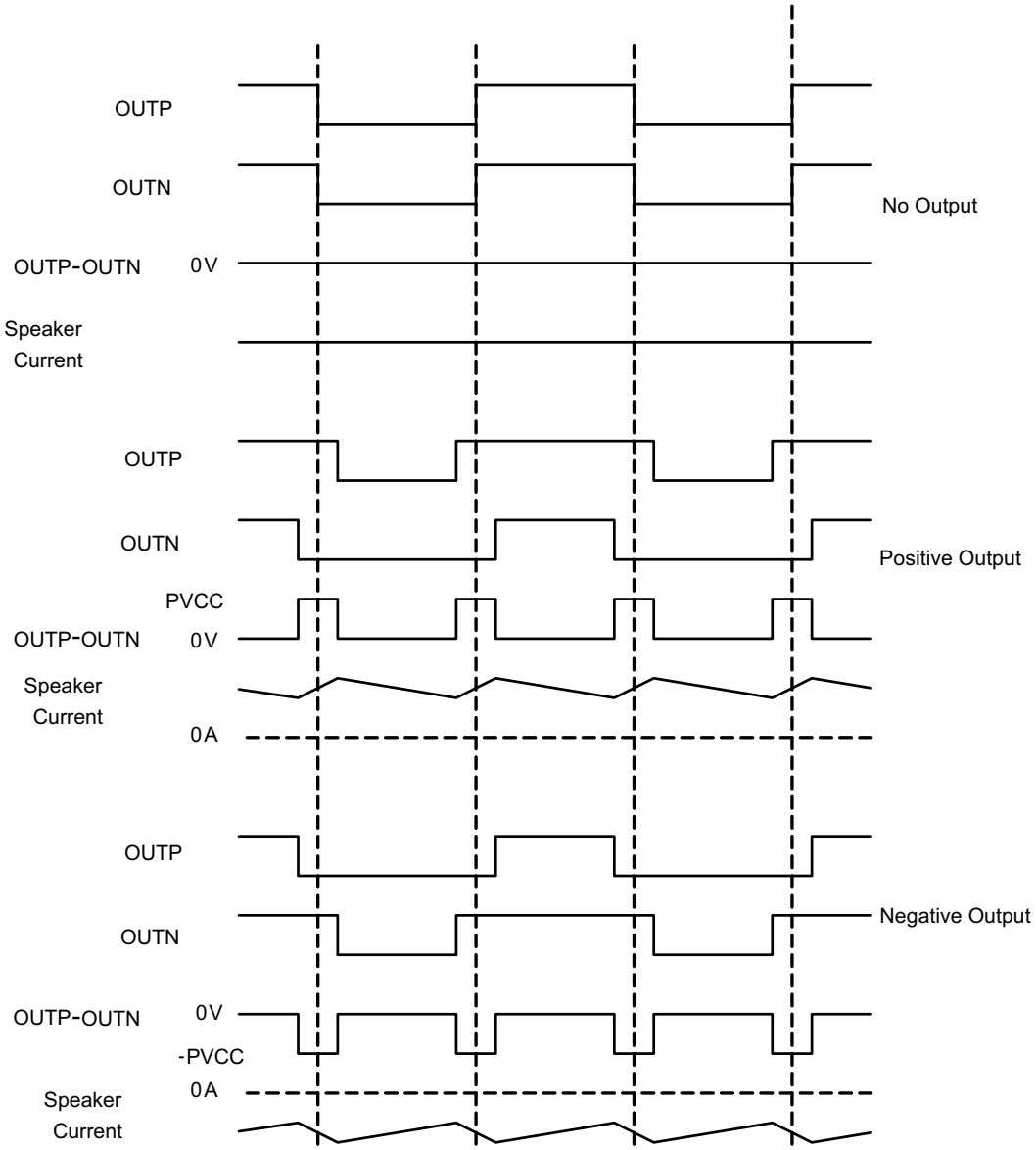


Figure 7-9. BD Mode Modualtion

7.4.8.2 1SPW Modulation

The 1SPW mode alters the normal modulation scheme in order to achieve higher efficiency with a slight penalty in THD degradation and more attention required in the output filter selection. In Low Idle Current mode the outputs operate at ~17% modulation during idle conditions. When an audio signal is applied one output will decrease and one will increase. The decreasing output signal will quickly rail to GND at which point all the audio modulation takes place through the rising output. The result is that only one output is switching during a majority of the audio cycle. Efficiency is improved in this mode due to the reduction of switching losses.

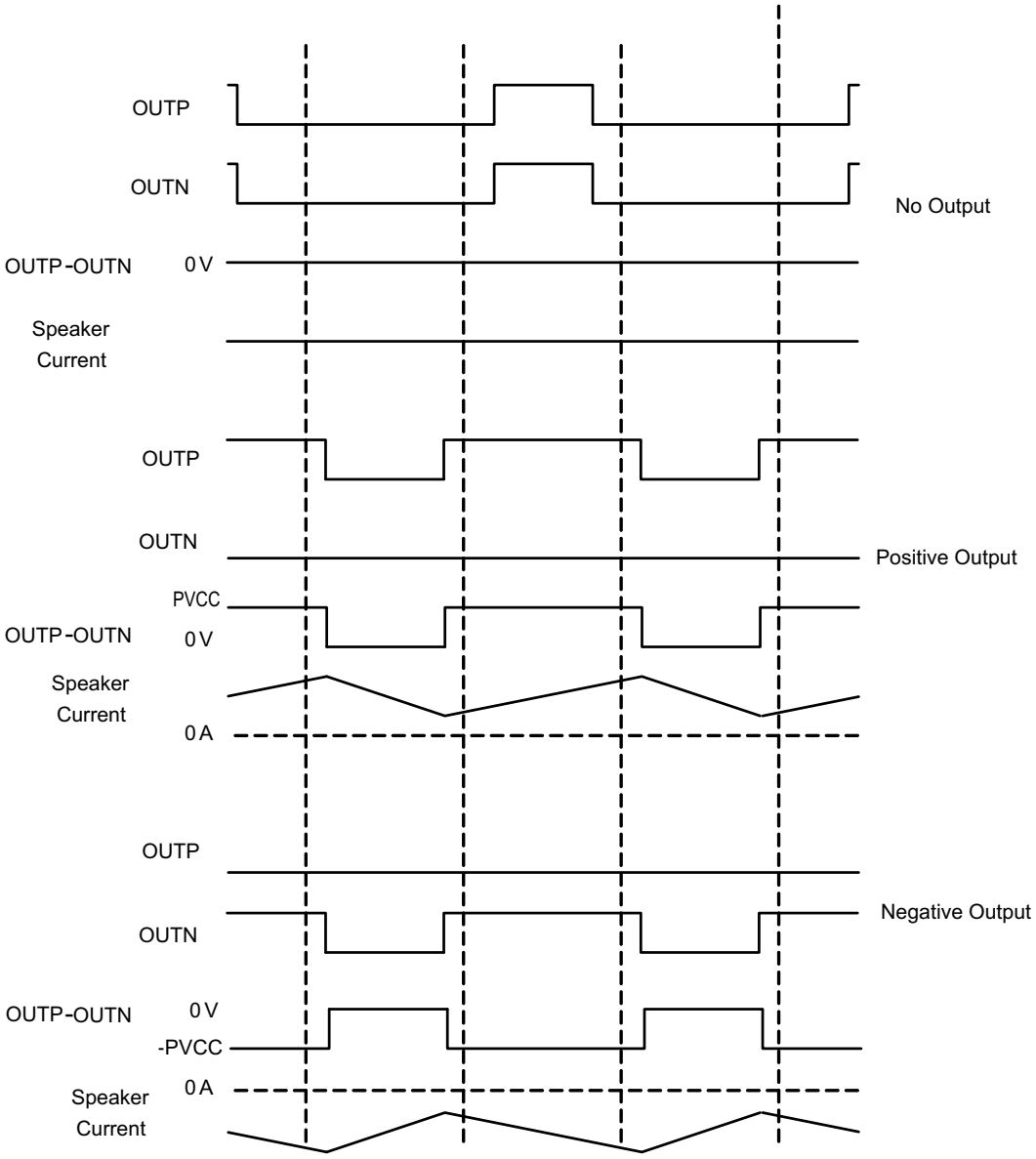


Figure 7-10. 1SPW Mode Modulation

7.4.8.3 Hybrid Modulation

Hybrid Modulation is designed to minimized power loss without compromising the THD+N performance, and is optimized for battery-powered applications. With Hybrid modulation enabled, device detects the input signal level and adjust PWM duty cycle dynamically based on PVDD. Hybrid modulation achieves ultra low idle current and maintains the same audio performance level as the BD Modulation. In order to minimize the power dissipation, low switching frequency (For example, Fsw = 384 kHz) with proper LC filter (15 µH + 0.68 µF or 22 µH + 0.68 µF) is recommended.

Note

1) With Hybrid Modulation, users need to input the system's PVDD value via device development App.

2) With Hybrid Modulation, Change device state from Deep Sleep Mode to Play Mode, specific sequence is required:

1. Set device's PWM Modulation to BD or 1SPW mode via Register (Book0/Page0/Register0x02h, Bit [1:0]).
2. Set device to Hi-Z state via Register (Book0/Page0/Register0x03h, Bit [1:0]).
3. Delay 2ms.
4. Set device's PWM Modulation to Hybrid mode via Register (Book0/Page0/Register0x02h, Bit [1:0]).
5. Delay 15ms.
6. Set device to Play state via Register (Book0/Page0/Register0x03h, Bit [1:0]).

7.5 Programming and Control

7.5.1 I^{2}C Serial Communication Bus

The device has a bidirectional serial control interface that is compatible with the Inter IC (I^2)C bus protocol and supports 100 and 400-kHz data transfer rates for random and sequential write and read operations as a slave device. Because the TAS5822M register map and DSP memory spans multi pages, the user should change from page to page before writing individual register or DSP memory. Changing from page to page is accomplished via register 0 on each page. This register value selects the page address, from 0 to 255.

7.5.2 Slave Address

The TAS5822M device has 7 bits for the slave address. The first five bits (MSBs) of the slave address are factory preset to 01011(0x5x). The next two bits of address byte are the device select bits which can be user-defined by ADR/ $\overline{\text{FAULT}}$ pin in Table 7-6.

Table 7-6. I^{2}C Slave Address Configuration

ADR/ $\overline{\text{FAULT}}$ PIN Configuration	MSBs					User Define		LSB
4.7k Ω to DVDD	0	1	0	1	1	0	0	R/ $\overline{\text{W}}$
15kΩ to DVDD	0	1	0	1	1	0	1	R/ $\overline{\text{W}}$
47kΩ to DVDD	0	1	0	1	1	1	0	R/ $\overline{\text{W}}$
120kΩ to DVDD	0	1	0	1	1	1	1	R/ $\overline{\text{W}}$

7.5.2.1 Random Write

As shown in Figure 7-11, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I^{2}C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit is a 0. After receiving the correct I^{2}C device address and the read/write bit, the device responds with an acknowledge bit. Next, the master transmits the address byte corresponding to the internal memory address being accessed. After receiving the address byte, the device again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the device again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

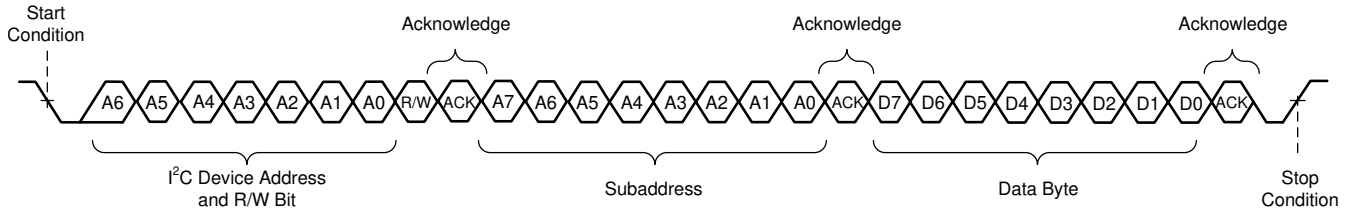


Figure 7-11. Random Write Transfer

7.5.2.2 Sequential Write

A sequential data-write transfer is identical to a single-byte data-write transfer except that multiple data bytes are transmitted by the master to the device as shown in Figure 7-12. After receiving each data byte, the device responds with an acknowledge bit and the I^2 subaddress is automatically incremented by one.

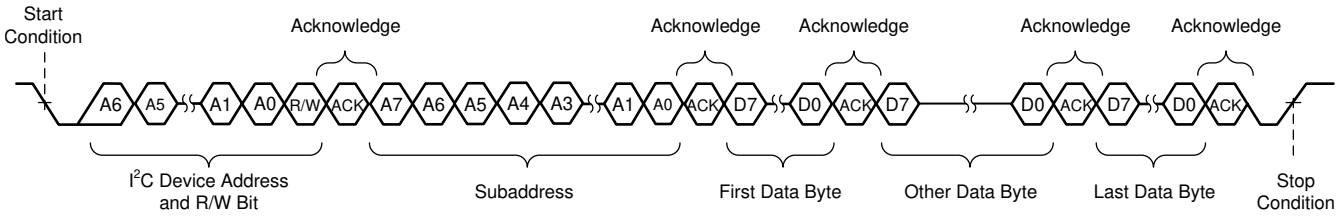


Figure 7-12. Sequential Write Transfer

7.5.2.3 Random Read

As shown in Figure 7-13, a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I^{2}C device address and the read/write bit. For the data-read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is a 0. After receiving the address and the read/write bit, the device responds with an acknowledge bit. In addition, after sending the internal memory address byte, the master device transmits another start condition followed by the address and the read/write bit again. This time the read/write bit is a 1, indicating a read transfer. After receiving the address and the read/write bit, the device again responds with an acknowledge bit. Next, the device transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data-read transfer.

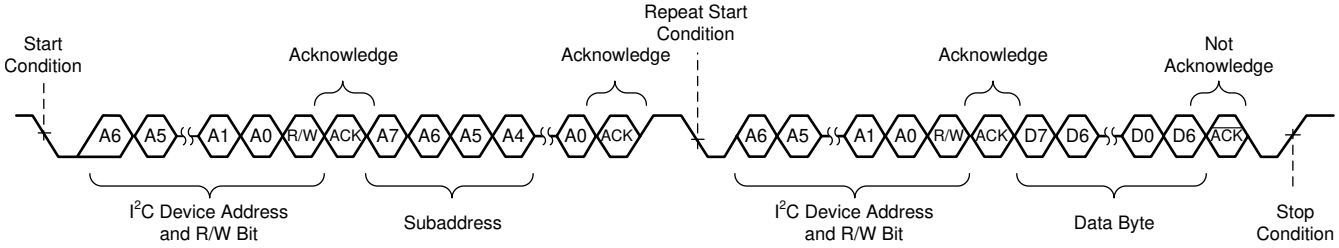


Figure 7-13. Random Read Transfer

7.5.2.4 Sequential Read

A sequential data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the device to the master device as shown in Figure 7-14. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte and automatically increments the I^{2}C sub address by one. After receiving the last data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the transfer.

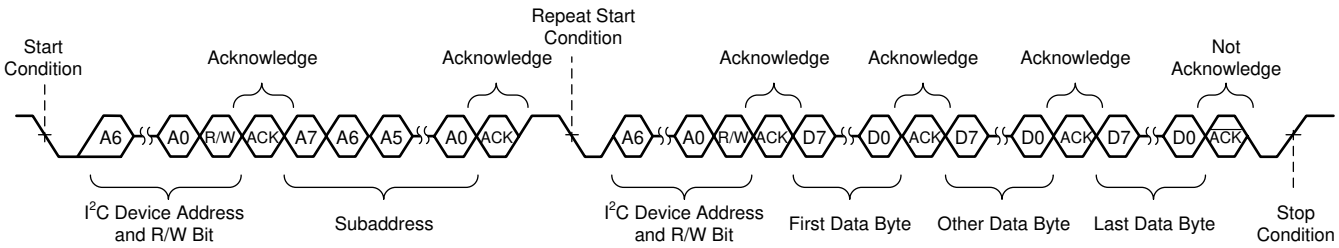


Figure 7-14. Sequential Read Transfer

7.5.2.5 DSP Memory Book, Page and BQ update

The TAS5822M device supports the I^{2}C serial bus and the data transmission protocol for standard and fast mode as a slave device.

The DSP memory is arranged in books, pages, and registers. Each book has several pages and each page has several registers.

Because the TAS5822M register map spans several books and pages, the user must select the correct book and page before writing individual register bits or bytes.

To change the book, the user must be on page 0x00. In register 0x7f on page 0x00 you can change the book. On page 0x00 of each book, register 0x7f is used to change the book. Register 0x00 of each page is used to change the page. To change a book first write 0x00 to register 0x00 to switch to page 0 then write the book number to register 0x7f on page 0. To change between pages in a book, simply write the page number to register 0x00.

All the Biquad Filters coefficients are addressed in Book 0xAA. The five coefficients of every Biquad Filter should be written entirely and sequentially from the lowest address to the highest.

7.5.2.6 Example Use

Example 1, The following is a sample script for configuring a device on I^{2}C slave address 0x58 and set the device switching frequency to 768kHz with Class D loop bandwidth to 175kHz, 1SPW Modulation:

w 58 00 00 #Go to Page0

w 58 7f 00 #Change the Book to 0x00

w 58 00 00 #Go to Page 0x00

w 58 02 01 #Set switching frequency to 768kHz with 1SPW Modulation

w 58 53 60 #Set Class D Loop Bandwidth to 175kHz

Example 2, The following is a sample script for configuring a device on I^{2}C slave address 0x58 and using the DSP host memory to change the digital volume to the default value of 0dB:

w 58 00 00 #Go to Page 0

w 58 7f 8c #Change the Book to 0x8C

w 58 00 2a #Go to Page 0x2a

w 58 24 00 80 00 00 #change digital volume to 0dB

7.5.2.7 Checksum

This device supports two different check sum schemes, a cyclic redundancy check (CRC) checksum and an Exclusive (XOR) checksum. Register reads do not change checksum, but writes to even nonexistent registers will change the checksum. Both checksums are 8-bit checksums and both are available together simultaneously. The checksums can be reset by writing a starting value (eg. 0x 00 00 00 00) to their respective 4-byte register locations.

7.5.2.7.1 Cyclic Redundancy Check (CRC) Checksum

The 8-bit CRC checksum used is the 0x7 polynomial (CRC-8-CCITT I.432.1; ATM HEC, ISDN HEC and cell delineation, (1 + x1 + x2 + x8)). A major advantage of the CRC checksum is that it is input order sensitive. The CRC supports all I^{2}C transactions, excluding book and page switching. The CRC checksum is read from register 0x7E on page0 of any book (B_x, Page_0, Reg_126). The CRC checksum can be reset by writing 0x00 to the same register locations where the CRC checksum is valid.

7.5.2.7.2 Exclusive or (XOR) Checksum

The Xor checksum is a simpler checksum scheme. It performs sequential XOR of each register byte write with the previous 8-bit checksum register value. XOR supports only Book 0x8C, and excludes page switching and all

registers in Page 0x00 of Book 0x8C. XOR checksum is read from location register 0x7D on page 0x00 of book 0x8C (B_140, Page_0, Reg_125). The XOR Checksum can be reset by writing 0x00 to the same register location where it is read.

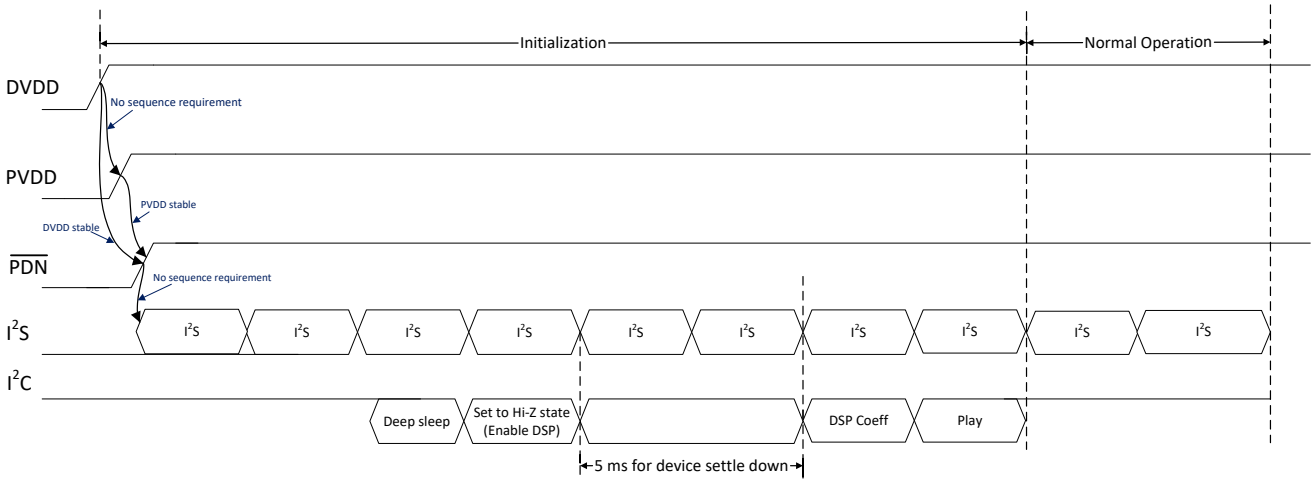
7.5.3 Control via Software

- Startup Procedures
- Shutdown Procedures

7.5.3.1 Startup Procedures

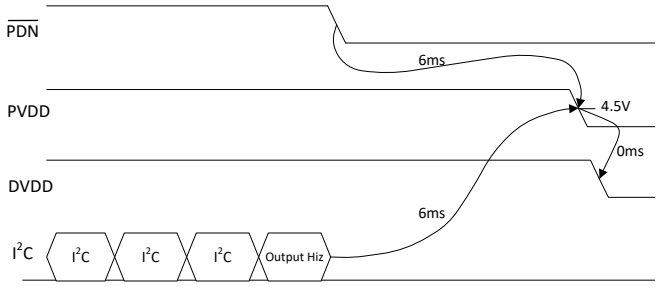
1. Configure ADR/ $\overline{\text{FAULT}}$ pin with proper setting for I^{2}C device address.
2. Bring up power supplies (it does not matter if PVDD or DVDD comes up first).
3. Once all power supplies are stable, bring up the $\overline{\text{PDN}}$ HIGH.
4. Once I^{2}S clock are stable, configure the device via the I^{2}C control port based on the user cases (Make sure the $\overline{\text{PDN}}$ pin = HIGH before I^{2}C control port operating).
5. The device is now in normal operation.

Figure 7-15. Startup sequence



7.5.3.2 Shutdown Procedures

1. The device is in normal operation.
2. Configure the Register 0x03h -D[1:0]=00 (DEEP SLEEP) via the I^{2}C control port or Pull $\overline{\text{PDN}}$ low.
3. The clocks can now be stopped and the power supplies brought down.
4. The device is now fully shutdown and powered off.



- Before PVDD/DVDD power down, Class D Output driver needs to be disabled by $\overline{\text{PDN}}$ or by I^{2}C.
- At least 6ms delay needed based on LRCLK (Fs) = 48kHz,Digital volume ramp down update every sample period, decreased by 0.5dB for each update, digital volume =24dB. Change the value of register 0x4C and 0x4E or change the LRCLK rate, the delay changes.

Figure 7-16. Power down sequence

7.5.3.3 Protection and Monitoring

7.5.3.3.1 Over current Shutdown (OCSD)

Under severe short-circuit event, such as a short to PVDD or ground, the device uses a peak-current detector, and the affected channel shuts down in < 100 ns if the peak current are enough. The shutdown speed depends on a number of factors, such as the impedance of the short circuit, supply voltage, and switching frequency. The user may restart the affected channel via I^2C. An OCSD event activates the fault pin, and the I^2C fault register saves a record. If the supply or ground short is strong enough to exceed the peak current threshold but not severe enough to trigger the OSCD, the peak current limiter prevents excess current from damaging the output FETs, and operation returns to normal after the short is removed.

7.5.3.3.2 Speaker DC Protection

If the device measures a >1.9 V (Typical) DC offset and continue more than 570 ms (typical) on the output stage, the ADR/ $\overline{\text{FAULT}}$ line will be pulled low and set the OUTxx outputs to Hi-Z state to protect speaker, signifying a fault in Register 0x70 in Book0/Page0. This fault report bit in Register 0x70 keeps 1 and device keeps in Hi-Z mode unless clear it by Register 0x78 in Book0/Page0 manually.

7.5.3.3.3 Device Over Temperature Protection

Once the die temperature exceed 160°C (Typical), device will set the output driver from Play mode to Hi-Z Mode. Over temperature shutdown fault reported by Register 0x72 in Book0/Page0. Set this fault's behavior to Auto-recovery mode, device will come back to play mode automatically once the die temperature drop down to 150°C or device needs re-enter into play mode by clearing fault with Register 0x78 in Book0/Page0.

7.5.3.3.4 Over Voltage Protection

Once the PVDD voltage exceed the $OVE_{THRES(PVDD)}$ (28.1 V Typical), device will set the output driver from Play mode to Hi-Z mode. Over voltage fault reported by Register 0x71 in Book0/Page0. Once PVDD drop below 27.5 V (Typical), device will come back to Play mode. But this bit still keeps 1 unless clear it by Register 0x78 in Book0/Page0 manually.

7.5.3.3.5 Under Voltage Protection

Once the PVDD voltage drop below the $UVE_{THRES(PVDD)}$ (4 V Typical), device will set the output driver from Play mode to Hi-Z mode. Under voltage fault reported by Register 0x71 in Book0/Page0. Once PVDD rise above 4.25 V (Typical), device will come back to Play mode. But this bit still keeps 1 unless clear it by Register 0x78 in Book0/Page0 manually.

7.5.3.3.6 Clock Fault

Once there has any Clock error occurs (Clock Halt, SCLK/LRCLK Ratio Error, Pll unlock, FS error) , Register 0x37 and Register 0x39 monitor these errors and real-time report with details, device will enter into Hi-Z mode. Clock Fault reported in Register 0x71 in Book0/Page0. Once the clock error been removed, device will come back to play mode automatically. But this bit still keeps 1 unless clear it by Register 0x78 in Book0/Page0 manually.

7.6 Register Maps

7.6.1 CONTROL PORT Registers

Table 7-7 lists the memory-mapped registers for the CONTROL PORT. All register offset addresses not listed in Table 7-7 should be considered as reserved locations and the register contents should not be modified.

Table 7-7. CONTROL PORT Registers

Offset	Acronym	Register Name	Section
1h	RESET_CTRL	Register 1	Section 7.6.1.1
2h	DEVICE_CTRL_1	Register 2	Section 7.6.1.2
3h	DEVICE_CTRL_2	Register 3	Section 7.6.1.3
Fh	I2C_PAGE_AUTO_INC	Register 15	Section 7.6.1.4
28h	SIG_CH_CTRL	Register 40	Section 7.6.1.5
29h	CLOCK_DET_CTRL	Register 41	Section 7.6.1.6
30h	SDOUT_SEL	Register 48	Section 7.6.1.7
31h	I2S_CTRL	Register 49	Section 7.6.1.8
33h	SAP_CTRL1	Register 51	Section 7.6.1.9
34h	SAP_CTRL2	Register 52	Section 7.6.1.10
35h	SAP_CTRL3	Register 53	Section 7.6.1.11
37h	FS_MON	Register 55	Section 7.6.1.12
38h	BCK_MON	Register 56	Section 7.6.1.13
39h	CLKDET_STATUS	Register 57	Section 7.6.1.14
4Ch	DIG_VOL	Register 76	Section 7.6.1.15
4Eh	DIG_VOL_CTRL1	Register 78	Section 7.6.1.16
4Fh	DIG_VOL_CTRL2	Register 79	Section 7.6.1.17
50h	AUTO_MUTE_CTRL	Register 80	Section 7.6.1.18
51h	AUTO_MUTE_TIME	Register 81	Section 7.6.1.19
52h	AMUTE_DELAY	Register 82	Section 7.6.1.20
53h	ANA_CTRL	Register 83	Section 7.6.1.21
54h	AGAIN	Register 84	Section 7.6.1.22
5Ch	BQ_WR_CTRL1	Register 92	Section 7.6.1.23
5Dh	DAC_CTRL	Register 93	Section 7.6.1.24
60h	ADR_PIN_CTRL	Register 96	Section 7.6.1.25
61h	ADR_PIN_CONFIG	Register 97	Section 7.6.1.26
66h	DSP_MISC	Register 102	Section 7.6.1.27
67h	DIE_ID	Register 103	Section 7.6.1.28
68h	POWER_STATE	Register 104	Section 7.6.1.29
69h	AUTOMUTE_STATE	Register 105	Section 7.6.1.30
6Ah	PHASE_CTRL	Register 106	Section 7.6.1.31
6Bh	SS_CTRL0	Register 107	Section 7.6.1.32
6Ch	SS_CTRL1	Register 108	Section 7.6.1.33
6Dh	SS_CTRL2	Register 109	Section 7.6.1.34
6Eh	SS_CTRL3	Register 110	Section 7.6.1.35
6Fh	SS_CTRL4	Register 111	Section 7.6.1.36
70h	CHAN_FAULT	Register 112	Section 7.6.1.37
71h	GLOBAL_FAULT1	Register 113	Section 7.6.1.38
72h	GLOBAL_FAULT2	Register 114	Section 7.6.1.39
73h	OT WARNING	Register 115	Section 7.6.1.40
74h	PIN_CONTROL1	Register 116	Section 7.6.1.41

Table 7-7. CONTROL PORT Registers (continued)

Offset	Acronym	Register Name	Section
75h	PIN_CONTROL2	Register 117	Section 7.6.1.42
78h	FAULT_CLEAR	Register 120	Section 7.6.1.44

Complex bit access types are encoded to fit into small table cells. Table 7-8 shows the codes that are used for access types in this section.

Table 7-8. CONTROL PORT Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.1.1 RESET_CTRL Register (Offset = 1h) [reset = 0x00]

RESET_CTRL is shown in Figure 7-13 and described in Table 7-9.

Return to Table 7-7.

Figure 7-13. RESET_CTRL Register

7	6	5	4	3	2	1	0
RESERVED			RST_MOD	RESERVED			RST_REG
R/W			W	R			W

Table 7-9. RESET_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	This bit is reserved
4	RST_MOD	W	0	WRITE CLEAR BIT Reset Modules WRITE CLEAR BIT Reset full digital core This bit resets full digital signal chain (Include DSP and Control Port Registers). Since the DSP is also reset, the coeffient RAM content will also be cleared by the DSP. 0: Normal 1: Reset modules
3-1	RESERVED	R	000	This bit is reserved
0	RST_CONTROL_REG	W	0	WRITE CLEAR BIT Reset Registers This bit resets the control port registers back to their initial values. The RAM content is not cleared. 0: Normal 1: Reset control port registers

7.6.1.2 DEVICE_CTRL_1 Register (Offset = 2h) [reset = 0x00]

DEVICE_CTRL_1 is shown in Figure 7-14 and described in Table 7-10.

Return to Table 7-7.

Figure 7-14. DEVICE_CTRL_1 Register

7	6	5	4	3	2	1	0
RESERVED	FSW_SEL			RESERVED	DAMP_PBTL	DAMP_MOD	
R/W	R/W			R/W	R/W	R/W	

Table 7-10. DEVICE_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6-4	FSW_SEL	R/W	000	SELECT FSW. 000:768K 001:384K 010:310K 011:480K 100:576K 101:1.024MHz 110:Reserved 111:Reserved
3	RESERVED	R/W	0	This bit is reserved
2	DAMP_PBTL	R/W	0	0: SET DAMP TO BTL MODE 1:SET DAMP TO PBTL MODE
1-0	DAMP_MOD	R/W	00	00: BD MODE 01: 1SPW MODE (Recommended) 10: HYBRID MODE (Recommended)

7.6.1.3 DEVICE_CTRL_2 Register (Offset = 3h) [reset = 0x10]

DEVICE_CTRL_2 is shown in Figure 7-15 and described in Table 7-11.

Return to Table 7-7.

Figure 7-15. DEVICE_CTRL_2 Register

7	6	5	4	3	2	1	0
RESERVED			DIS_DSP	MUTE	RESERVED	CTRL_STATE	
R/W			R/W	R/W	R/W	R/W	

Table 7-11. DEVICE_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	This bit is reserved
4	DIS_DSP	R/W	1	DSP reset When the bit is made 0, DSP will start powering up and send out data. This needs to be made 0 only after all the input clocks are settled so that DMA channels do not go out of sync. 0: Normal operation 1: Reset the DSP
3	MUTE	R/W	0	Mute both Left Channel and Right Channel This bit issues soft mute request for the left channel and right channel. The volume will be smoothly ramped down/up to avoid pop/click noise. 0: Normal volume 1: Mute
2	Reserved	R/W	0	This bit is reserved
1-0	CTRL_STATE	R/W	00	Device state control register 00: Deep Sleep 01: Sleep 10: Hiz, 11: PLAY

7.6.1.4 I2C_PAGE_AUTO_INC Register (Offset = Fh) [reset = 0x00]

I2C_PAGE_AUTO_INC is shown in Figure 7-16 and described in Table 7-12.

Return to Table 7-7.

Figure 7-16. I2C_PAGE_AUTO_INC Register

7	6	5	4	3	2	1	0
RESERVED				PAGE_AUTOINC_REG	RESERVED		
R/W				R/W	R/W		

Table 7-12. I2C_PAGE_AUTO_INC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	This bit is reserved
3	PAGE_AUTOINC_REG	R/W	0	Page auto increment disable Disable page auto increment mode. for non -zero books. When end of page is reached it goes back to 8th address location of next page when this bit is 0. When this bit is 1 it goes to 0 th location of current page itself like in older part. 0: Enable Page auto increment 1: Disable Page auto increment
2-0	RESERVED	R/W	000	This bit is reserved

7.6.1.5 SIG_CH_CTRL Register (Offset = 28h) [reset = 0x00]

SIG_CH_CTRL is shown in Figure 7-17 and described in Table 7-13.

Return to Table 7-7.

Figure 7-17. SIG_CH_CTRL Register

7	6	5	4	3	2	1	0
BCK_RATIO_CONFIGURE				FS_MODE			
R/W				R/W			

Table 7-13. SIG_CH_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BCK_RATIO_CONFIGURE	R/W	0000	These bits indicate the configured BCK ratio, the number of BCK clocks in one audio frame. 4'b0011:32FS 4'b0101:64FS 4'b0111:128FS 4'b1001:256FS 4'b1011:512FS
3-0	FS_MODE	R/W	0000	FS Speed Mode These bits select the FS operation mode, which must be set according to the current audio sampling rate. 4 'b0000 Auto detection 4 'b0110 32KHz 4 'b1000 44.1KHz 4'b1001 48KHz 4 'b1010 88.2KHz 4 'b1011 96KHz Others Reserved

7.6.1.6 CLOCK_DET_CTRL Register (Offset = 29h) [reset = 0x00]

CLOCK_DET_CTRL is shown in Figure 7-18 and described in Table 7-14.

Return to Table 7-7.

Figure 7-18. CLOCK_DET_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	DIS_DET_PLL	DIS_DET_BCLK_RANGE	DIS_DET_FS	DIS_DET_BCLK	DIS_DET_MISS	RESERVED	DIS_DET_LOCK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 7-14. CLOCK_DET_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6	DIS_DET_PLL	R/W	0	Ignore PLL overate Detection This bit controls whether to ignore the PLL overrate detection. The PLL must be slow than 150MHz or an error will be reported. When ignored, a PLL overrate error will not cause a clock error. 0: Regard PLL overrate detection 1: Ignore PLL overrate detection
5	DIS_DET_BCLK_RANGE	R/W	0	Ignore BCK Range Detection This bit controls whether to ignore the BCK range detection. The BCK must be stable between 256KHz and 50MHz or an error will be reported. When ignored, a BCK range error will not cause a clock error. 0: Regard BCK Range detection 1: Ignore BCK Range detection
4	DIS_DET_FS	R/W	0	Ignore FS Error Detection This bit controls whether to ignore the FS Error detection. When ignored, FS error will not cause a clock error.But CLKDET_STATUS will report fs error. 0: Regard FS detection 1: Ignore FS detection
3	DIS_DET_BCLK	R/W	0	Ignore BCK Detection This bit controls whether to ignore the BCK detection against LRCK. The BCK must be stable between 32FS and 512FS inclusive or an error will be reported. When ignored, a BCK error will not cause a clock error. 0: Regard BCK detection 1: Ignore BCK detection
2	DIS_DET_MISS	R/W	0	Ignore BCK Missing Detection This bit controls whether to ignore the BCK missing detection. When ignored an BCK missing will not cause a clock error. 0: Regard BCK missing detection 1: Ignore BCK missing detection
1	RESERVED	R/W	0	This bit is reserved
0	DIS_DET_LOCK	R/W	0	This bit is reserved

7.6.1.7 SDOUT_SEL Register (Offset = 30h) [reset = 0h]

SDOUT_SEL is shown in Figure 7-19 and described in Table 7-15.

Return to Table 7-7.

Figure 7-19. SDOUT_SEL Register

7	6	5	4	3	2	1	0
RESERVED							SDOUT_SEL
							R/W

Table 7-15. SDOUT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED		0	This bit is reserved
0	SDOUT_SEL	R	0	SDOUT Select. This bit selects what is being output as SDOUT pin. 0: SDOUT is the DSP output (post-processing) 1: SDOUT is the DSP input (pre-processing)

7.6.1.8 I2S_CTRL Register (Offset = 31h) [reset = 0x00]

I2S_CTRL is shown in Figure 7-20 and described in Table 7-16.

Return to Table 7-7.

Figure 7-20. I2S_CTRL Register

7	6	5	4	3	2	1	0
RESERVED		BCK_INV	RESERVED		RESERVED		RESERVED
R/W		R/W	R/W	R	R		R/W

Table 7-16. I2S_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	00	This bit is reserved
5	BCK_INV	R/W	0	BCK Polarity This bit sets the inverted BCK mode. In inverted BCK mode, the DAC assumes that the LRCK and DIN edges are aligned to the rising edge of the BCK. Normally they are assumed to be aligned to the falling edge of the BCK. 0: Normal BCK mode 1: Inverted BCK mode
4-0	RESERVED	R/W	00000	This bit is reserved

7.6.1.9 SAP_CTRL1 Register (Offset = 33h) [reset = 0x02]

SAP_CTRL1 is shown in Figure 7-21 and described in Table 7-17.

Return to Table 7-7.

Figure 7-21. SAP_CTRL1 Register

7	6	5	4	3	2	1	0
I2S_SHIFT_MSB		DATA_FORMAT		I2S_LRCLK_PULSE		WORD_LENGTH	
R/W		R/W		R/W		R/W	

Table 7-17. SAP_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	I2S_SHIFT_MSB	R/W	00	I2S Shift MSB [9:8]. See details in Table 7-18.
5-4	DATA_FORMAT	R/W	00	I2S Data Format These bits control both input and output audio interface formats for DAC operation. 00: I2S 01: TDM/DSP 10: RTJ 11: LTJ
3-2	I2S_LRCLK_PULSE	R/W	00	01: lrclk pulse < 8 SCLK
1-0	WORD_LENGTH	R/W	10	I2S Word Length These bits control both input and output audio interface sample word lengths for DAC operation. 00: 16 bits 01: 20 bits 10: 24 bits 11: 32 bits

7.6.1.10 SAP_CTRL2 Register (Offset = 34h) [reset = 0x00]

SAP_CTRL2 is shown in Figure 7-22 and described in Table 7-18.

Return to Table 7-7.

Figure 7-22. SAP_CTRL2 Register

7	6	5	4	3	2	1	0
I2S_SHIFT							
R/W							

Table 7-18. SAP_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	I2S_SHIFT	R/W	00000000	I^2S Shift LSB [7:0] These bits control the offset of audio data in the audio frame for both input and output. The offset is defined as the number of BCK from the starting (MSB) of audio frame to the starting of the desired audio sample. I2S Shift MSB [9:8] locates in Section 7.6.1.9 . 000000000: offset = 0 BCK (no offset) 000000001: ofsset = 1 BCK 000000010: offset = 2 BCKs and 111111111: offset = 512 BCKs

7.6.1.11 SAP_CTRL3 Register (Offset = 35h) [reset = 0x11]

SAP_CTRL3 is shown in Figure 7-23 and described in Table 7-19.

Return to Table 7-7.

Figure 7-23. SAP_CTRL3 Register

7	6	5	4	3	2	1	0
RESERVED		LEFT_DAC_DPATH		RESERVED		RIGHT_DAC_DPATH	
R/W		R/W		R/W		R/W	

Table 7-19. SAP_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	00	This bit is reserved
5-4	LEFT_DAC_DPATH	R/W	01	Left DAC Data Path. These bits control the left channel audio data path connection. 00: Zero data (mute) 01: Left channel data 10: Right channel data 11: Reserved (do not set)
3-2	RESERVED	R/W	00	This bit is reserved
1-0	RIGHT_DAC_DPATH	R/W	01	Right DAC Data Path. These bits control the right channel audio data path connection. 00: Zero data (mute) 01: Right channel data 10: Left channel data 11: Reserved (do not set)

7.6.1.12 FS_MON Register (Offset = 37h) [reset = 0x00]

FS_MON is shown in Figure 7-24 and described in Table 7-20.

Return to Table 7-7.

Figure 7-24. FS_MON Register

7	6	5	4	3	2	1	0
RESERVED		BCLK_RATIO_HIGH		FS			
R/W		R		R			

Table 7-20. FS_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	00	This bit is reserved
5-4	BCLK_RATIO_HIGH	R	00	2 msbs of detected BCK ratio
3-0	FS	R	0000	These bits indicate the currently detected audio sampling rate. 0000 FS Error 0010 8KHz 0100 16KHz 0110 32KHz 1000 Reserved 1001 48KHz 1011 96KHz 1101 192KHz Others Reserved

7.6.1.13 BCK_MON Register (Offset = 38h) [reset = 0x00]

BCK_MON is shown in Figure 7-25 and described in Table 7-21.

Return to Table 7-7.

Figure 7-25. BCK_MON Register

7	6	5	4	3	2	1	0
BCLK_RATIO_LOW							
R							

Table 7-21. BCK_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BCLK_RATIO_LOW	R	00000000	These bits indicate the currently detected BCK ratio, the number of BCK clocks in one audio frame. BCK = 32 FS~512 FS

7.6.1.14 CLKDET_STATUS Register (Offset = 39h) [reset = 0x00]

CLKDET_STATUS is shown in Figure 7-26 and described in Table 7-22.

Return to Table 7-7.

Figure 7-26. CLKDET_STATUS Register

7	6	5	4	3	2	1	0
RESERVED		DET_STATUS					
R/W		R					

Table 7-22. CLKDET_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	00	This bit is reserved
5	DET_STATUS	R	0	This bit indicates whether the BCLK is overrate or underrate
4		R	0	This bit indicates whether the PLL is overrate
3		R	0	This bit indicates whether the PLL is locked or not. The PLL will be reported as unlocked when it is disabled.
2		R	0	This bit indicates whether the BCK is missing or not.
1		R	0	This bit indicates whether the BCK is valid or not. The BCK ratio must be stable and in the range of 32-512FS to be valid.
0		R	0	In auto detection mode(reg_fsmode=0),this bit indicated whether the audio sampling rate is valid or not. In non auto detection mode(reg_fsmode!=0), Fs error indicates that configured fs is different with detected fs. Even FS Error Detection Ignore is set, this flag will be also asserted.

7.6.1.15 DIG_VOL Register (Offset = 4Ch) [reset = 30h]

DIG_VOL is shown in Figure 7-27 and described in Table 7-23.

Return to Table 7-7.

Figure 7-27. DIG_VOL Register

7	6	5	4	3	2	1	0
PGA_LEFT							
R/W							

Table 7-23. DIG_VOL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PGA	R/W	00110000	Digital Volume These bits control both left and right channel digital volume. The digital volume is 24 dB to -103 dB in -0.5 dB step. 00000000: +24.0 dB 00000001: +23.5 dB ..... and 00101111: +0.5 dB 00110000: 0.0 dB 00110001: -0.5 dB ..... 11111110: -103 dB 11111111: Mute

7.6.1.16 DIG_VOL_CTRL1 Register (Offset = 4Eh) [reset = 0x33]

DIG_VOL_CTRL1 is shown in Figure 7-28 and described in Table 7-24.

Return to Table 7-7.

Figure 7-28. DIG_VOL_CTRL1 Register

7	6	5	4	3	2	1	0
PGA_RAMP_DOWN_SPEED		PGA_RAMP_DOWN_STEP		PGA_RAMP_UP_SPEED		PGA_RAMP_UP_STEP	
R/W		R/W		R/W		R/W	

Table 7-24. DIG_VOL_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PGA_RAMP_DOWN_SPEED	R/W	00	Digital Volume Normal Ramp Down Frequency These bits control the frequency of the digital volume updates when the volume is ramping down. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
5-4	PGA_RAMP_DOWN_STEP	R/W	11	Digital Volume Normal Ramp Down Step These bits control the step of the digital volume updates when the volume is ramping down. 00: Decrement by 4 dB for each update 01: Decrement by 2 dB for each update 10: Decrement by 1 dB for each update 11: Decrement by 0.5 dB for each update
3-2	PGA_RAMP_UP_SPEED	R/W	00	Digital Volume Normal Ramp Up Frequency These bits control the frequency of the digital volume updates when the volume is ramping up. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly restore the volume (Instant unmute)
1-0	PGA_RAMP_UP_STEP	R/W	11	Digital Volume Normal Ramp Up Step These bits control the step of the digital volume updates when the volume is ramping up. 00: Increment by 4 dB for each updat e 01: Increment by 2 dB for each update 10: Increment by 1 dB for each update 11: Increment by 0.5 dB for each update

7.6.1.17 DIG_VOL_CTRL2 Register (Offset = 4Fh) [reset = 0x30]

DIG_VOL_CTRL2 is shown in Figure 7-29 and described in Table 7-25.

Return to Table 7-7.

Figure 7-29. DIG_VOL_CTRL2 Register

7	6	5	4	3	2	1	0
FAST_RAMP_DOWN_SPEED		FAST_RAMP_DOWN_STEP		RESERVED			
R/W		R/W		R/W			

Table 7-25. DIG_VOL_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	FAST_RAMP_DOWN_SPEED	R/W	00	Digital Volume Emergency Ramp Down Frequency These bits control the frequency of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute. 00: Update every 1 FS period 01: Update every 2 FS periods 10: Update every 4 FS periods 11: Directly set the volume to zero (Instant mute)
5-4	FAST_RAMP_DOWN_STEP	R/W	11	Digital Volume Emergency Ramp Down Step These bits control the step of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute. 00: Decrement by 4 dB for each update 01: Decrement by 2 dB for each update 10: Decrement by 1 dB for each update 11: Decrement by 0.5 dB for each update
3-0	RESERVED	R/W	0000	This bit is reserved

7.6.1.18 AUTO_MUTE_CTRL Register (Offset = 50h) [reset = 0x07]

AUTO_MUTE_CTRL is shown in Figure 7-30 and described in Table 7-26.

Return to Table 7-7.

Figure 7-30. AUTO_MUTE_CTRL Register

7	6	5	4	3	2	1	0
RESERVED					REG_AUTO_MUTE_CTRL		
R/W					R/W		

Table 7-26. AUTO_MUTE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	00000	This bit is reserved
2	REG_AUTO_MUTE_CTRL	R/W	1	0: Auto mute left channel and right channel independently. 1: Auto mute left and right channels only when both channels are about to be auto muted.
1			1	0: Disable right channel auto mute 1: Enable right channel auto mute
0			1	0: Disable left channel auto mute 1: Enable left channel auto mute

7.6.1.19 AUTO_MUTE_TIME Register (Offset = 51h) [reset = 0x00]

AUTO_MUTE_TIME is shown in Figure 7-31 and described in Table 7-27.

Return to Table 7-7.

Figure 7-31. AUTO_MUTE_TIME Register

7	6	5	4	3	2	1	0
RESERVED	AUTOMUTE_TIME_LEFT			RESERVED	AUTOMUTE_TIME_RIGHT		
R/W	R/W			R/W	R/W		

Table 7-27. AUTO_MUTE_TIME Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6-4	AUTOMUTE_TIME_LEFT	R/W	000	Auto Mute Time for Left Channel These bits specify the length of consecutive zero samples at left channel before the channel can be auto muted. The times shown are for 96 kHz sampling rate and will scale with other rates. 000: 11.5 ms 001: 53 ms 010: 106.5 ms 011: 266.5 ms 100: 0.535 sec 101: 1.065 sec 110: 2.665 sec 111: 5.33 sec
3	RESERVED	R/W	0	This bit is reserved
2-0	AUTOMUTE_TIME_RIGHT	R/W	000	Auto Mute Time for Right Channel These bits specify the length of consecutive zero samples at right channel before the channel can be auto muted. The times shown are for 96 kHz sampling rate and will scale with other rates. 000: 11.5 ms 001: 53 ms 010: 106.5 ms 011: 266.5 ms 100: 0.535 sec 101: 1.065 sec 110: 2.665 sec 111: 5.33 sec

7.6.1.20 AMUTE_DELAY Register (Offset = 52h) [reset = 0x00]

AMUTE_DELAY is shown in Figure 7-32 and described in Table 7-28.

Return to Table 7-7.

Figure 7-32. AMUTE_DELAY Register

7	6	5	4	3	2	1	0
AMUTE_DLY							
R/W							

Table 7-28. AMUTE_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	AMUTE_DLY	R/W	00000000	AMUTE Delay These bits control the delay before the complete digital mute to the assertion of analog mute. This is to allow the non-mute audio samples to completely flow out through analog parts before the assertion of the analog mute. 00000000: No delay 00000001: 1 LRCK delay 00000010: 2 LRCK delay ..... 11111111: 255 LRCK delay

7.6.1.21 ANA_CTRL Register (Offset = 53h) [reset = 0x00]

ANA_CTRL is shown in Figure 7-33 and described in Table 7-29.

Return to Table 7-7.

Figure 7-33. ANA_CTRL Register

7	6	5	4	3	2	1	0
ANA_CTRL							
R/W							

Table 7-29. ANA_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ANA_CTRL	R/W	0	Fast Hiz control enable in clock halt
6-5			00	Class-D bandwidth control, "00": 80kHz; "01": 100kHz; "10": 120kHz; "11": 175kHz. With 768kHz or 1.024MHz switching frequency, bandwidth need set to 175kHz for best audio performance
4-1			0000	These bits are reserved
0			0	Channel L and R PWM output of phase control . 1: In phase 0: Out of phase

7.6.1.22 AGAIN Register (Offset = 54h) [reset = 0x00]

AGAIN is shown in Figure 7-34 and described in Table 7-30.

Return to Table 7-7.

Figure 7-34. AGAIN Register

7	6	5	4	3	2	1	0
RESERVED			ANA_GAIN				
R/W			R/W				

Table 7-30. AGAIN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	This bit is reserved
4-0	ANA_GAIN	R/W	00000	Analog Gain Control This bit controls the analog gain. 00000: 0 dB (29.5V peak voltage) 00001:-0.5db 11111: -15.5 dB

7.6.1.23 BQ_WR_CTRL1 Register (Offset = 5Ch) [reset = 0x00]

BQ_WR_CTRL1 is shown in Figure 7-35 and described in Table 7-31.

Return to Table 7-7.

Figure 7-35. BQ_WR_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED							BQ_WR_FIRST_COEF
R/W							R/W

Table 7-31. BQ_WR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000000	This bit is reserved
0	BQ_WR_FIRST_COEF	R/W	0	Indicate the first coefficient of a BQ is starting to write.

7.6.1.24 DAC_CTRL Register (Offset = 5Dh) [reset = 0xF8]

DAC_CTRL is shown in Figure 7-36 and described in Table 7-32.

Return to Table 7-7.

Figure 7-36. DAC_CTRL Register

7	6	5	4	3	2	1	0
DAC_FREQUENCY_SEL	DAC_DITHER_EN		DAC_DITHER			DAC_CTRL_DEM_SEL	
R/W	R/W		R/W			R/W	

Table 7-32. DAC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DAC_FREQUENCY_SEL	R/W	1	DAC Frequency Selection 0: 6.144MHz 1: 3.072MHz
6-5	DAC_DITHER_EN	R/W	11	DITHER_EN, 00: Disable both stage dither 01: Enable main stage dither 10: Enable second stage dither 11: Enable both stage dither
4-2	DAC_DITHER	R/W	110	Dither level 100: -2^-7 101: -2^-8 110: -2^-9 111: -2^-10 000: -2^-13 001: -2^-14 010: -2^-15 011: -2^-16
1-0	DAC_CTRL_DEM_SEL	R/W	00	00: Enable DAC DEM (Dynamic-Element-Matching) 11: Disable DAC DEM (Dynamic-Element-Matching)

7.6.1.25 ADR_PIN_CTRL Register (Offset = 60h) [reset = 0h]

ADR_PIN_CTRL is shown in Figure 7-37 and described in Table 7-33.

Return to Table 7-7.

Figure 7-37. ADR_PIN_CTRL Register

7	6	5	4	3	2	1	0
RESERVED							ADR_OE
							R/W - 0x0

Table 7-33. ADR_PIN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000000	This bit is reserved
0	ADR_OE	R/W	0	ADR Output Enable This bit sets the direction of the ADR pin 0: ADR is input 1: ADR is output

7.6.1.26 ADR_PIN_CONFIG Register (Offset = 61h) [reset = 0x00]

ADR_PIN_CONFIG is shown in Figure 7-38 and described in Table 7-34.

Return to Table 7-7.

Figure 7-38. ADR_PIN_CONFIG Register

7	6	5	4	3	2	1	0
RESERVED			ADR_PIN_CONFIG				
R/W							

Table 7-34. ADR_PIN_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	This bit is reserved
4-0	ADR_PIN_CONFIG	R/W	00000	00000: off (low) 00011: Auto mute flag (asserted when both L and R channels are auto muted) 00100: Auto mute flag for left channel 00101: Auto mute flag for right channel 00110: Clock invalid flag (clock error or clock missing) 00111: Reserved 01000: Reserved 01001: Reserved 01011: ADR as FAULTZ output

7.6.1.27 DSP_MISC Register (Offset = 66h) [reset = 0h]

DSP_MISC is shown in Figure 7-39 and described in Table 7-35.

Return to Table 7-7.

Figure 7-39. DSP_MISC Register

7	6	5	4	3	2	1	0
BYPASS_CONTROL							
R/W							

Table 7-35. DSP_MISC Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	BYPASS CONTROL	R/W	0000	These bits are reserved
3			0	1: Left and Right will have use unique coef 0: Right channel will share left channel coefficient
2			0	This bit is reserved
1			0	1: Bypass DRC
0			0	1: Bypass EQ

7.6.1.28 DIE_ID Register (Offset = 67h) [reset = 0h]

DIE_ID is shown in Figure 7-40 and described in Table 7-36.

Return to Table 7-7.

Figure 7-40. DIE_ID Register

7	6	5	4	3	2	1	0
DIE_ID							
R-0h							

Table 7-36. DIE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIE_ID	R	0h	DIE ID

7.6.1.29 POWER_STATE Register (Offset = 68h) [reset = 0x00]

POWER_STATE is shown in Figure 7-41 and described in Table 7-37.

Return to Table 7-7.

Figure 7-41. POWER_STATE Register

7	6	5	4	3	2	1	0
STATE_RPT							
R							

Table 7-37. POWER_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	Reserved	R	000000	These bits are reserved
1-0	STATE_RPT	R	00	00: Deep sleep 01: Seep 10: HIZ 11: Play

7.6.1.30 AUTOMUTE_STATE Register (Offset = 69h) [reset = 0x00]

AUTOMUTE_STATE is shown in Figure 7-42 and described in Table 7-38.

Return to Table 7-7.

Figure 7-42. AUTOMUTE_STATE Register

7	6	5	4	3	2	1	0
RESERVED						ZERO_RIGHT_MON	ZERO_LEFT_MON
R						R	R

Table 7-38. AUTOMUTE_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000	This bit is reserved
1	ZERO_RIGHT_MON	R	0	This bit indicates the auto mute status for right channel. 0: Not auto muted 1: Auto muted
0	ZERO_LEFT_MON	R	0	This bit indicates the auto mute status for left channel. 0: Not auto muted 1: Auto muted

7.6.1.31 PHASE_CTRL Register (Offset = 6Ah) [reset = 0x00]

PHASE_CTRL is shown in Figure 7-43 and described in Table 7-39.

Return to Table 7-7.

Figure 7-43. PHASE_CTRL Register

7	6	5	4	3	2	1	0
RESERVED				RAMP_PHASE_SEL		I2S_SYNC_EN	PHASE_SYNC_EN
R/W				R/W		R/W	R/W

Table 7-39. PHASE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	This bit is reserved
3-2	RAMP_PHASE_SEL	R/W	00	Select ramp clock phase when multi devices integrated in one system to reduce EMI and peak supply peak current, it is recomended set all devices the same RAMP frequency and same spread spectrum. it must be set before driving device into PLAY mode if this feature is needed. 00: phase 0 01: phase1 10: phase2 11: phase3
1	I2S_SYNC_EN	R/W	0	Use I2S to synchronize output PWM phase 0: Disable 1: Enable
0	PHASE_SYNC_EN	R/W	0	0: RAMP phase sync disable 1: RAMP phase sync enable

7.6.1.32 SS_CTRL0 Register (Offset = 6Bh) [reset = 0x00]

SS_CTRL0 is shown in Figure 7-44 and described in Table 7-40.

Return to Table 7-7.

Figure 7-44. SS_CTRL0 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	SS_PRE_DIV_SEL	SS_MANUAL_MODE	RESERVED		SS_RDM_EN	SS_TRI_EN
R/W	R/W	R/W	R/W	R/W		R/W	R/W

Table 7-40. SS_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6	RESERVED	R/W	0	This bit is reserved
5	SS_PRE_DIV_SEL	R/W	0	Select pll clock divide 2 as source clock in manual mode
4	SS_MANUAL_MODE	R/W	0	Set ramp ss controller to manual mode
3-2	RESERVED	R/W	0	This bit is reserved
1	SS_RDM_EN	R/W	0	Random SS enable
0	SS_TRI_EN	R/W	0	Triangle SS enable

7.6.1.33 SS_CTRL1 Register (Offset = 6Ch) [reset = 0x00]

SS_CTRL1 is shown in Figure 7-45 and described in Table 7-41.

Return to Table 7-7.

Figure 7-45. SS_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED	SS_RDM_CTRL			SS_TRI_CTRL			
R/W	R/W			R/W			

Table 7-41. SS_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6-4	SS_RDM_CTRL	R/W	000	Random SS range control
3-0	SS_TRI_CTRL	R/W	0000	Triangle SS frequency and range control

7.6.1.34 SS_CTRL2 Register (Offset = 6Dh) [reset = 0x50]

SS_CTRL2 is shown in Figure 7-46 and described in Table 7-42.

Return to Table 7-7.

Figure 7-46. SS_CTRL2 Register

7	6	5	4	3	2	1	0
TM_FREQ_CTRL							
R/W							

Table 7-42. SS_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TM_FREQ_CTRL	R/W	01010000	Control ramp frequency in manual mode, F=61440000/N

7.6.1.35 SS_CTRL3 Register (Offset = 6Eh) [reset = 0x11]

SS_CTRL3 is shown in Figure 7-47 and described in Table 7-43.

Return to Table 7-7.

Figure 7-47. SS_CTRL3 Register

7	6	5	4	3	2	1	0
TM_DSTEP_CTRL				TM_USTEP_CTRL			
R/W				R/W			

Table 7-43. SS_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	SS_TM_DSTEP_CTRL	R/W	0001	Control triangel mode spread spectrum fall step in ramp ss manual mode
3-0	SS_TM_USTEP_CTRL	R/W	0001	Control triangle mode spread spectrum rise step in ramp ss manual mode

7.6.1.36 SS_CTRL4 Register (Offset = 6Fh) [reset = 0x24]

SS_CTRL4 is shown in Figure 7-48 and described in Table 7-44.

Return to Table 7-7.

Figure 7-48. SS_CTRL4 Register

7	6	5	4	3	2	1	0
RESERVED	TM_AMP_CTRL		SS_TM_PERIOD_BOUNDRY				
R/W	R/W		R/W				

Table 7-44. SS_CTRL4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	This bit is reserved
6-5	TM_AMP_CTRL	R/W	01	Control ramp amp ctrl in ramp ss manual model
4-0	SS_TM_PERIOD_BOUNDRY	R/W	00100	Control triangle mode spread spectrum boundary in ramp ss manual mode

7.6.1.37 CHAN_FAULT Register (Offset = 70h) [reset = 0x00]

CHAN_FAULT is shown in Figure 7-49 and described in Table 7-45.

Return to Table 7-7.

Figure 7-49. CHAN_FAULT Register

7	6	5	4	3	2	1	0
RESERVED				CH1_DC_1	CH2_DC_1	CH1_OC_I	CH2_OC_I
R				R	R	R	R

Table 7-45. CHAN_FAULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000	This bit is reserved
3	CH1_DC_1	R	0	Left channel DC fault. Once there is a DC fault, this bit will set to 1. Class D output will set to Hi-Z. Report by $\overline{\text{FAULT}}$ pin (Pin 10). Clear this fault by setting bit 7 of Section 7.6.1.44 to 1 or this bit keeps 1.
2	CH2_DC_1	R	0	Right channel DC fault. Once there is a DC fault, this bit will set to 1. Class D output will set to Hi-Z. Report by $\overline{\text{FAULT}}$ pin (Pin 10). Clear this fault by setting bit 7 of Section 7.6.1.44 to 1 or this bit keeps 1.
1	CH1_OC_I	R	0	Left channel over current fault. Once there is an OC fault, this bit will set to 1. Class D output will set to Hi-Z. Report by $\overline{\text{FAULT}}$ pin (Pin 10). Clear this fault by setting bit 7 of Section 7.6.1.44 to 1 or this bit keeps 1.
0	CH2_OC_I	R	0	Right channel over current fault. Once there is an OC fault, this bit will set to 1. Class D output will set to Hi-Z. Report by $\overline{\text{FAULT}}$ pin (Pin 10). Clear this fault by setting bit 7 of Section 7.6.1.44 to 1 or this bit keeps 1.

7.6.1.38 GLOBAL_FAULT1 Register (Offset = 71h) [reset = 0h]

GLOBAL_FAULT1 is shown in Figure 7-50 and described in Table 7-46.

Return to Table 7-7.

Figure 7-50. GLOBAL_FAULT1 Register

7	6	5	4	3	2	1	0
OTP_CRC_ERROR	BQ_WR_ERROR				CLK_FAULT_I	PVDD_OV_I	PVDD_UV_I
R	R				R	R	R

Table 7-46. GLOBAL_FAULT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OTP_CRC_ERROR	R	0h	Indicate OTP CRC check error.
6	BQ_WR_ERROR	R	0h	The recent BQ is written failed
5-3	RESERVED	R	0h	This bit is reserved
2	CLK_FAULT_I	R	0h	Clock fault. Once there is a Clock fault, this bit will set to 1. Class D output will set to Hi-Z. Report by $\overline{\text{FAULT}}$ pin (Pin 10). Clock fault works with an auto-recovery mode, once the clock error removes, device automatically returns to the previous state. Clear this fault by setting bit 7 of Section 7.6.1.44 to 1 or this bit keeps 1.

Table 7-46. GLOBAL_FAULT1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	PVDD_OV_I	R	0h	PVDD OV fault. Once there is an OV fault, this bit will set to 1. Class D output will set to Hi-Z. Report by $\overline{\text{FAULT}}$ pin (Pin 10). OV fault works with an auto-recovery mode, once the OV error removes, device automatically returns to the previous state. Clear this fault by setting bit 7 of Section 7.6.1.44 to 1 or this bit keeps 1. Once OV fault been cleared by Register 0x78, even the OV fault still exist (Device still keeps in Hi-Z state due to High PVDD), PVDD_OV_I keeps 0 unless the OV fault been triggered again (PVDD drop below the OV threshold and rise again).
0	PVDD_UV_I	R	0h	PVDD UV fault. Once there is an UV fault, this bit will set to 1. Class D output will set to Hi-Z. Report by $\overline{\text{FAULT}}$ pin (Pin 10). UV fault works with an auto-recovery mode, once the UV error removes, device automatically returns to the previous state. Clear this fault by setting bit 7 of Section 7.6.1.44 to 1 or this bit keeps 1. Once UV fault been cleared by Register 0x78, even the UV fault still exist (Device still keep in Hi-Z state due to Low PVDD), PVDD_UV_I keeps 0 unless the UV fault been triggered again (PVDD rise above the UV threshold and fall again).

7.6.1.39 GLOBAL_FAULT2 Register (Offset = 72h) [reset = 0h]

GLOBAL_FAULT2 is shown in Figure 7-51 and described in Table 7-47.

Return to Table 7-7.

Figure 7-51. GLOBAL_FAULT2 Register

7	6	5	4	3	2	1	0
RESERVED					RESERVED		OTSD_I
R					R		R

Table 7-47. GLOBAL_FAULT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000	This bit is reserved
0	OTSD_I	R	0	Over temperature shut down fault. Once there is an OT fault, this bit will set to 1. Class D output will set to Hi-Z. Report by $\overline{\text{FAULT}}$ pin (Pin 10). OT fault works with an auto-recovery mode by setting bit 4 of Section 7.6.1.43 to 1, once the OT error removes, device automatically returns to the previous state. Once OT fault been cleared by Register 0x78, even the OT still exist (Junction temperature exceed 160°C), device will start playing. This is a risk may destroy device, so suggest to set device to OT autorecovery mode or keep Hi-Z state until the OT warning disappear. OTSD_I keeps 0 unless the OT fault been triggered again (Temperature drop below the threshold and exceed the threshold again).

7.6.1.40 OT WARNING Register (Offset = 73h) [reset = 0x00]

OT_WARNING is shown in Figure 7-52 and described in Table 7-48.

Return to Table 7-7.

Figure 7-52. OT_WARNING Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED			OTW	RESERVED	
R		R		R	R	R	R

Table 7-48. OT_WARNING Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00	This bit is reserved
5-4	RESERVED	R	00	This bit is reserved
3	OTW	R	0	Over temperature warning ,135C
2-0	RESERVED	R	000	This bit is reserved

7.6.1.41 PIN_CONTROL1 Register (Offset = 74h) [reset = 0x00]

PIN_CONTROL1 is shown in Figure 7-53 and described in Table 7-49.

Return to Table 7-7.

Figure 7-53. PIN_CONTROL1 Register

7	6	5	4	3	2	1	0
MASK_OTSD	Reserved	Reserved	MASK_CLK_FAULT	MASK_PVDD_UV	MASK_PVDD_OV	MASK_DC	MASK_OC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 7-49. PIN_CONTROL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MASK_OTSD	R/W	0	Mask OTSD fault report
6	RESERVED	R/W	0	This bit is reserved
5	RESERVED	R/W	0	This bit is reserved
4	MASK_CLK_FAULT	R/W	0	Mask clock fault report by setting this bit to 1.
3	MASK_PVDD_UV	R/W	0	Mask PVDD UV fault report by setting this bit to 1.
2	MASK_PVDD_OV	R/W	0	Mask PVDD OV fault report by setting this bit to 1.
1	MASK_DC	R/W	0	Mask DC fault report by setting this bit to 1.
0	MASK_OC	R/W	0	Mask OC fault report by setting this bit to 1.

7.6.1.42 PIN_CONTROL2 Register (Offset = 75h) [reset = 0xF8]

PIN_CONTROL2 is shown in Figure 7-54 and described in Table 7-50.

Return to Table 7-7.

Figure 7-54. PIN_CONTROL2 Register

7	6	5	4	3	2	1	0
RESERVED		CLKFLT_LATCH_EN	OTSD_LATCH_EN	OTW_LATCH_EN	MASK_OTW	RESERVED	
		R/W	R/W	R/W	R/W		

Table 7-50. PIN_CONTROL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	11	This bit is reserved
5	CLKFLT_LATCH_EN	R/W	1	Enable clock fault latch by setting this bit to 1.
4	OTSD_LATCH_EN	R/W	1	Enable OTSD fault latch by setting this bit to 1.
3	OTW_LATCH_EN	R/W	1	Enable OT warning latch by setting this bit to 1.
2	MASK_OTW	R/W	0	Mask OT warning report by setting this bit to 1.
1-0	RESERVED	R/W	00	This bit is reserved

7.6.1.43 MISC_CONTROL Register (Offset = 76h) [reset = 0x00]

MISC_CONTROL is shown in Figure 7-55 and described in Table 7-51.

Return to Table 7-7.

Figure 7-55. MISC_CONTROL Register

7	6	5	4	3	2	1	0
DET_STATUS_LATCH	RESERVED		OTSD_AUTO_REC_EN	RESERVED			
R/W	R/W		R/W	R/W			

Table 7-51. MISC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DET_STATUS_LATCH	R/W	0	1:Latch clock detection status 0:Don't latch clock detection status
6-5	RESERVED	R/W	00	This bit is reserved
4	OTSD_AUTO_REC_EN	R/W	0	OTSD auto recovery enable by setting this bit to 1.
3-0	RESERVED	R/W	0000	This bit is reserved

7.6.1.44 FAULT_CLEAR Register (Offset = 78h) [reset = 0x00]

FAULT_CLEAR is shown in Figure 7-56 and described in Table 7-52.

Return to Table 7-7.

Figure 7-56. FAULT_CLEAR Register

7	6	5	4	3	2	1	0
ANALOG_FAULT_CLEAR	RESERVED						
W	R/W						

Table 7-52. FAULT_CLEAR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ANALOG_FAULT_CLEAR	W	0	WRITE CLEAR BIT once write this bit to 1, device will clear analog fault
6-0	RESERVED	R/W	0000000	This bit is reserved

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

This section details the information required to configure the device for several popular configurations and provides guidance on integrating the TAS5822M device into the larger system.

8.2 Typical Applications

8.2.1 2.0 (Stereo BTL) System

In the 2.0 system, two channels are presented to the amplifier via the digital input signal. These two channels are amplified and then sent to two separate speakers. In some cases, the amplified signal is further separated based upon frequency by a passive crossover network after the L-C filter. Even so, the application is considered 2.0.

Most commonly, the two channels are a pair of signals called a stereo pair, with one channel containing the audio for the left channel and the other channel containing the audio for the right channel. While certainly the two channels can contain any two audio channels, such as two surround channels of a multi-channel speaker system, the most popular occurrence in two channels systems is a stereo pair.

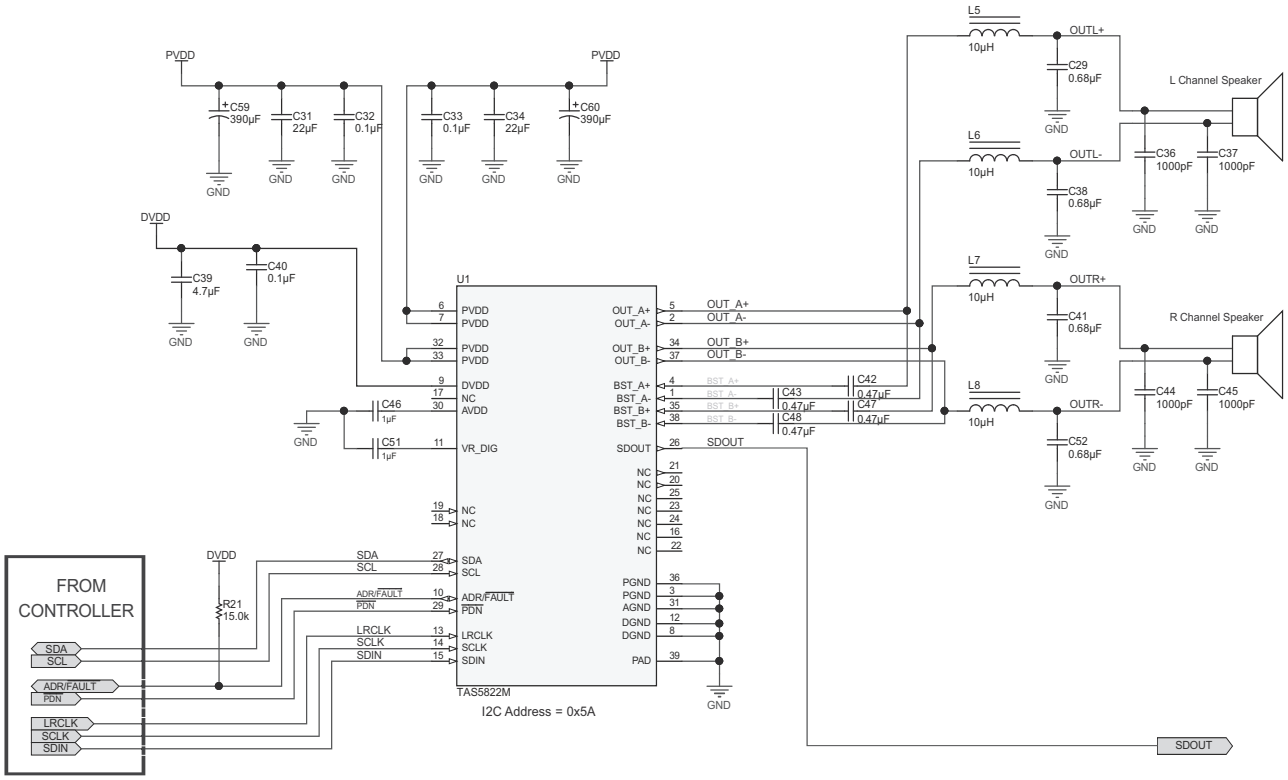
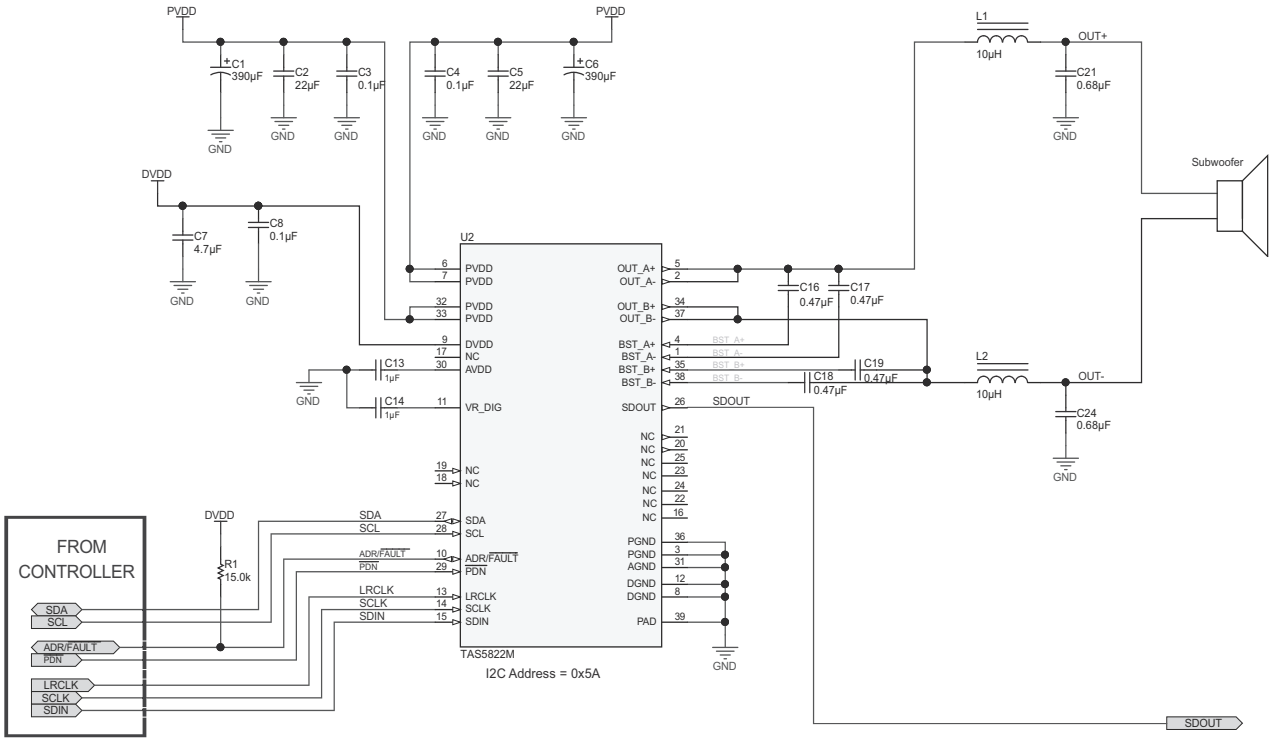


Figure 8-1. 2.0 (Stereo BTL) System Application Schematic

8.2.2 MONO (PBTL) System

In MONO mode, TAS5822M can be used as PBTL mode to drive sub-woofer with more output power.

Figure 8-2. Mono (PBTL) System Application Schematic



8.2.2.1 Design Requirements

Table 8-1. Design Parameters

PARAMETER	VALUE
PVDD	4.5V-24V
DVDD	1.8V or 3.3V
Speaker Load	6Ω/8Ω in BTL Mode, 3Ω/4Ω in PBTL Mode
LC Filter	10uH+0.68uF

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Bootstrap Capacitors

The output stage of the TAS5822M uses a high-side NMOS driver, rather than a PMOS driver. To generate the gate driver voltage for the high-side NMOS, a bootstrap capacitor for each output terminal acts as a floating power supply for the switching cycle. Use 0.47-µF capacitors to connect the appropriate output pin (OUT_X) to the bootstrap pin (BST_X). For example, connect a 0.47-µF capacitor between OUT_A and BST_A for

bootstrapping the A channel. Similarly, connect another 0.47-µF capacitor between the OUT_B and BST_B pins for the B channel inverting output.

8.2.2.2.2 Inductor Selections

It is required that the peak current is smaller than the OCP (Over current protection) value which is 7A (Typical) , there are 3 cases which cause high peak current flow through inductor.

1. During power up (idle state, no audio input), the duty cycle increases from 0 to θ. There has a start-up current which flow through inductor to set up the common mode voltage (PVDD×θ).

Note

θ = 0.5 (BD Modulation), 0.14 (1SPW Modulation), 0.14 (Hybrid Modulation)

Start-up Current shows the start-up current related to different Fsw, PVDD, Inductance and different PWM modulation scheme. Start-up current should within device's OCE_{THRES}.

Table 8-2. Start-up Current

Modulation Scheme	PVDD (V)	F_{SW} ((kHz))	LC filter	Startup Peak Current (A)
BD	13.5	384	4.7 µH + 0.68 µF	2.88
			10 µH + 0.68 µF	2
		768	4.7 µH + 0.68 µF	2.64
			10 µH + 0.68 µF	1.84
	18	384	4.7 µH + 0.68 µF	3.84
			10 µH + 0.68 µF	2.64
		768	4.7 µH + 0.68 µF	3.52
			10 µH + 0.68 µF	2.4
	24	384	4.7 µH + 0.68 µF	**5.4**
			10 µH + 0.68 µF	3.76
		768	4.7 µH + 0.68 µF	**5**
			10 µH + 0.68 µF	3.12
1SPW	13.5	384	4.7 µH + 0.68 µF	1.28
			10 µH + 0.68 µF	0.96
		768	4.7 µH + 0.68 µF	1.12
			10 µH + 0.68 µF	0.72
	18	384	4.7 µH + 0.68 µF	1.84
			10 µH + 0.68 µF	1.2
		768	4.7 µH + 0.68 µF	1.52
			10 µH + 0.68 µF	1.04
	24	384	4.7 µH + 0.68 µF	2.6
			10 µH + 0.68 µF	1.6
		768	4.7 µH + 0.68 µF	2.4
			10 µH + 0.68 µF	1.36

Figure 8-3 and Figure 8-4 shows how modulation scheme affect the start-up current. OUTP_PWM is Class D amplifier's PWM output, OUTP_FILTER is the common mode voltage on the capacitor of LC filter.

2. During music playing, some audio burst signal (high frequency) with very hard PVDD clipping will cause PWM duty cycle increase dramatically. This is the worst case and it rarely happens.

$$I_{peak\_clipping} \approx PVDD \times (1-\theta)/(F_{sw} \times L) \quad (1)$$

3. Peak current due to Max output power. Ignore the ripple current flow through capacitor.

$$I_{peak\_output\_power} \approx \sqrt{2 \times Max\_Output\_Power / R_{speaker\_Load}} \quad (2)$$

Same PVDD and switching frequency, larger inductance means smaller idle current for lower power dissipation. It's suggested that inductor's saturation current Isat, is larger than the amplifier's peak current during power-up and playing audio. In addition, the effective inductance at the peak current is required to be at least 80% of the inductance value in LC filter recommendation to meet datasheet specifications.

Table 8-3. LC filter recommendation

Switching Frequency (kHz)	Modulation Scheme	Recommended Minimum Inductance (uH) for LC filter design
1024	1SPW	3.3 µH (or larger) + Capacitor (0.22uF~0.68uF)
768		4.7 µH (or larger) + Capacitor (0.22uF~0.68uF)
384 or 480		10 µH (or larger) +Capacitor (0.22uF~0.68uF)
384~1024	BD	8.2uH (or Larger) +Capacitor (0.22uF~0.68uF)

8.2.2.2.3 Power Supply Decoupling

To ensure high efficiency, low THD, and high PSRR, proper power supply decoupling is necessary. Noise transients on the power supply lines are short duration voltage spikes. These spikes can contain frequency components that extend into the hundreds of megahertz. The power supply input must be decoupled with some good quality, low ESL, Low ESR capacitors larger than 22 µF. These capacitors bypasses low frequency noise to the ground plane. For high frequency decoupling, place 1-µF or 0.1-µF capacitors as close as possible to the PVDD pins of the device.

8.2.2.2.4 Output EMI Filtering

The TAS5822M device is often used with a low-pass filter, which is used to filter out the carrier frequency of the PWM modulated output. This filter is frequently referred to as the L-C Filter, due to the presence of an inductive element L and a capacitive element C to make up the 2-pole filter.

The L-C filter removes the carrier frequency, reducing electromagnetic emissions and smoothing the current waveform which is drawn from the power supply. The presence and size of the L-C filter is determined by several system level constraints. In some low-power use cases that have no other circuits which are sensitive to EMI, a simple ferrite bead or a ferrite bead plus a capacitor can replace the tradition large inductor and capacitor that are commonly used. In other high-power applications, large toroid inductors are required for maximum power and film capacitors can be used due to audio characteristics. Refer to the application report Class-D LC Filter Design (SLOA119) for a detailed description on the proper component selection and design of an L-C filter based upon the desired load and response.

8.2.2.3 Application Performance Plots

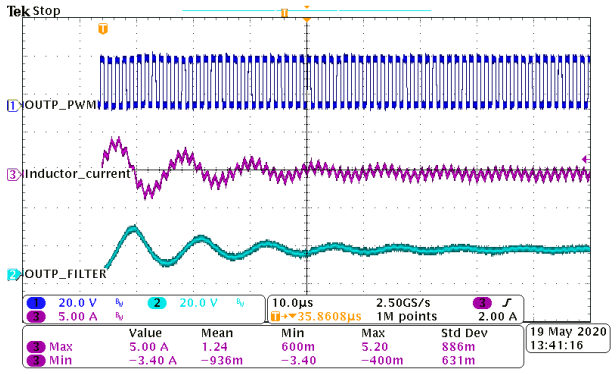


Figure 8-3. Start-up Current (Fsw = 768 kHz, LC filter = 4.7 µH + 0.68 µF, PVDD = 24 V, BD Modulation)

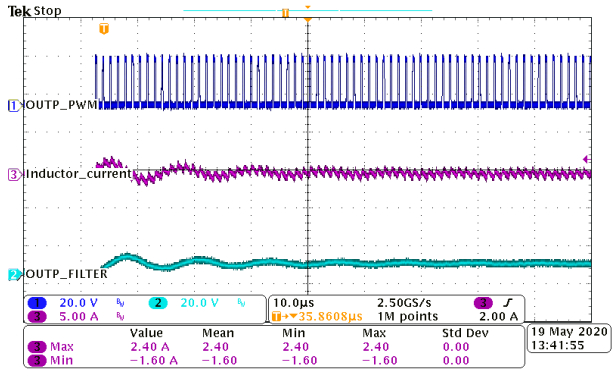


Figure 8-4. Start-up Current (Fsw = 768 kHz, LC filter = 4.7 µH + 0.68 µF, PVDD = 24 V, 1SPW Modulation)

9 Power Supply Recommendations

The device requires three power supplies for proper operation. A high-voltage supply calls PVDD is required to power the output stage of the speaker amplifier and its associated circuitry. One low-voltage power supply which is calls DVDD is required to power the various low-power portions of the device. The allowable voltage range for both PVDD and DVDD supply are listed in the Recommended Operating Conditions table. The two power supplies do not have a required power-up sequence. The power supplies can be powered on in any order. But once the device has been initialized, PVDD must keep within the normal operation voltage. Once PVDD lower than 3.5V, all registers need re-initialize again. Recommends waiting 1 ms to 5 ms for the DVDD power supplies to stabilize before starting I^2C communication and providing stable I^2S clock before enabling the device outputs.

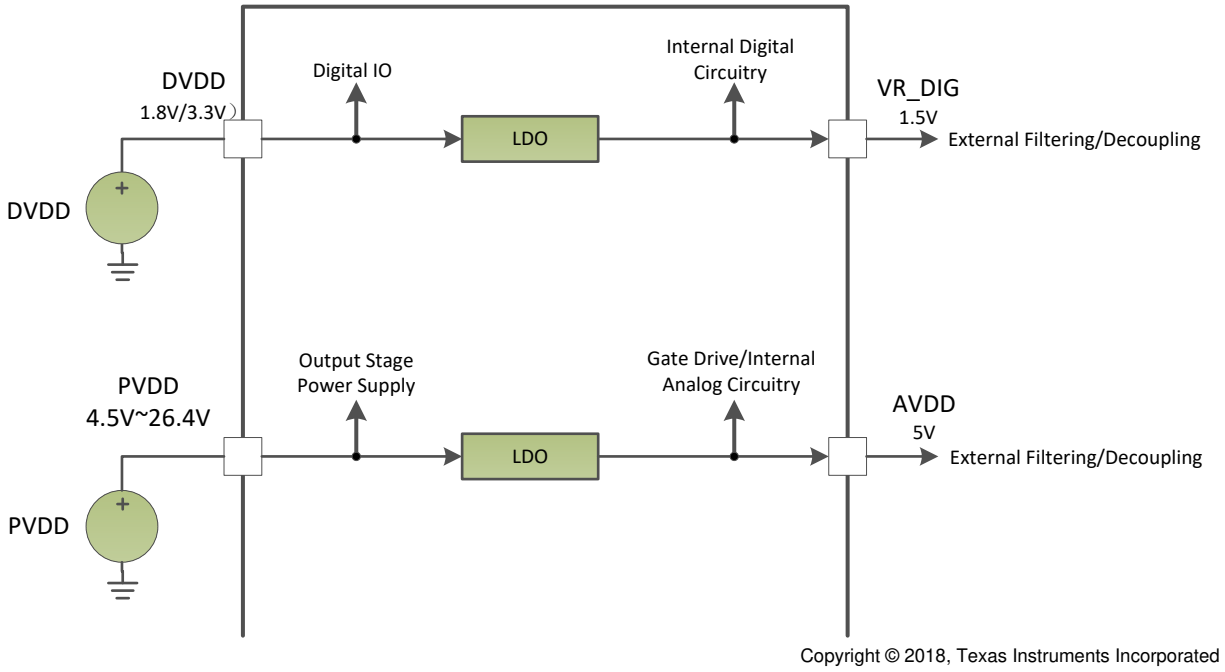


Figure 9-1. Power Supply Function Block Diagram

9.1 DVDD Supply

The DVDD supply that is required from the system is used to power several portions of the device. As shown in Figure 9-1, it provides power to the DVDD pin. Proper connection, routing and decoupling techniques are highlighted in the *Section 8* section and the *Section 10.2* section and must be followed as closely as possible for proper operation and performance.

Some portions of the device also require a separate power supply that is a lower voltage than the DVDD supply. To simplify the power supply requirements for the system, the TAS5822M device includes an integrated low dropout (LDO) linear regulator to create this supply. This linear regulator is internally connected to the DVDD supply and its output is presented on the VR_REG pin, providing a connection point for an external bypass capacitor. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuity. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

9.2 PVDD Supply

The output stage of the speaker amplifier drives the load using the PVDD supply. This is the power supply which provides the drive current to the load during playback. Proper connection, routing, and decoupling techniques are highlighted in the EVM and must be followed as closely as possible for proper operation and performance. Due to the high-voltage switching of the output stage, it is particularly important to properly decouple the output power stages in the manner described in the TAS5822M device . Lack of proper decoupling, like that shown in the *Section 8*, results in voltage spikes which can damage the device.

A separate power supply is required to drive the gates of the MOSFETs used in the output stage of the speaker amplifier. This power supply is derived from the PVDD supply via an integrated linear regulator. A GVDD pin is provided for the attachment of decoupling capacitor for the gate drive voltage regulator. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

Another separate power supply is derived from the PVDD supply via an integrated linear regulator is AVDD. AVDD pin is provided for the attachment of decoupling capacitor for the TAS5822M internal circuitry. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

10 Layout

10.1 Layout Guidelines

10.1.1 General Guidelines for Audio Amplifiers

Audio amplifiers which incorporate switching output stages must have special attention paid to their layout and the layout of the supporting components used around them. The system level performance metrics, including thermal performance, electromagnetic compliance (EMC), device reliability, and audio performance are all affected by the device and supporting component layout.

Ideally, the guidance provided in the applications section with regard to device and component selection can be followed by precise adherence to the layout guidance shown in the *Section 10.2* section. These examples represent exemplary baseline balance of the engineering trade-offs involved with lying out the device. These designs can be modified slightly as needed to meet the needs of a given application. In some applications, for instance, solution size can be compromised to improve thermal performance through the use of additional contiguous copper neat the device. Conversely, EMI performance can be prioritized over thermal performance by routing on internal traces and incorporating a via picket-fence and additional filtering components. In all cases, it is recommended to start from the guidance shown in the *Section 10.2* section and work with TI field application engineers or through the E2E community to modify it based upon the application specific goals.

10.1.2 Importance of PVDD Bypass Capacitor Placement on PVDD Network

Placing the bypassing and decoupling capacitors close to supply has long been understood in the industry. This applies to DVDD, AVDD and PVDD. However, the capacitors on the PVDD net for the TAS5822M device deserve special attention.

The small bypass capacitors on the PVDD lines of the DUT must be placed as close to the PVDD pins as possible. Not only dose placing these device far away from the pins increase the electromagnetic interference in the system, but doing so can also negatively affect the reliability of the device. Placement of these components too far from the TAS5822M device can cause ringing on the output pins that can cause the voltage on the output pin to exceed the maximum allowable ratings shown in the *Absolute Maximum Ratings* table, damaging the deice . For that reason, the capacitors on the PVDD net must be no further away from their associated PVDD pins than what is shown in the example layouts in the *Section 10.2* section.

10.1.3 Optimizing Thermal Performance

Follow the layout example shown in the Figure 10-1 to achieve the best balance of solution size, thermal, audio, and electromagnetic performance. In some cases, deviation from this guidance can be required due to design constraints which cannot be avoided. In these instances, the system designer should ensure that the heat can get out of the device and into the ambient air surrounding the device. Fortunately, the heat created in the device naturally travels away from the device and into the lower temperature structures around the device.

10.1.3.1 Device, Copper, and Component Layout

Primarily, the goal of the PCB design is to minimize the thermal impedance in the path to those cooler structures. These tips should be followed to achieve that goal:

- Avoid placing other heat producing components or structures near the amplifier (including above or below in the end equipment).
- If possible, use a higher layer count PCB to provide more heat sinking capability for the TAS5822M device and to prevent traces and copper signal and power planes from breaking up the contiguous copper on the top and bottom layer.
- Place the TAS5822M device away from the edge of the PCB when possible to ensure that the heat can travel away from the device on all four sides.
- Avoid cutting off the flow of heat from the TAS5822MM device to the surrounding areas with traces or via strings. Instead, route traces perpendicular to the device and line up vias in columns which are perpendicular to the device.
- Unless the area between two pads of a passive component is large enough to allow copper to flow in between the two pads, orient it so that the narrow end of the passive component is facing the TAS5782M device.

- Because the ground pins are the best conductors of heat in the package, maintain a contiguous ground plane from the ground pins to the PCB area surrounding the device for as many of the ground pins as possible.

10.1.3.2 Stencil Pattern

The recommended drawings for the TAS5822M device PCB foot print and associated stencil pattern are shown at the end of this document in the package addendum. Additionally, baseline recommendations for the via arrangement under and around the device are given as a starting point for the PCB design. This guidance is provided to suit the majority of manufacturing capabilities in the industry and prioritizes manufacturability over all other performance criteria. In elevated ambient temperature or under high-power dissipation use-cases, this guidance may be too conservative and advanced PCB design techniques may be used to improve thermal performance of the system.

Note

The customer must verify that deviation from the guidance shown in the package addendum, including the deviation explained in this section, meets the customer's quality, reliability, and manufacturability goals.

10.1.3.2.1 PCB footprint and Via Arrangement

The PCB footprint (also known as a symbol or land pattern) communicates to the PCB fabrication vendor the shape and position of the copper patterns to which the TAS5822M device will be soldered. This footprint can be followed directly from the guidance in the package addendum at the end of this data sheet. It is important to make sure that the thermal pad, which connects electrically and thermally to the PowerPAD™ of the TAS5822M device, be made no smaller than what is specified in the package addendum. This ensures that the TAS5822M device has the largest interface possible to move heat from the device to the board.

The via pattern shown in the package addendum provides an improved interface to carry the heat from the device through to the layers of the PCB, because small diameter plated vias (with minimally-sized annular rings) present a low thermal-impedance path from the device into the PCB. Once into the PCB, the heat travels away from the device and into the surrounding structures and air. By increasing the number of vias, as shown in the *Section 10.2* section, this interface can benefit from improved thermal performance.

Note

Vias can obstruct heat flow if they are not constructed properly.

More notes on the construction and placement of vias are as follows:

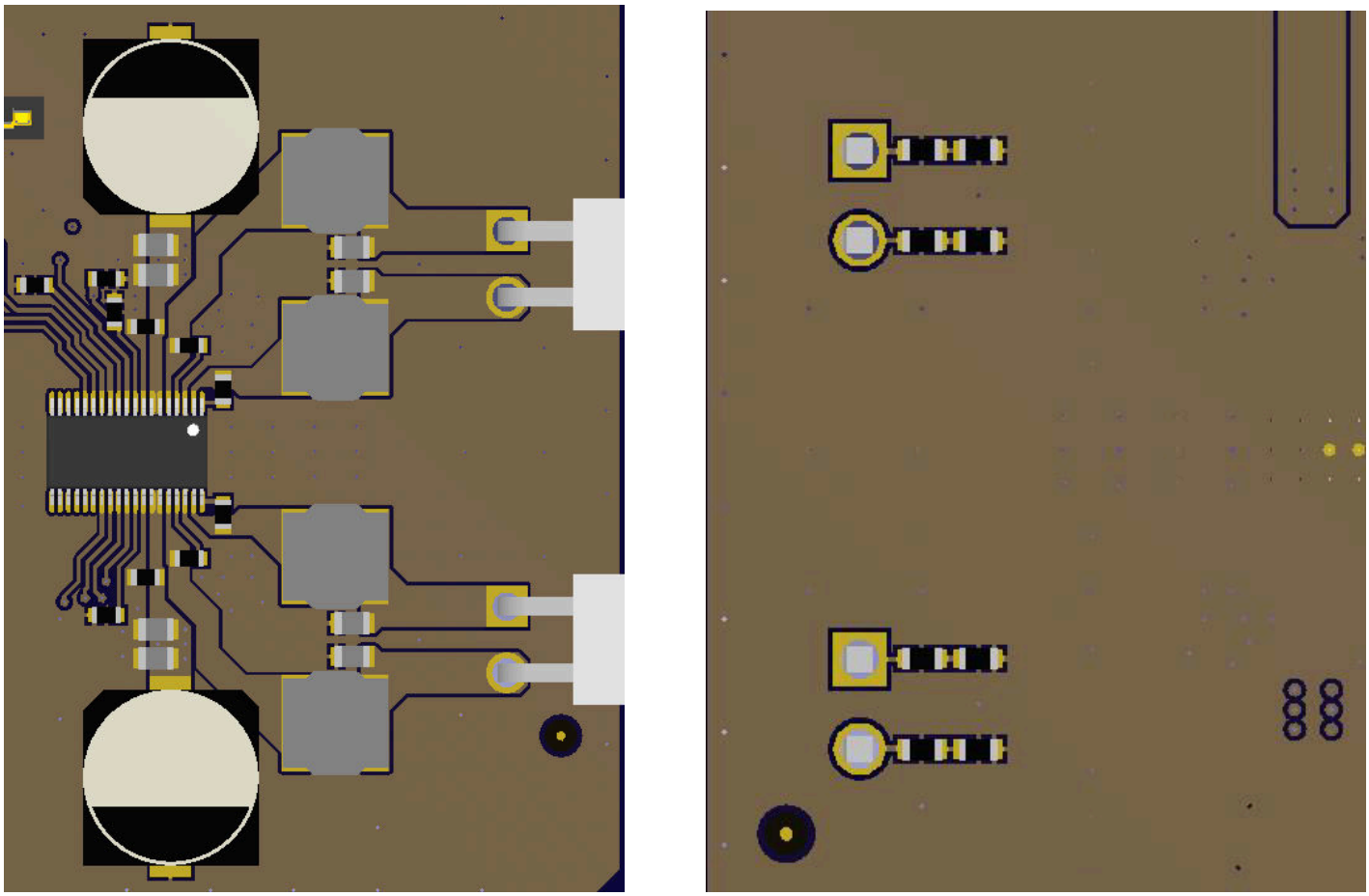
- Remove thermal reliefs on thermal vias, because they impede the flow of heat through the via.
- Vias filled with thermally conductive material are best, but a simple plated via can be used to avoid the additional cost of filled vias.
- The diameter of the drull must be 8 mm or less. Also, the distance between the via barrel and the surrounding planes should be minimized to help heat flow from the via into the surrounding copper material. In all cases, minimum spacing should be determined by the voltages present on the planes surrounding the via and minimized wherever possible.
- Vias should be arranged in columns, which extend in a line radially from the heat source to the surrounding area. This arrangement is shown in the *Section 10.2* section.
- Ensure that vias do not cut off power current flow from the power supply through the planes on internal layers. If needed, remove some vias that are farthest from the TAS5822M device to open up the current path to and from the device.

10.1.3.2.2 Solder Stencil

During the PCB assembly process, a piece of metal called a stencil on top of the PCB and deposits solder paste on the PCB wherever there is an opening (called an aperture) in the stencil. The stencil determines the quantity and the location of solder paste that is applied to the PCB in the electronic manufacturing process. In most cases, the aperture for each of the component pads is almost the same size as the pad itself. However, the thermal pad on the PCB is large and depositing a large, single deposition of solder paste would lead to

manufacturing issues. Instead, the solder is applied to the board in multiple apertures, to allow the solder paste to out gas during the assembly process and reduce the risk of solder bridging under the device. This structure is called an aperture array, and is shown in the *Section 10.2* section. It is important that the total area of the aperture array (the area of all of the small apertures combined) covers between 70% and 80% of the area of the thermal pad itself.

10.2 Layout Example



Top Layer 3D layout

Bot Layer 3D layout

Figure 10-1. 2.0 (Stereo BTL) 3-D View

11 Device and Documentation Support

11.1 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.2 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.4 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TAS5822MDCPR	Active	Production	HTSSOP (DCP) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TAS5822M
TAS5822MDCPR.A	Active	Production	HTSSOP (DCP) | 38	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TAS5822M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

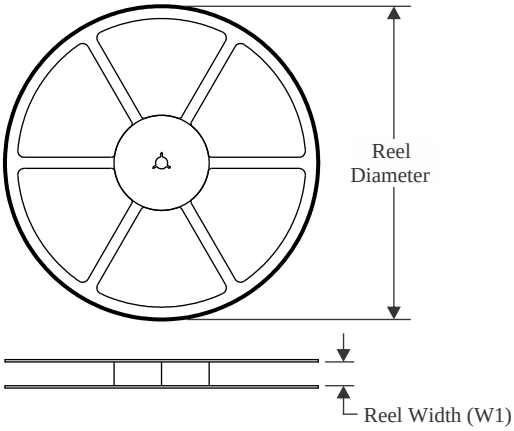
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

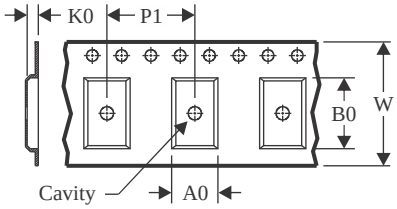
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

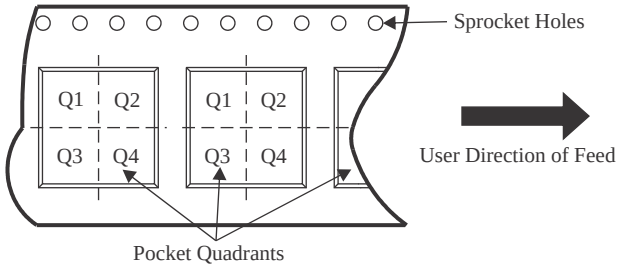


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

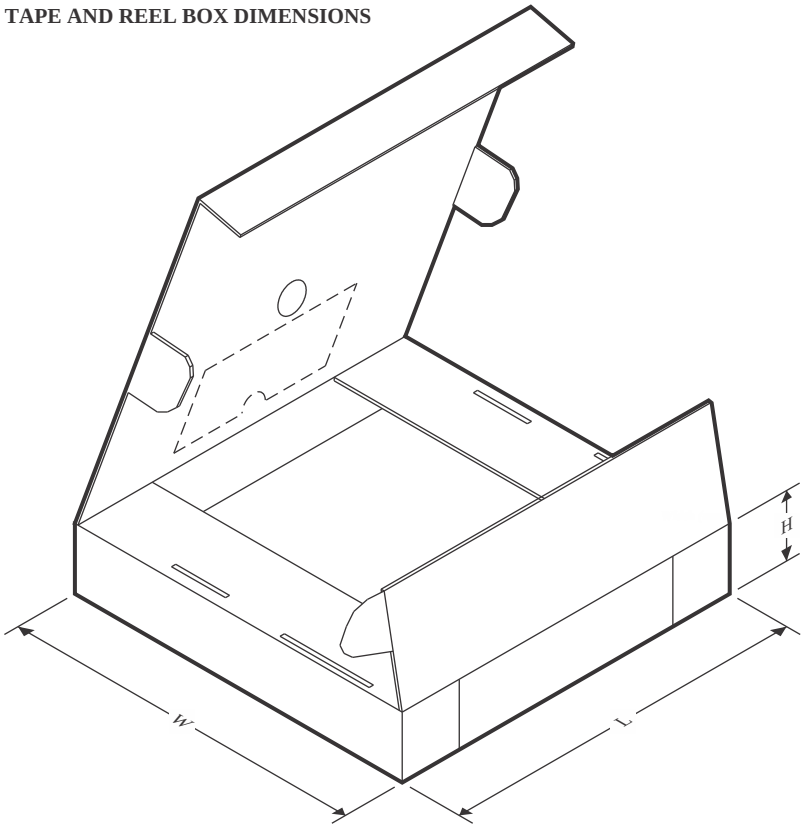
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5822MDCPR	HTSSOP	DCP	38	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5822MDCPR	HTSSOP	DCP	38	2000	353.0	353.0	32.0

GENERIC PACKAGE VIEW

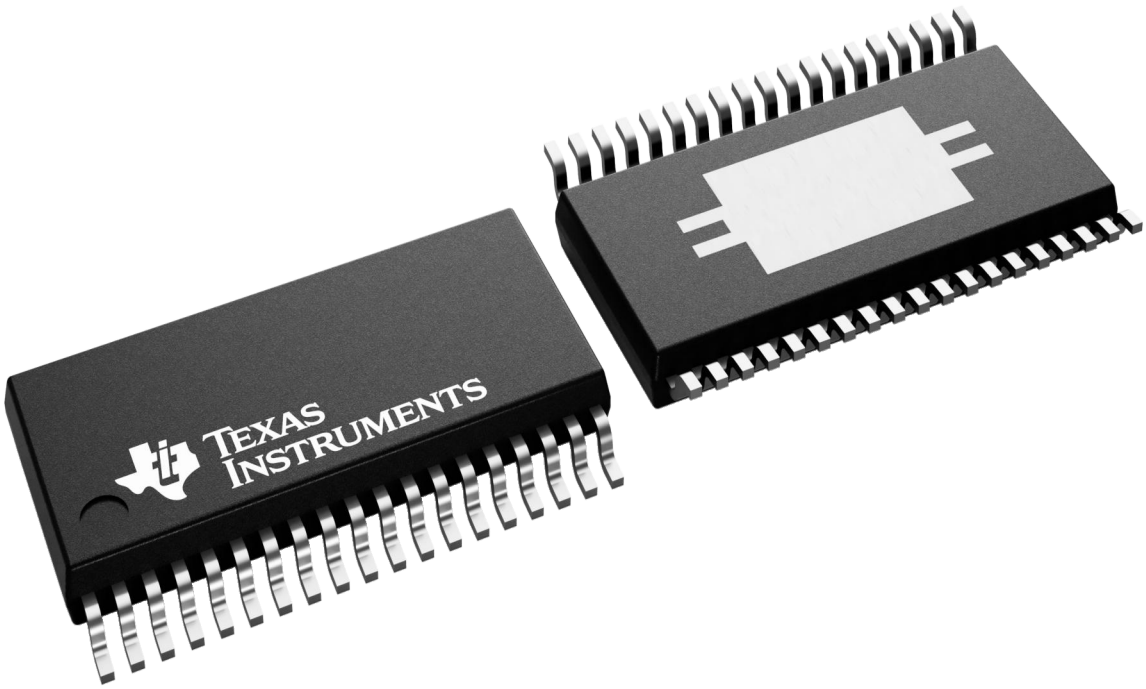
DCP 38

PowerPAD TSSOP - 1.2 mm max height

4.4 x 9.7, 0.5 mm pitch

SMALL OUTLINE PACKAGE

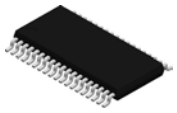
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224560/B

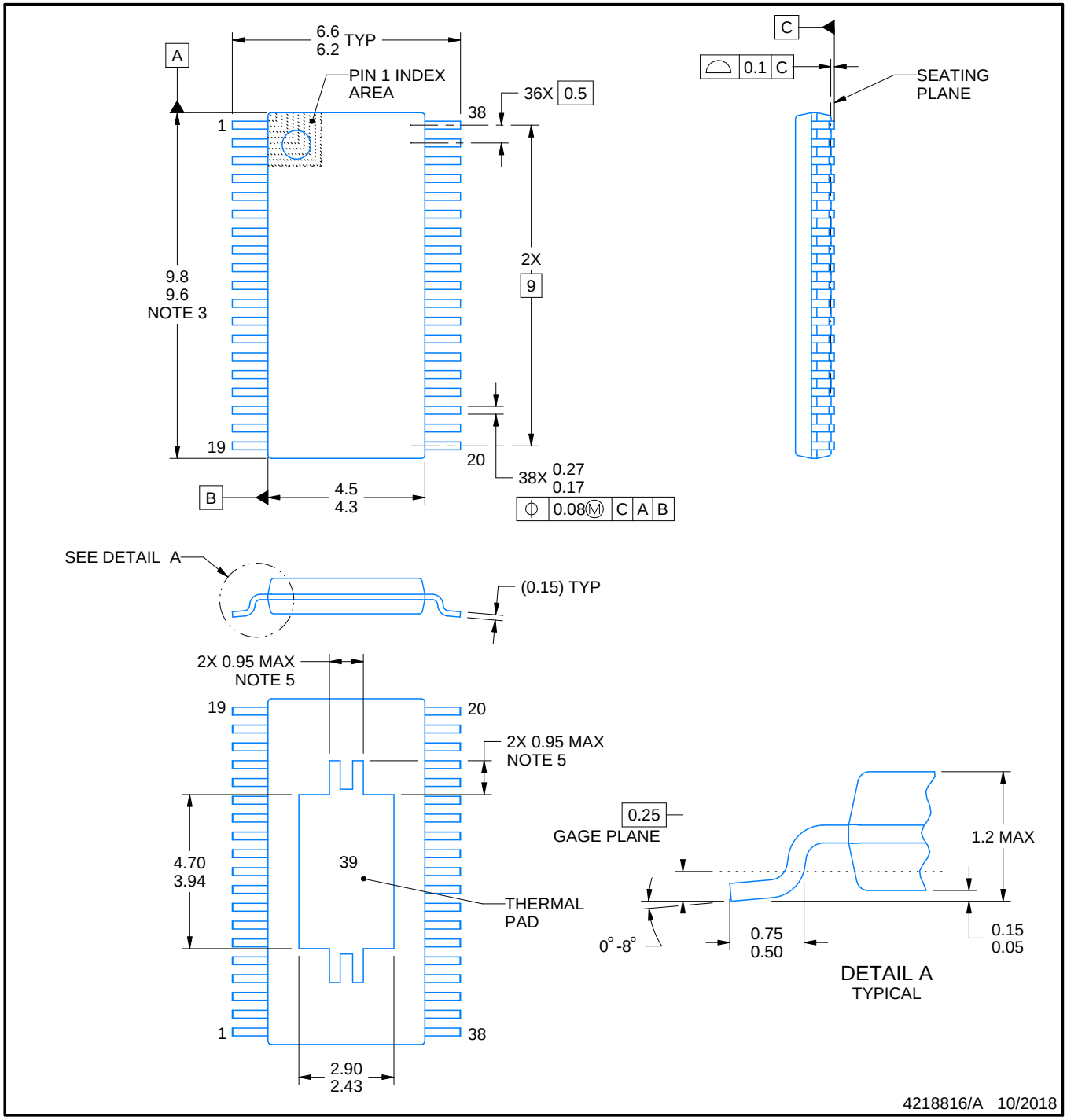
PACKAGE OUTLINE

DCP0038A



PowerPAD™ TSSOP - 1.2 mm max height

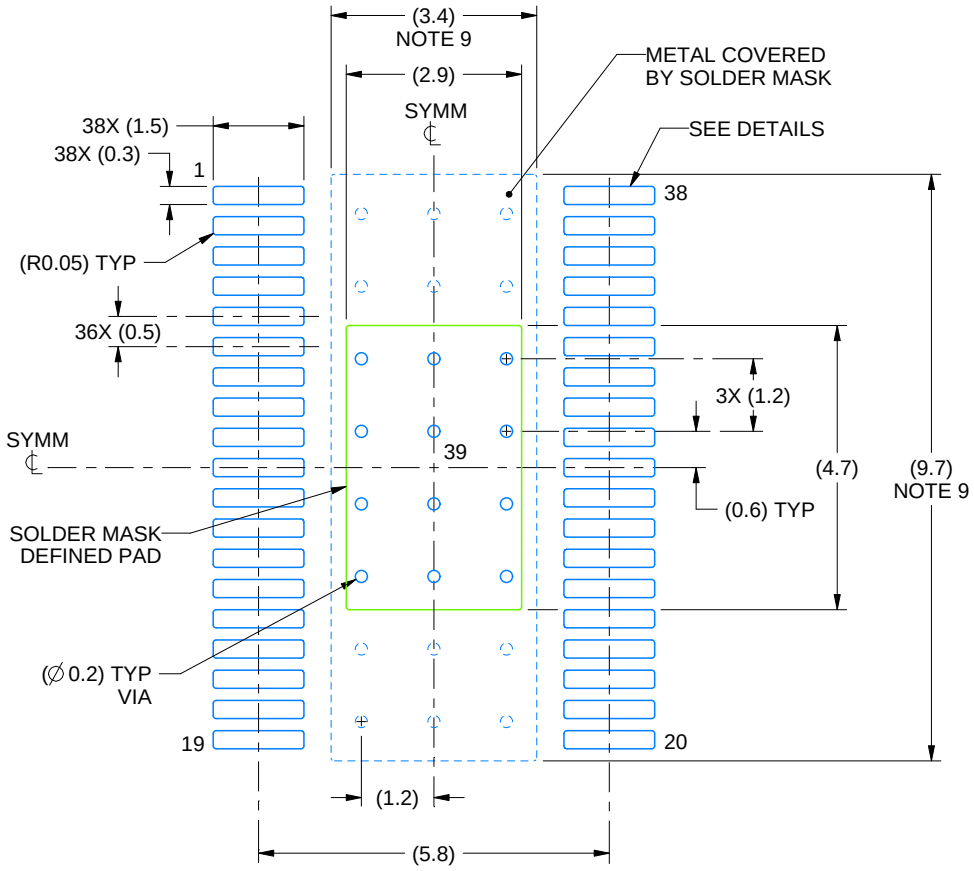
SMALL OUTLINE PACKAGE



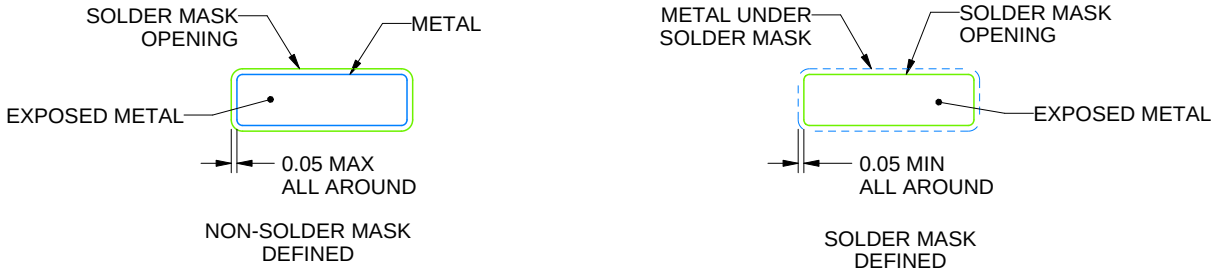
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

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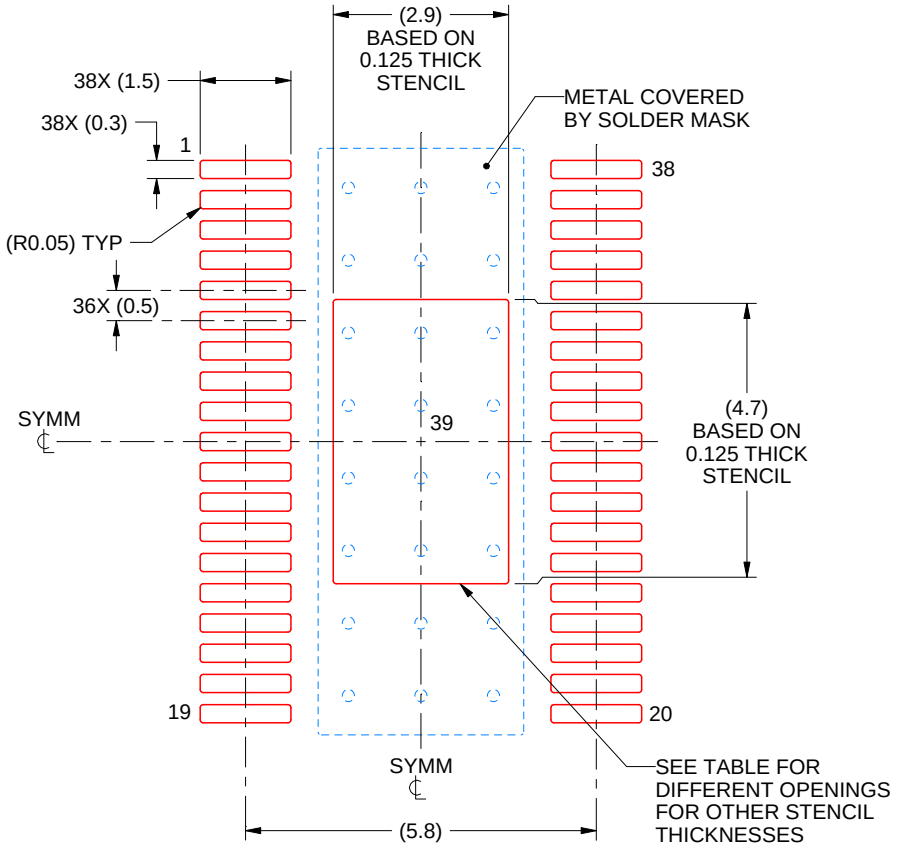
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.24 X 5.25
0.125	2.90 X 4.70 (SHOWN)
0.15	2.65 X 4.29
0.175	2.45 X 3.97

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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