THS4531A Ultra Low-Power, Rail-to-Rail Output, Fully Differential Amplifier

1 Features

- Ultra Low-Power:
  - Voltage: 2.5 V to 5.5 V
  - Current: 250 µA
  - Power-Down Mode: 0.5 µA (Typical)
- Fully Differential Architecture
- Bandwidth: 36 MHz (Av = 1 V/V)
- Slew Rate: 200 V/µs
- THD: –120 dBc at 1 kHz (1 V_{RMS}, R_L= 2 kΩ)
- Input Voltage Noise: 10 nV/$\sqrt{Hz}$ (f = 1 kHz)
- High DC Accuracy:
  - V_{OS}: ±100 µV
  - V_{OS} Drift: ±3 µV/˚C (–40°C to +125°C)
  - A_{OL}: 114 dB
- Rail-to-Rail Output (RRO)
- Negative Rail Input (NRI)
- Output Common-Mode Control
- 8-Pin SOIC (D) and VSSOP (DGK)
- 10-Pin WQFN (RUN)

2 Applications

- Low-Power SAR, ΔΣ ADC Driver
- Low-Power, High Performance:
  - Differential-to-Differential Amplifier
  - Single-Ended to Differential Amplifier
- Low-Power, Wide-Bandwidth Differential Driver
- Low-Power, Wide-Bandwidth Differential Signal Conditioning
- High-Channel Count and Power Dense Systems

3 Description

The THS4531A device is a low-power, fully differential amplifier with input common-mode range below the negative rail and rail-to-rail output. The device is designed for low-power data acquisition systems and high-density applications where power consumption and dissipation is critical.

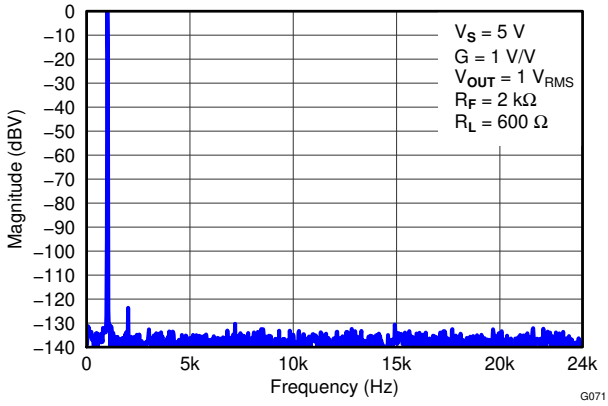
The device features accurate output common-mode control that allows for DC coupling when driving analog-to-digital converters (ADCs). This control, coupled with the input common-mode range below the negative rail and rail-to-rail output, allows for easy interface from single-ended ground-referenced signal sources to successive-approximation registers (SARs), and delta-sigma (ΔΣ) ADCs using only single-supply 2.5-V to 5-V power. The THS4531A is also a valuable tool for general-purpose, low-power differential signal conditioning applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
THS4531A	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	WQFN (10)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

1-kHz FFT Plot on Audio Analyzer



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 **Features** ... 1
2 **Applications** ... 1
3 **Description** ... 1
4 **Revision History** ... 2
5 **Related Products** ... 3
6 **Pin Configuration and Functions** ... 4
7 **Specifications** ... 5
7.1 Absolute Maximum Ratings ... 5
7.2 ESD Ratings ... 5
7.3 Recommended Operating Conditions ... 5
7.4 Thermal Information ... 5
7.5 Electrical Characteristics: V_S = 2.7 V ... 6
7.6 Electrical Characteristics: V_S = 5 V ... 8
7.7 Typical Characteristics ... 11
8 **Detailed Description** ... 24
8.1 Overview ... 24
8.2 Functional Block Diagram ... 24
8.3 Feature Description ... 24
8.4 Device Functional Modes ... 26
9 **Application and Implementation** ... 27
9.1 Application Information ... 27
9.2 Typical Applications ... 35
10 **Power Supply Recommendations** ... 45
11 **Layout** ... 45
11.1 Layout Guidelines ... 45
11.2 Layout Example ... 46
12 **Device and Documentation Support** ... 47
12.1 Device Support ... 47
12.2 Documentation Support ... 47
12.3 Community Resources ... 48
12.4 Trademarks ... 48
12.5 Electrostatic Discharge Caution ... 48
12.6 Glossary ... 48
13 **Mechanical, Packaging, and Orderable Information** ... 48

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (January 2016) to Revision D	Page
• Changed maximum range of the continuous input current, I_i From: *0.75 mA* To: *10 mA*	5

Changes from Revision B (June 2015) to Revision C	Page
• Changed Equation 5 for clarification	40

Changes from Revision A (January 2013) to Revision B	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Original (December 2012) to Revision A	Page
• Changed graph title from "V_{OS} OVER TEMPERATURE" to "SMALL-SIGNAL FREQUENCY RESPONSE"	18

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5 Related Products

Table 1. Related Amplifiers

DEVICE	BW (MHz)	I_Q (mA)	THD (dBc) at 100 kHz	V_N (nV/√Hz)	RAIL-TO-RAIL	DUAL PART NUMBERS
THS4531A	36	0.25	–104	10	Negative In, Out	THS4532
THS4121	100	16	–79	5.4	Out	
THS4521	145	1.14	–120	4.6	Negative In, Out	THS4522
THS4131	150	16	–107	1.3	No	
THS4520	620	14.2	–107	2	Out	
THS4541	850	10.1	–137	2.2	Negative In, Out	

Table 2. Related Precision ADCs

DEVICE	BITS	MAX DATA RATE (kSPS)	NOMINAL SUPPLY (V)	NOMINAL I_{CC} (mA) MAX CLK RATE	TYPICAL POWER (mW) MAX CLK RATE
ADS8881	18	1000	5	1.1	5.5
ADS8861	16	1000	3.3	1.67	5.3
ADS8321E	16	100	5	0.9	4.5
ADS7945	14	2000	5	2.32	5.8/ch (dual)
ADS7044	12	1000	3	0.3	0.9

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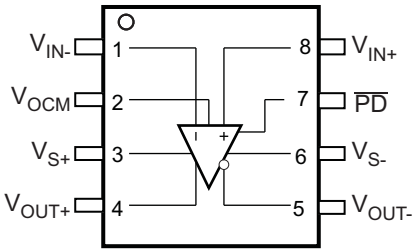
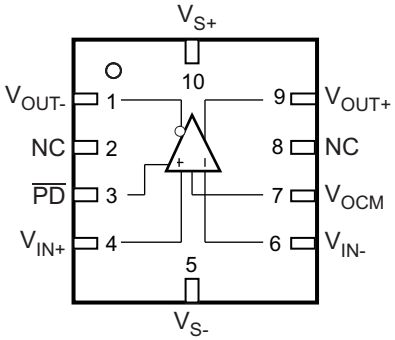
6 Pin Configuration and Functions

D and DGK Packages
8-Pin SOIC and VSSOP
Top View



RUN Package
10-Pin WQFN
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC, VSSOP	WQFN		
NC	—	2 8	—	No internal connection
$\overline{PD}$	7	3	I	Power-down, $\overline{PD}$ = logic low = low power mode, $\overline{PD}$ = logic high = normal operation **(PIN MUST BE DRIVEN)**
V_{IN+}	8	4	I	Non-inverted amplifier input
$V_{IN–}$	1	6	I	Inverting amplifier input
V_{OCM}	2	7	I	Common-mode voltage input
V_{OUT+}	4	9	O	Non-inverted amplifier output
$V_{OUT–}$	5	1	O	Inverted amplifier output
V_{S+}	3	10	I	Amplifier positive power-supply input
$V_{S–}$	6	5	I	Amplifier negative power-supply input. On multichannel devices, $V_{S–}$ is tied together.

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7 Specifications

7.1 Absolute Maximum Ratings

	MIN	MAX	UNIT
Supply voltage, V_{S-} to V_{S+}		5.5	
Input/output voltage, $V_{IN\pm}$, $V_{OUT\pm}$, and V_{OCM} pins	(V_{S-}) – 0.7	(V_{S+}) + 0.7	V
Differential input voltage, V_{ID}		1	V
Continuous output current, I_O		50	mA
Continuous input current, I_i		10	mA
Continuous power dissipation	See *Thermal Information*		
Maximum junction temperature, T_J		150	°C
Operating free-air temperature, T_A	–40	125	°C
Storage temperature, T_{stg}	–65	150	°C

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±3000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{S+}	Single-supply voltage	2.7	5	5.4	V
T_A	Ambient temperature	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC (1)		THS4531A			UNIT
		D (SOIC)	DGK (VSSOP)	RUN (WQFN)	
		8 PINS	8 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	133	198	163	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78	84	66	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	73	120	113	°C/W
ψ_{JT}	Junction-to-top characterization parameter	26	19	17	°C/W
ψ_{JB}	Junction-to-board characterization parameter	73	118	113	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: V_S = 2.7 V

Test conditions at T_A ≈ 25°C, V_{S+} = 2.7 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP}, R_F = 2 kΩ, R_L = 2 kΩ differential, G = 1 V/V, single-ended input, differential output, and output referenced to mid-supply, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL
AC PERFORMANCE						
Small-signal bandwidth	V_{OUT} = 100 mV_{PP}, G = 1		34		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 2		16			
	V_{OUT} = 100 mV_{PP}, G = 5		6			
	V_{OUT} = 100 mV_{PP}, G = 10		2.7			
Gain-bandwidth product	V_{OUT} = 100 mV_{PP}, G = 10		27		MHz	C
Large-signal bandwidth	V_{OUT} = 2 V_{PP}, G = 1		34		MHz	C
Bandwidth for 0.1-dB flatness	V_{OUT} = 2 V_{PP}, G = 1		12		MHz	C
Slew rate, rise/fall, 25% to 75%	V_{OUT} = 2-V step		190/320		V/µs	C
Rise/fall time, 10% to 90%	V_{OUT} = 2-V step		6		ns	C
Settling time to 1%	V_{OUT} = 2-V step		25		ns	C
Settling time to 0.1%	V_{OUT} = 2-V step		60		ns	C
Settling time to 0.01%	V_{OUT} = 2-V step		150		ns	C
Overshoot/undershoot	V_{OUT} = 2-V step		1%			C
2nd-order harmonic distortion	f = 1 kHz, V_{OUT} = 2 V_{PP}		–122		dBc	C
	f = 10 kHz		–127			
	f = 1 MHz		–59			
3rd-order harmonic distortion	f = 1 kHz, V_{OUT} = 2 V_{PP}		–136		dBc	C
	f = 10 kHz		–135			
	f = 1 MHz		–70			
2nd-order intermodulation distortion	f = 1 MHz, 200-kHz tone spacing, V_{OUT} = 1 Vpp each tone		–83		dBc	C
3rd-order intermodulation distortion	f = 1 MHz, 200-kHz tone spacing, V_{OUT} = 1 Vpp each tone		–81		dBc	C
Input voltage noise	f = 1 kHz		10		nV/√Hz	C
Voltage noise 1/f corner frequency			45		Hz	C
Input current noise	f = 100 kHz		0.25		pA/√Hz	C
Current noise 1/f corner frequency			6.5		kHz	C
Overdrive recovery time	Overdrive = 0.5 V		65		ns	C
Output balance error	V_{OUT} = 100 mV, f = 1 MHz		–65		dB	C
Closed-loop output impedance	f = 1 MHz (differential)		2.5		Ω	C
DC PERFORMANCE						
Open-loop voltage gain (A_{OL})		100	113		dB	A
Input-referred offset voltage	T_A = 25°C	–400	±100	400	µV	A
	T_A = 0°C to +70°C	–715		715		B
	T_A = –40°C to +85°C	–855		855		
	T_A = –40°C to +125°C	–1300		1300		
Input offset voltage drift(1)	T_A = 0°C to 70°C	–7	±2	7	µV/°C	B
	T_A = –40°C to +85°C	–7	±2	7		
	T_A = –40°C to +125°C	–9	±3	9		

(1) Input offset voltage drift, input bias current drift, and input offset current drift are average values calculated by taking data at the end points, computing the difference, and dividing by the temperature range.

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Electrical Characteristics: V_S = 2.7 V (continued)

Test conditions at T_A ≈ 25°C, V_{S+} = 2.7 V, $V_{S–}$ = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP}, R_F = 2 kΩ, R_L = 2 kΩ differential, G = 1 V/V, single-ended input, differential output, and output referenced to mid-supply, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL
Input bias current(2)	T_A = 25°C		200	250	nA	A
	T_A = 0°C to +70°C			275		B
	T_A = –40°C to +85°C			286		
	T_A = –40°C to +125°C			305		
Input bias current drift(1)	T_A = 0°C to +70°C		0.45	0.55	nA/°C	B
	T_A = –40°C to +85°C		0.45	0.55		
	T_A = –40°C to +125°C		0.45	0.55		
Input offset current	T_A = 25°C	–50	±5	50	nA	A
	T_A = 0°C to +70°C	–55		55		B
	T_A = –40°C to +85°C	–57		57		
	T_A = –40°C to +125°C	–60		60		
Input offset current drift(1)	T_A = 0°C to +70°C	–0.1	±0.03	0.1	nA/°C	B
	T_A = –40°C to +85°C	–0.1	±0.03	0.1		
	T_A = –40°C to +125°C	–0.1	±0.03	0.1		
INPUT						
Common-mode input low	T_A = 25°C, CMRR > 87 dB		$V_{S–}$ – 0.2	$V_{S–}$	V	A
	T_A = –40°C to +125°C, CMRR > 87 dB		$V_{S–}$ – 0.2	$V_{S–}$		B
Common-mode input high	T_A = 25°C, CMRR > 87 dB	V_{S+} – 1.2	V_{S+} – 1.1		V	A
	T_A = –40°C to +125°C, CMRR > 87 dB	V_{S+} – 1.2	V_{S+} – 1.1			B
Common-mode rejection ratio		90	116		dB	A
Input impedance differential mode			200 || 1		kΩ || pF	C
OUTPUT						
Single-ended output voltage: low	T_A = 25°C		$V_{S–}$ + 0.06	$V_{S–}$ + 0.2	V	A
	T_A = –40°C to +125°C		$V_{S–}$ + 0.06	$V_{S–}$ + 0.2		B
Single-ended output voltage: high	T_A = 25°C	V_{S+} – 0.2	V_{S+} – 0.11		V	A
	T_A = –40°C to +125°C	V_{S+} – 0.2	V_{S+} – 0.11			B
Output saturation voltage: high/low			110/60		mV	C
Linear output current drive	T_A = 25°C, R_L = 6 Ω	±15	±22		mA	A
	T_A = –40°C to +125°C	±15				B
POWER SUPPLY						
Specified operating voltage		2.5	2.7	5.5	V	B
Quiescent operating current/ch	T_A = 25°C, $\overline{PD}$ = V_{S+}		230	330	µA	A
	T_A = –40°C to +125°C, $\overline{PD}$ = V_{S+}		270	370		B
Power-supply rejection (PSRR)		87	108		dB	A
POWER DOWN						
Enable voltage threshold	Specified on above 2.1 V			2.1	V	A
Disable voltage threshold	Specified off below 0.7 V	0.7			V	A
Disable pin bias current	$\overline{PD}$ = $V_{S–}$ + 0.5 V		50	500	nA	A
Power-down quiescent current	$\overline{PD}$ = $V_{S–}$ + 0.5 V		0.5	2	µA	A
Turnon time delay	Time from $\overline{PD}$ = high to V_{OUT} = 90% of final value, R_L= 200 Ω		650		ns	C

(2) Positive current is out of the device inputs.

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Electrical Characteristics: V_S = 2.7 V (continued)

Test conditions at T_A ≈ 25°C, V_{S+} = 2.7 V, $V_{S–}$ = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP}, R_F = 2 kΩ, R_L = 2 kΩ differential, G = 1 V/V, single-ended input, differential output, and output referenced to mid-supply, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL
Turnoff time delay	Time from $\overline{PD}$ = low to V_{OUT} = 10% of original value, R_L= 200 Ω		20		ns	C
OUTPUT COMMON-MODE VOLTAGE CONTROL (V_{OCM})						
Small-signal bandwidth	V_{OCM} input = 100 mV_{PP}		23		MHz	C
Slew rate	V_{OCM} input = 1 V_{STEP}		14		V/µs	C
Gain		0.99	0.996	1.01	V/V	A
Common-mode offset voltage	Offset = output common-mode voltage – V_{OCM} input voltage	–5	±1	5	mV	A
V_{OCM} input bias current	V_{OCM} = (V_{S+} + $V_{S–}$)/2	–100	±20	100	nA	A
V_{OCM} input voltage range		0.8	0.75 to 1.9	1.75	V	A
V_{OCM} input impedance			100 || 1.6		kΩ || pF	C
Default voltage offset from (V_{S+} + $V_{S–}$)/2	Offset = output common-mode voltage – (V_{S+} + $V_{S–}$)/2 with V_{OCM} input floating	–10	±3	10	mV	A

7.6 Electrical Characteristics: V_S = 5 V

Test conditions at T_A ≈ 25°C, V_{S+} = 5 V, $V_{S–}$ = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP}, R_F = 2 kΩ, R_L = 2 kΩ differential, G = 1 V/V, single-ended input, differential output, and output referenced to mid-supply, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL
AC PERFORMANCE						
Small-signal bandwidth	V_{OUT} = 100 mV_{PP}, G = 1		36		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 2		17			
	V_{OUT} = 100 mV_{PP}, G = 5		6			
	V_{OUT} = 100 mV_{PP}, G = 10		2.7			
Gain-bandwidth product	V_{OUT} = 100 mV_{PP}, G = 10		27		MHz	C
Large-signal bandwidth	V_{OUT} = 2 V_{PP}, G = 1		36		MHz	C
Bandwidth for 0.1-dB flatness	V_{OUT} = 2 V_{PP}, G = 1		15		MHz	C
Slew rate, rise/fall, 25% to 75%	V_{OUT} = 2 V_{Step}		220/390		V/µs	C
Rise/fall time, 10% to 90%	V_{OUT} = 2 V_{Step}		5		ns	C
Settling time to 1%	V_{OUT} = 2 V_{Step}		25		ns	C
Settling time to 0.1%	V_{OUT} = 2 V_{Step}		60		ns	C
Settling time to 0.01%	V_{OUT} = 2 V_{Step}		150		ns	C
Overshoot/undershoot	V_{OUT} = 2 V_{Step}		1%			C
2nd-order harmonic distortion	f = 1 kHz, V_{OUT} = 2 V_{PP}		–129		dBc	C
	f = 10 kHz		–128			
	f = 1 MHz		–60			
3rd-order harmonic distortion	f = 1 kHz, V_{OUT} = 2 V_{PP}		–138		dBc	C
	f = 10 kHz		–137			
	f = 1 MHz		–71			
2nd-order intermodulation distortion	f = 1 MHz, 200-kHz tone spacing, V_{OUT} = 1 Vpp each tone		–85		dBc	C
3rd-order intermodulation distortion	f = 1 MHz, 200-kHz tone spacing, V_{OUT} = 1 Vpp each tone		–83		dBc	C
Input voltage noise	f = 1 kHz		10		nV/√Hz	C
Voltage noise 1/f corner frequency			45		Hz	C

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Electrical Characteristics: V_S = 5 V (continued)

Test conditions at T_A ≈ 25°C, V_{S+} = 5 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP}, R_F = 2 kΩ, R_L = 2 kΩ differential, G = 1 V/V, single-ended input, differential output, and output referenced to mid-supply, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL
Input current noise	f = 100 kHz		0.25		pA/√Hz	C
Current noise 1/f corner frequency			6.5		kHz	C
Overdrive recovery time	Overdrive = 0.5 V		65		ns	C
Output balance error	V_{OUT} = 100 mV, f = 1 MHz		–67		dB	C
Closed-loop output impedance	f = 1 MHz (differential)		2.5		Ω	C
DC PERFORMANCE						
Open-loop voltage gain (A_{OL})		100	114		dB	A
Input-referred offset voltage	T_A = 25°C	–400	±100	400	µV	A
	T_A = 0°C to +70°C	–715		715		B
	T_A = –40°C to +85°C	–855		855		
	T_A = –40°C to +125°C	–1300		1300		
Input offset voltage drift(1)	T_A = 0°C to +70°C	–7	±2	7	µV/°C	B
	T_A = –40°C to +85°C	–7	±2	7		
	T_A = –40°C to +125°C	–9	±3	9		
Input bias current(2)	T_A = 25°C		200	250	nA	A
	T_A = 0°C to +70°C			279		B
	T_A = –40°C to +85°C			292		
	T_A = –40°C to +125°C			315		
Input bias current drift(1)	T_A = 0°C to +70°C		0.5	0.65	nA/°C	B
	T_A = –40°C to +85°C		0.5	0.65		
	T_A = –40°C to +125°C		0.5	0.65		
Input offset current	T_A = 25°C	–50	±5	50	nA	A
	T_A = 0°C to +70°C	–55		55		B
	T_A = –40°C to +85°C	–57		57		
	T_A = –40°C to +125°C	–60		60		
Input offset current drift(1)	T_A = 0°C to +70°C	–0.1	±0.03	0.1	nA/°C	B
	T_A = –40°C to +85°C	–0.1	±0.03	0.1		
	T_A = –40°C to +125°C	–0.1	±0.03	0.1		
INPUT						
Common-mode input: low	T_A = 25°C, CMRR > 87 dB		V_{S-} – 0.2	V_{S-}	V	A
	T_A = –40°C to +125°C, CMRR > 87 dB		V_{S-} – 0.2	V_{S-}		B
Common-mode input: high	T_A = 25°C, CMRR > 87 dB	V_{S+} – 1.2	V_{S+} –1.1		V	A
	T_A = –40°C to +125°C, CMRR > 87 dB	V_{S+} – 1.2	V_{S+} –1.1			B
Common-mode rejection ratio		90	116		dB	A
Input impedance differential mode			200 || 1		kΩ || pF	C
OUTPUT						
Linear output voltage: low	T_A = 25°C		V_{S-} + 0.1	V_{S-} + 0.2	V	A
	T_A = –40°C to +125°C		V_{S-} + 0.1	V_{S-} + 0.2		B
Linear output voltage: high	T_A = 25°C	V_{S+} – 0.25	V_{S+} – 0.12		V	A
	T_A = –40°C to +125°C	V_{S+} – 0.25	V_{S+} – 0.12			B
Output saturation voltage: high/low			120/100		mV	C

(1) Input offset voltage drift, input bias current drift, and input offset current drift are average values calculated by taking data at the end points, computing the difference, and dividing by the temperature range.
(2) Positive current is out of the device inputs.

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Electrical Characteristics: V_S = 5 V (continued)

Test conditions at T_A ≈ 25°C, V_{S+} = 5 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP}, R_F = 2 kΩ, R_L = 2 kΩ differential, G = 1 V/V, single-ended input, differential output, and output referenced to mid-supply, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL
Linear output current drive	T_A = 25°C, R_L = 6Ω	±15	±25		mA	A
	T_A = –40°C to +125°C	±15				B
POWER SUPPLY						
Specified operating voltage		2.5	5	5.5	V	B
Quiescent operating current/ch	T_A = 25°C, $\overline{PD}$ = V_{S+}		250	350	µA	A
	T_A = –40°C to 125°C, $\overline{PD}$ = V_{S+}		290	390		B
Power-supply rejection (PSRR)		87	108		dB	A
POWER DOWN						
Enable voltage threshold	Specified on above 2.1 V			2.1	V	A
Disable voltage threshold	Specified off below 0.7 V	0.7			V	A
Disable pin bias current	$\overline{PD}$ = V_{S-} + 0.5 V		50	500	nA	A
Power-down quiescent current	$\overline{PD}$ = V_{S-} + 0.5 V		0.5	2	µA	A
Turnon time delay	Time from $\overline{PD}$ = high to V_{OUT} = 90% of final value, R_L= 200 Ω		600		ns	C
Turnoff time delay	Time from $\overline{PD}$ = low to V_{OUT} = 10% of original value, R_L= 200 Ω		15		ns	C
OUTPUT COMMON-MODE VOLTAGE CONTROL (V_{OCM})						
Small-signal bandwidth	V_{OCM} input = 100 mV_{PP}		24		MHz	C
Slew rate	V_{OCM} input = 1 V_{STEP}		15		V/µs	C
Gain		0.99	0.996	1.01	V/V	A
Common-mode offset voltage	Offset = output common-mode voltage – V_{OCM} input voltage	–5	±1	5	mV	A
V_{OCM} input bias current	V_{OCM} = (V_{S+} + V_{S-})/2		±20	±120	nA	A
V_{OCM} input voltage range		0.95	0.75 to 4.15	4.0	V	A
V_{OCM} input impedance			65 || 0.86		kΩ || pF	C
Default voltage offset from (V_{S+} + V_{S-})/2	Offset = output common-mode voltage – (V_{S+} + V_{S-})/2 with V_{OCM} input floating	–10	±3	10	mV	A

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7.7 Typical Characteristics

Table 3. Table Of Graphs

Description	V_S = 2.7 V	V_S = 5 V
Small-signal frequency response	Figure 1	Figure 34
Large-signal frequency response	Figure 2	Figure 35
Large- and small- signal pulse response	Figure 3	Figure 36
Single-ended slew rate versus V_{OUT} step	Figure 4	Figure 37
Differential slew rate versus V_{OUT} step	Figure 5	Figure 38
Overdrive recovery	Figure 6	Figure 39
10-kHz FFT on audio analyzer	Figure 7	Figure 40
Harmonic distortion versus Frequency	Figure 8	Figure 41
Harmonic distortion versus Output voltage at 1 MHz	Figure 9	Figure 42
Harmonic distortion versus Gain at 1 MHz	Figure 10	Figure 43
Harmonic distortion versus Load at 1 MHz	Figure 11	Figure 44
Harmonic distortion versus V_{OCM} at 1 MHz	Figure 12	Figure 45
Two-tone, 2nd and 3rd order intermodulation distortion versus Frequency	Figure 13	Figure 46
Single-ended output voltage swing versus Load resistance	Figure 14	Figure 47
Single-ended output saturation voltage versus Load current	Figure 15	Figure 48
Main amplifier differential output impedance versus Frequency	Figure 16	Figure 49
Frequncy response versus C_{LOAD}	Figure 17	Figure 50
R_O versus C_{LOAD}	Figure 18	Figure 51
Rejection ratio versus Frequency	Figure 19	Figure 52
Turnon time	Figure 20	Figure 53
Turnoff time	Figure 21	Figure 54
Input-referred voltage noise and current noise spectral density	Figure 22	Figure 55
Main amplifier differential open-loop gain and phase versus Frequency	Figure 23	Figure 56
Output balance error versus Frequency	Figure 24	Figure 57
V_{OCM} small signal frequency response	Figure 25	Figure 58
V_{OCM} large and small signal pulse response	Figure 26	Figure 59
V_{OCM} input impedance versus frequency	Figure 27	Figure 60
Count versus input offset current	Figure 28	Figure 61
Count versus input offset current temperature drift	Figure 29	Figure 62
Input offset current versus temperature	Figure 30	Figure 63
Count versus input offset voltage	Figure 31	Figure 64
Count versus input offset voltage temperature drift	Figure 32	Figure 65
Input offset voltage versus temperature	Figure 33	Figure 66

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7.7.1 Typical Characteristics: V_S = 2.7 V

Test conditions unless otherwise noted: V_{S+} = 2.7 V, V_{S-} = 0 V, CM = open, V_{OUT} = 2 Vpp, R_F = 2 kΩ, R_L = 2 kΩ Differential, G = 1 V/V, Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply, T_A ≈ 25°C, unless otherwise noted.

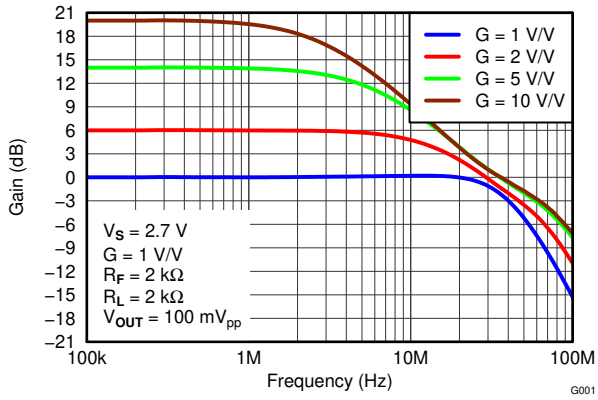

Figure 1. Small-Signal Frequency Response

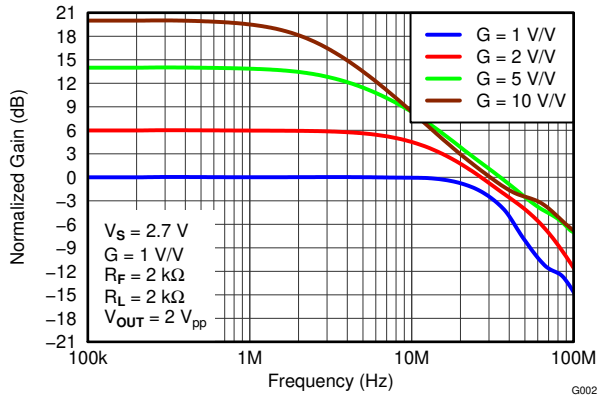

Figure 2. Large-Signal Frequency Response

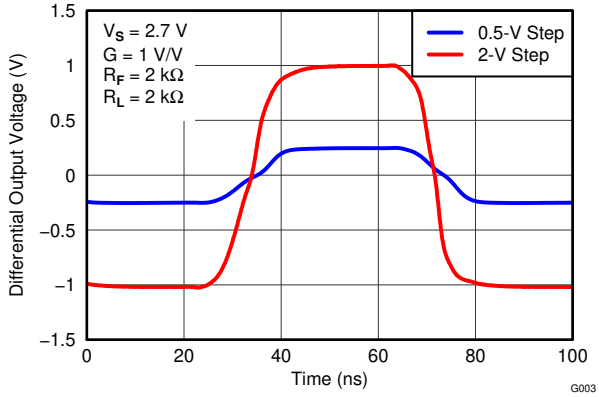

Figure 3. Large- and Small-Signal Pulse Response

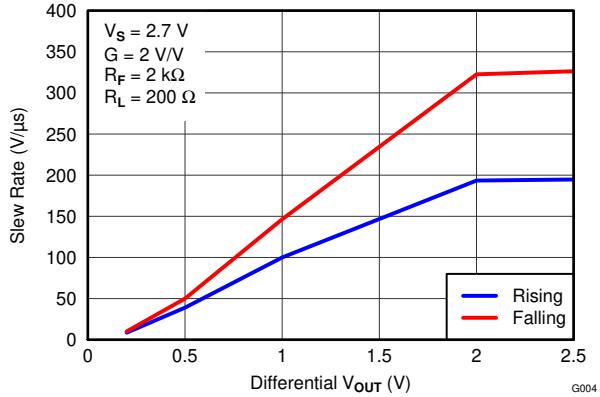

Figure 4. Single-Ended Slew Rate vs V_{OUT} Step

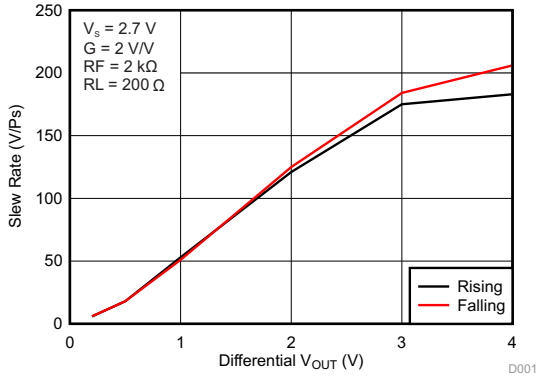

Figure 5. Differential Slew Rate vs V_{OUT} Step

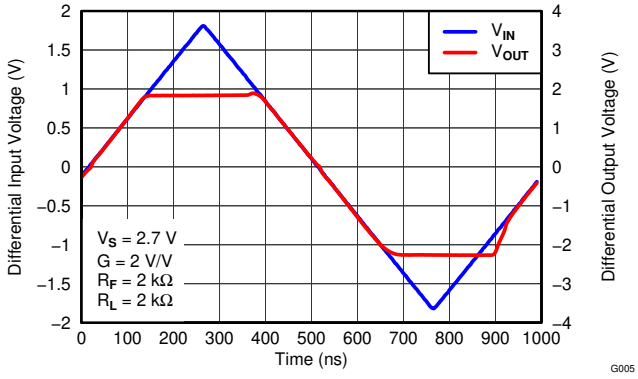

Figure 6. Overdrive Recovery

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Typical Characteristics: V_S = 2.7 V (continued)

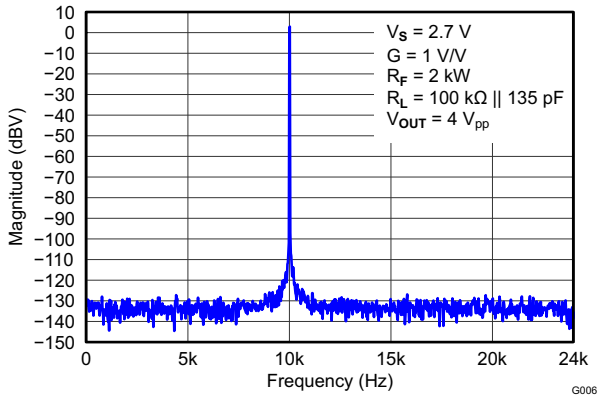

Figure 7. 10-kHz FFT On Audio Analyzer

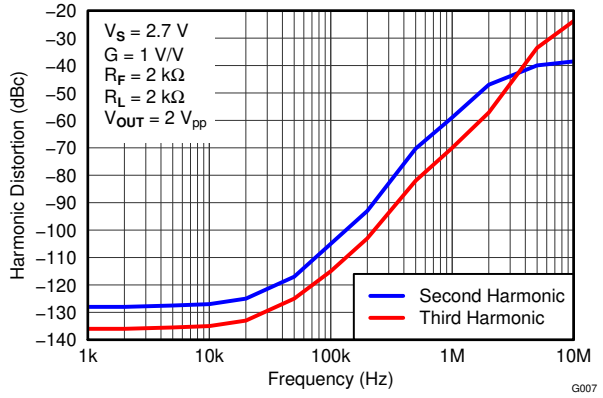

Figure 8. Harmonic Distortion vs Frequency

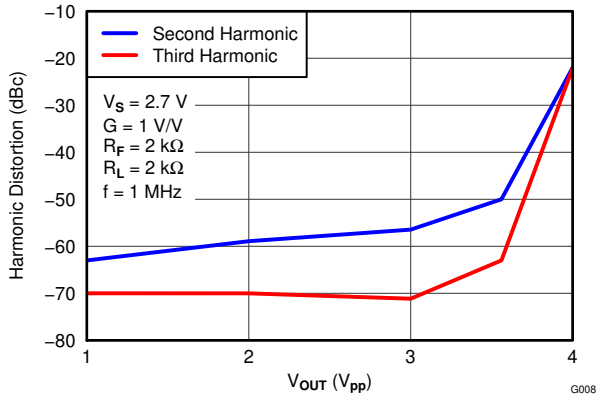

Figure 9. Harmonic Distortion vs Output Voltage at 1 MHz

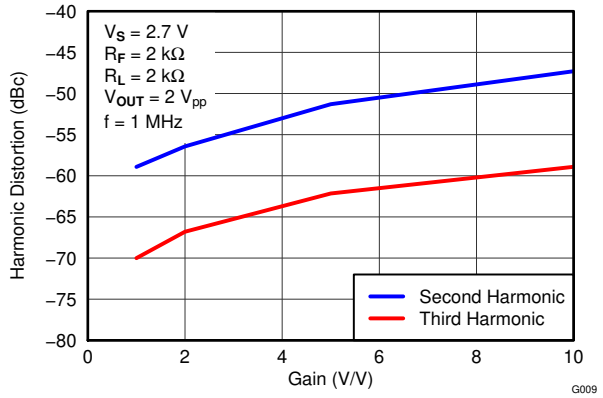

Figure 10. Harmonic Distortion vs Gain at 1 MHz

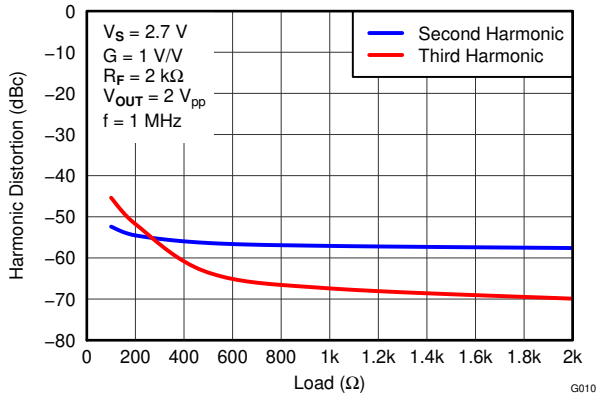

Figure 11. Harmonic Distortion vs Load at 1 MHz

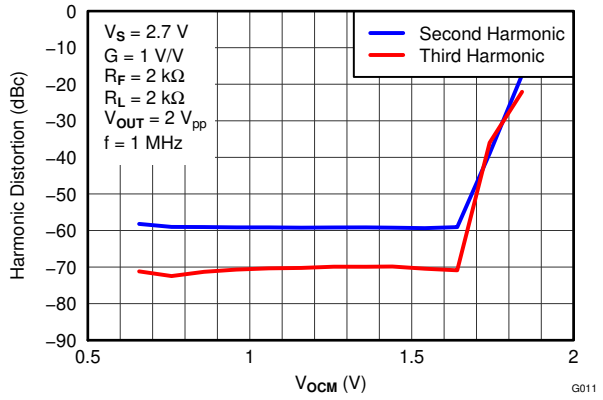

Figure 12. Harmonic Distortion vs V_{OCM} at 1 MHz

Typical Characteristics: V_S = 2.7 V (continued)

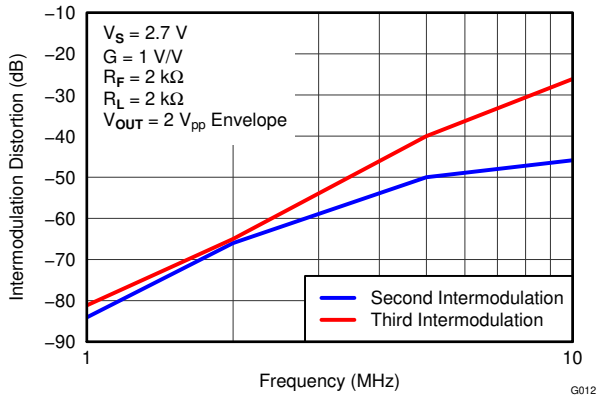

Figure 13. Two-Tone, 2nd and 3rd Order Intermodulation Distortion vs Frequency

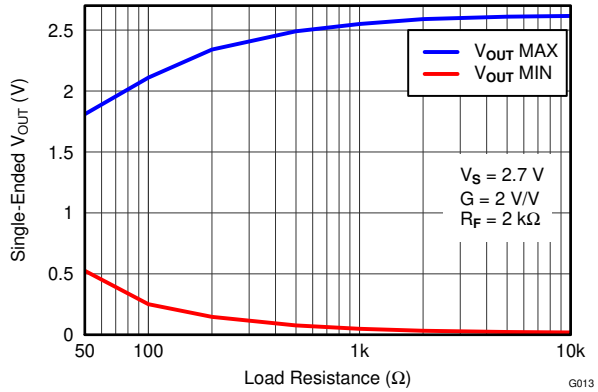

Figure 14. Single-Ended Output Voltage Swing vs Load Resistance

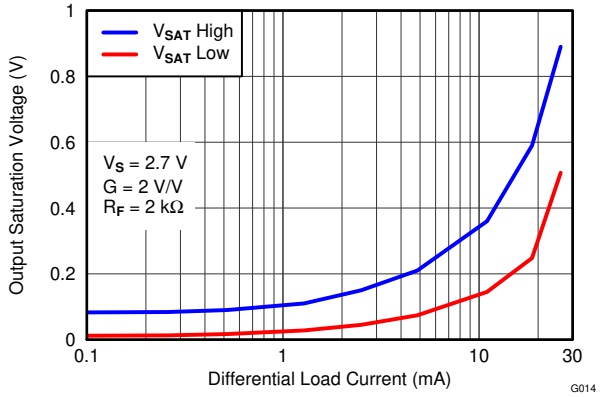

Figure 15. Single-Ended Output Saturation Voltage vs Load Current

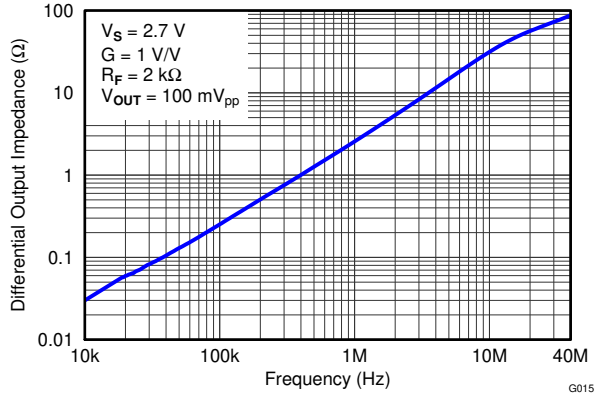

Figure 16. Main Amplifier Differential Output Impedance vs Frequency

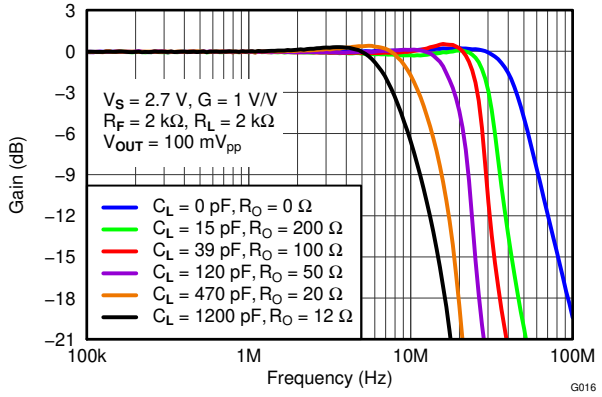

Figure 17. Frequency Response vs C_{LOAD}

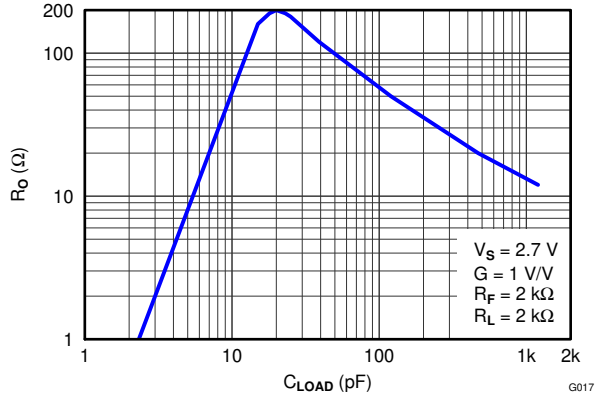

Figure 18. R_O vs C_{LOAD}

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Typical Characteristics: V_S = 2.7 V (continued)

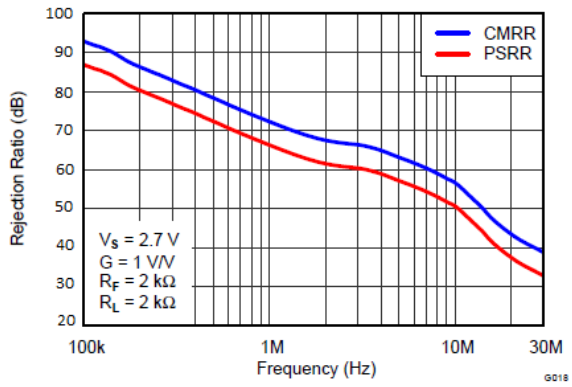

Figure 19. Rejection Ratio vs Frequency

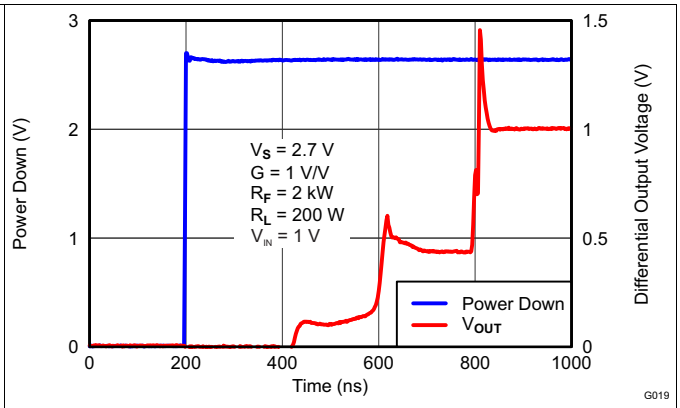

Figure 20. Turnon Time

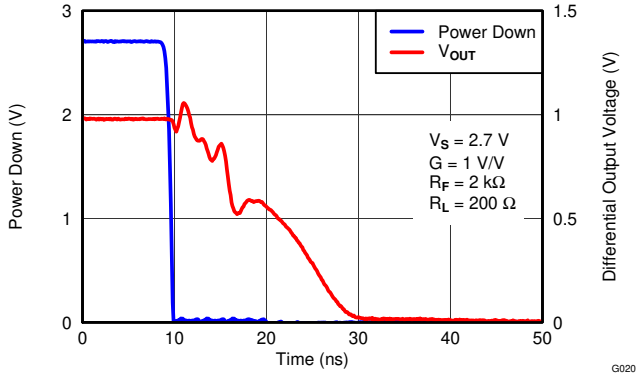

Figure 21. Turnoff Time

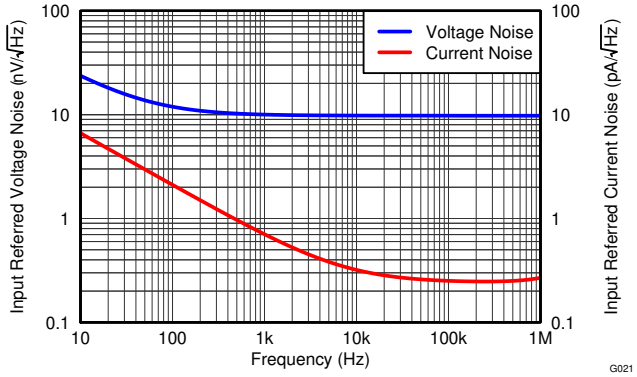

Figure 22. Input-Referred Voltage Noise and Current Noise Spectral Density

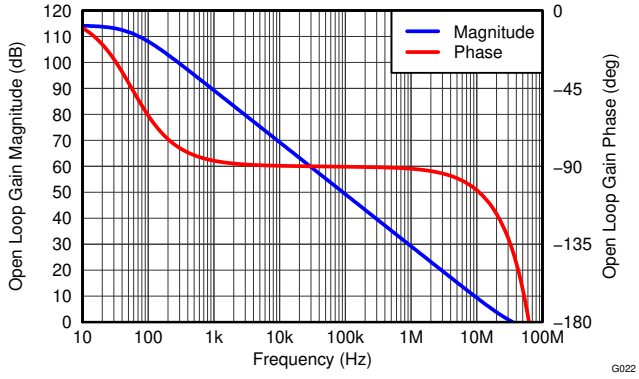

Figure 23. Main Amplifier Differential Open-Loop Gain and Phase vs Frequency

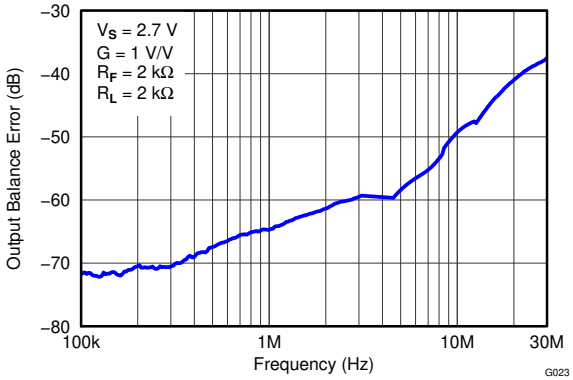

Figure 24. Output Balance Error vs Frequency

Typical Characteristics: V_S = 2.7 V (continued)

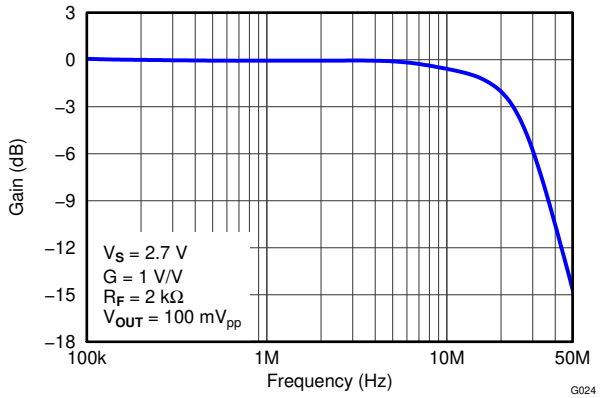

Figure 25. V_{OCM} Small-Signal Frequency Response

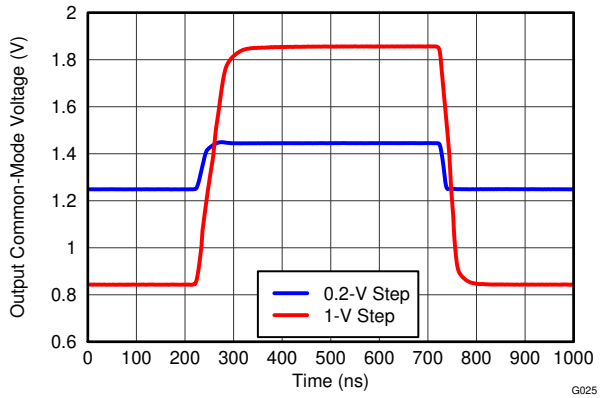

Figure 26. V_{OCM} Large- and Small Signal Pulse Response

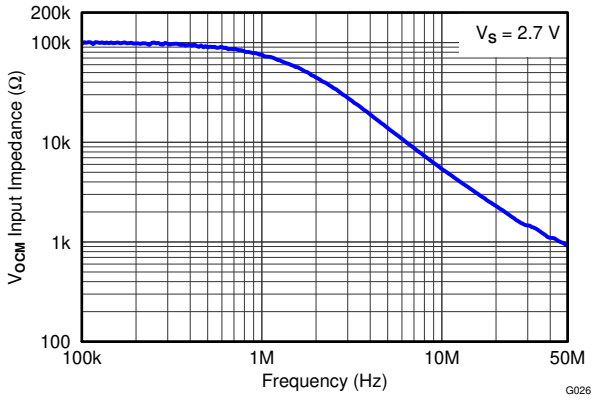

Figure 27. V_{OCM} Input Impedance vs Frequency

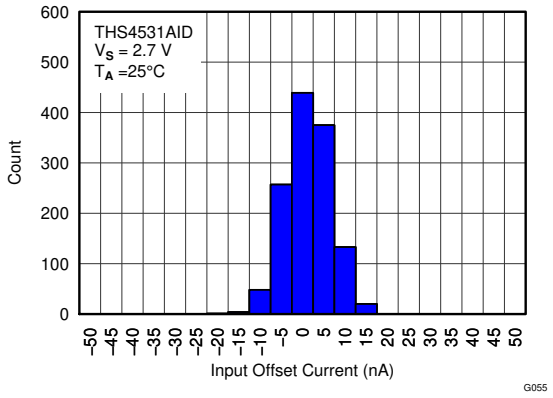

Figure 28. Input Offset Current Histogram

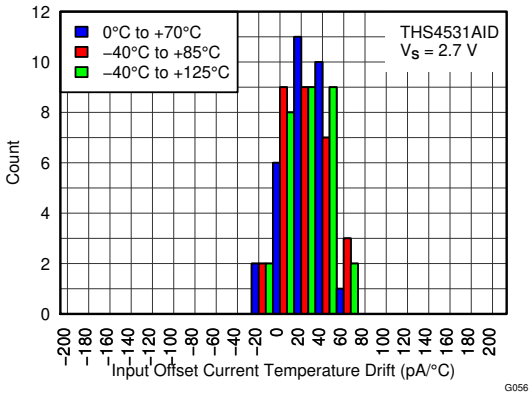

Figure 29. Input Offset Current Temp Drift Histogram

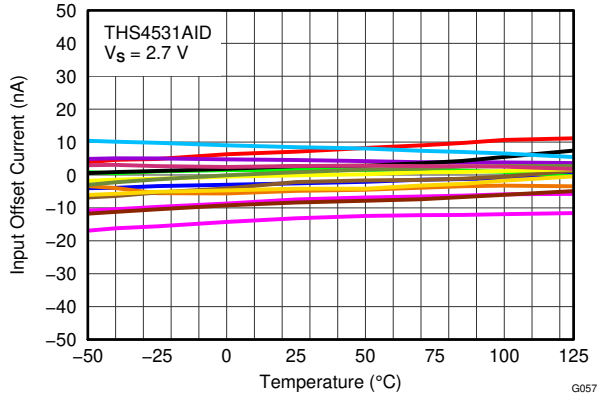

Figure 30. Input Offset Current vs Temperature

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Typical Characteristics: V_S = 2.7 V (continued)

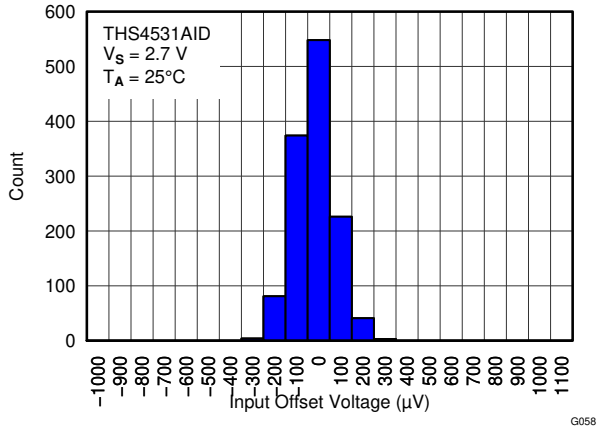

Figure 31. Input Offset Voltage Histogram

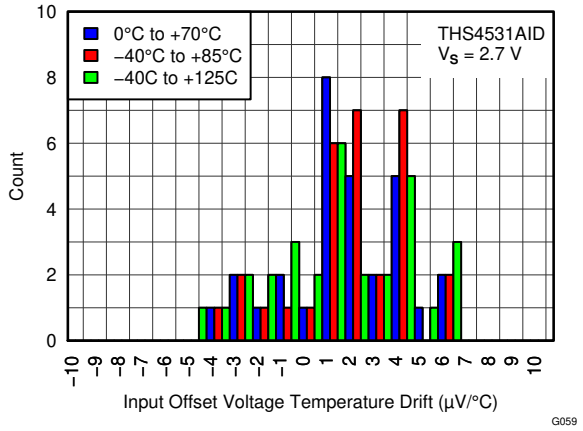

Figure 32. Input Offset Voltage Temp Drift Histogram

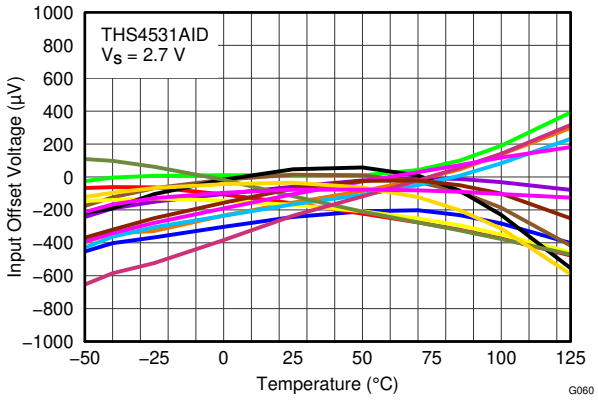

Figure 33. Input Offset Voltage vs Temperature

7.7.2 Typical Characteristics: V_S = 5 V

Test conditions unless otherwise noted: V_{S+} = 5 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 Vpp, R_F = 2 kΩ, R_L = 2 kΩ Differential, G = 1 V/V, Single-Ended Input, Differential Output, Input and Output Referenced to mid-supply, T_A = 25°C, unless otherwise noted.

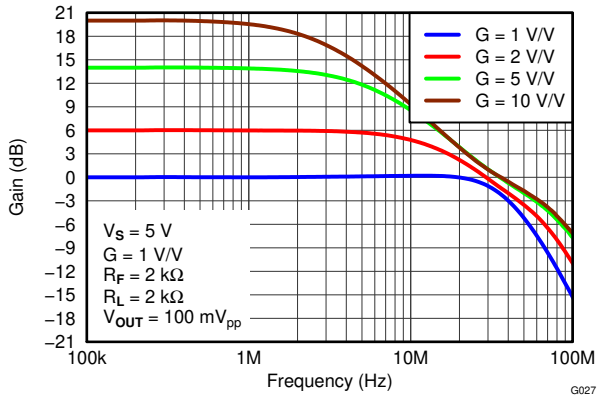

Figure 34. Small-Signal Frequency Response

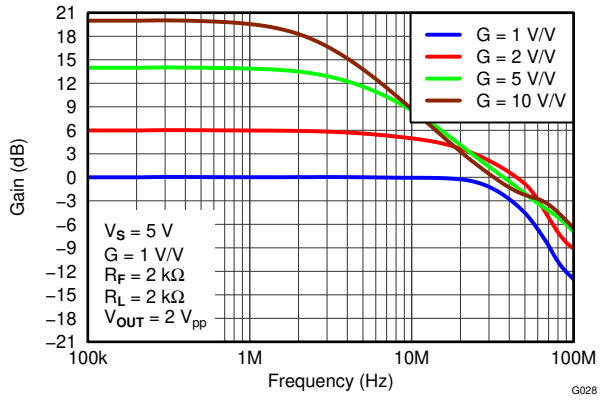

Figure 35. Large-Signal Frequency Response

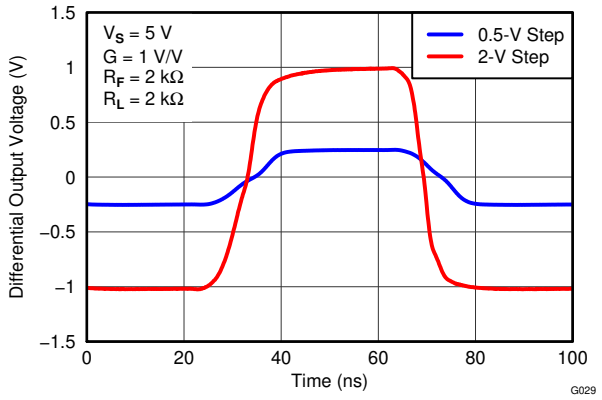

Figure 36. Large- and Small-signal Pulse Response

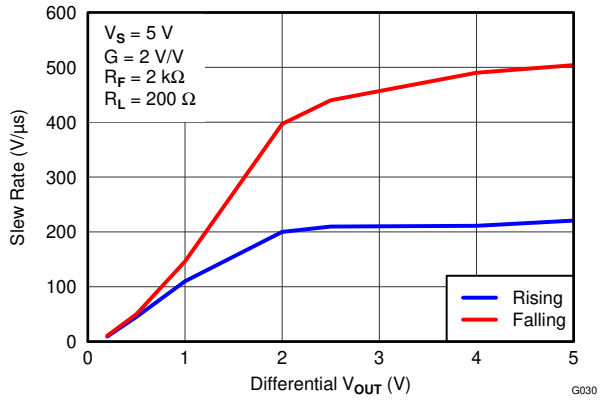

Figure 37. Single-Ended Slew Rate vs V_{OUT} Step

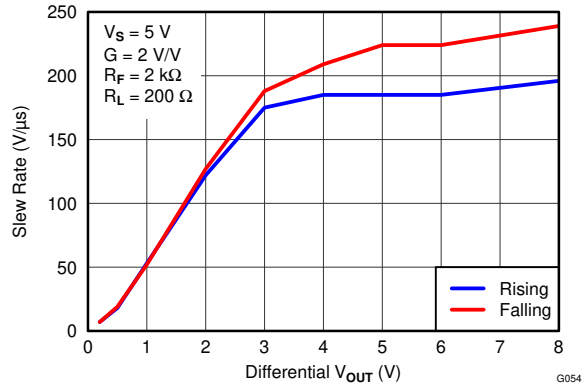

Figure 38. Differential Slew Rate vs V_{OUT} Step

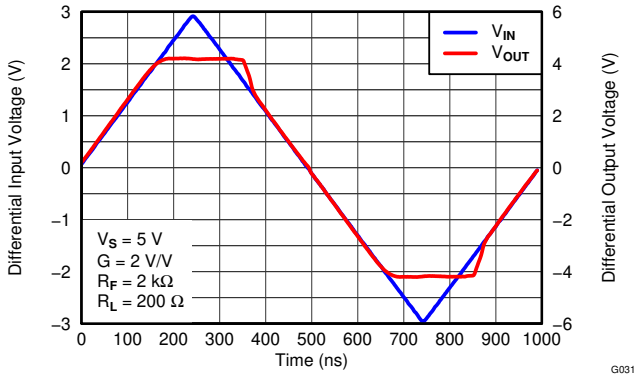

Figure 39. Overdrive Recovery

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Typical Characteristics: V_S = 5 V (continued)

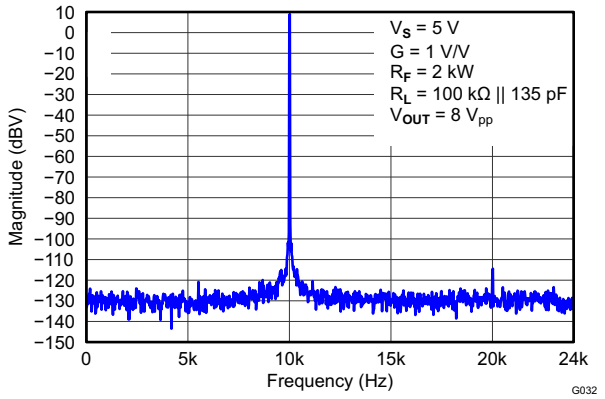

Figure 40. 10-kHz FFT On Audio Analyzer

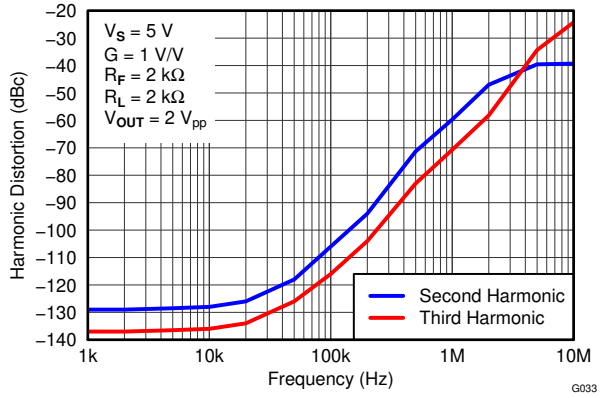

Figure 41. Harmonic Distortion vs Frequency

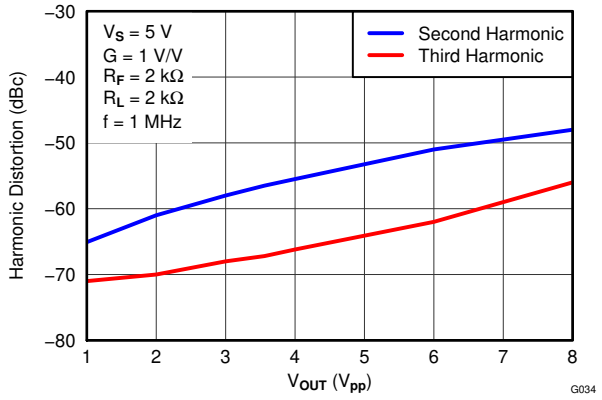

Figure 42. Harmonic Distortion vs Output Voltage at 1 MHz

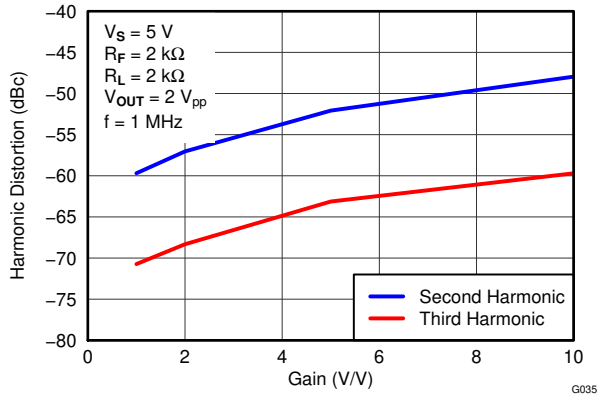

Figure 43. Harmonic Distortion vs Gain at 1 MHz

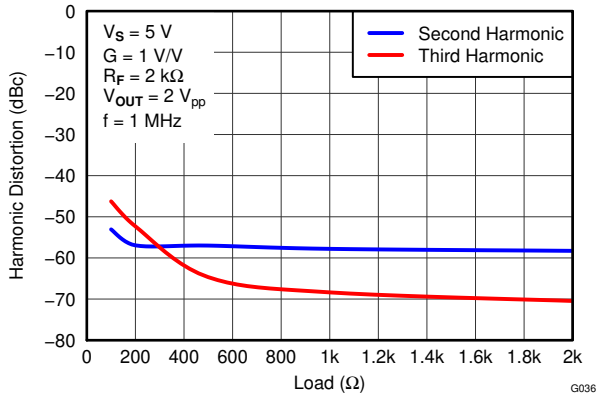

Figure 44. Harmonic Distortion vs Load at 1 MHz

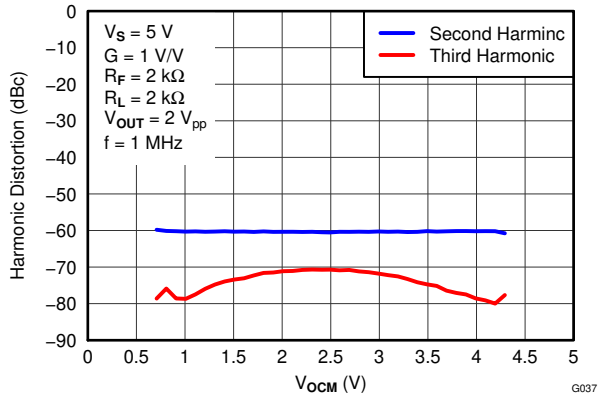

Figure 45. Harmonic Distortion vs V_{OCM} at 1 MHz

Typical Characteristics: V_S = 5 V (continued)

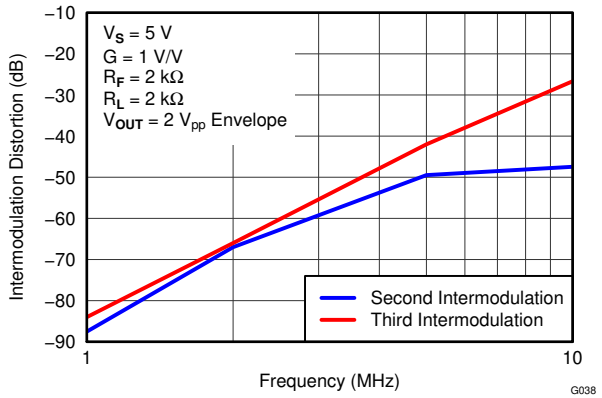

Figure 46. Two-Tone, 2nd and 3rd Order Intermodulation Distortion vs Frequency

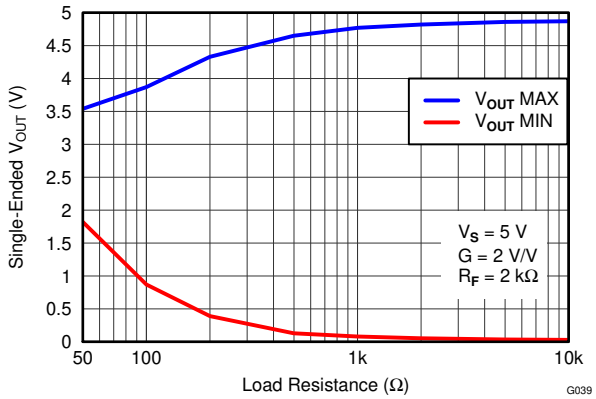

Figure 47. Single-Ended Output Voltage Swing vs Load Resistance

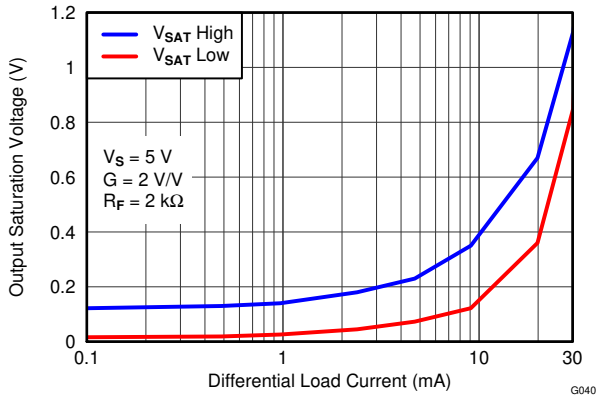

Figure 48. Single-Ended Output Saturation Voltage vs Load Current

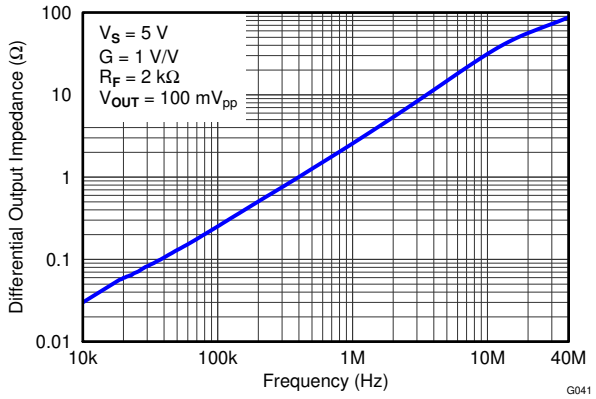

Figure 49. Main Amplifier Differential Output Impedance vs Frequency

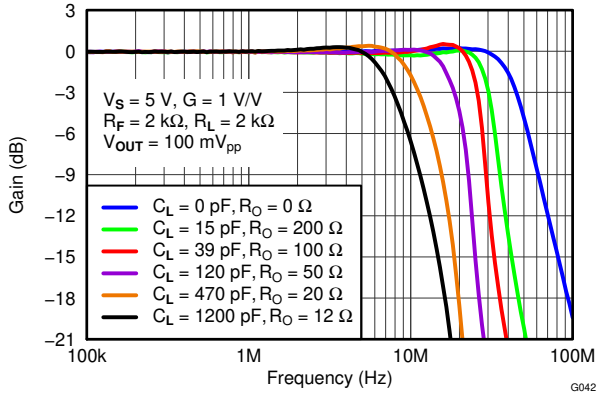

Figure 50. Frequency Response vs C_{LOAD}

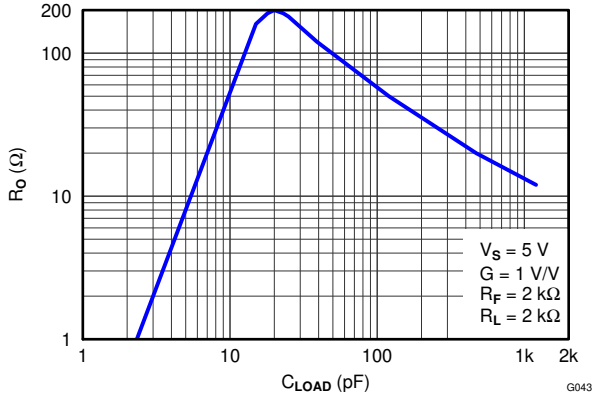

Figure 51. R_O vs C_{LOAD}

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Typical Characteristics: V_S = 5 V (continued)

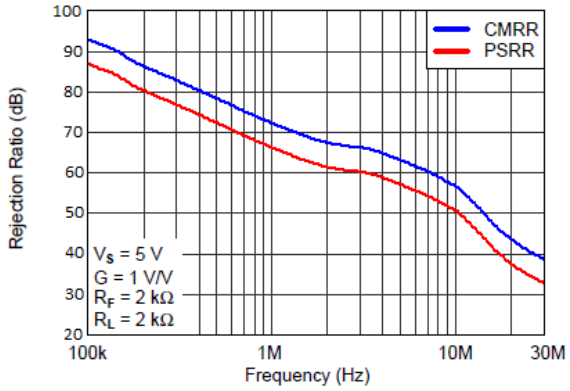

Figure 52. Rejection Ratio vs Frequency

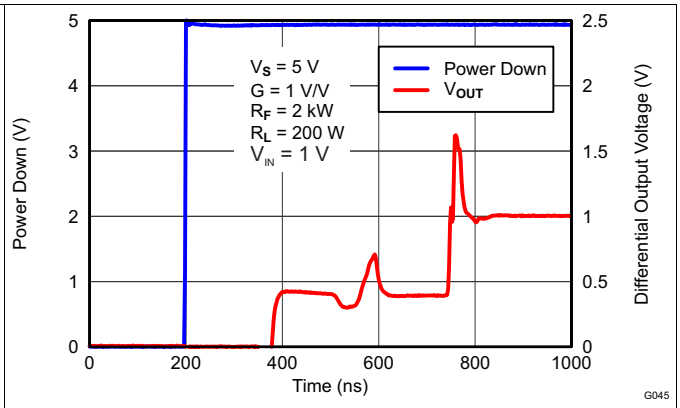

Figure 53. Turnon Time

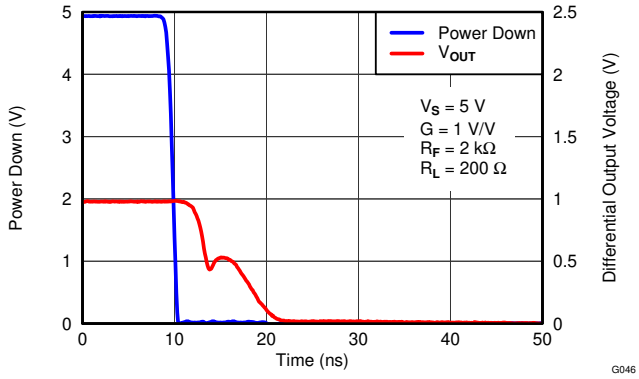

Figure 54. Turnoff Time

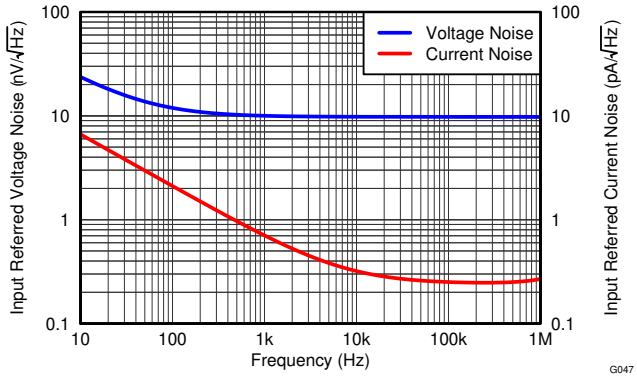

Figure 55. Input-referred Voltage Noise and Current Noise Spectral Density

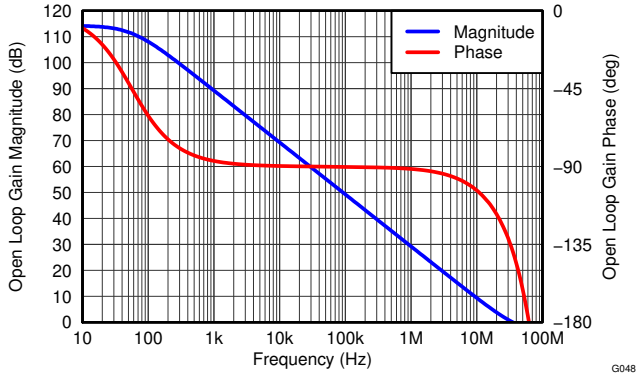

Figure 56. Main Amplifier Differential Open-Loop Gain and Phase vs Frequency

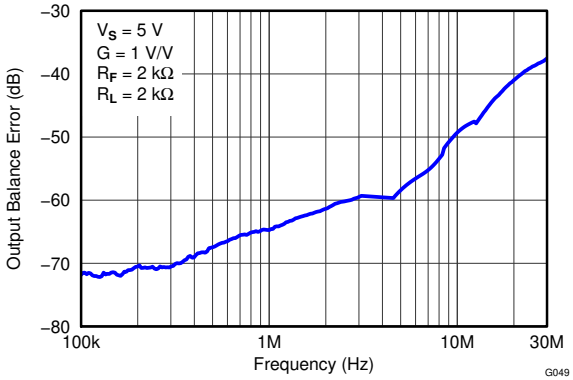

Figure 57. Output Balance Error vs Frequency

Typical Characteristics: V_S = 5 V (continued)

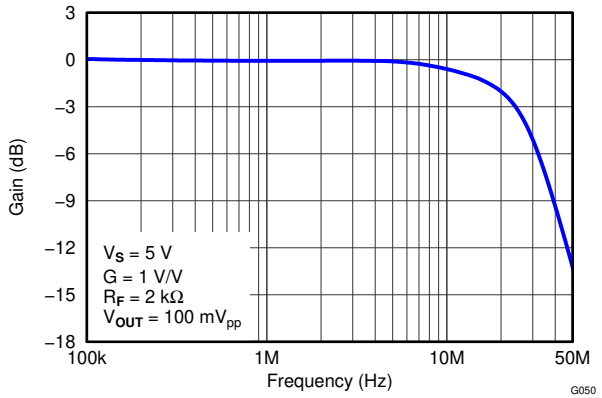

Figure 58. V_{OCM} Small-Signal Frequency Response

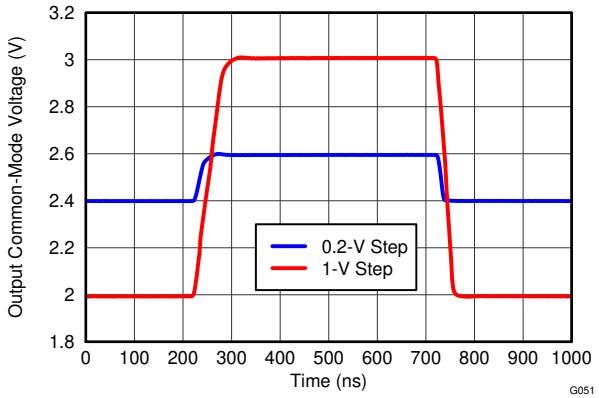

Figure 59. V_{OCM} Large- and Small Signal Pulse Response

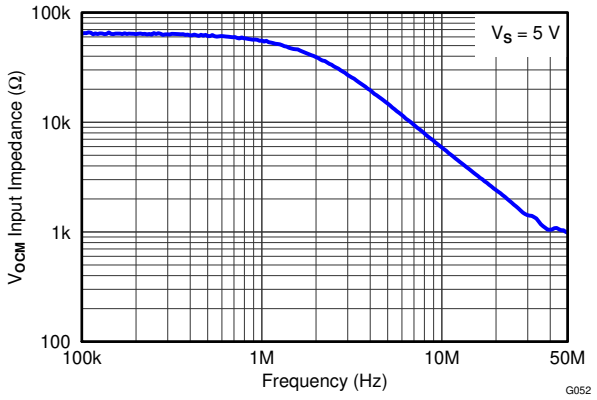

Figure 60. V_{OCM} Input Impedance vs Frequency

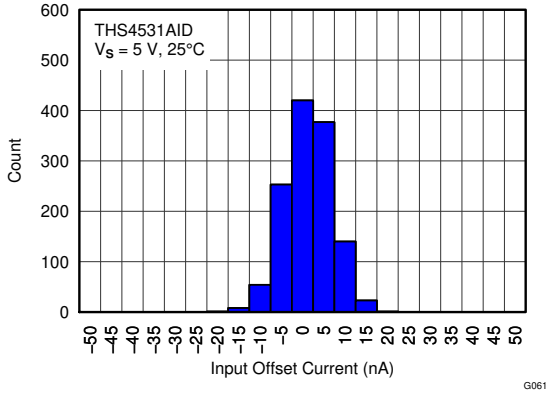

Figure 61. Input Offset Current Histogram

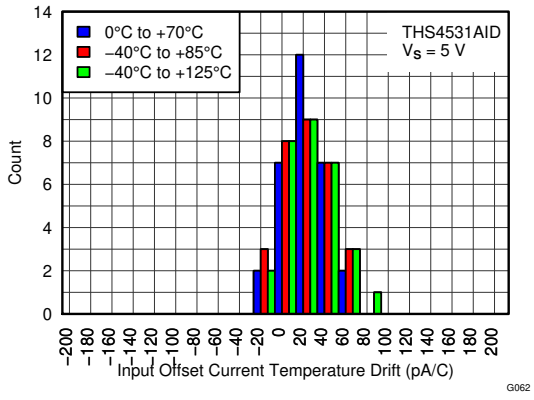

Figure 62. Input Offset Current Temp Drift Histogram

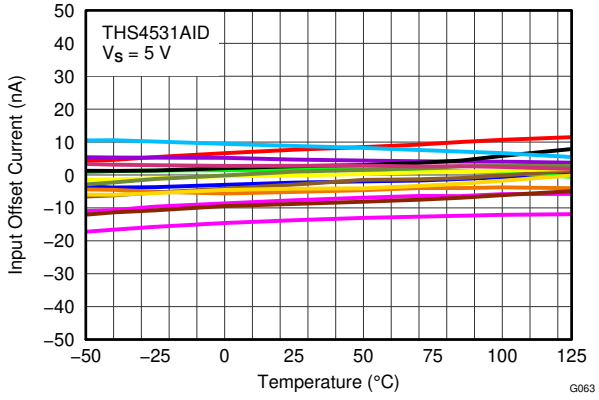

Figure 63. Input Offset Current vs Temperature

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Typical Characteristics: V_S = 5 V (continued)

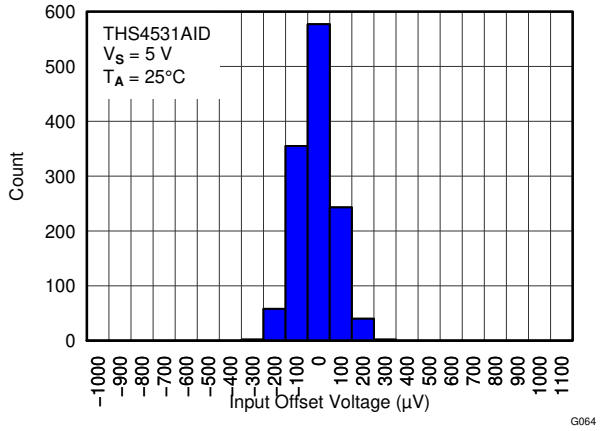


Figure 64. Input Offset Voltage Histogram

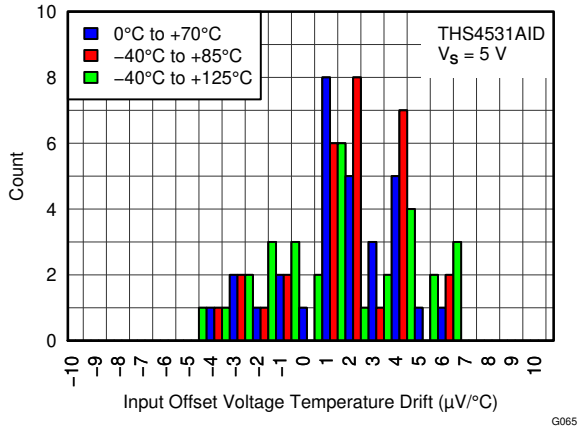


Figure 65. Input Offset Voltage Temp Drift Histogram

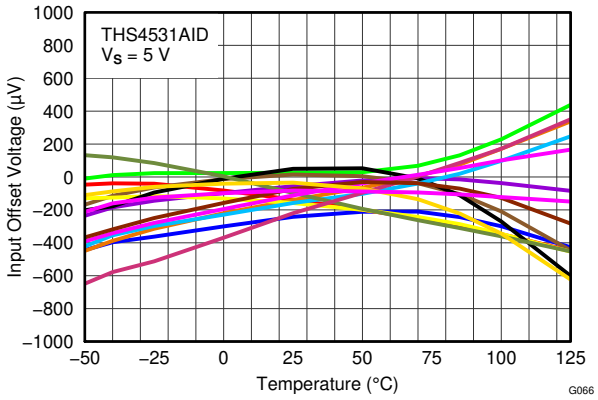


Figure 66. Input Offset Voltage vs Temperature

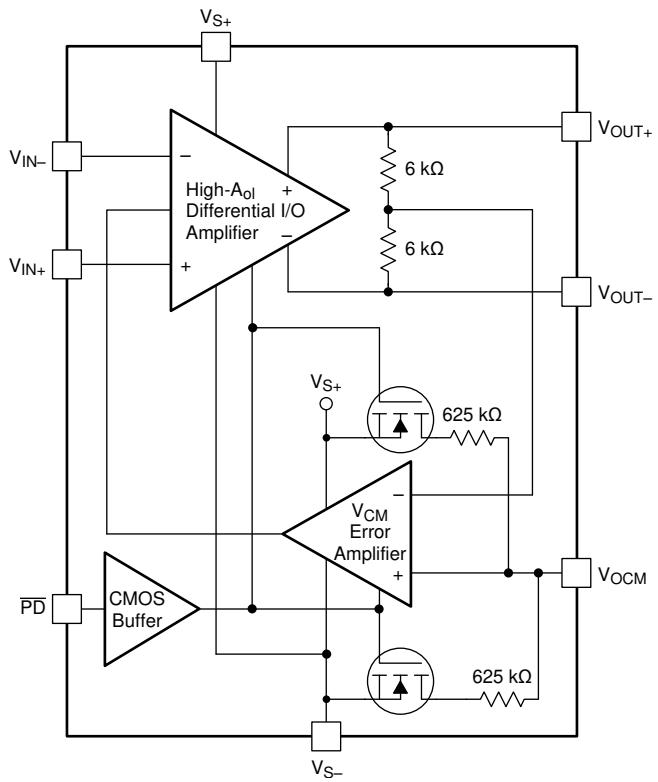
8 Detailed Description

8.1 Overview

As shown in the *Functional Block Diagram*, the THS4531A device is comprised of three functional blocks: a fully-differential amplifier with high open-loop gain of 114 dB, a servo amplifier to set the common-mode voltage of the output equal to the V_{OCM} input, and a power-down circuit to greatly reduce the power consumption when the device is idle.

The common-mode voltage servo has impressive performance specifications of ±1% maximum gain error, ±5-mV maximum voltage offset, and 24-MHz bandwidth.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Common-Mode Voltage Range

The input common-model voltage of a fully differential op amp is the voltage at the positive and negative (+ and –) input pins of the op amp.

Do not violate the input common-mode voltage range (V_{ICR}) of the op amp. Assuming the op amp is in linear operation, the voltage across the input pins is only a few millivolts at most. Therefore finding the voltage at one input pin determines the input common-mode voltage of the op amp.

Use Equation 1 to calculate the voltage with the negative input as a summing node.

$$\left(V_{OUT+} \times \frac{R_G}{R_G + R_F}\right) + \left(V_{IN-} \times \frac{R_F}{R_G + R_F}\right) \tag{1}$$

To determine the V_{ICR} of the op amp, the voltage at the negative input is evaluated at the extremes of V_{OUT+}.

As the gain of the op amp increases, the input common-mode voltage becomes closer and closer to the input common-mode voltage of the source.

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Feature Description (continued)

8.3.1.1 Setting the Output Common-Mode Voltage

The output common-model voltage is set by the voltage at the V_{OCM} pin and the internal circuit works to maintain the output common-mode voltage as close as possible to this voltage. If left unconnected, the output common-mode is set to mid-supply by internal circuitry, which may be over-driven from an external source. Figure 67 is representative of the V_{OCM} input. The internal V_{OCM} circuit has about 24-MHz of –3-dB bandwidth, which is required for best performance, but it is intended to be a DC bias input pin. Bypass capacitors are recommended on this pin to reduce noise. Use Equation 2 to calculate the external current required to overdrive the internal resistor divider.

$$I_{EXT} = \frac{2V_{OCM} - (V_{S+} + V_{S-})}{625\ k\Omega}$$

where

- V_{OCM} is the voltage applied to the V_{OCM} pin. (2)

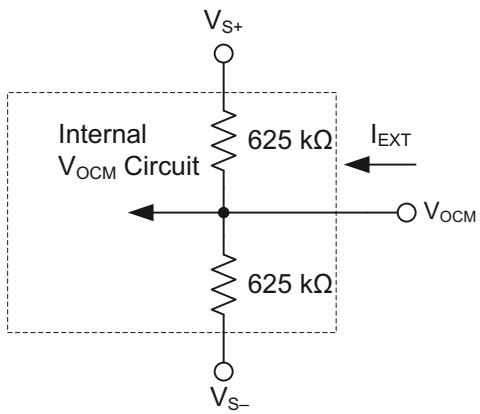

Figure 67. Simplified V_{OCM} Input Circuit

8.3.2 Power Down

The power down pin is internally connected to a CMOS stage which must be driven to a minimum of 2.1 V to ensure proper high logic.

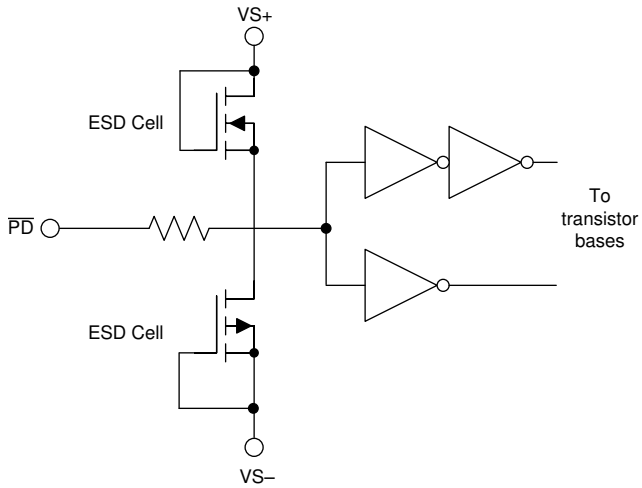

Figure 68. Simplified Power-Down Internal Circuit

If 1.8-V logic is used to drive the pin, a shoot through current of up to 100 µA may develop in the digital logic causing the overall quiescent current to exceed the 2 µA of maximum disabled quiescent current specified in the *Electrical Characteristics: V_S = 2.7 V*.

Feature Description (continued)

To properly interface to 1.8-V logic with minimal increase in additional current draw, a logic-level translator like the SN74AVC1T45 device can be used.

Alternatively, the same function can be achieved using a diode and pullup resistor as shown in Figure 69.

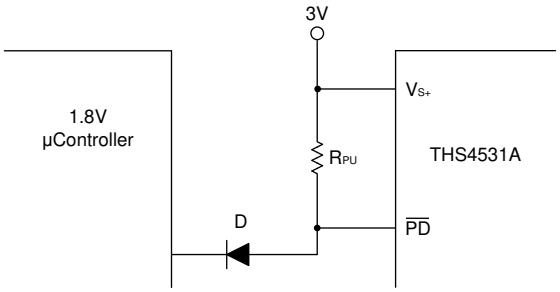

Figure 69. THS4531A Power Down Interface to 1.8-V Logic Microcontroller

The voltage at the power down pin will be a function of the supply voltage, input logic level, and diode drop. As long as the diode is forward biased, the power down voltage is calculated using Equation 3.

$$V_{PD} = V_L + V_f$$

where

- V_L is the logic level voltage.
- V_f is the forward voltage drop across the diode. (3)

This means for 1.8-V logic, the forward voltage of the diode should be greater than 0.3 V but less than 0.7 V to keep the power down logic level above 2.1 V and less than 0.7 V respectively.

For example, if 1N914 is selected as the diode with a forward voltage of approximately 0.4 V, the translated logic voltages will be 0.4 V for disabled operation and 2.2 V for enabled operation.

Use Equation 4 to calculate the additional current draw.

$$i_{PD} = \frac{V_{CC} - (V_L + V_f)}{R_{PU}} \quad (4)$$

Equation 2 shows that larger values of RPU result in a smaller additional current. A reasonable value of RPU is 500 kΩ where an additional current draw of 5.2 µA is expected while the device is in operation and 1.6 µA when disabled.

8.4 Device Functional Modes

The THS4531A has two functional modes: full-power mode and power-down mode. The power-down mode reduces the quiescent current of the device to 500 nA from a typical value of 290 µA with a 5-V supply.

With a turnon time of only 600 ns and a turnoff time of 15 ns, the power-down mode can be used to greatly reduce the average power consumption of the device without sacrificing system performance.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Figure 70 shows the general test circuit built on the EVM that was used for testing the THS4531A. For simplicity, power supply decoupling is not shown – see *Layout* for recommendations. Depending on the test conditions, component values are changed per Table 4 and Table 5, or as otherwise noted. Some of the signal generators used are AC-coupled 50-Ω sources and a 0.22-µF capacitor and 49.9-Ω resistor to ground are inserted across R_{IT} on the un-driven or alternate input as shown to balance the circuit. A split-power supply is used to ease the interface to common lab test equipment, but if properly biased, the amplifier can be operated single-supply as described in the applications section with no impact on performance. For most of the tests, the devices are tested with single ended input and a transformer on the output to convert the differential output to single ended because common lab test equipment have single ended inputs and outputs. Performance is the same or better with differential input and differential output.

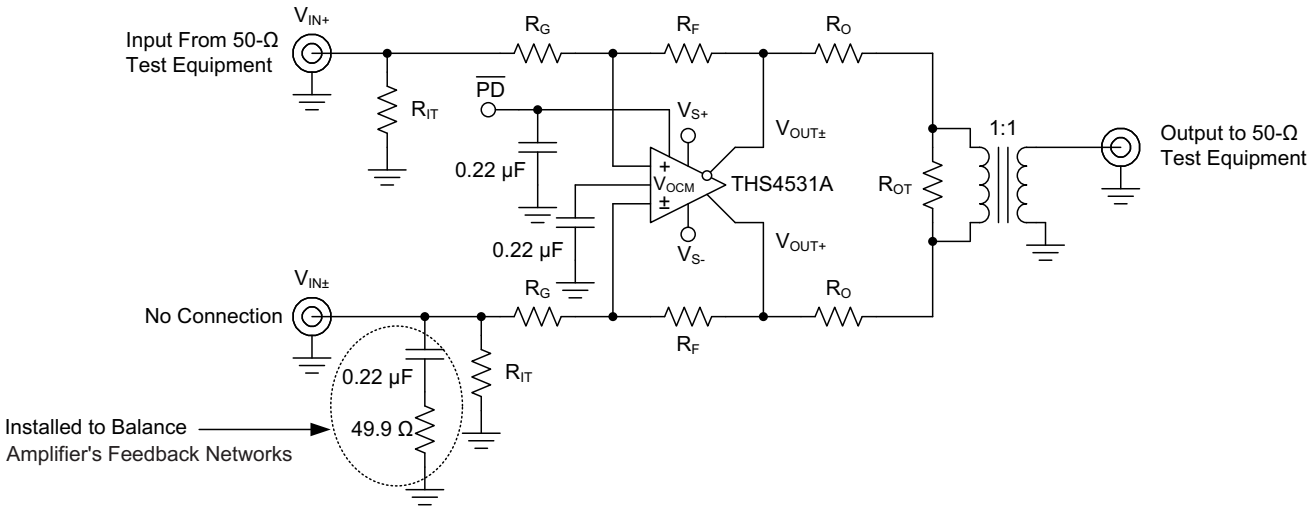

Figure 70. General Test Circuit

Table 4. Gain Component Values for Single-Ended Input(1)

GAIN	R_F	R_G	R_{IT}
1 V/V	2 kΩ	2 kΩ	51.1 Ω
2 V/V	2 kΩ	1 kΩ	52.3 Ω
5 V/V	2 kΩ	392 Ω	53.6 Ω
10 V/V	2 kΩ	187 Ω	57.6 Ω

(1) Components are chosen to achieve gain and 50-Ω input termination. Resistor values shown are closest standard values so gains are approximate.

Table 5. Load Component Values For 1:1 Differential to Single-Ended Output Transformer(1)

R_L	R_O	R_{OT}	ATTEN (dB)
100 Ω	25 Ω	open	6
200 Ω	84.5 Ω	71.5 Ω	16.7
500 Ω	237 Ω	56.2 Ω	25.6
1 kΩ	487 Ω	52.3 Ω	31.8
2 kΩ	976 Ω	51.1 Ω	38

(1) The total load includes 50-Ω termination by the test equipment. Components are chosen to achieve load and 50-Ω line termination through a 1:1 transformer. Resistor values shown are closest standard values so loads are approximate.

Because of the voltage divider on the output formed by the load component values, the output of the amplifier is attenuated. The column *ATTEN* in Table 5 shows the attenuation expected from the resistor divider. When using a transformer at the output as shown in Figure 70, the signal has slightly more loss because of transformer insertion loss, and these numbers are approximate. The standard output load used for most tests is 2 kΩ with associated 38 dB of loss.

9.1.1 Frequency Response, and Output Impedance

The circuit shown in Figure 70 is used to measure the frequency response of the amplifier.

A network analyzer is used as the signal source and the measurement device. The output impedance of the network analyzer is 50 Ω and is AC coupled. R_{IT} and R_G are selected to impedance match to 50 Ω and maintain the proper gain. To balance the amplifier, a 49.9-Ω resistor and blocking capacitor to ground is inserted across R_{IT} on the alternate input.

The output is routed to the input of the network analyzer through 50-Ω coax. For a 2k load, 38 dB is added to the measurement to refer back to the output of the amplifier according to Table 5.

For output impedance, the signal is injected at V_{OUT} with V_{IN} left open. The voltage drop across the 2x R_O resistors is measured with a high impedance differential probe and used to calculate the impedance into the output of the amplifier.

9.1.2 Distortion

At 1 MHz and above, the circuit shown in Figure 70 is used to measure harmonic, intermodulation distortion, and output impedance of the amplifier.

A signal generator is used as the signal source and the output is measured with a spectrum analyzer. The output impedance of the signal generator is 50 Ω and is AC coupled. R_{IT} and R_G are chosen to impedance match to 50 Ω and maintain the proper gain. To balance the amplifier, a 0.22-µF capacitor and 49.9-Ω resistor to ground is inserted across R_{IT} on the alternate input. A low-pass filter is inserted in series with the input to reduce harmonics generated by the signal source. The level of the fundamental is measured and then a high-pass filter is inserted at the output to reduce the fundamental so it does not generate distortion in the input of the spectrum analyzer.

Distortion in the audio band is measured using an audio analyzer. Refer to the *Audio Performance* section for details.

9.1.3 Slew Rate, Transient Response, Settling Time, Overdrive, Output Voltage, and Turnon and Turnoff Time

The circuit shown in Figure 71 is used to measure slew rate, transient response, settling time, overdrive recovery, and output voltage swing. Turnon and turnoff times are measured with 50-Ω input termination on the $\overline{PD}$ input, by replacing the 0.22-µF capacitor with 49.9-Ω resistor.

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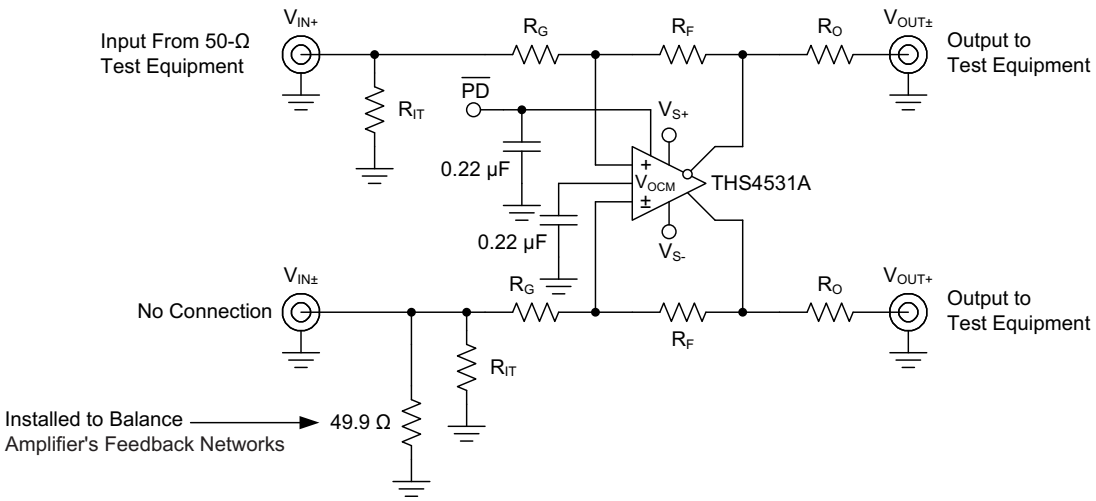

Figure 71. Slew Rate, Transient Response, Settling Time, Z_O, Overdrive Recovery, V_{OUT} Swing, and Turn-On and Turn-Off Test Circuit

9.1.4 Common-Mode and Power Supply Rejection

The circuit shown in Figure 72 is used to measure the CMRR. The signal from the network analyzer is applied common-mode to the input.

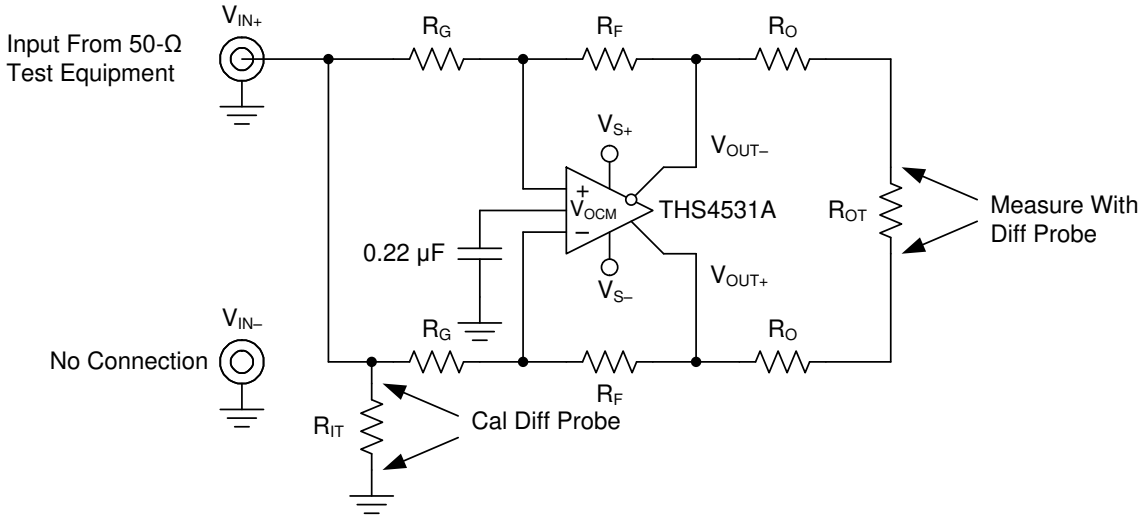

Figure 72. CMRR Test Circuit

Figure 73 is used to measure the PSRR of V_{S+} and V_{S-}. The power supply is applied to the network DC offset input of the analyzer. For both CMRR and PSRR, the output is probed using a high impedance differential probe across R_{OT}. The calculated CMRR and PSRR are referred to the input of the device.

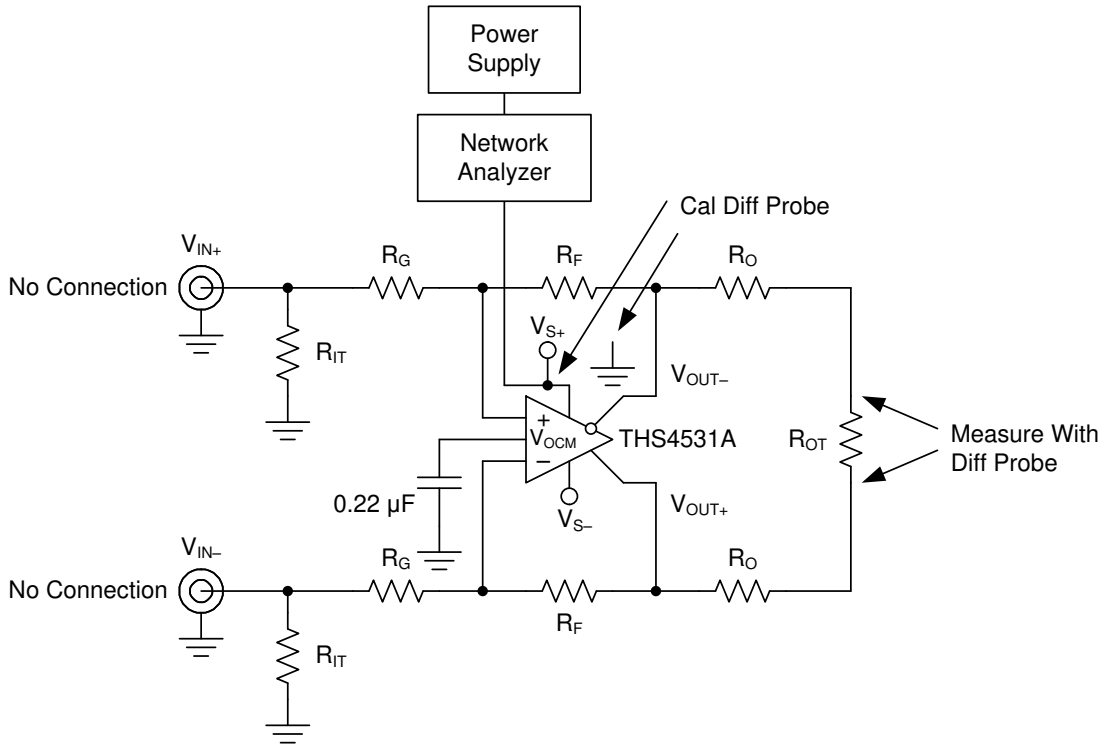

Figure 73. PSRR Test Circuit

9.1.5 V_{OCM} Input

The circuit shown in Figure 74 is used to measure the transient response, frequency response, and input impedance of the V_{OCM} input. For these tests, the cal point is across the 49.9 Ω V_{OCM} termination resistor. Transient response and frequency response are measured with R_{CM} = 0 Ω and using a high impedance differential probe at the summing junction of the two R_O resistors, with respect to ground. The input impedance is measured using a high impedance differential probe at the V_{OCM} pin and the drop across R_{CM} is used to calculate the impedance into the V_{OCM} input of the amplifier.

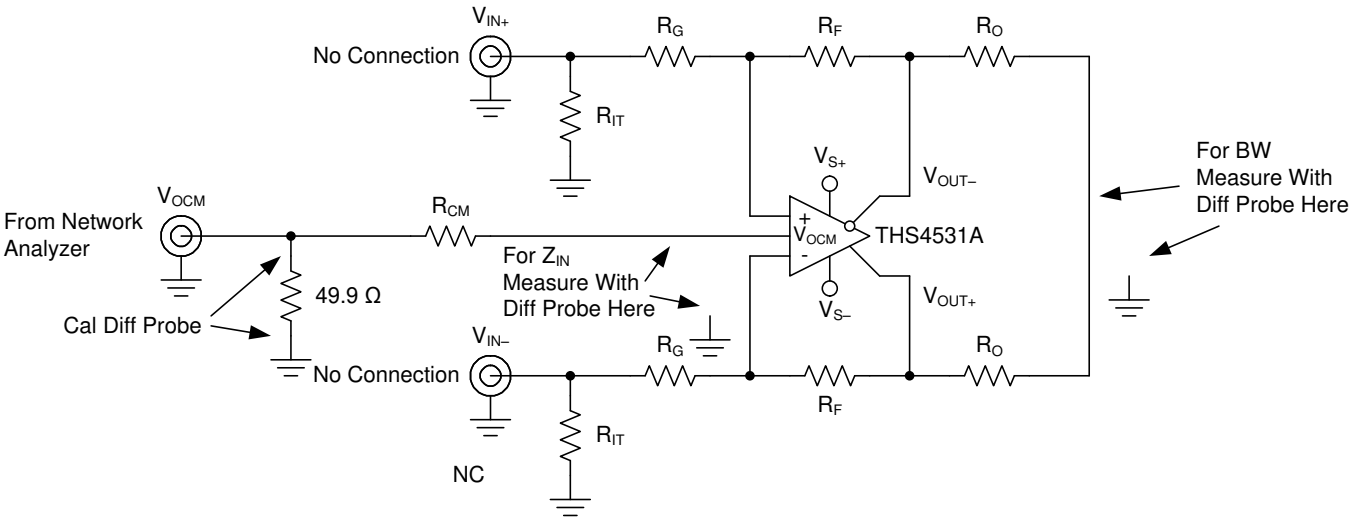

Figure 74. V_{OCM} Input Test Circuit

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9.1.6 Balance Error

The circuit shown in Figure 75 is used to measure the balance error of the main differential amplifier. A network analyzer is used as the signal source and the measurement device. The output impedance of the network analyzer is 50 Ω and is DC coupled. R_{IT} and R_G are chosen to impedance match to 50 Ω and maintain the proper gain. To balance the amplifier, a 49.9-Ω resistor to ground is inserted across R_{IT} on the alternate input. The output is measured using a high impedance differential probe at the summing junction of the two R_O resistors, with respect to ground.

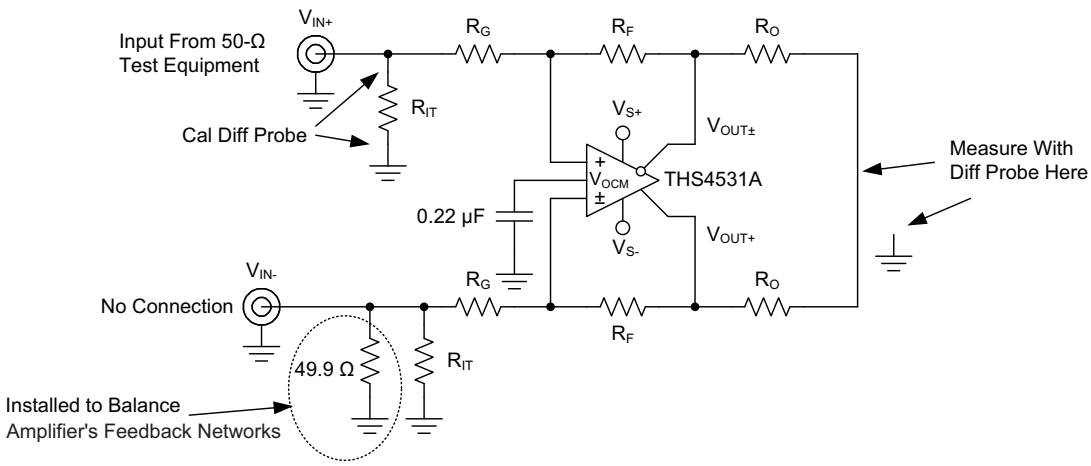

Figure 75. Balance Error Test Circuit

9.1.7 Single-Supply Operation

To facilitate testing with common lab equipment, the THS4531A EVM is built to allow for split-supply operation and most of the data presented in this data sheet was taken with split-supply power inputs. The device is designed for use with single-supply power operation and can easily be used with single-supply power without degrading the performance. The only requirement is to bias the device properly and the specifications in this data sheet are given for single supply operation.

9.1.8 Low-Power Applications and the Effects of Resistor Values on Bandwidth

The THS4531A is designed for the nominal value of R_F to be 2 kΩ. This gives excellent distortion performance, maximum bandwidth, best flatness, and best pulse response. It also loads the amplifier. For example; in gain of 1 with $R_F = R_G = 2$ kΩ, R_G to ground, and $V_{OUT+} = 4$ V, 1 mA of current will flow through the feedback path to ground. In low power applications, reducing this current is desirable by increasing the gain setting resistors values. Using larger value gain resistors has three primary side effects (other than lower power) because of the interaction with the device and PCB parasitic capacitance:

- Lowers the bandwidth.
- Lowers the phase margin.
  - This causes peaking in the frequency response.
  - This also causes overshoot and ringing in the pulse response.
- Increases the output noise.

Figure 76 shows the small signal frequency response for gain of 1 with R_F and R_G equal to 2 kΩ, 10 kΩ, and 100 kΩ. The test was done with $R_L = 2$ kΩ. Because of loading effects of R_L, lower values may reduce the peaking, but higher values will not have a significant effect.

As expected, larger value gain resistors cause lower bandwidth and peaking in the response (peaking in frequency response is synonymous with overshoot and ringing in pulse response). These effects are caused by the feedback pole created by the summing-junction capacitance and these larger Rf values.

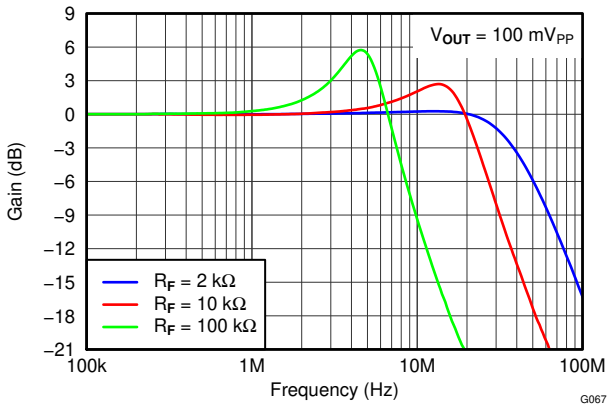

Figure 76. THS4531A Frequency Response with Various Gain Setting Resistor Values

9.1.9 Driving Capacitive Loads

The THS4531A is designed for a nominal parasitic capacitive load of 2 pF (differentially). When driving capacitive loads greater than this, TI recommends using small resisters (R_O) in series with the output as close to the device as possible. Without R_O, capacitance on the output interacts with the output impedance of the amplifier causing phase shift in the loop gain of the amplifier that reduces the phase margin resulting in:

- Peaking in the frequency response.
- Overshoot, undershoot, and ringing in the time domain response with a pulse or square-wave signal.
- May lead to instability or oscillation.

Inserting R_O compensates the phase shift and restores the phase margin, but it also limits bandwidth. The circuit shown in Figure 71 is used to test for best R_O versus capacitive loads, C_L, with a capacitance placed differential across the V_{OUT+} and V_{OUT-} along with 2-kΩ load resistor, and the output is measure with a differential probe. Figure 77 shows the suggested values of R_O versus capacitive loads, C_L, and Figure 78 shows the frequency response with various values. Performance is the same on both 2.7-V and 5-V supply.

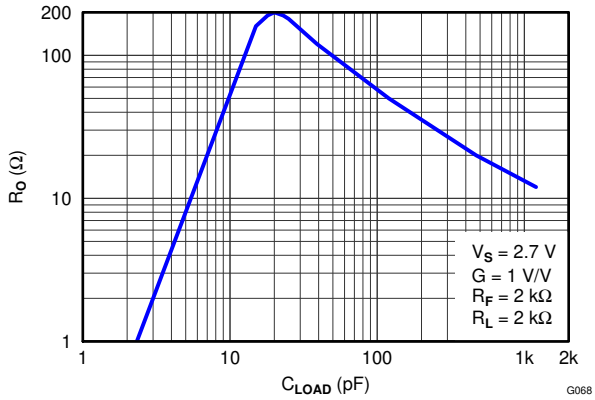

Figure 77. Recommended Series Output Resistor vs Capacitive Load for Flat Frequency Response

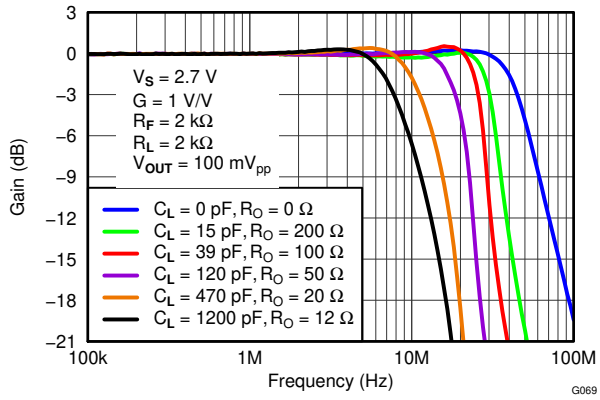

Figure 78. Frequency Response for Various R_O and C_L Values

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9.1.10 Audio Performance

The THS4531A provides excellent audio performance with very low quiescent power. To show performance in the audio band, the device was tested with an audio analyzer. THD+N and FFT tests were run at 1-Vrms output voltage. Performance is the same on both 2.7-V and 5-V supply. Figure 79 is the test circuit used, and Figure 80 and Figure 81 show performance of the analyzer. In the FFT plot the harmonic spurs are at the testing limit of the analyzer, which means the THS4531A is actually much better than can be directly measured. Because the THS4531A distortion performance cannot be directly measured in the audio band it is estimated from measurement in high noise gain configuration correlated with simulation.

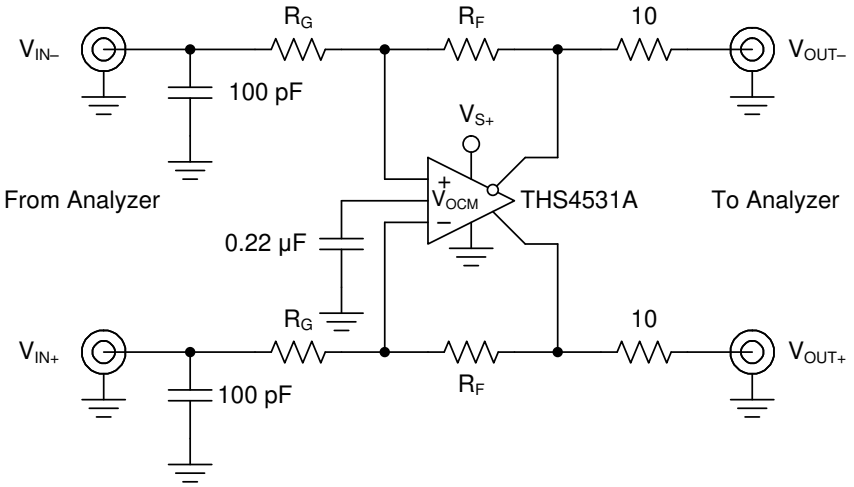

Figure 79. THS4531A Audio Analyzer Test Circuit

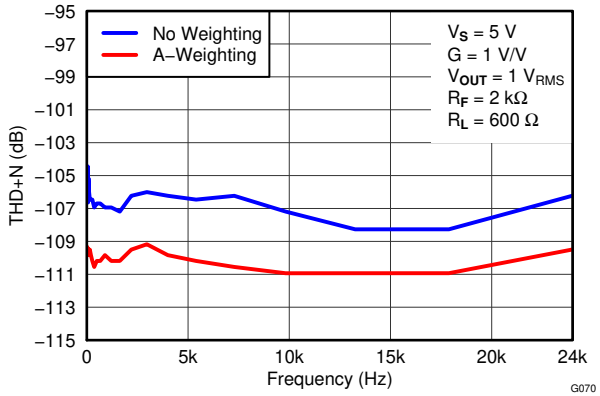

Figure 80. THD+N on Audio Analyzer, 10 Hz to 24 kHz

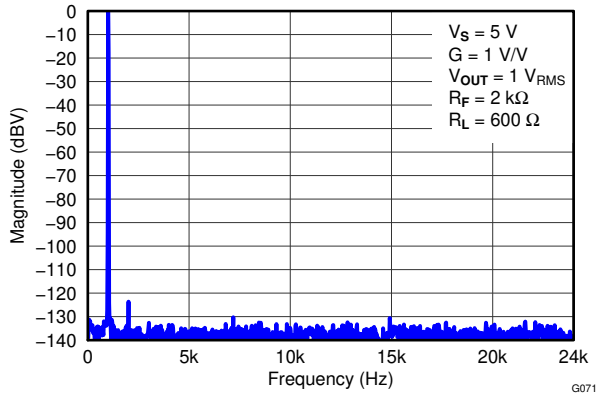

Figure 81. 1-kHz FFT Plot on Audio Analyzer

9.1.11 Audio On and Off Pop Performance

The THS4531A is tested to show on and off pop performance by connecting a speaker between the differential outputs and switching on and off the power supply, and also by using the power down function of the THS4531A. Testing was done with and without tones. During these tests no audible pop could be heard.

With no input tone, Figure 82 shows the voltage waveforms when switching power on to the THS4531A and Figure 83 shows voltage waveforms when turning power off. The transients during power on and off show no audible pop should be heard.

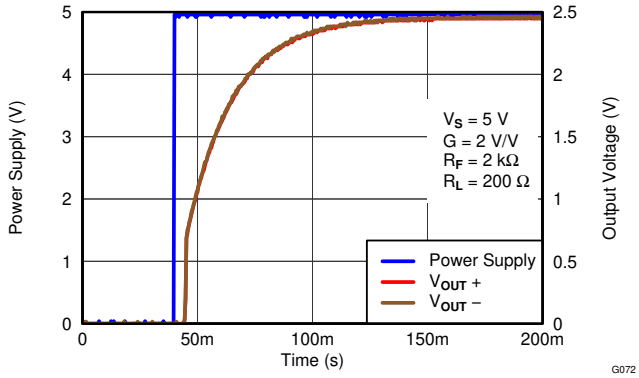

Figure 82. Power Supply Turnon Pop Performance

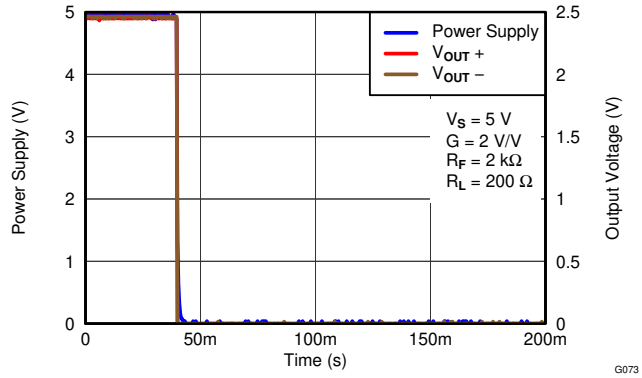

Figure 83. Power Supply Turnoff Pop Performance

With no input tone, Figure 84 shows the voltage waveforms using the $\overline{PD}$ pin to enable and disable the THS4531A. The transients during power on and off show no audible pop should be heard.

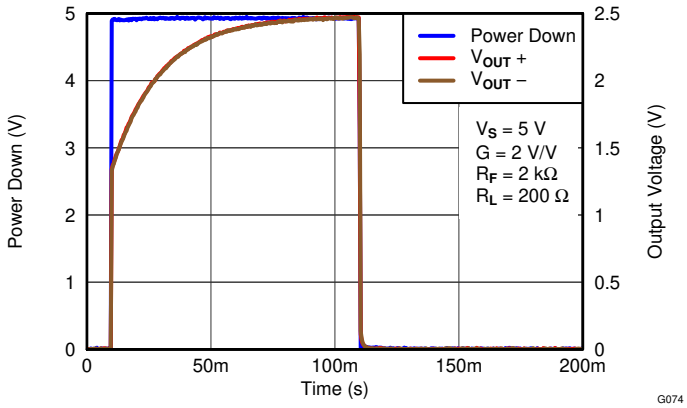

Figure 84. $\overline{PD}$ Enable Pop Performance

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9.2 Typical Applications

The following circuits show application information for the THS4531A. For simplicity, power-supply decoupling capacitors are not shown in these diagrams; see the *Layout Guidelines* section for suggested guidelines. For more details on the use and operation of fully differential amplifiers, refer to the Application Report *Fully-Differential Amplifiers* (SLOA054), available for download from the TI website at www.ti.com.

9.2.1 SAR ADC Performance: THS4531A and ADS8321 Combined Performance

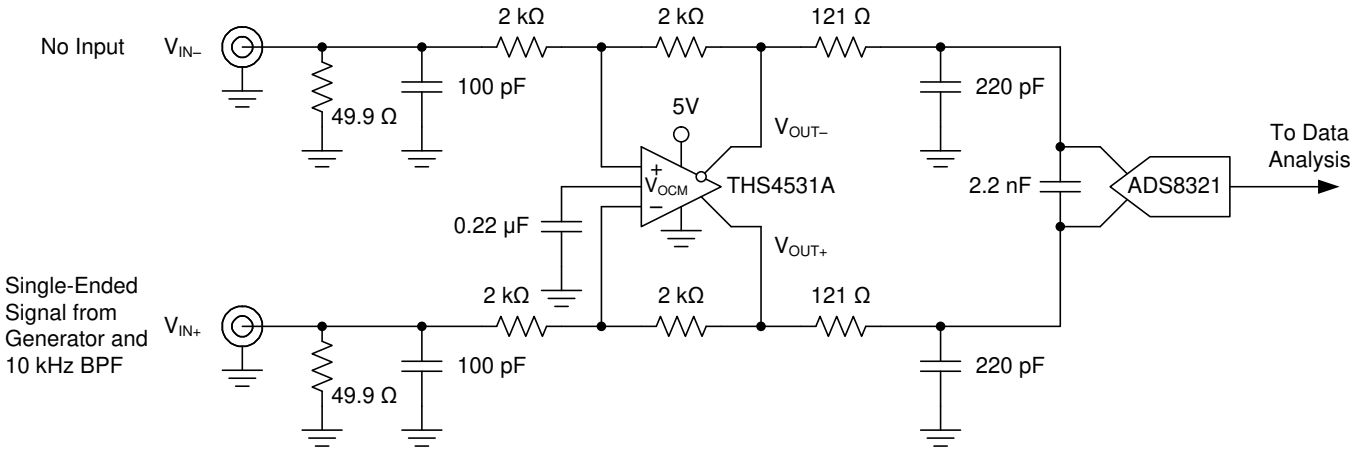

Figure 85. THS4531A and ADS8321 Test Circuit

9.2.1.1 Design Requirements

To show achievable performance with a high performance SAR ADC, the THS4531A is tested as the drive amplifier for the ADS8321. The ADS8321 is a 16-bit, SAR ADC that offers excellent AC and DC performance, with ultra-low power and small size. The circuit shown in Figure 85 is used to test the performance. Data was taken using the ADS8321 at 100 kSPS with input frequency of 10 kHz and signal levels 0.5 dB below full scale. The FFT plot of the spectral performance is in Figure 86. A summary of the FFT analysis results are in Table 6 along with ADS8321 typical data sheet performance at f_S = 100 kSPS. Refer to its data sheet for more information.

9.2.1.2 Detailed Design Procedure

The standard ADS8321 EVM and THS4531A EVM are modified to implement the schematic in Figure 85 and used to test the performance of the THS4531A as a drive amplifier. With single supply +5-V supply the output common-mode of the THS4531A defaults to +2.5 V as required at the input of the ADS8321 so the V_{OCM} input of the THS4531A simply bypassed to GND with 0.22-µF capacitor. The summary of results of the FFT analysis versus typical data sheet performance shown in Table 6 show that the THS4531A will make an excellent drive amplifier for this ADC.

Typical Applications (continued)

9.2.1.3 Application Curve

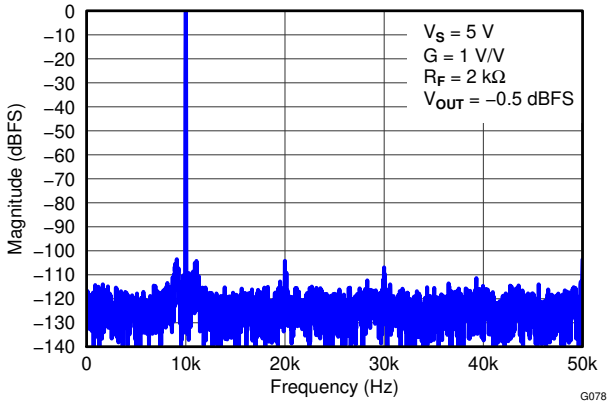

Figure 86. THS4531A + ADS8321 1-kHz FFT

Table 6. 10-kHz FFT Analysis Summary

CONFIGURATION	TONE	SIGNAL	SNR	THD	SINAD	SFDR
THS4531A + ADS8321	10 kHz	–0.5 dBFS	87 dBc	–96 dBc	87 dBc	100 dBc
ADS8321 Data Sheet (typical)	10 kHz	–0.5 dBFS	87 dBc	–86 dBc	84 dBc	86 dBc

9.2.2 Audio ADC Driver Performance: THS4531A and PCM4204 Combined Performance

To show achievable performance with a high performance audio ADC, the THS4531A is tested as the drive amplifier for the PCM4204. The PCM4204 is a high-performance, four-channel analog-to-digital converter (ADC) designed for professional and broadcast audio applications. The PCM4204 architecture uses a 1-bit delta-sigma modulator per channel incorporating an advanced dither scheme for improved dynamic performance, and supports PCM output data. The PCM4204 provides flexible serial port interface and many other advanced features. Refer to the PCM4204 data sheet for more information. Figure 87 shows the circuit.

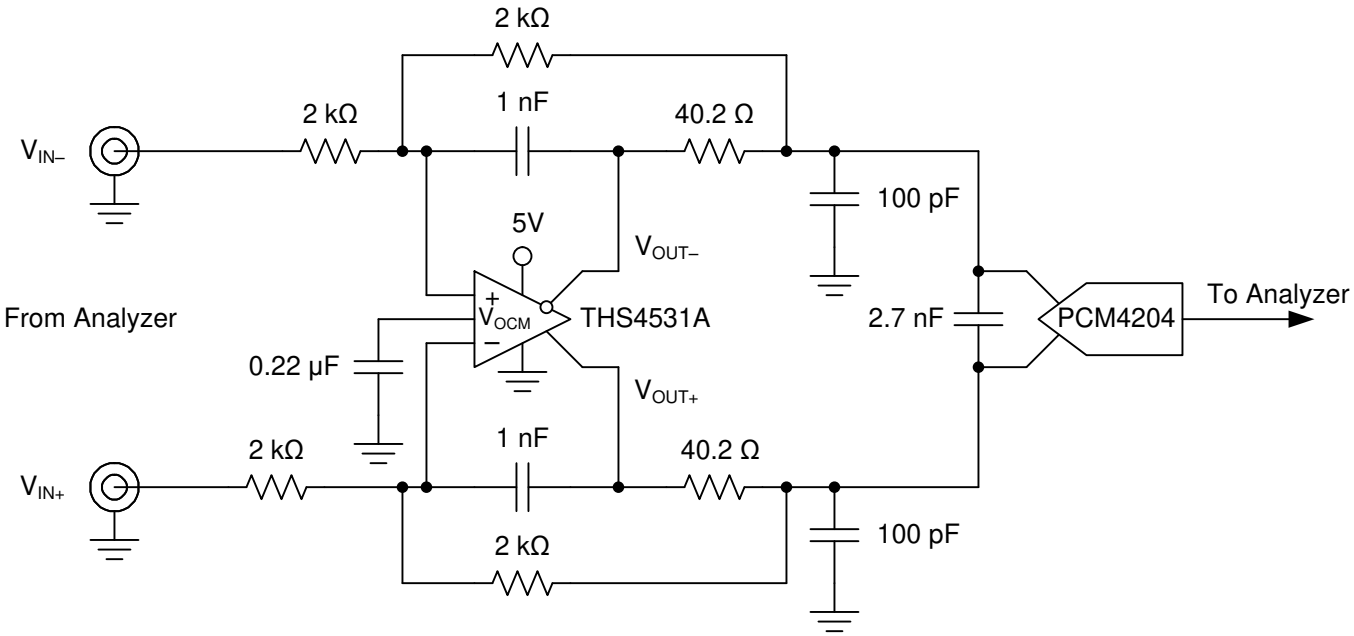

Figure 87. THS4531A and PCM4204 Test Circuit

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9.2.2.1 Detailed Design Procedure

The PCM4204 EVM is used to test the audio performance of the THS4531A as a drive amplifier. The standard PCM4204 EVM is provided with 4x OPA1632 fully differential amplifiers, which use the same pin out as the THS4531A. For testing, one of these amplifiers is replaced with a THS4531A device in same package (MSOP), gain changed to 1 V/V, and power supply changed to single supply 5 V. With single supply +5-V supply the output common-mode of the THS4531A defaults to 2.5 V as required at the input of the PCM4204. So the resistor connecting the V_{OCM} input of the THS4531A to the input common-mode drive from the PCM4204 is optional and no performance change was noted with it connected or removed. The EVM power connections were modified by connecting positive supply inputs, 15 V, 5 VA, and 5 VD, to a 5-V external power supply (EXT 3.3 was not used) and connecting –15 V and all ground inputs to ground on the external power supply so only one external 5-V supply was needed to power all devices on the EVM.

An audio analyzer is used to provide an analog audio input to the EVM and the PCM formatted digital output is read by the digital input on the analyzer. Data was taken at f_S = 96 kHz, and audio output uses PCM format. Other data rates and formats are expected to show similar performance in line with that shown in the data sheet.

9.2.2.2 Application Curves

Figure 88 shows the THD+N vs Frequency with no weighting and Figure 89 shows an FFT with 1-kHz input tone. Input signal to the PCM4204 for these tests is –0.5 dBFS. Table 7 summarizes results of testing using the THS4531A + PCM4204 versus typical Data Sheet performance, and show it make an excellent drive amplifier for this ADC.

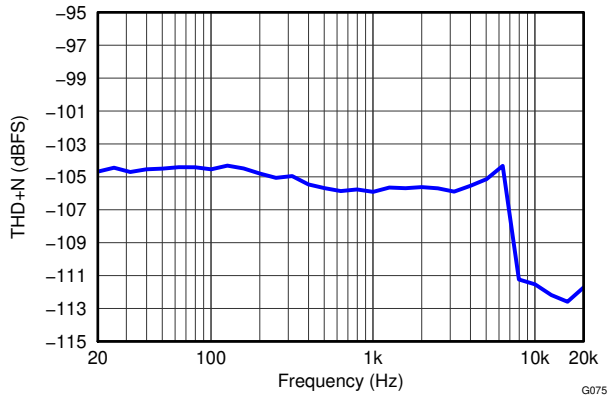

Figure 88. THS4531A + PCM4204 THD+N vs Frequency With No Weighting

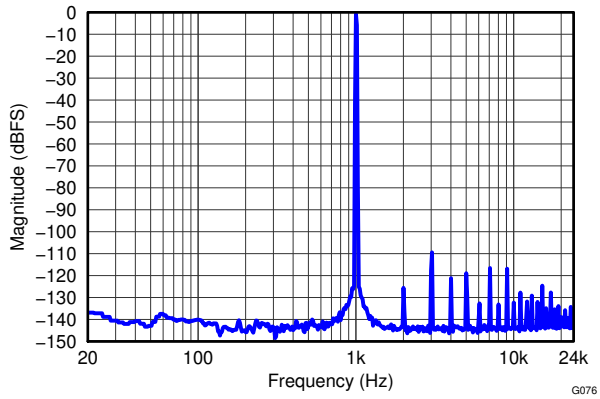

Figure 89. THS4531A + PCM4204 1-kHz FFT

Table 7. 1-kHz AC Analysis: Test Circuit versus PCM4204 Data Sheet Typical Specifications (f_S = 96 kSPS)

CONFIGURATION	TONE	THD + N
THS4531A + PCM4204	1 kHz	–106 dB
PCM4204 Data Sheet (typical)	1 kHz	–103 dB

9.2.3 SAR ADC Performance: THS4531A and ADS7945 Combined Performance

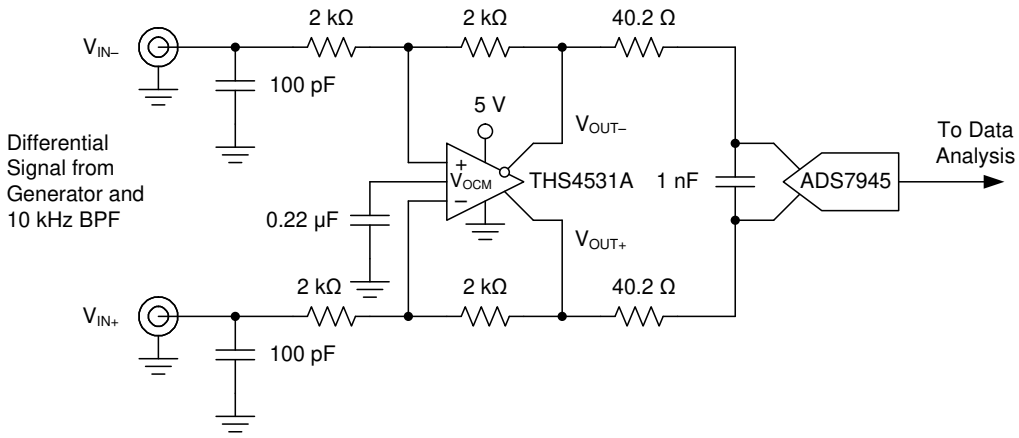

Figure 90. THS4531A and ADS7945 Test Circuit

9.2.3.1 Design Requirements

To show achievable performance with a high performance SAR ADC, the THS4531A is tested as the drive amplifier for the ADS7945. The ADS7945 is a 14-bit, SAR ADC that offers excellent AC and DC performance, with low power and small size. The circuit shown in Figure 90 is used to test the performance. Data was taken using the ADS7945 at 2MSPS with input frequency of 10 kHz and signal level 0.5 dB below full scale. The FFT plot of the spectral performance is in Figure 91. A summary of the FFT analysis results are in Table 8 along with ADS7945 typical data sheet performance at f_S = 2 MSPS. Refer to the data sheet for more information.

9.2.3.2 Detailed Design Procedure

The standard ADS7945 EVM and THS4531A EVM are modified to implement the schematic in Figure 90 and used to test the performance of the THS4531A as a drive amplifier. With single supply 5 V supply the output common-mode of the THS4531A defaults to +2.5 V as required at the input of the ADS7945 so the V_{OCM} input of the THS4531A simply bypassed to GND with 0.22-µF capacitor. The summary of results of the FFT analysis versus typical data sheet performance shown in Table 8 show that the THS4531A will make an excellent drive amplifier for this ADC.

9.2.3.3 Application Curve

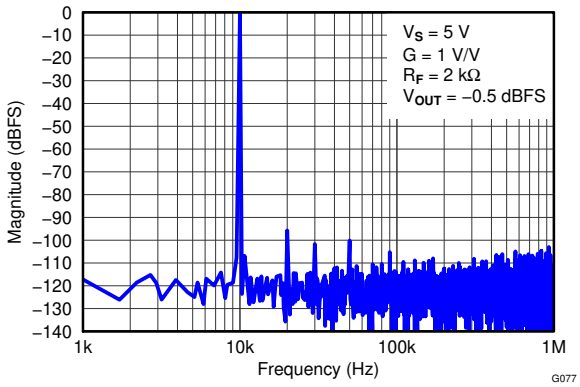

Figure 91. THS4531A and ADS7945 Test Circuit

Table 8. 10-kHz FFT Analysis Summary

CONFIGURATION	TONE	SIGNAL	SNR	THD	SFDR
THS4531A + ADS7945	10 kHz	–0.5 dBFS	83 dBc	–93 dBc	96 dBc
ADS7945 Data Sheet (typ)	10 kHz	–0.5 dBFS	84 dBc	–92 dBc	94 dBc

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9.2.4 Differential-Input to Differential-Output Amplifier

The THS4531A is a fully differential op amp and can be used to amplify differential input signals to differential output signals. A basic block diagram of the circuit is shown in Figure 92 (V_{OCM} and $\overline{PD}$ inputs not shown). The gain of the circuit is set by R_F divided by R_G.

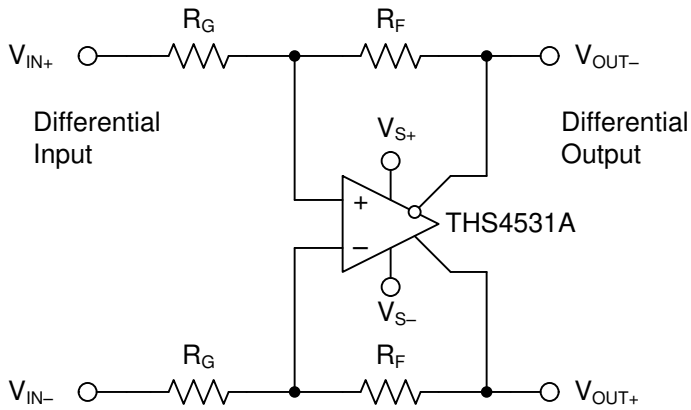

Figure 92. Differential Input to Differential Output Amplifier

9.2.4.1 AC-Coupled, Differential-Input to Differential-Output Design Issues

There are two typical ways to use the THS4531A family with an AC-coupled differential source. In the first method, the source is differential and can be coupled in through two blocking capacitors. The second method uses either a single-ended or a differential source and couples in through a transformer (or balun). Figure 93 shows a typical blocking capacitor approach to a differential input. An optional differential-input termination resistor (R_M) is included in this design. This R_M element allows the input R_G resistors to be scaled up while still delivering lower differential input impedance to the source. In this example, the R_G elements sum to show a 500-Ω differential impedance, while the R_M element combines in parallel to give a net 100-Ω, AC-coupled, differential impedance to the source. Again, the design proceeds ideally by selecting the R_F element values, then the R_G to set the differential gain, then an R_M element (if needed) to achieve the target input impedance. Alternatively, the R_M element can be eliminated, the R_G elements set to the desired input impedance, and R_F set to the get the differential gain (R_F / R_G).

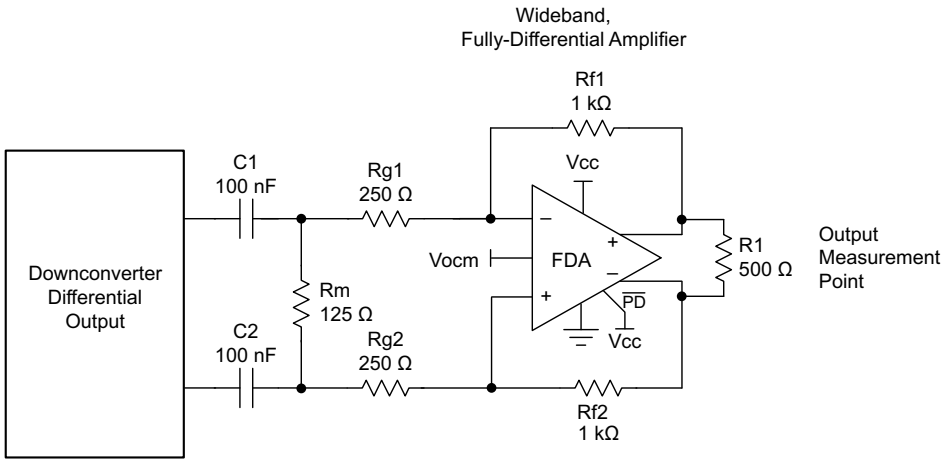

Figure 93. Example Down-Converting Mixer Delivering an AC-Coupled Differential Signal to the THS4531A

The DC biasing here is very simple. The output V_{OCM} is set by the input control voltage; and because there is no DC-current path for the output common-mode voltage, that DC bias also sets the input pins common-mode operating points.

9.2.5 Single-Ended to Differential FDA Configuration

9.2.5.1 Input Impedance

The designs so far have included a source impedance, R_S, that must be matched by R_T and R_{G1}. The total impedance at the junction of R_T and R_{G1} for the circuit of Figure 97 is the parallel combination of R_T to ground, and the ZA (active impedance) presented by R_{G1}. The expression for ZA, assuming R_{G2} is set to obtain the differential divider balance, is given by Equation 5:

$$ZA = \frac{\left(2R_{G1} + R_F\left(1 + \frac{R_{G1}}{R_{G2}}\right)\right)}{2 + \frac{R_F}{R_{G2}}} \tag{5}$$

For designs that do not need impedance matching, for instance where the input is driven from the low-impedance output of another amplifier, $R_{G1} = R_{G2}$ is the single-to-differential design used without an R_T to ground. Setting $R_{G1} = R_{G2} = R_G$ in Equation 5 produces Equation 6, which is the input impedance of a simple-input FDA driven from a low-impedance, single-ended source.

$$ZA = 2R_G \frac{\left(1 + \frac{R_F}{R_G}\right)}{2 + \frac{R_F}{R_G}} \tag{6}$$

In this case, setting a target gain as $R_F / R_G \equiv \alpha$, and then setting the desired input impedance allows the R_G element to be resolved first. Then the R_F is set to get the target gain. For example, targeting an input impedance of 200 Ω with a gain of 4 V/V, Equation 7 calculates the R_G value. Multiplying this required R_G value by a gain of 4 gives the R_F value and the design of Figure 94.

$$R_G = ZA \frac{2 + \alpha}{2(1 + \alpha)} \tag{7}$$

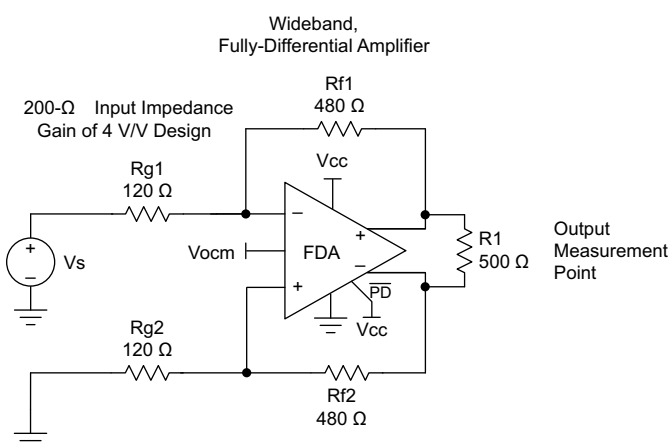

Figure 94. 200-Ω Input Impedance, Single-Ended to Differential DC-Coupled Design With Gain of 4 V/V

After being designed, this circuit can also be AC-coupled by adding blocking caps in series with the two 120-Ω R_G resistors. This active input impedance has the advantage of increasing the apparent load to the prior stage using lower resistors values, leading to lower output noise for a given gain target.

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9.2.6 Single-Ended Input to Differential Output Amplifier

The THS4531A can also be used to amplify and convert single-ended input signals to differential output signals. A basic block diagram of the circuit is shown in Figure 95 (V_{OCM} and $\overline{PD}$ inputs not shown). The gain of the circuit is again set by R_F divided by R_G.

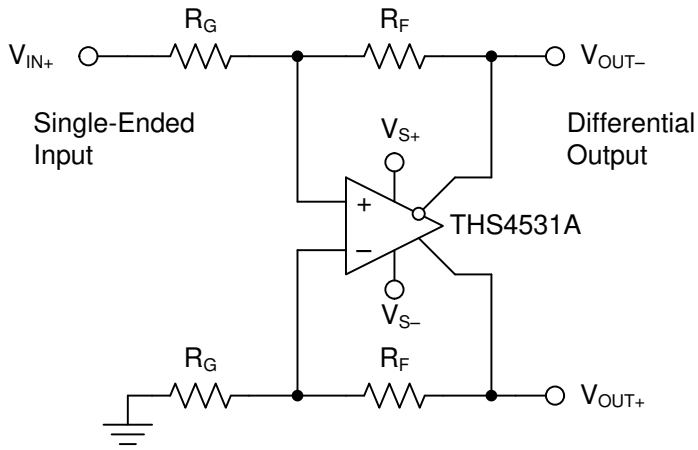

Figure 95. Single-Ended Input to Differential Output Amplifier

9.2.6.1 AC-Coupled Signal Path Considerations for Single-Ended Input to Differential Output Conversion

When the signal path can be AC-coupled, the DC biasing for the THS4531A family becomes a relatively simple task. In all designs, start by defining the output common-mode voltage. The AC-coupling issue can be separated for the input and output sides of an FDA design. The input can be AC-coupled and the output DC-coupled, or the output can be ac-coupled and the input dc-coupled, or they can both be AC-coupled.

One situation where the output might be DC-coupled (for an AC-coupled input), is when driving directly into an ADC where the V_{OCM} control voltage uses the ADC common-mode reference to directly bias the FDA output common-mode to the required ADC input common-mode. In any case, the design starts by setting the desired V_{OCM}.

When an AC-coupled path follows the output pins, the best linearity is achieved by operating V_{OCM} at midsupply. The V_{OCM} voltage must be within the linear range for the common-mode loop, as specified in the headroom specifications (approximately 0.91 V greater than the negative supply and 1.1 V less than the positive supply). If the output path is also ac-coupled, simply letting the V_{OCM} control pin float is usually preferred to get a midsupply default V_{OCM} bias with minimal elements. To limit noise, place a 0.1-µF decoupling capacitor on the V_{OCM} pin to ground.

After V_{OCM} is defined, check the target output voltage swing to ensure that the V_{OCM} plus the positive and negative output swing on each side do not clip into the supplies. If the desired output differential swing is defined as V_{OPP}, divide by 4 to obtain the $\pm V_P$ swing around V_{OCM} at each of the two output pins (each pin operates 180° out of phase with the other). Check that V_{OCM} $\pm V_P$ does not exceed the absolute supply rails for this rail-to-rail output (RRO) device.

Going to the device input pins side, because both the source and balancing resistor on the nonsignal input side are DC-blocked (see Figure 96), no common-mode current flows from the output common-mode voltage, thus setting the input common-mode equal to the output common-mode voltage.

This input headroom also sets a limit for higher V_{OCM} voltages. Because the input V_{ICM} is the output V_{OCM} for ac-coupled sources, the 1.2-V minimum headroom for the input pins to the positive supply overrides the 1.1-V headroom limit for the output V_{OCM}. Also, the input signal moves this input V_{ICM} around the dc bias point, as described in the section *Resistor Design Equations for the Single-Ended to Differential Configuration of the FDA*.

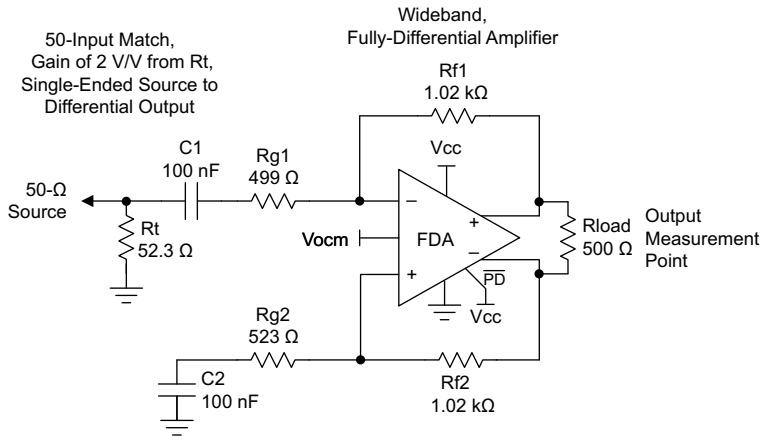

Figure 96. AC-Coupled, Single-Ended Source to a Differential Gain of 2 V/V Test Circuit

9.2.6.2 DC-Coupled Input Signal Path Considerations for Single-Ended to Differential Conversion

The output considerations remain the same as for the AC-coupled design. Again, the input can be DC-coupled while the output is AC-coupled. A DC-coupled input with an AC-coupled output might have some advantages to move the input V_{ICM} down if the source is ground referenced. When the source is DC-coupled into the THS4531A family (see Figure 97), both sides of the input circuit must be DC-coupled to retain differential balance. Normally, the nonsignal input side has an R_G element biased to whatever the source midrange is expected to be. Providing this midscale reference gives a balanced differential swing around V_{OCM} at the outputs.

Often, R_{G2} is simply grounded for DC-coupled, bipolar-input applications. This configuration gives a balanced differential output if the source is swinging around ground. If the source swings from ground to some positive voltage, grounding R_{G2} gives a unipolar output differential swing from both outputs at V_{OCM} (when the input is at ground) to one polarity of swing. Biasing R_{G2} to an expected midpoint for the input signal creates a differential output swing around V_{OCM}.

One significant consideration for a DC-coupled input is that V_{OCM} sets up a common-mode bias current from the output back through R_F and R_G to the source on both sides of the feedback. Without input balancing networks, the source must sink or source this DC current. After the input signal range and biasing on the other R_G element is set, check that the voltage divider from V_{OCM} to V_{IN} through R_F and R_G (and possibly R_S) establishes an input V_{ICM} at the device input pins that is in range.

If the average source is at ground, the negative rail input stage for the THS4531A family is in range for applications using a single positive supply and a positive output V_{OCM} setting because this DC current lifts the average FDA input summing junctions up off of ground to a positive voltage (the average of the V+ and V– input pin voltages on the FDA).

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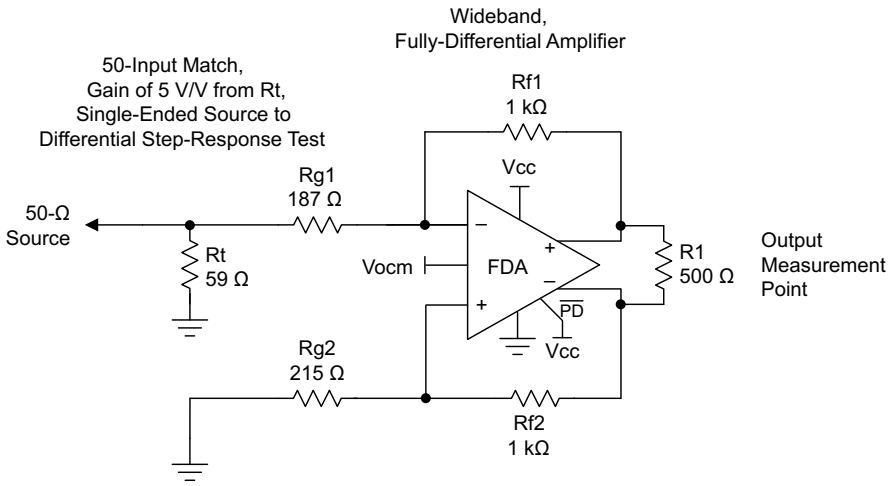

Figure 97. DC-Coupled, Single-Ended-to-Differential, Set for a Gain of 5 V/V

9.2.6.3 Resistor Design Equations for the Single-Ended to Differential Configuration of the FDA

The design equations for setting the resistors around an FDA to convert from a single-ended input signal to differential output can be approached from several directions. Here, several critical assumptions are made to simplify the results:

- The feedback resistors are selected first and set equal on the two sides.
- The DC and AC impedances from the summing junctions back to the signal source and ground (or a bias voltage on the nonsignal input side) are set equal to retain feedback divider balance on each side of the FDA.

Both of these assumptions are typical for delivering the best dynamic range through the FDA signal path.

After the feedback resistor values are chosen, the aim is to solve for the R_T (a termination resistor to ground on the signal input side), R_{G1} (the input gain resistor for the signal path), and R_{G2} (the matching gain resistor on the nonsignal input side); see Figure 96 and Figure 97. The same resistor solutions can be applied to either AC- or DC-coupled paths. Adding blocking capacitors in the input-signal chain is a simple option. Adding these blocking capacitors after the R_T element (as shown in Figure 96) has the advantage of removing any DC currents in the feedback path from the output V_{OCM} to ground.

Earlier approaches to the solutions for R_T and R_{G1} (when the input must be matched to a source impedance, R_S) follow an iterative approach. This complexity arises from the active input impedance at the R_{G1} input. When the FDA is used to convert a single-ended signal to differential, the common-mode input voltage at the FDA inputs must move with the input signal to generate the inverted output signal as a current in the R_{G2} element. A more recent solution is shown as Equation 8, where a quadratic in R_T can be solved for an exact value. This quadratic emerges from the simultaneous solution for a matched input impedance and target gain. The only inputs required are:

- The selected R_F value.
- The target voltage gain (A_v) from the input of R_T to the differential output voltage.
- The desired input impedance at the junction of R_T and R_{G1} to match R_S.

Solving this quadratic for R_T starts the solution sequence, as shown in Equation 8:

$$R_T^2 - R_T \frac{2R_S\left(2R_F + \frac{R_S}{2}A_V^2\right)}{2R_F(2 + A_V) - R_S A_V(4 + A_V)} - \frac{2R_F R_S^2 A_V}{2R_F(2 + A_V) - R_S A_V(4 + A_V)} = 0 \tag{8}$$

Being a quadratic, there are limits to the range of solutions. Specifically, after R_F and R_S are chosen, there is physically a maximum gain beyond which Equation 8 starts to solve for negative R_T values (if input matching is a requirement). With R_F selected, use Equation 9 to verify that the maximum gain is greater than the desired gain.

$$A_{V(MAX)} = \left(\frac{R_F}{R_S} - 2\right) \times \left[1 + \sqrt{1 + \frac{4\frac{R_F}{R_S}}{\left(\frac{R_F}{R_S} - 2\right)^2}}\right] \tag{9}$$

If the achievable $A_{V(MAX)}$ is less than desired, increase the R_F value. After R_T is derived from Equation 8, the R_{G1} element is given by Equation 10:

$$R_{G1} = \frac{2\frac{R_F}{A_V} - R_S}{1 + \frac{R_S}{R_T}} \tag{10}$$

Then, the simplest approach is to use a single $R_{G2} = R_T \parallel R_S + R_{G1}$ on the nonsignal input side. Often, this approach is shown as the separate R_{G1} and R_S elements. Using these separate elements provides a better divider match on the two feedback paths, but a single R_{G2} is often acceptable. A direct solution for R_{G2} is given as Equation 11:

$$R_{G2} = \frac{2\frac{R_F}{A_V}}{1 + \frac{R_S}{R_T}} \tag{11}$$

This design proceeds from a target input impedance matched to R_S, signal gain A_v from the matched input to the differential output voltage, and a selected R_F value. The nominal R_F value chosen for the THS4531A family characterization is 2 kΩ. As discussed previously, going lower improves noise and phase margin, but reduces the total output load impedance possibly degrading harmonic distortion. Going higher increases the output noise, and might reduce the loop-phase margin because of the feedback pole to the input capacitance, but reduces the total loading on the outputs.

Using Equation 9 to Equation 11 to sweep the target gain from 1 to $A_{V(MAX)}$ < 10 V/V gives Table 9, which shows exact values for R_T, R_{G1}, and R_{G2}, where a 50-Ω source must be matched while setting the two feedback resistors to 2 kΩ. One possible solution for 1% standard values is shown, and the resulting actual input impedance and gain with % errors to the targets are also shown in Table 9.

Table 9. Rf = 2 kΩ, Matched Input to 50 Ω, Gain of 1 to 10-V/V Single-Ended to Differential(1)

Av	Rt, EXACT (Ω)	Rt 1%	Rg1, EXACT (Ω)	Rg1 1%	Rg2, EXACT (Ω)	Rg2 1%	ACTUAL Z_{IN}	%ERR TO Rs	ACTUAL GAIN	%ERR TO Av
1	51	51.1	1996.5	2000	2021.8	2000	50.1	0.3	0.998	–0.2
2	51.7	52.3	996.9	1000	1022.5	1020	50.5	1.0	1.994	–0.3
3	52.5	52.3	656.1	649	681.7	681	49.7	–0.5	3.032	1.1
4	53.2	53.6	491.5	487	517.4	523	50.2	0.4	4.035	0.9
5	54	53.6	388	392	413.9	412	49.6	–0.9	4.953	–0.9
6	54.7	54.9	322.7	324	348.9	348	49.9	–0.2	5.978	–0.4
7	55.5	54.9	272.9	274	299.1	301	49.1	–1.7	6.974	–0.4
8	56.3	56.2	238.1	237	264.6	267	49.3	–1.3	8.034	0.4
9	57.1	57.6	211.2	210	237.9	237	49.7	–0.6	9.044	0.5
10	57.9	57.6	187.4	187	214.1	215	48.9	–2.3	10.017	0.2

(1) R_F = 2 kΩ, R_S = 50 Ω.

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These equations and design flow apply to any FDA. Using the feedback resistor value as a starting point is particularly useful for current-feedback-based FDAs such as the LMH6554, where the value of these feedback resistors determines the frequency response flatness. Similar tables can be built using the equations provided here for other source impedances, R_F values, and gain ranges.

The TINA model correctly shows this actively-set input impedance in the single-ended to differential configuration, and is a good tool to validate the gains, input impedances, response shapes, and noise issues.

9.2.7 Differential Input to Single-Ended Output Amplifier

Fully differential op amps like the THS4531A are not recommended for differential to single-ended conversion. This application is best performed with an instrumentation amplifier or with a standard op amp configured as a classic differential amplifier. See application section of the OPA835 data sheet (SLOS713).

10 Power Supply Recommendations

The THS4531A is principally intended to operate with a nominal single-supply voltage of 3 V to 5 V. Supply-voltage tolerances are supported with the specified operating range of 2.5 V (10% low on a 3-V nominal supply) and 5.5 V (8% high on a 5-V nominal supply). Supply decoupling is required, as described in *Application and Implementation*. Split (or bipolar) supplies can be used with the THS4531A, as long as the total value across the device remains less than 5.5 V (absolute maximum).

Using a negative supply to deliver a true swing to ground output in driving SAR ADCs may be desired. While the THS4531A quotes a rail-to-rail output, linear operation requires approximately a 200-mV headroom to the supply rails. One easy option for extending the linear output swing to ground is to provide the small negative supply voltage required using the LM7705 fixed –230-mV, negative-supply generator. This low-cost, fixed negative-supply generator accepts the 3- to 5-V positive supply input used by the THS4531A and provides a –230-mV supply for the negative rail. Using the LM7705 provides an effective solution, as shown in the *Extending Rail-to-Rail Output Range for Fully Differential Amplifiers to Include True Zero Volts*, TI Designs TIDU187.

11 Layout

11.1 Layout Guidelines

The THS4531A EVM (SLOU356) should be used as a reference when designing the circuit board. TI recommends following the EVM layout of the external components near to the amplifier, ground plane construction, and power routing as closely as possible. General guidelines are:

1. Signal routing should be direct and as short as possible into and out of the op amp.
2. The feedback path should be short and direct avoiding vias if possible.
3. Ground or power planes should be removed from directly under the amplifier's input and output pins.
4. A series output resistor is recommended to be placed as near to the output pin as possible. See Figure 77 for recommended values given expected capacitive load of design.
5. A 2.2-µF power supply decoupling capacitor should be placed within 2 inches of the device and can be shared with other op amps. For split supply, a capacitor is required for both supplies.
6. A 0.1-µF power supply decoupling capacitor should be placed as near to the power supply pins as possible. Preferably within 0.1 inch. For split supply, a capacitor is required for both supplies.
7. The $\overline{PD}$ pin uses TTL logic levels referenced to the negative supply voltage (V_{S-}). When not used it should tied to the positive supply to enable the amplifier. When used, it must be actively driven high or low and should not be left in an indeterminate logic state. A bypass capacitor is not required, but can be used for robustness in noisy environments.

11.2 Layout Example

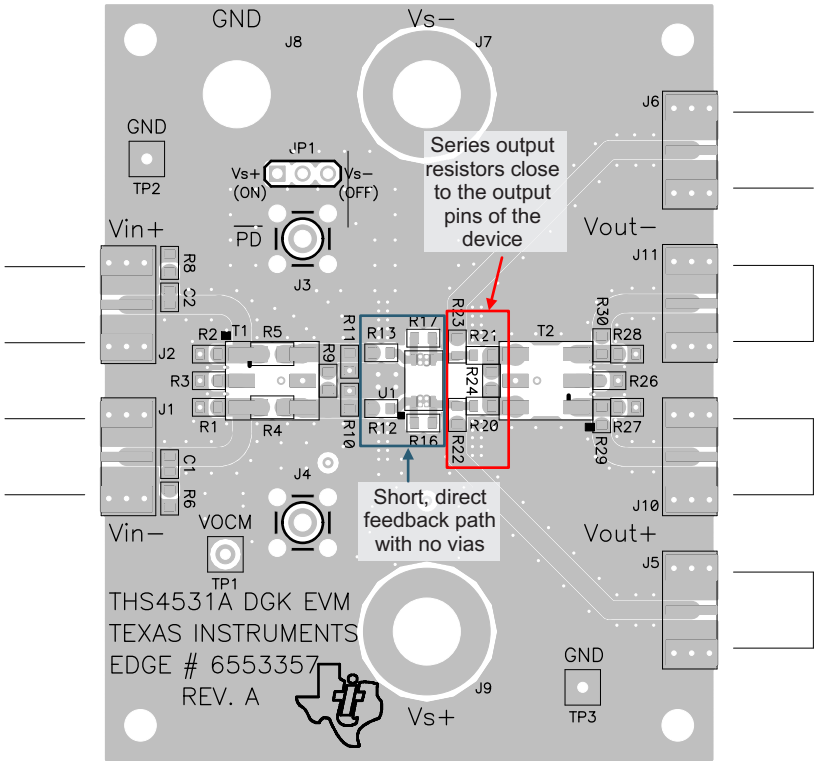

Figure 98. THS4531ADGKEVM Top Layer 1

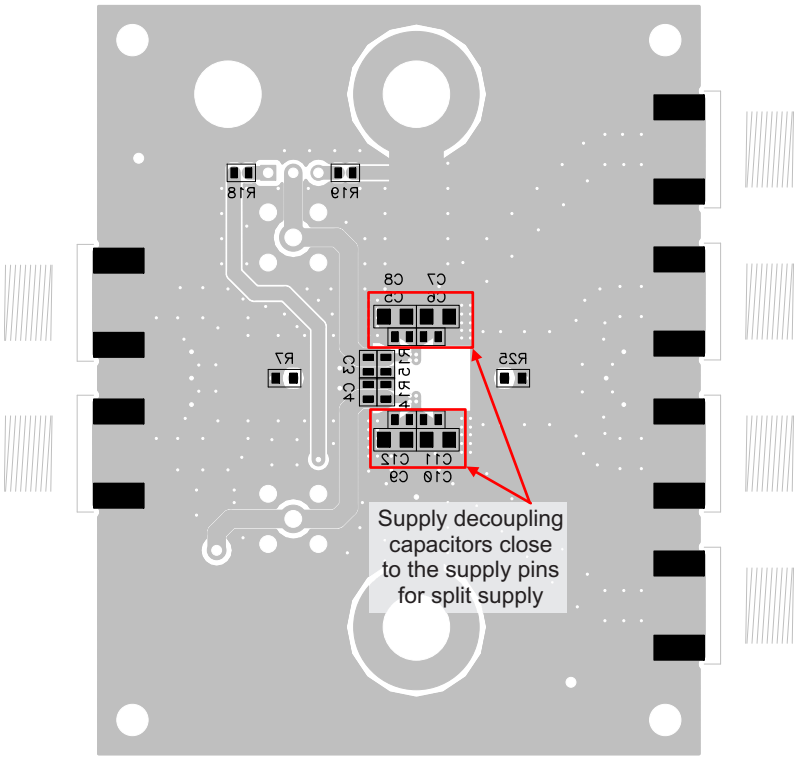

Figure 99. THS4531ADGKEVM Ground Layer 2

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Layout Example (continued)

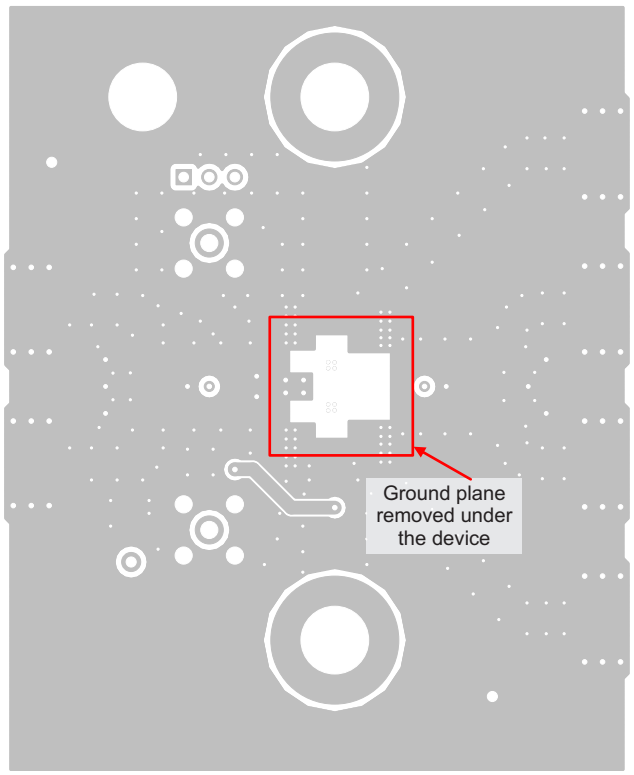

Figure 100. THS4531ADGKEVM Ground Layer 3

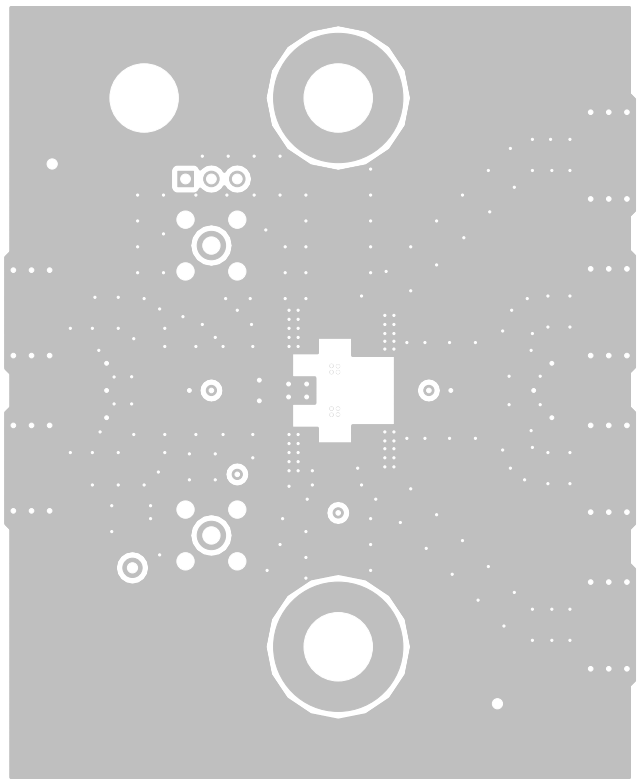

Figure 101. THS4531ADGKEVM Bottom Layer 4

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Documentation Support

For related documentation see the following:

- ADS7945 and ADS7946 *14-Bit, 2 MSPS, Dual-Channel, Differential/Single-Ended, Ultralow-Power Analog-to-Digital Converters*, SBAS539
- ADS8321 *16-Bit, High Speed, MicroPower Sampling Analog-to-Digital converter*, SBAS123
- *Extending Rail-to-Rail Output Range for Fully Differential Amplifiers to Include True Zero Volts*, TIDU187
- *Fully-Differential Amplifiers*, SLOA054
- *OPAx835 Ultra Low-Power, Rail-to-Rail Out, Negative Rail In, VFB Op Amp*, SLOS713
- PCM4204 *High-Performance 24-Bit, 216kHz Sampling Four-Channel Audio Analog-to-Digital Converter*, SBAS327
- *SN74AVC1T45 Single-Bit Dual-Supply Bus Transceiver with Configurable Voltage Translation and 3-State Outputs*, SCES530
- *THS4531ADGKEVM Evaluation Module*, SLOU356

12.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

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All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS4531AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T4531A
THS4531AID.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T4531A
THS4531AIDGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	531A
THS4531AIDGK.B	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	531A
THS4531AIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	531A
THS4531AIDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	531A
THS4531AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T4531A
THS4531AIDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T4531A
THS4531AIRUNR	Active	Production	QFN (RUN) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	531A
THS4531AIRUNR.B	Active	Production	QFN (RUN) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	531A
THS4531AIRUNT	Active	Production	QFN (RUN) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	531A
THS4531AIRUNT.B	Active	Production	QFN (RUN) | 10	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	531A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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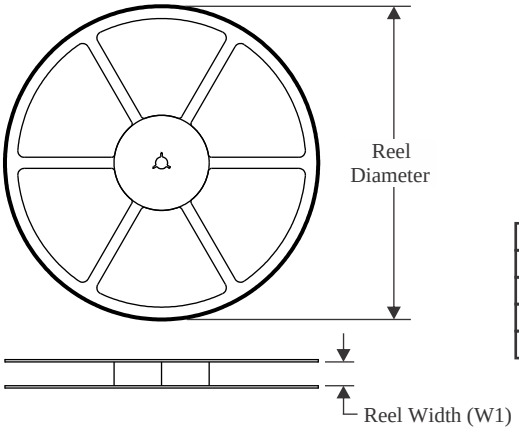
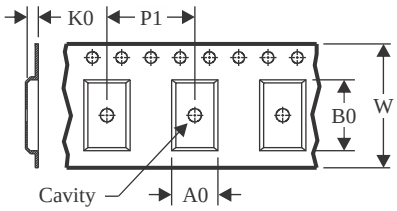
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

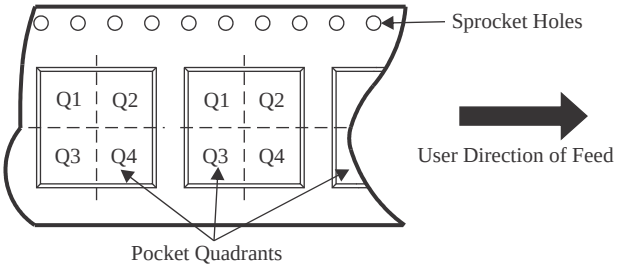


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

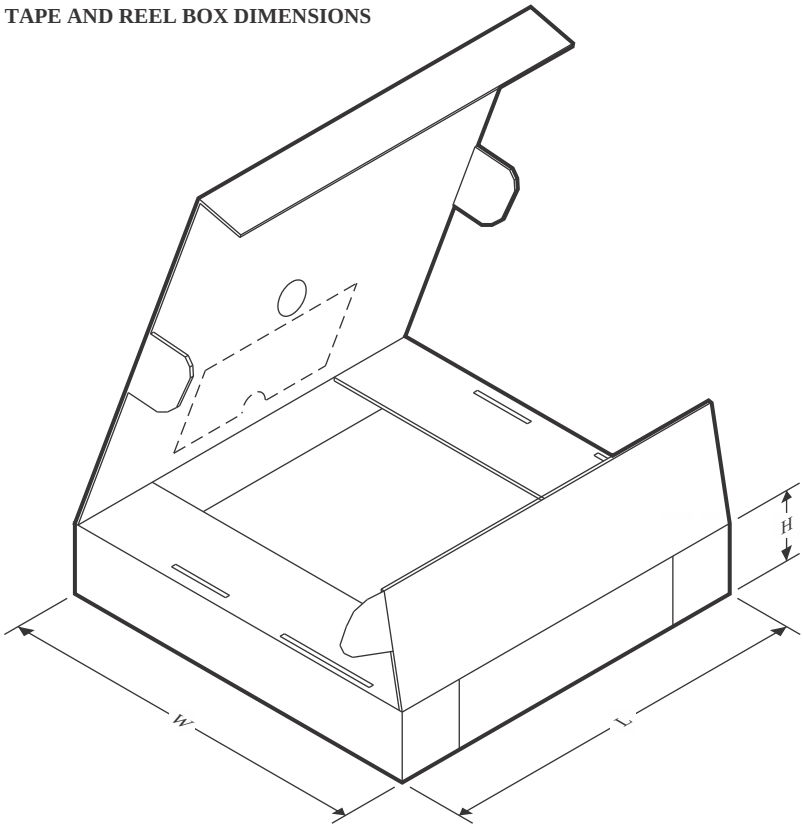
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4531AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
THS4531AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4531AIRUNR	QFN	RUN	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
THS4531AIRUNT	QFN	RUN	10	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

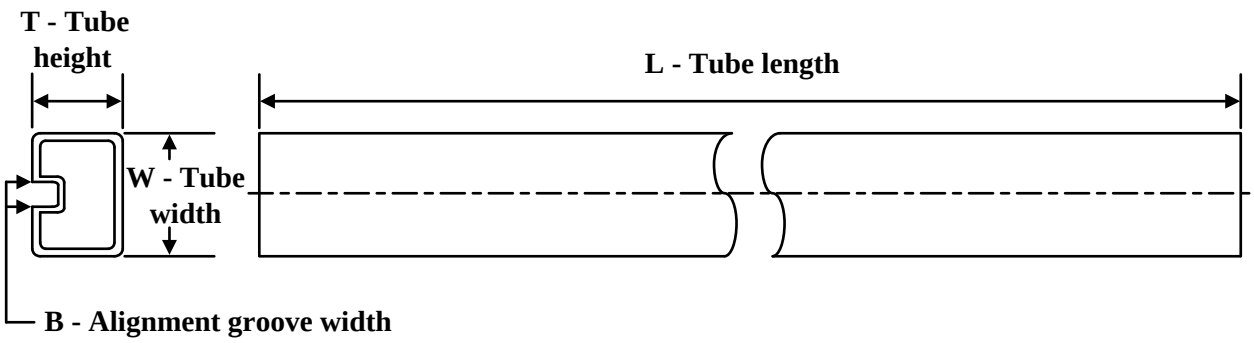
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4531AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
THS4531AIDR	SOIC	D	8	2500	353.0	353.0	32.0
THS4531AIRUNR	QFN	RUN	10	3000	213.0	191.0	35.0
THS4531AIRUNT	QFN	RUN	10	250	213.0	191.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS4531AID	D	SOIC	8	75	506.6	8	3940	4.32
THS4531AID.B	D	SOIC	8	75	506.6	8	3940	4.32
THS4531AIDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
THS4531AIDGK.B	DGK	VSSOP	8	80	330	6.55	500	2.88

GENERIC PACKAGE VIEW

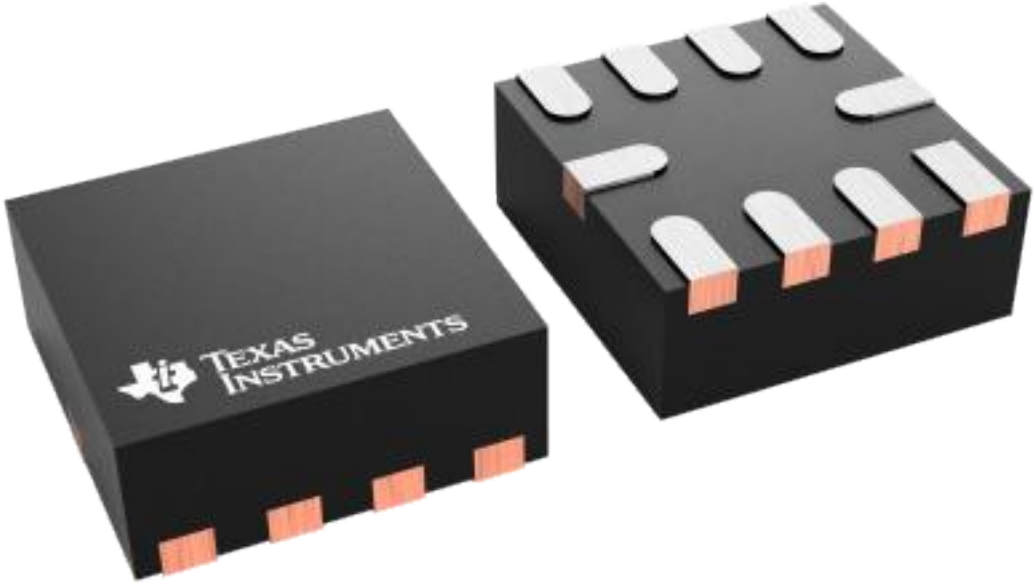
RUN 10

WQFN - 0.8 mm max height

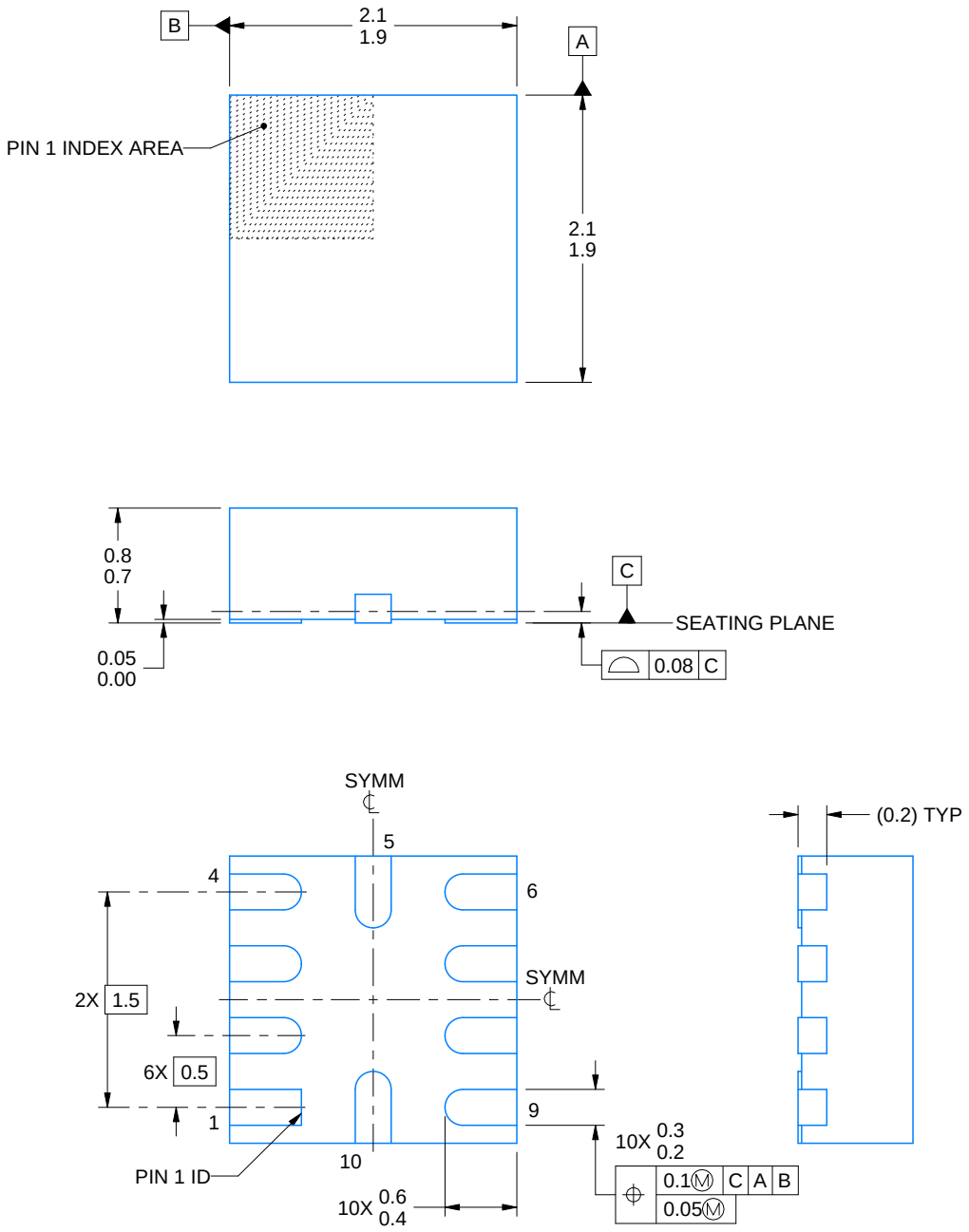
2 X 2, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



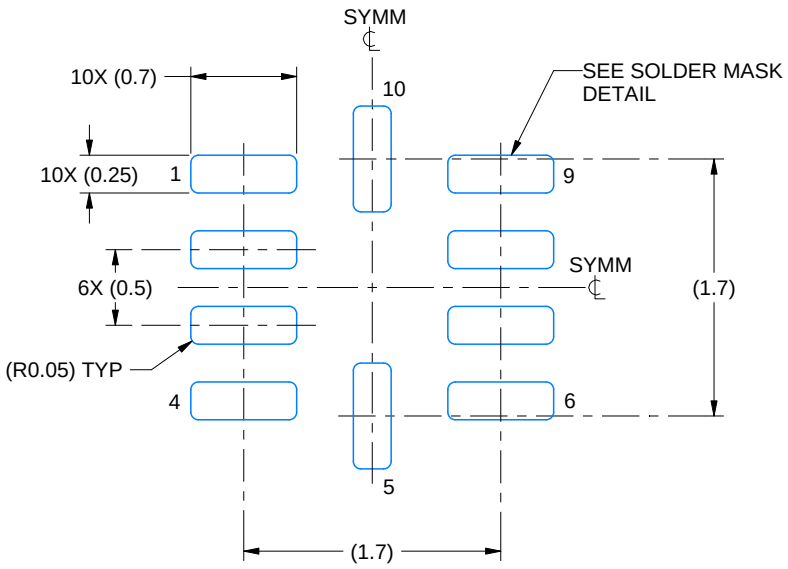
4228249/A



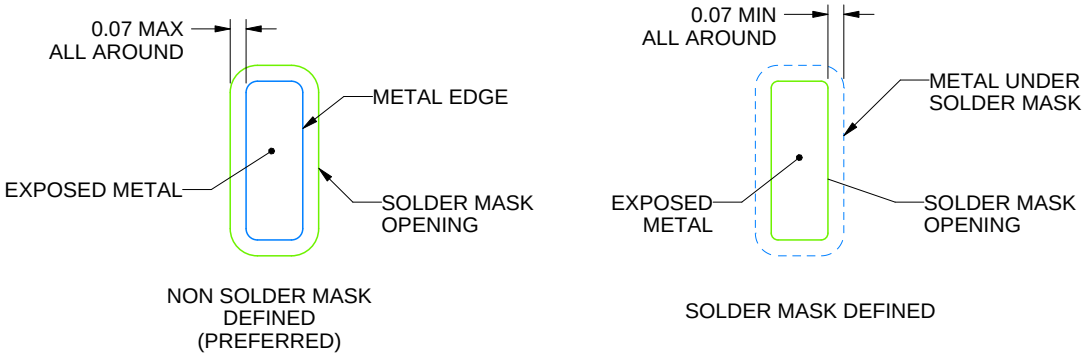
4220470/A 05/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

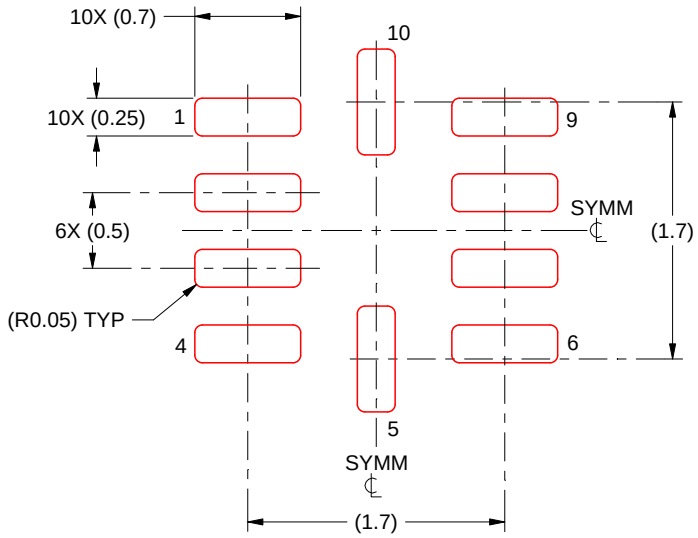


SOLDER MASK DETAILS

4220470/A 05/2020

NOTES: (continued)

3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

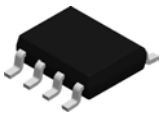


SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

4220470/A 05/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

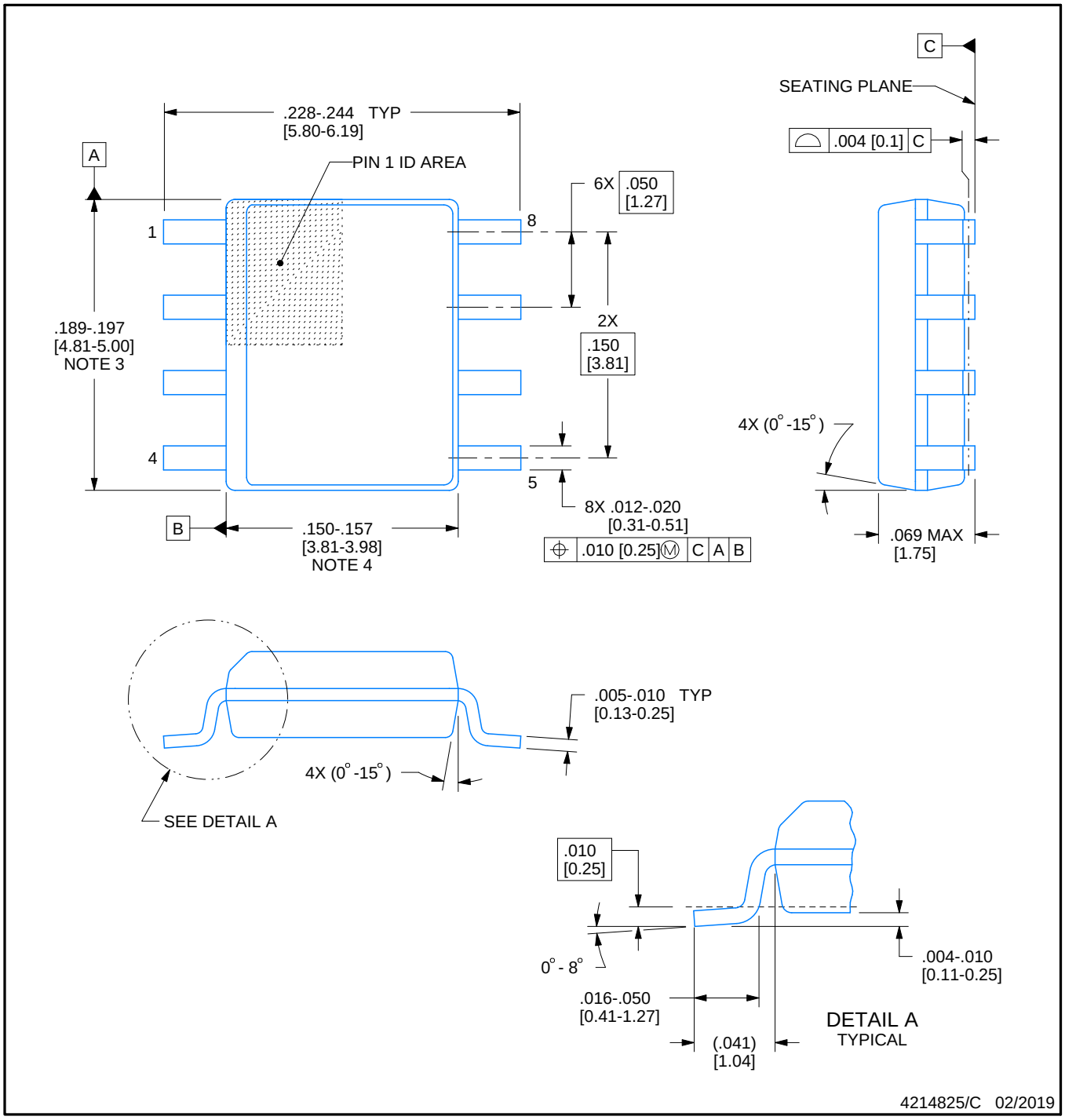


PACKAGE OUTLINE

D0008A

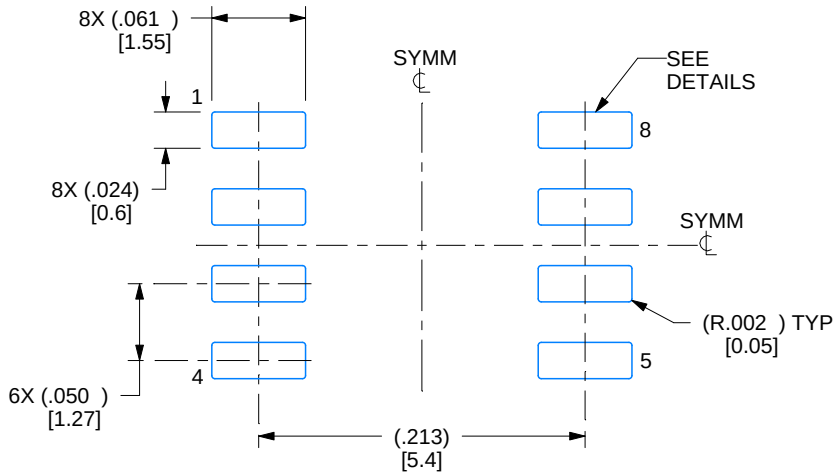
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

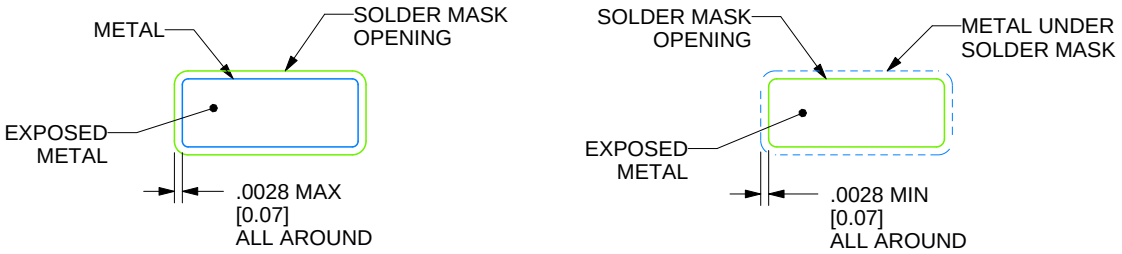


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

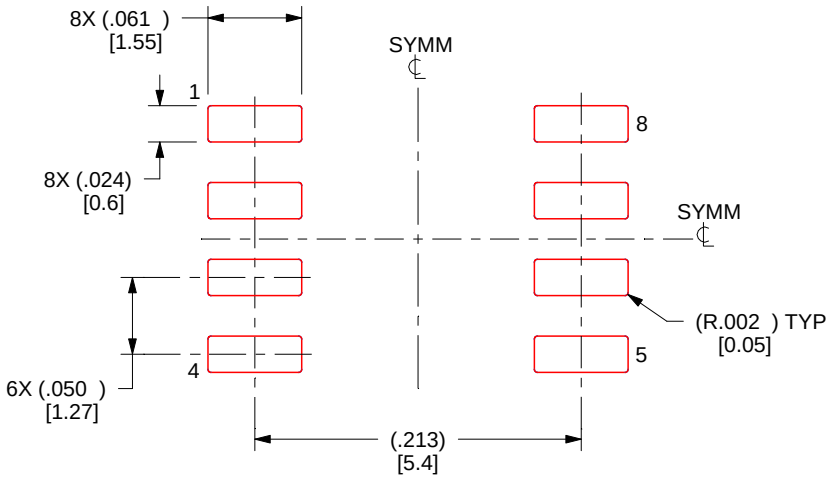


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

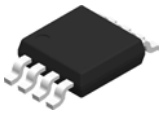
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

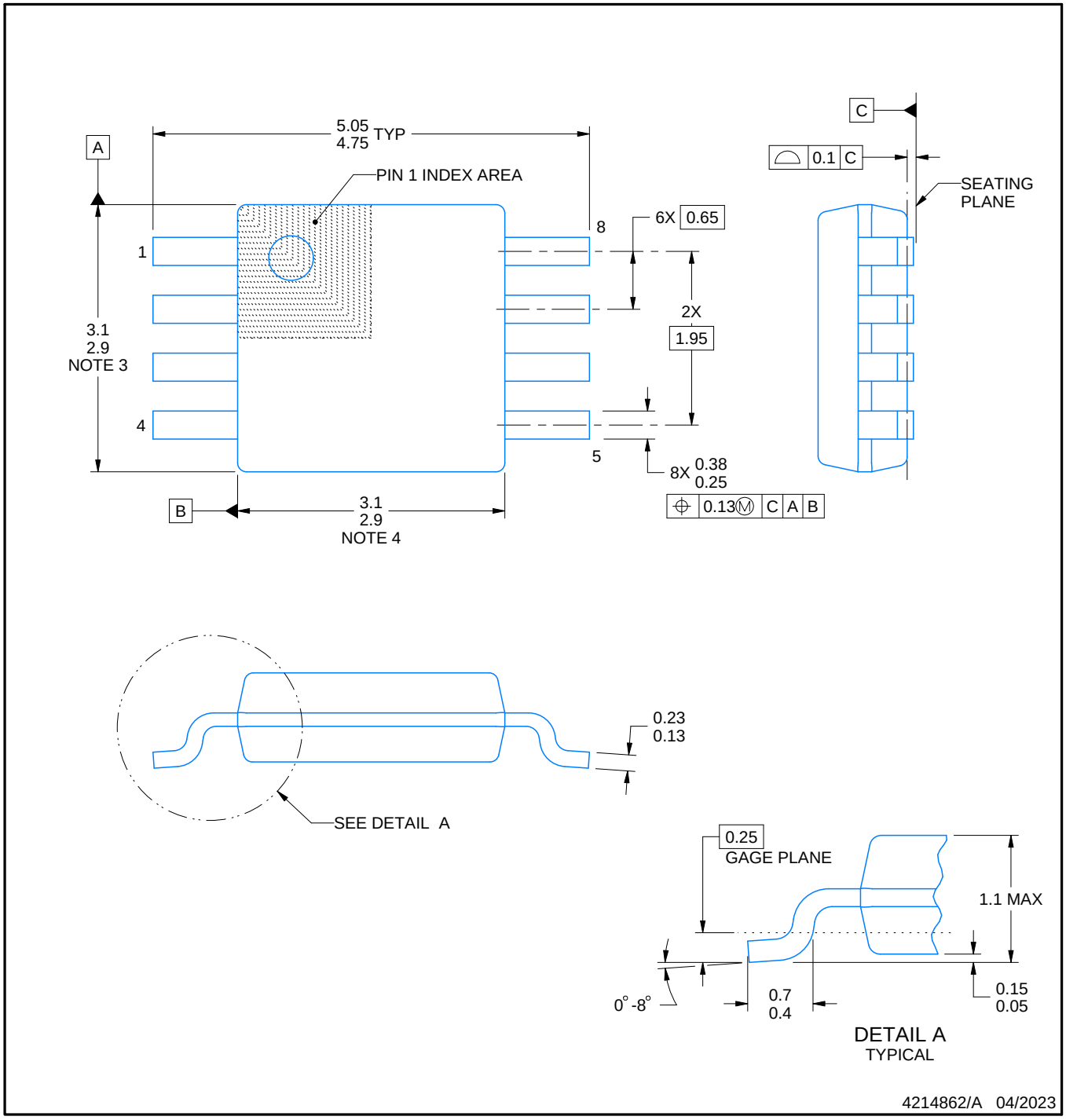
PACKAGE OUTLINE

DGK0008A



VSSOP - 1.1 mm max height

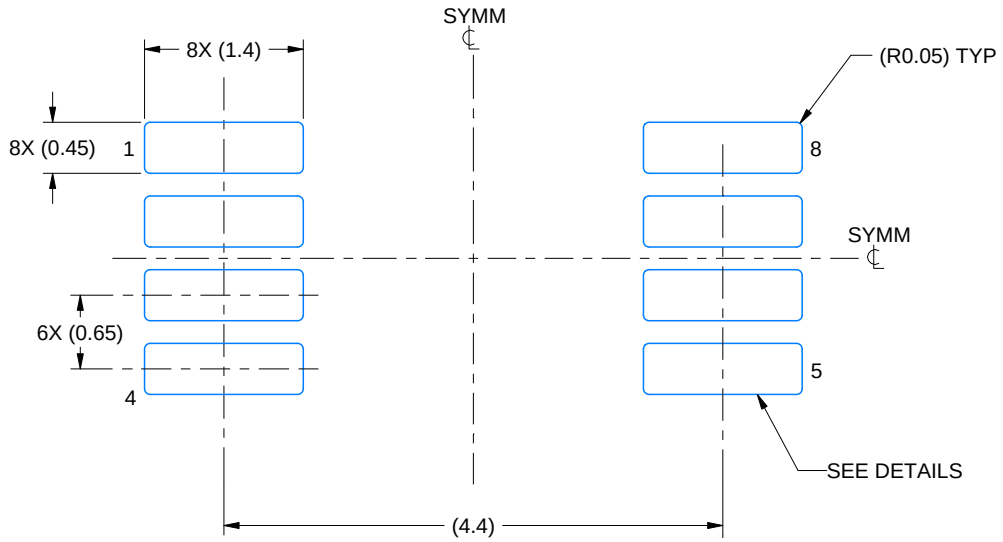
SMALL OUTLINE PACKAGE



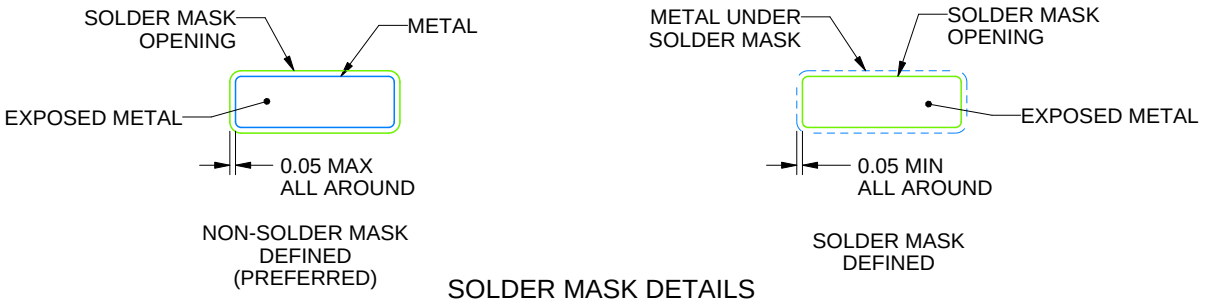
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

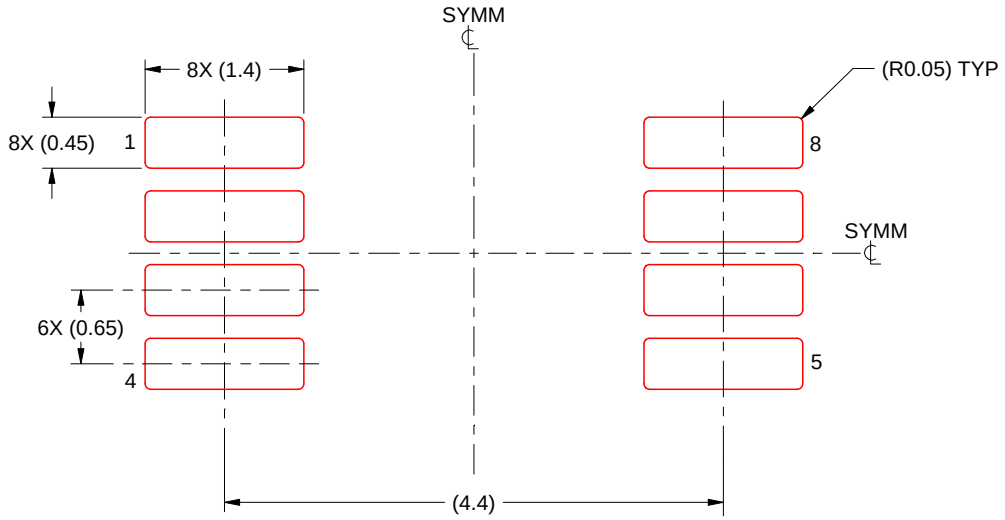


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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