

# TLC1549C, TLC1549I, TLC1549M 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

- 10-Bit-Resolution A/D Converter
- Inherent Sample and Hold
- Total Unadjusted Error . . .  $\pm 1$  LSB Max
- On-Chip System Clock
- Terminal Compatible With TLC549 and TLV1549
- CMOS Technology

## description

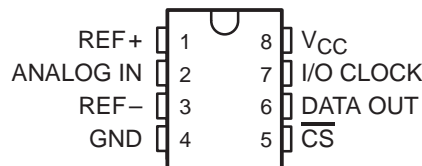
The TLC1549C, TLC1549I, and TLC1549M are 10-bit, switched-capacitor, successive-approximation analog-to-digital converters. These devices have two digital inputs and a 3-state output [chip select ( $\overline{CS}$ ), input-output clock (I/O CLOCK), and data output (DATA OUT)] that provide a three-wire interface to the serial port of a host processor.

The sample-and-hold function is automatic. The converter incorporated in these devices features differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating free-air temperature range.

The TLC1549C is characterized for operation from 0°C to 70°C. The TLC1549I is characterized for operation from -40°C to 85°C. The TLC1549M is characterized for operation over the full military temperature range of -55°C to 125°C.

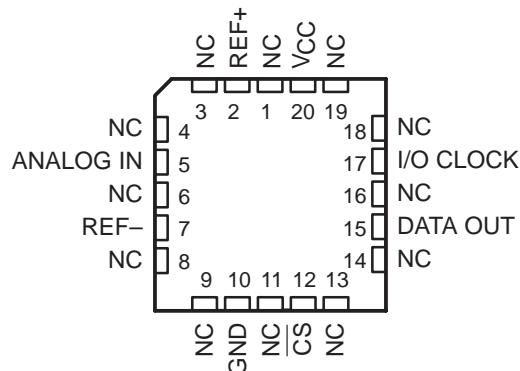
D, JG, OR P PACKAGE

(TOP VIEW)



FK PACKAGE

(TOP VIEW)



NC – No internal connection

## AVAILABLE OPTIONS

T <sub>A</sub>	PACKAGE			
	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)
0°C to 70°C	TLC1549CD	—	—	TLC1549CP
-40°C to 85°C	TLC1549ID	—	—	TLC1549IP
-55°C to 125°C	—	TLC1549MFK	TLC1549MJG	—



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1995, Texas Instruments Incorporated

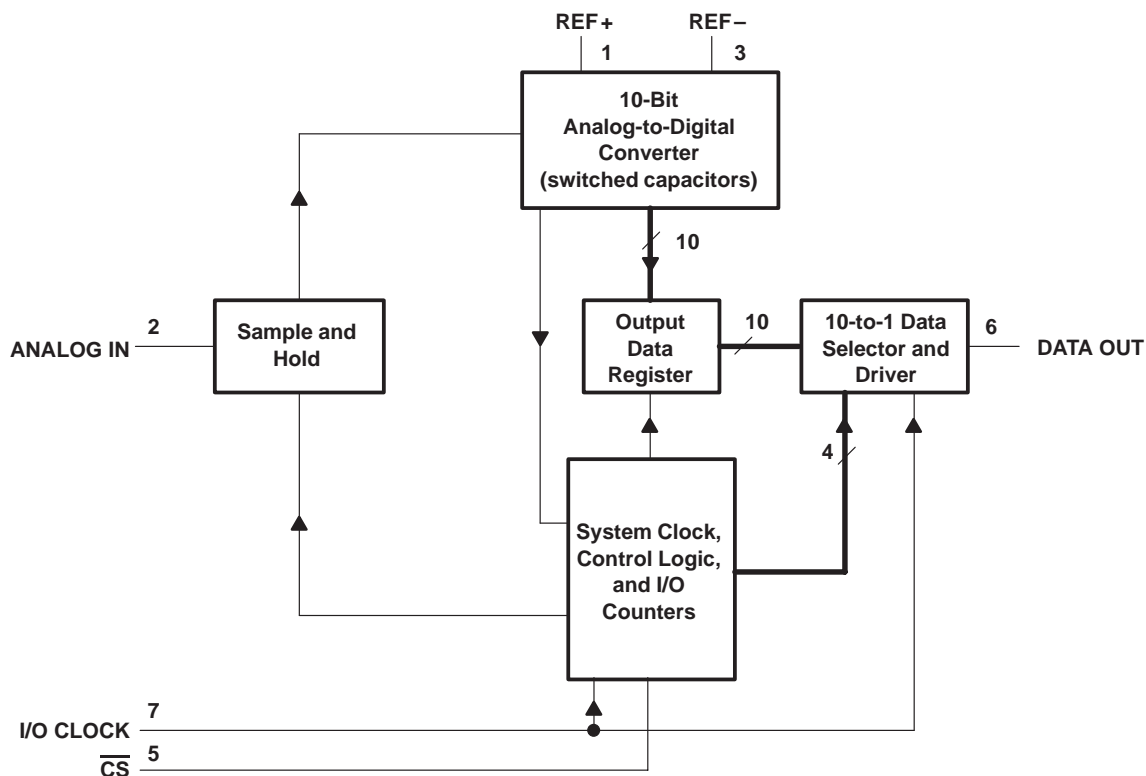
# TLC1549C, TLC1549I, TLC1549M

## 10-BIT ANALOG-TO-DIGITAL CONVERTERS

### WITH SERIAL CONTROL

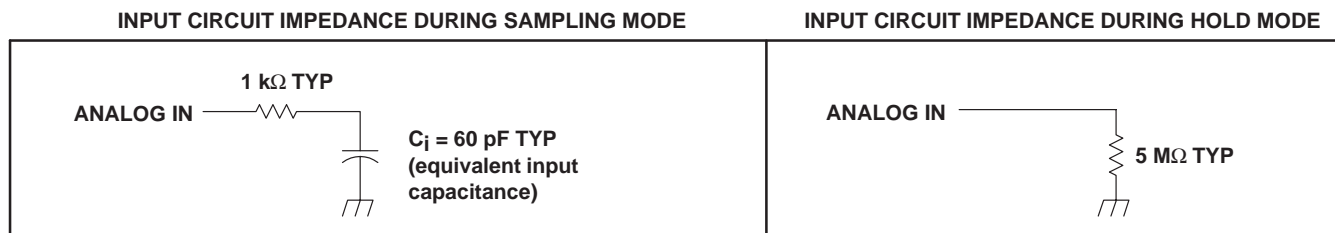
SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

#### functional block diagram



Terminal numbers shown are for the D, JG, and P packages only.

#### typical equivalent inputs



**TLC1549C, TLC1549I, TLC1549M**  
**10-BIT ANALOG-TO-DIGITAL CONVERTERS**  
**WITH SERIAL CONTROL**

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

### Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
ANALOG IN	2	I	Analog signal input. The driving source impedance should be $\leq 1\text{ k}\Omega$ . The external driving source to ANALOG IN should have a current capability $\geq 10\text{ mA}$ .
$\overline{\text{CS}}$	5	I	Chip select. A high-to-low transition on $\overline{\text{CS}}$ resets the internal counters and controls and enables DATA OUT and I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock. A low-to-high transition disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.
DATA OUT	6	O	This 3-state serial output for the A/D conversion result is in the high-impedance state when $\overline{\text{CS}}$ is high and active when $\overline{\text{CS}}$ is low. With a valid chip select, DATA OUT is removed from the high-impedance state and is driven to the logic level corresponding to the MSB value of the previous conversion result. The next falling edge of I/O CLOCK drives DATAOUT to the logic level corresponding to the next most significant bit, and the remaining bits are shifted out in order with the LSB appearing on the ninth falling edge of I/O CLOCK. On the tenth falling edge of I/O CLOCK, DATA OUT is driven to a low logic level so that serial interface data transfers of more than ten clocks produce zeroes as the unused LSBs.
GND	4		The ground return for internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND.
I/O CLOCK	7	I	Input/output clock. I/O CLOCK receives the serial I/O CLOCK input and performs the following three functions: 1) On the third falling edge of I/O CLOCK, the analog input voltage begins charging the capacitor array and continues to do so until the tenth falling edge of I/O CLOCK. 2) It shifts the nine remaining bits of the previous conversion data out on DATA OUT. 3) It transfers control of the conversion to the internal state controller on the falling edge of the tenth clock.
REF +	1	I	The upper reference voltage value (nominally $V_{\text{CC}}$ ) is applied to REF+. The maximum input voltage range is determined by the difference between the voltage applied to REF+ and the voltage applied to REF-.
REF -	3	I	The lower reference voltage value (nominally ground) is applied to REF-.
$V_{\text{CC}}$	8		Positive supply voltage

#### detailed description

With chip select ( $\overline{\text{CS}}$ ) inactive (high), I/O CLOCK is initially disabled and DATA OUT is in the high impedance state. When the serial interface takes  $\overline{\text{CS}}$  active (low), the conversion sequence begins with the enabling of I/O CLOCK and the removal of DATA OUT from the high-impedance state. The serial interface then provides the I/O CLOCK sequence to I/O CLOCK and receives the previous conversion result from DATA OUT. I/O CLOCK receives an input sequence that is between 10 and 16 clocks long from the host serial interface. The first ten I/O clocks provide the control timing for sampling the analog input.

There are six basic serial interface timing modes that can be used with the TLC1549. These modes are determined by the speed of I/O CLOCK and the operation of  $\overline{\text{CS}}$  as shown in Table 1. These modes are (1) a fast mode with a 10-clock transfer and  $\overline{\text{CS}}$  inactive (high) between transfers, (2) a fast mode with a 10-clock transfer and  $\overline{\text{CS}}$  active (low) continuously, (3) a fast mode with an 11- to 16-clock transfer and  $\overline{\text{CS}}$  inactive (high) between transfers, (4) a fast mode with a 16-bit transfer and  $\overline{\text{CS}}$  active (low) continuously, (5) a slow mode with an 11- to 16-clock transfer and  $\overline{\text{CS}}$  inactive (high) between transfers, and (6) a slow mode with a 16-clock transfer and  $\overline{\text{CS}}$  active (low) continuously.

The MSB of the previous conversion appears on DATA OUT on the falling edge of  $\overline{\text{CS}}$  in mode 1, mode 3, and mode 5, within  $21\text{ }\mu\text{s}$  from the falling edge of the tenth I/O CLOCK in mode 2 and mode 4, and following the sixteenth clock falling edge in mode 6. The remaining nine bits are shifted out on the next nine falling edges of I/O CLOCK. Ten bits of data are transmitted to the host serial interface through DATA OUT. The number of serial clock pulses used also depends on the mode of operation, but a minimum of ten clock pulses is required for conversion to begin. On the tenth clock falling edge, the internal logic takes DATA OUT low to ensure that the remaining bit values are zero if the I/O CLOCK transfer is more than ten clocks long.

Table 1 lists the operational modes with respect to the state of  $\overline{\text{CS}}$ , the number of I/O serial transfer clocks that can be used, and the timing on which the MSB of the previous conversion appears at the output.



# TLC1549C, TLC1549I, TLC1549M

## 10-BIT ANALOG-TO-DIGITAL CONVERTERS

### WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

#### detailed description

**Table 1. Mode Operation**

MODES		$\overline{CS}$	NO. OF I/O CLOCKS	MSB AT Terminal 6†	TIMING DIAGRAM
Fast Modes	Mode 1	High between conversion cycles	10	$\overline{CS}$ falling edge	Figure 6
	Mode 2	Low continuously	10	Within 21 $\mu$ s	Figure 7
	Mode 3	High between conversion cycles	11 to 16‡	$\overline{CS}$ falling edge	Figure 8
	Mode 4	Low continuously	16‡	Within 21 $\mu$ s	Figure 9
Slow Modes	Mode 5	High between conversion cycles	11 to 16‡	$\overline{CS}$ falling edge	Figure 10
	Mode 6	Low continuously	16‡	16th clock falling edge	Figure 11

† This timing also initiates serial interface communication.

‡ No more than 16 clocks should be used.

All the modes require a minimum period of 21  $\mu$ s after the falling edge of the tenth I/O CLOCK before a new transfer sequence can begin. During a serial I/O CLOCK data transfer,  $\overline{CS}$  must be active (low) so that I/O CLOCK is enabled. When  $\overline{CS}$  is toggled between data transfers (modes 1, 3, and 5), the transitions at  $\overline{CS}$  are recognized as valid only if the level is maintained for a minimum period of 1.425  $\mu$ s after the transition. If the transfer is more than ten I/O clocks (modes 3, 4, 5, and 6), the rising edge of the eleventh clock must occur within 9.5  $\mu$ s after the falling edge of the tenth I/O CLOCK; otherwise, the device could lose synchronization with the host serial interface and  $\overline{CS}$  has to be toggled to restore proper operation.

#### fast modes

The TLC1549 is in a fast mode when the serial I/O CLOCK data transfer is completed within 21  $\mu$ s from the falling edge of the tenth I/O CLOCK. With a ten-clock serial transfer, the device can only run in a fast mode.

##### **mode 1: fast mode, $\overline{CS}$ inactive (high) between transfers, 10-clock transfer**

In this mode,  $\overline{CS}$  is inactive (high) between serial I/O CLOCK transfers and each transfer is ten clocks long. The falling edge of  $\overline{CS}$  begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of  $\overline{CS}$  ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of  $\overline{CS}$  disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.

##### **mode 2: fast mode, $\overline{CS}$ active (low) continuously, 10-clock transfer**

In this mode,  $\overline{CS}$  is active (low) between serial I/O CLOCK transfers and each transfer is ten clocks long. After the initial conversion cycle,  $\overline{CS}$  is held active (low) for subsequent conversions. Within 21  $\mu$ s after the falling edge of the tenth I/O CLOCK, the MSB of the previous conversion appears at DATA OUT.

##### **mode 3: fast mode, $\overline{CS}$ inactive (high) between transfers, 11- to 16-clock transfer**

In this mode,  $\overline{CS}$  is inactive (high) between serial I/O CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of  $\overline{CS}$  begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of  $\overline{CS}$  ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of  $\overline{CS}$  disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.

##### **mode 4: fast mode, $\overline{CS}$ active (low) continuously, 16-clock transfer**

In this mode,  $\overline{CS}$  is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle,  $\overline{CS}$  is held active (low) for subsequent conversions. Within 21  $\mu$ s after the falling edge of the tenth I/O CLOCK, the MSB of the previous conversion appears at DATA OUT.

#### slow modes

In a slow mode, the serial I/O CLOCK data transfer is completed after 21  $\mu$ s from the falling edge of the tenth I/O CLOCK.



---

**mode 5: slow mode,  $\overline{CS}$  inactive (high) between transfers, 11- to 16-clock transfer**

In this mode,  $\overline{CS}$  is inactive (high) between serial I/O CLOCK transfers and each transfer can be 11 to 16 clocks long. The falling edge of  $\overline{CS}$  begins the sequence by removing DATA OUT from the high-impedance state. The rising edge of  $\overline{CS}$  ends the sequence by returning DATA OUT to the high-impedance state within the specified delay time. Also, the rising edge of  $\overline{CS}$  disables I/O CLOCK within a setup time plus two falling edges of the internal system clock.

**mode 6: slow mode,  $\overline{CS}$  active (low) continuously, 16-clock transfer**

In this mode,  $\overline{CS}$  is active (low) between serial I/O CLOCK transfers and each transfer must be exactly 16 clocks long. After the initial conversion cycle,  $\overline{CS}$  is held active (low) for subsequent conversions. The falling edge of the sixteenth I/O CLOCK then begins each sequence by removing DATA OUT from the low state, allowing the MSB of the previous conversion to appear immediately at DATA OUT. The device is then ready for the next 16 clock transfer initiated by the serial interface.

**analog input sampling**

Sampling of the analog input starts on the falling edge of the third I/O CLOCK, and sampling continues for seven I/O CLOCK periods. The sample is held on the falling edge of the tenth I/O CLOCK.

**converter and analog input**

The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the  $S_C$  switch and all  $S_T$  switches simultaneously. This action charges all the capacitors to the input voltage.

In the next phase of the conversion process, all  $S_T$  and  $S_C$  switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REF–) voltage. In the switching sequence, ten capacitors are examined separately until all ten bits are identified and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 512). Node 512 of this capacitor is switched to the REF+ voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REF–. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half  $V_{CC}$ ), a bit 0 is placed in the output register and the 512-weight capacitor is switched to REF–. If the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register and this 512-weight capacitor remains connected to REF+ through the remainder of the successive-approximation process. The process is repeated for the 256-weight capacitor, the 128-weight capacitor, and so forth down the line until all bits are determined.

With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to determine the bits from MSB to LSB.

# TLC1549C, TLC1549I, TLC1549M

## 10-BIT ANALOG-TO-DIGITAL CONVERTERS

### WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

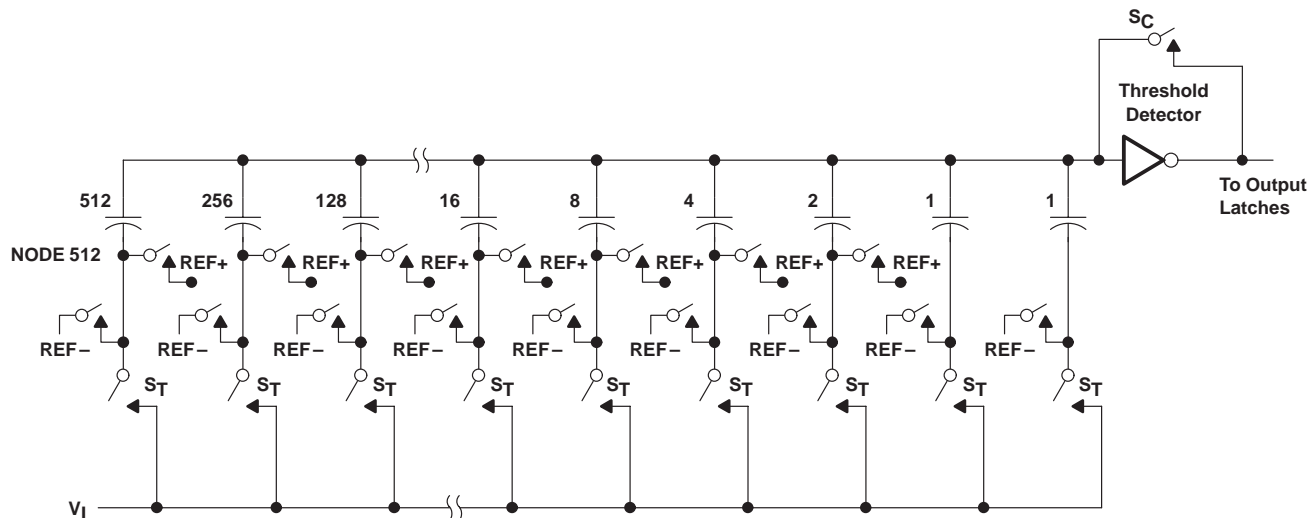


Figure 1. Simplified Model of the Successive-Approximation System

#### chip-select operation

The trailing edge of  $\overline{CS}$  starts all modes of operation, and  $\overline{CS}$  can abort a conversion sequence in any mode. A high-to-low transition on  $\overline{CS}$  within the specified time during a  $\overline{CS}$  an ongoing cycle aborts the cycle, and the device returns to the initial state (the contents of the output data register remain at the previous conversion result). Care should be exercised to prevent  $\overline{CS}$  from being taken low close to completion of conversion because the output data may be corrupted.

#### reference voltage inputs

There are two reference inputs used with the TLC1549: REF+ and REF-. These voltage values establish the upper and lower limits of the analog input to produce a full-scale and zero reading respectively. The values of REF+, REF-, and the analog input should not exceed the positive supply or be lower than GND consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REF+ and at zero when the input signal is equal to or lower than REF-.

# TLC1549C, TLC1549I, TLC1549M

## 10-BIT ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1): TLC1549C, TLC1549I .....	–0.5 V to 6.5 V
TLC1549M .....	–0.5 V to 6 V
Input voltage range, $V_I$ (any input) .....	–0.3 V to $V_{CC} + 0.3$ V
Output voltage range, $V_O$ .....	–0.3 V to $V_{CC} + 0.3$ V
Positive reference voltage, $V_{ref+}$ .....	$V_{CC} + 0.1$ V
Negative reference voltage, $V_{ref-}$ .....	–0.1 V
Peak input current (any input) .....	±20 mA
Peak total input current (all inputs) .....	±30 mA
Operating free-air temperature range, $T_A$ : TLC1549C .....	0°C to 70°C
TLC1549I .....	–40°C to 85°C
TLC1549M .....	–55°C to 125°C
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds .....	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to ground with REF– and GND wired together (unless otherwise noted).

### recommended operating conditions

		MIN	NOM	MAX	UNIT	
Supply voltage, $V_{CC}$		4.5	5	5.5	V	
Positive reference voltage, $V_{ref+}$ (see Note 2)		$V_{CC}$			V	
Negative reference voltage, $V_{ref-}$ (see Note 2)		0			V	
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 2)		2.5	$V_{CC}$	$V_{CC} + 0.2$	V	
Analog input voltage (see Note 2)		0			$V_{CC}$	
High-level control input voltage, $V_{IH}$	$V_{CC} = 4.5$ V to 5.5 V	2			V	
Low-level control input voltage, $V_{IL}$	$V_{CC} = 4.5$ V to 5.5 V	0.8			V	
Clock frequency at I/O CLOCK (see Note 3)		0			2.1	
Setup time, $\overline{CS}$ low before first I/O CLOCK↑, $t_{su}(CS)$ (see Note 4)		1.425			μs	
Hold time, $\overline{CS}$ low after last I/O CLOCK↓, $t_h(CS)$		0			ns	
Pulse duration, I/O CLOCK high, $t_{wH}(I/O)$		190			ns	
Pulse duration, I/O CLOCK low, $t_{wL}(I/O)$		190			ns	
Transition time, I/O CLOCK, $t_t(I/O)$ (see Note 5 and Figure 5)		1			μs	
Transition time, $\overline{CS}$ , $t_t(CS)$		10			μs	
Operating free-air temperature, $T_A$	TLC1549C	0			70	°C
	TLC1549I	–40				
	TLC1549M	–55				

- NOTES:
2. Analog input voltages greater than that applied to REF+ convert as all ones (1111111111), while input voltages less than that applied to REF– convert as all zeros (0000000000). The TLC1549 is functional with reference voltages down to 1 V ( $V_{ref+} - V_{ref-}$ ); however, the electrical specifications are no longer applicable.
  3. For 11- to 16-bit transfers, after the tenth I/O CLOCK falling edge ( $\leq 2$  V) at least 1 I/O CLOCK rising edge ( $\geq 2$  V) must occur within 9.5 μs.
  4. To minimize errors caused by noise at  $\overline{CS}$ , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after  $\overline{CS}$ ↓ before responding to the I/O CLOCK. No attempt should be made to clock out the data until the minimum  $\overline{CS}$  setup time has elapsed.
  5. This is the time required for the clock input signal to fall from  $V_{IHmin}$  to  $V_{ILmax}$  or to rise from  $V_{ILmax}$  to  $V_{IHmin}$ . In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 μs for remote data-acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.





**TLC1549C, TLC1549I, TLC1549M**  
**10-BIT ANALOG-TO-DIGITAL CONVERTERS**  
**WITH SERIAL CONTROL**

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

**electrical characteristics over recommended operating free-air temperature range,  
 $V_{CC} = V_{ref+} = 4.5\text{ V to }5.5\text{ V}$ , I/O CLOCK frequency = 2.1 MHz (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
VOH	High-level output voltage	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -1.6\text{ mA}$	2.4			V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $I_{OH} = -20\text{ }\mu\text{A}$	$V_{CC} - 0.1$			
VOL	Low-level output voltage	$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 1.6\text{ mA}$			0.4	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$ , $I_{OL} = 20\text{ }\mu\text{A}$			0.1	
IOZ	Off-state (high-impedance-state) output current	$V_O = V_{CC}$ , $\overline{CS}$ at $V_{CC}$			10	$\mu\text{A}$
		$V_O = 0$ , $\overline{CS}$ at $V_{CC}$			-10	
I <sub>IH</sub>	High-level input current	$V_I = V_{CC}$	0.005		2.5	$\mu\text{A}$
I <sub>IL</sub>	Low-level input current	$V_I = 0$	-0.005		-2.5	$\mu\text{A}$
I <sub>CC</sub>	Operating supply current	$\overline{CS}$ at 0 V	0.8		2.5	mA
Analog input leakage current		$V_I = V_{CC}$			1	$\mu\text{A}$
		$V_I = 0$			-1	
Maximum static analog reference current into REF+		$V_{ref+} = V_{CC}$ , $V_{ref-} = \text{GND}$			10	$\mu\text{A}$
C <sub>i</sub>	Input capacitance	TLC1549C, I (Analog)	During sample cycle		30	pF
		TLC1549M (Analog)	During sample cycle		30	
		TLC1549C, I (Control)			5	
		TLC1549M (Control)			5	

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .





**TLC1549C, TLC1549I, TLC1549M**  
**10-BIT ANALOG-TO-DIGITAL CONVERTERS**  
**WITH SERIAL CONTROL**

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

**operating characteristics over recommended operating free-air temperature range,  
 $V_{CC} = V_{ref+} = 4.5\text{ V to }5.5\text{ V}$ , I/O CLOCK frequency = 2.1 MHz**

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$E_L$	Linearity error (see Note 6)			$\pm 1$	LSB
$E_{ZS}$	Zero-scale error (see Note 7)	See Note 2		$\pm 1$	LSB
$E_{FS}$	Full-scale error (see Note 7)	See Note 2		$\pm 1$	LSB
	Total unadjusted error (see Note 8)			$\pm 1$	LSB
$t_{conv}$	Conversion time	See Figures 6–10		21	$\mu\text{s}$
$t_c$	Total cycle time (access, sample, and conversion)	See Figures 6–10, See Note 9		21 + 10 I/O CLOCK periods	$\mu\text{s}$
$t_v$	Valid time, DATA OUT remains valid after I/O CLOCK $\downarrow$	See Figure 5	10		ns
$t_d(\text{I/O-DATA})$	Delay time, I/O CLOCK $\downarrow$ to DATA OUT valid	See Figure 5		240	ns
$t_{PZH}, t_{PZL}$	Enable time, $\overline{CS}\downarrow$ to DATA OUT (MSB driven)	See Figure 3		1.3	$\mu\text{s}$
$t_{PHZ}, t_{PLZ}$	Disable time, $\overline{CS}\uparrow$ to DATA OUT (high impedance)	See Figure 3		180	ns
$t_r(\text{bus})$	Rise time, data bus	See Figure 5		300	ns
$t_f(\text{bus})$	Fall time, data bus	See Figure 5		300	ns
$t_d(\text{I/O-CS})$	Delay time, tenth I/O CLOCK $\downarrow$ to $\overline{CS}\downarrow$ to abort conversion (see Note 10)			9	$\mu\text{s}$

- NOTES:
- Analog input voltages greater than that applied to REF + convert as all ones (111111111), while input voltages less than that applied to REF – convert as all zeros (000000000). The TLC1549 is functional with reference voltages down to 1 V ( $V_{ref+} - V_{ref-}$ ); however, the electrical specifications are no longer applicable.
  - Linearity error is the maximum deviation from the best straight line through the A/D transfer characteristics.
  - Zero error is the difference between 000000000 and the converted output for zero input voltage; full-scale error is the difference between 111111111 and the converted output for full-scale input voltage.
  - Total unadjusted error comprises linearity, zero, and full-scale errors.
  - I/O CLOCK period = 1/(I/O CLOCK frequency). Sampling begins on the falling edge of the third I/O CLOCK, continues for seven I/O CLOCK periods, and ends on the falling edge of the 10th I/O CLOCK (see Figure 5).
  - Any transitions of  $\overline{CS}$  are recognized as valid only if the level is maintained for a minimum of a setup time plus two falling edges of the internal clock (1.425  $\mu\text{s}$ ) after the transition.

TLC1549C, TLC1549I, TLC1549M  
 10-BIT ANALOG-TO-DIGITAL CONVERTERS  
 WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

PARAMETER MEASUREMENT INFORMATION

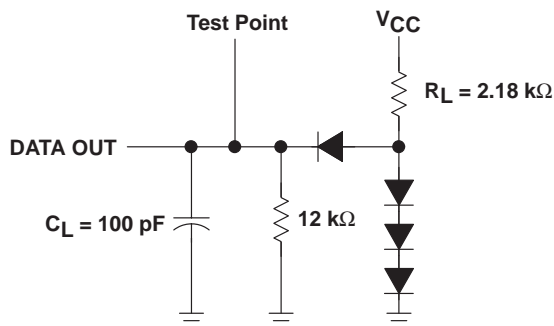


Figure 2. Load Circuit

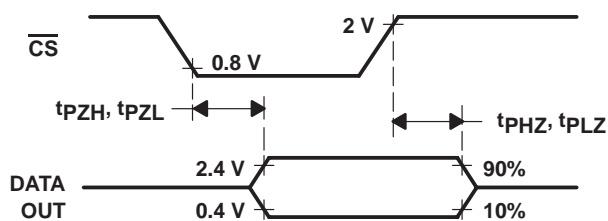


Figure 3. DATA OUT to Hi-Z Voltage Waveforms

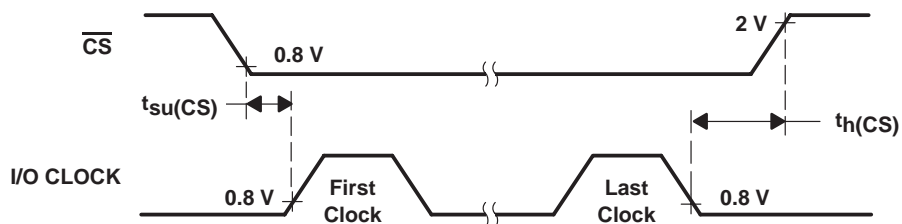


Figure 4. CS to I/O CLOCK Voltage Waveforms

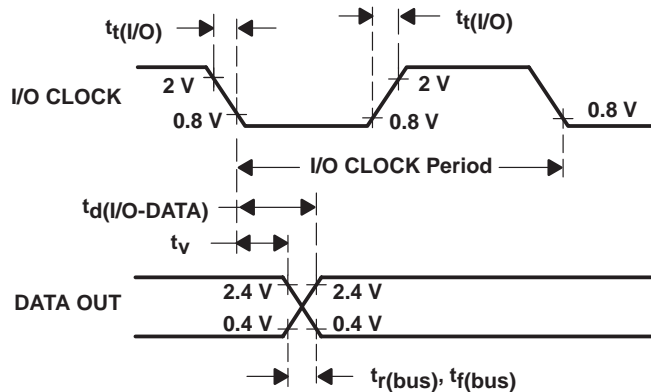


Figure 5. I/O CLOCK and DATA OUT Voltage Waveforms

TLC1549C, TLC1549I, TLC1549M  
 10-BIT ANALOG-TO-DIGITAL CONVERTERS  
 WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

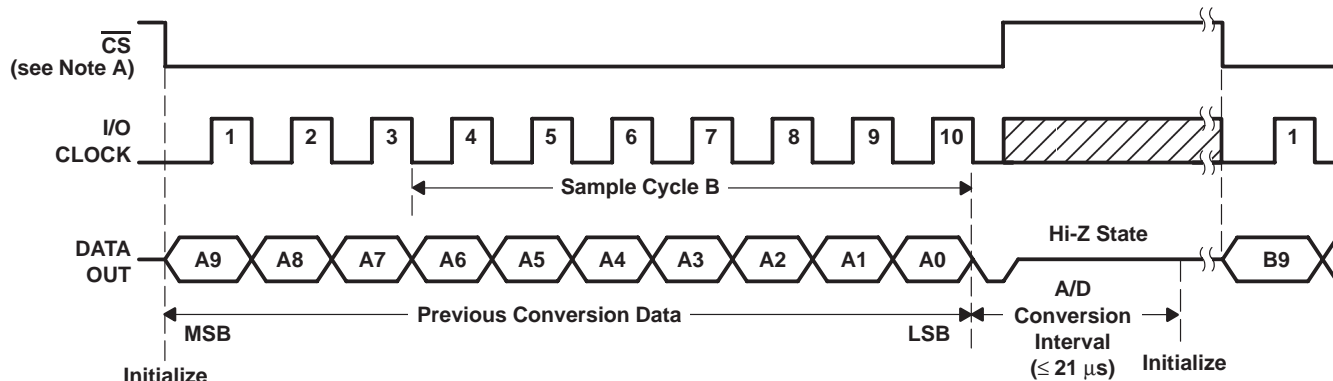


Figure 6. Timing for 10-Clock Transfer Using  $\overline{CS}$

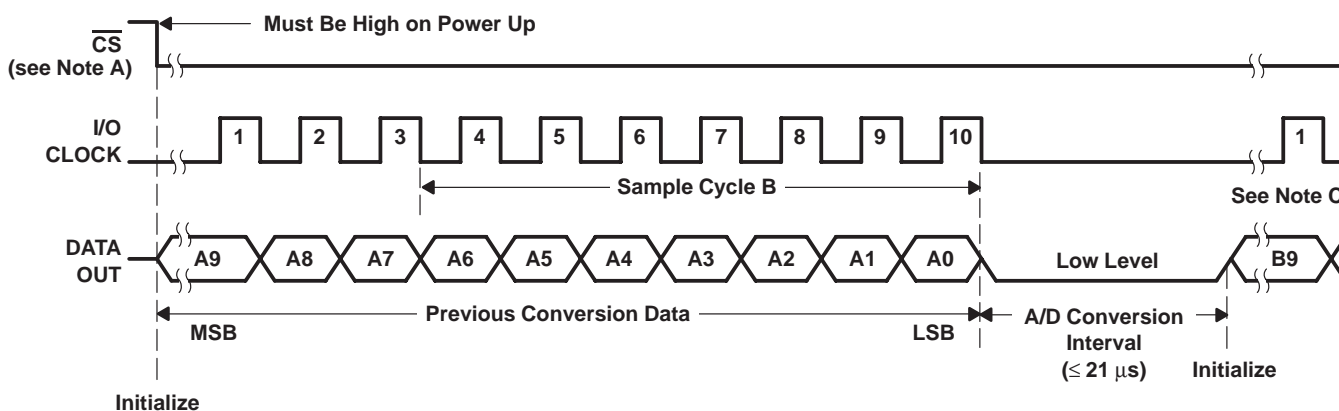


Figure 7. Timing for 10-Clock Transfer Not Using  $\overline{CS}$

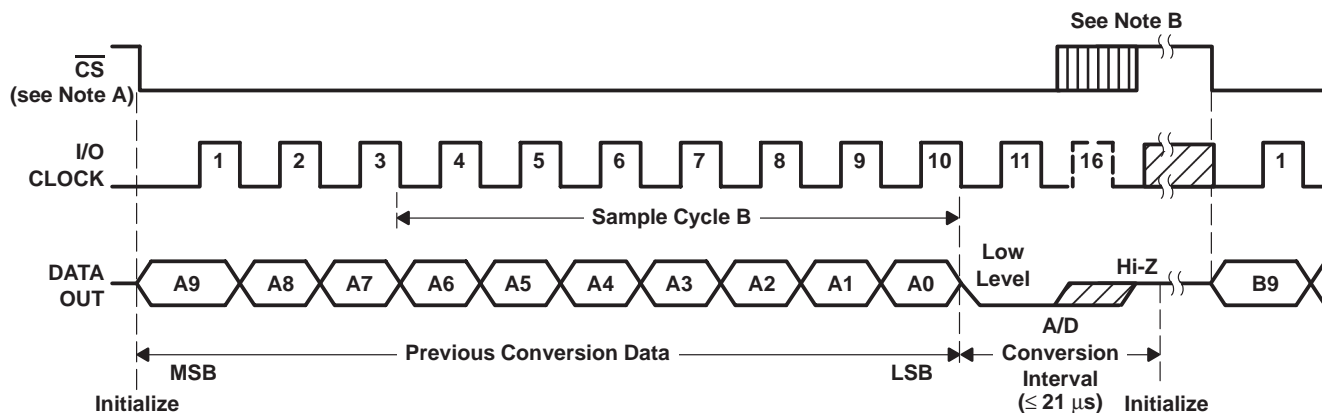


Figure 8. Timing for 11- to 16-Clock Transfer Using  $\overline{CS}$  (Serial Transfer Completed Within 21  $\mu$ s)

- NOTES:
- A. To minimize errors caused by noise at  $\overline{CS}$ , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after  $\overline{CS} \downarrow$  before responding to the I/O CLOCK. No attempt should be made to clock out the data until the minimum  $\overline{CS}$  setup time has elapsed.
  - B. A low-to-high transition of  $\overline{CS}$  disables I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.
  - C. The first I/O CLOCK must occur after the end of the previous conversion.

# TLC1549C, TLC1549I, TLC1549M

## 10-BIT ANALOG-TO-DIGITAL CONVERTERS

### WITH SERIAL CONTROL

SLAS059C – DECEMBER 1992 – REVISED MARCH 1995

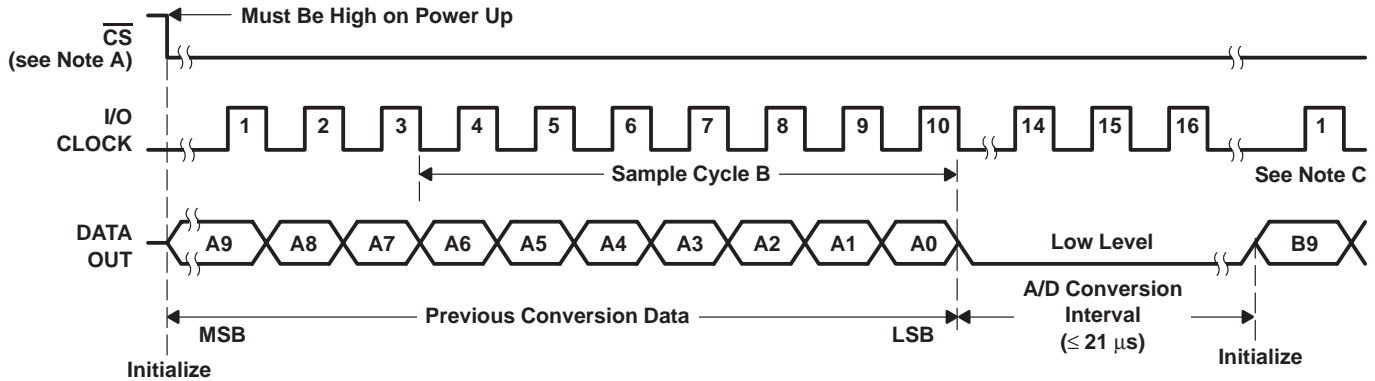


Figure 9. Timing for 16-Clock Transfer Not Using  $\overline{CS}$  (Serial Transfer Completed Within 21  $\mu s$ )

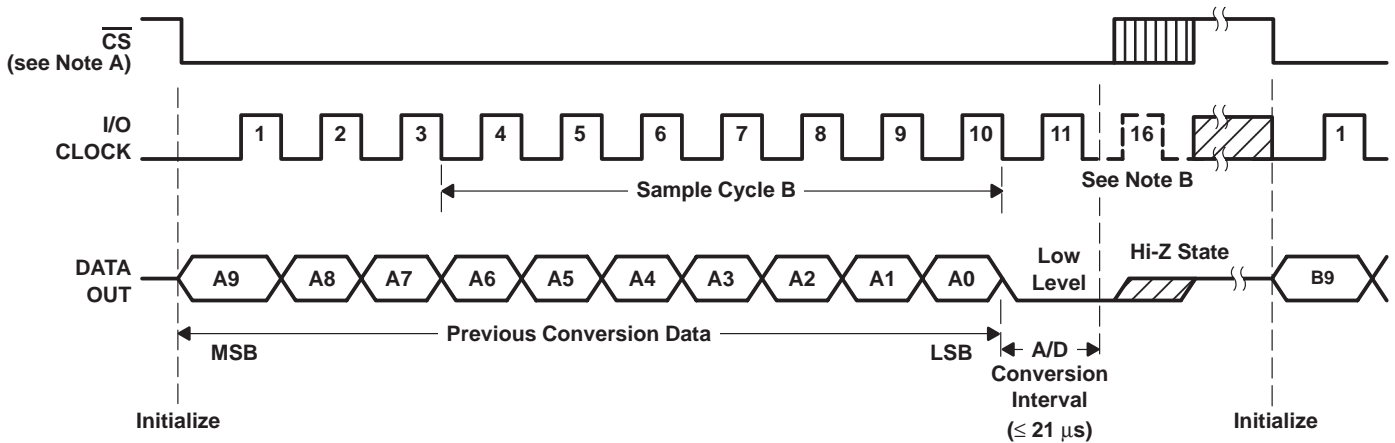


Figure 10. Timing for 11- to 16-Clock Transfer Using  $\overline{CS}$  (Serial Transfer Completed After 21  $\mu s$ )

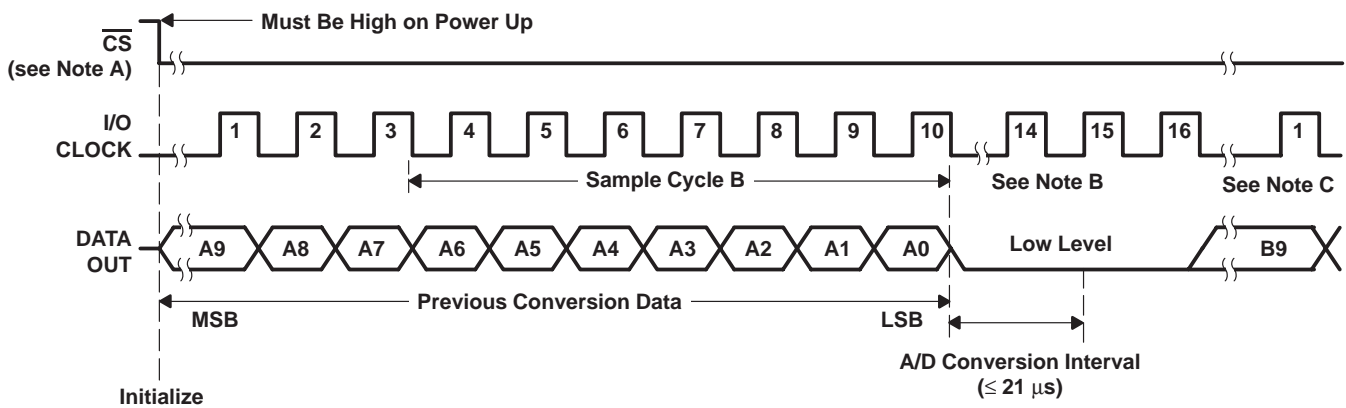
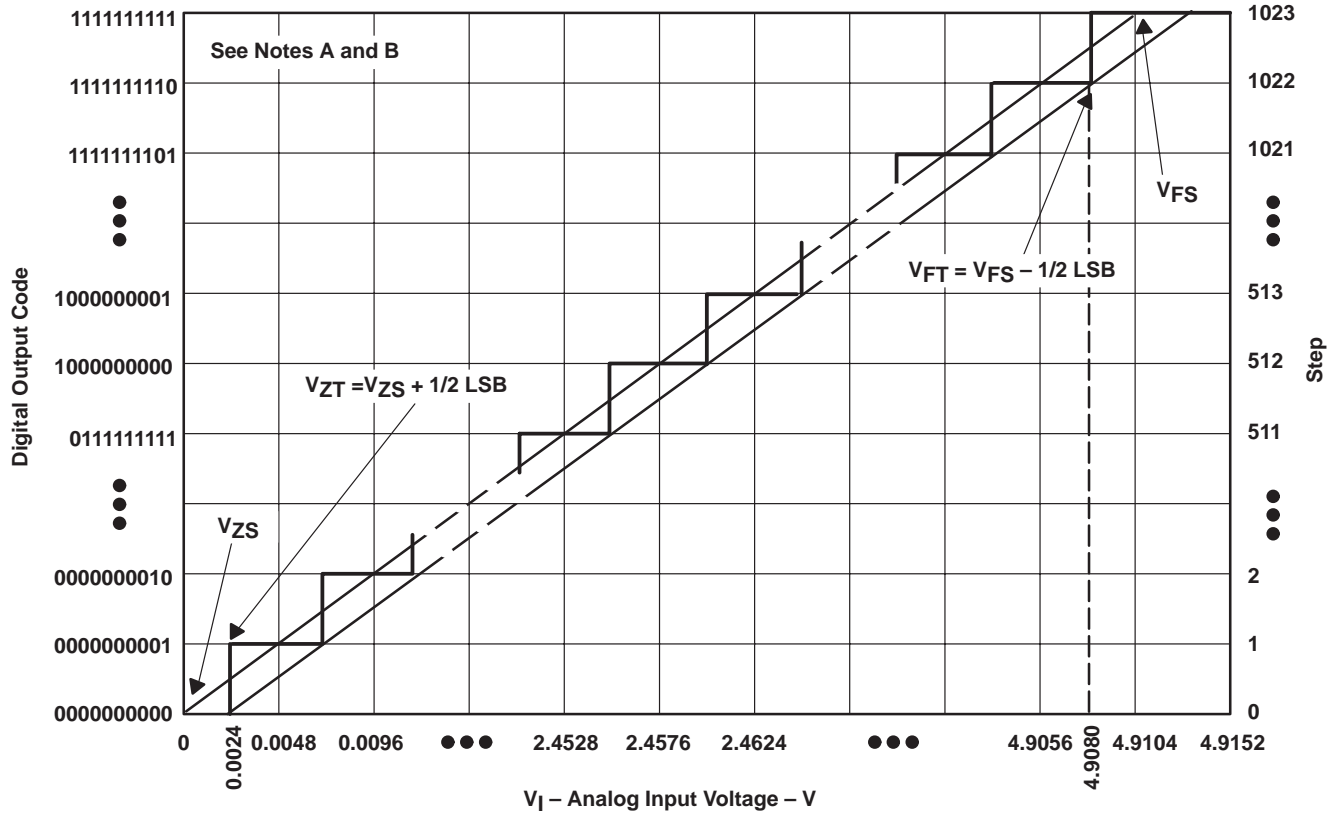


Figure 11. Timing for 16-Clock Transfer Not Using  $\overline{CS}$  (Serial Transfer Completed After 21  $\mu s$ )

- NOTES:
- A. To minimize errors caused by noise at  $\overline{CS}$ , the internal circuitry waits for a setup time plus two falling edges of the internal system clock after  $\overline{CS} \downarrow$  before responding to the I/O CLOCK. No attempt should be made to clock out the data until the minimum  $\overline{CS}$  setup time has elapsed.
  - B. A low-to-high transition of  $\overline{CS}$  disables I/O CLOCK within a maximum of a setup time plus two falling edges of the internal system clock.
  - C. The first I/O CLOCK must occur after the end of the previous conversion.

APPLICATION INFORMATION



- NOTES: A. This curve is based on the assumption that  $V_{ref+}$  and  $V_{ref-}$  have been adjusted so that the voltage at the transition from digital 0 to 1 ( $V_{ZT}$ ) is 0.0024 V and the transition to full scale ( $V_{FT}$ ) is 4.908 V. 1 LSB = 4.8 mV.  
 B. The full-scale value ( $V_{FS}$ ) is the step whose nominal midstep value has the highest absolute value. The zero-scale value ( $V_{ZS}$ ) is the step whose nominal midstep value equals zero.

Figure 12. Ideal Conversion Characteristics

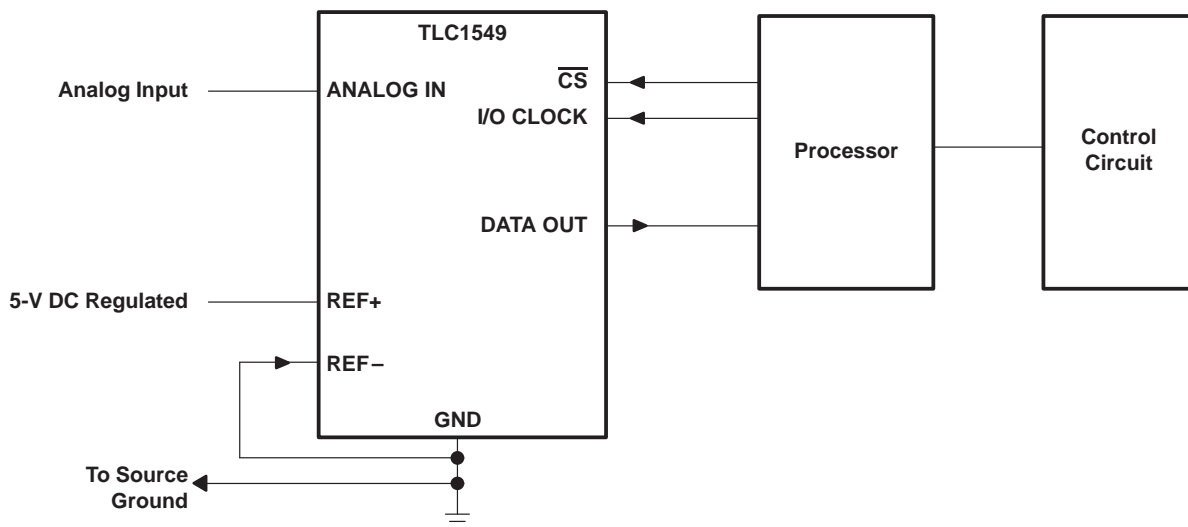


Figure 13. Typical Serial Interface

APPLICATION INFORMATION

simplified analog input analysis

Using the equivalent circuit in Figure 14, the time required to charge the analog input capacitance from 0 V to  $V_S$  within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S \left( 1 - e^{-t_c / R_t C_i} \right) \tag{1}$$

where

$$R_t = R_S + r_i$$

The final voltage to 1/2 LSB is given by

$$V_C (1/2 \text{ LSB}) = V_S - (V_S / 2048) \tag{2}$$

Equating equation 1 to equation 2 and solving for time  $t_c$  gives

$$V_S - (V_S / 2048) = V_S \left( 1 - e^{-t_c / R_t C_i} \right) \tag{3}$$

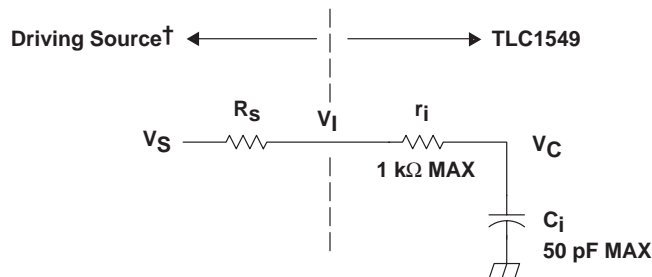
and

$$t_c (1/2 \text{ LSB}) = R_t \times C_i \times \ln(2048) \tag{4}$$

Therefore, with the values given the time for the analog input signal to settle is

$$t_c (1/2 \text{ LSB}) = (R_S + 1 \text{ k}\Omega) \times 60 \text{ pF} \times \ln(2048) \tag{5}$$

This time must be less than the converter sample time shown in the timing diagrams.



$V_I$  = Input Voltage at ANALOG IN  
 $V_S$  = External Driving Source Voltage  
 $R_S$  = Source Resistance  
 $r_i$  = Input Resistance  
 $C_i$  = Input Capacitance

† Driving source requirements:

- Noise and distortion for the source must be equivalent to the resolution of the converter.
- $R_S$  must be real at the input frequency.

Figure 14. Equivalent Input Circuit Including the Driving Source

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TLC1549CD</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C1549C
TLC1549CD.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C1549C
TLC1549CDG4	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C1549C
<a href="#">TLC1549CDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	C1549C
TLC1549CDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C1549C
<a href="#">TLC1549CP</a>	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TLC1549CP
TLC1549CP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC1549CP
<a href="#">TLC1549ID</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	C1549I
TLC1549ID.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C1549I
<a href="#">TLC1549IDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	C1549I
TLC1549IDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	C1549I
<a href="#">TLC1549IP</a>	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TLC1549IP
TLC1549IP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC1549IP
TLC1549IPE4	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	See TLC1549IP	TLC1549IP

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC1549CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC1549IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC1549CDR	SOIC	D	8	2500	350.0	350.0	43.0
TLC1549IDR	SOIC	D	8	2500	350.0	350.0	43.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLC1549CD	D	SOIC	8	75	505.46	6.76	3810	4
TLC1549CD.A	D	SOIC	8	75	505.46	6.76	3810	4
TLC1549CDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLC1549CP	P	PDIP	8	50	506	13.97	11230	4.32
TLC1549CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC1549ID	D	SOIC	8	75	505.46	6.76	3810	4
TLC1549ID.A	D	SOIC	8	75	505.46	6.76	3810	4
TLC1549IP	P	PDIP	8	50	506	13.97	11230	4.32
TLC1549IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC1549IPE4	P	PDIP	8	50	506	13.97	11230	4.32

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025