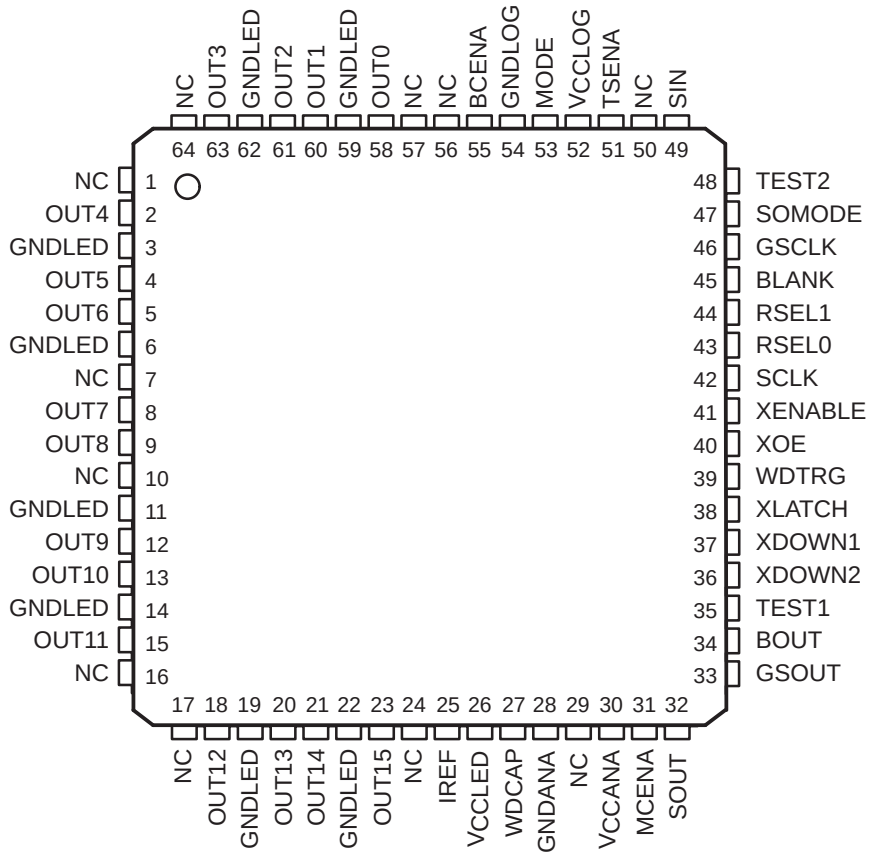
- **Drive Capability and Output Counts:**
  - **80 mA (Current Sink) × 16 Bits**
  - **120 mA (Current Sink) × 8 Bits**
- **Constant Current Output Range:**
  - **5 mA to 80 mA/10 mA to 120 mA (Selectable by MODE Terminal) (Current Value Setting for All Output Terminals Using External Resistor and Internal Brightness Control Register)**
- **Constant Current Accuracy ±4% (Maximum Error Between Bits)**
- **Voltage Applied to Constant Current Output Terminals:**
  - **Minimum 0.4 V (Output Current 5 mA to 40 mA)**
  - **Minimum 0.7 V (Output Current 40 mA to 80 mA)**
- **256 Gray Scale Display:**
  - **Pulse Width Control 256 Steps**
- **Brightness Adjustment:**
  - **Output Current Adjustment for 32 Steps (Adjustment for Brightness Deviation Between LED Modules)**
  - **8 Steps Brightness Control by 8 Times Speed Gray Scale Control Clock (Brightness Adjustment for Panel)**
- **Error Output Signal Check:**
  - **Check Error Output Signal Line Such as Protection Circuit When Operating**
- **Data Output Timing Selectable:**
  - **Select Data Output Timing for Shift Register Relative to Clock**
- **OVM (Output Voltage Monitor):**
  - **Monitor Voltage on Constant Current Output Terminals (Detect LED Disconnection and Short Circuit)**
- **WDT (Watchdog Timer):**
  - **Turn Output Off When Scan Signal Stopped**
- **TSD (Thermal Shut Down):**
  - **Turn Output Off When Junction Temperature Exceeds Limit**
- **Data Input:**
  - **Clock Synchronized 1 Bit Serial Input (Shmitt-Triggered Input)**
- **Data Output:**
  - **Clock Synchronized 1 Bit Serial Output (3-State Output)**
- **Input Signal Level:**
  - **CMOS Level**
- **Power Supply Voltage . . . 4.5 V to 5.5 V**
- **Maximum Output Voltage . . . 17 V**
- **Data Transfer Rate . . . 15 MHz (Max**
- **Gray Scale Clock Frequency . . . 8 MHz (Max)**
- **Operating Free-Air Temperature Range –20°C to 85°C**
- **64-Pin HTQFP Package (P_D = 4.9 W, T_A = 25°C)**

description

The TLC5905 is a constant current driver that incorporates shift register, data latch, constant current circuitry with a current value adjustable and 256 gray scale display that uses pulse width control. The output current can be selected as maximum 80 mA with 16 bits or 120 mA with 8 bit. The current value of the constant current output is set by one external resistor. After this device is mounted on a printed-circuit board (PCB), the brightness deviation between LED modules (ICs) can be adjusted using an external data input, and the brightness control for the panel can be accomplished by the brightness adjustment circuitry. Also, the device incorporates the output voltage monitor (OVM) used for LED open detection (LOD) by monitoring constant current output. Moreover, the device incorporates watchdog timer (WDT) circuitry, which turns constant current output off when the scan signal stops during dynamic scanning operation, and thermal shutdown (TSD) circuitry, which turns constant current output off when the junction temperature exceeds the limit.

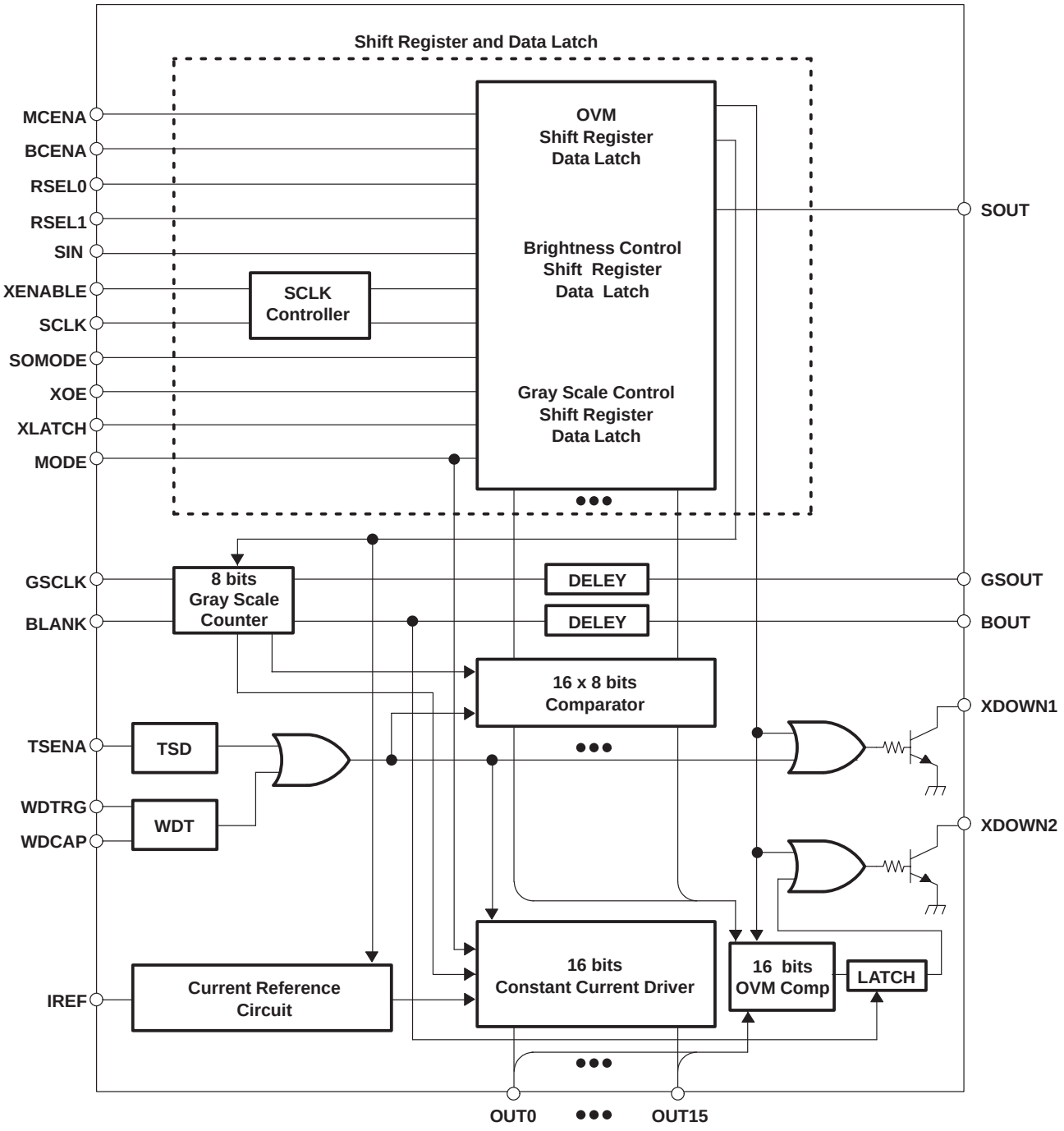
pin assignments

PAP PACKAGE
(TOP VIEW)



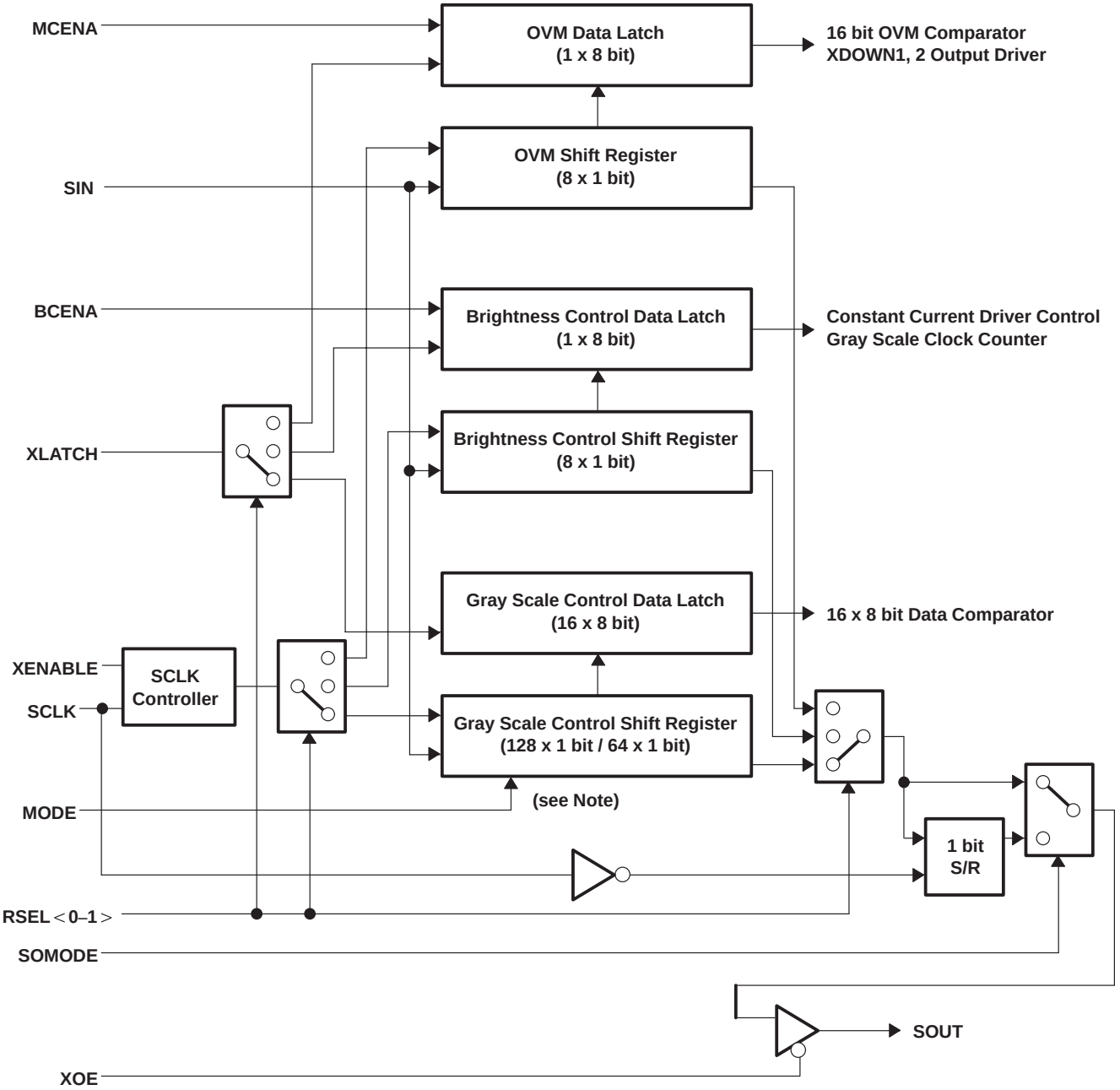
NC – No internal connection

functional block diagram



NOTE: All the input terminals are with Schmitt-triggered inverter except IREF and WDCAP.

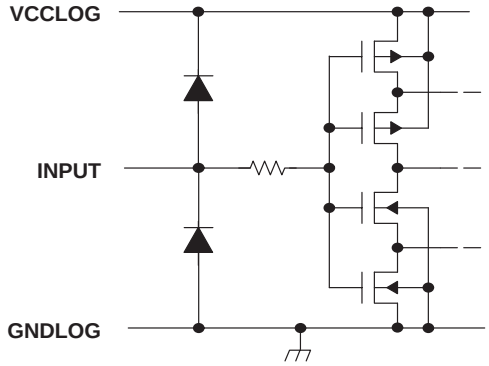
functional block diagram for shift register and data latch



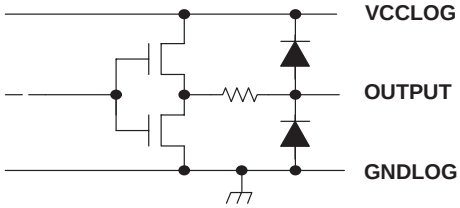
NOTE: Enclosed in ( ) is dependent on MODE pin selection.

equivalent input and output schematic diagrams

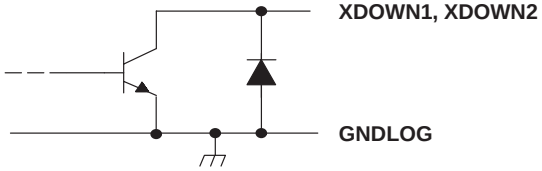
Input



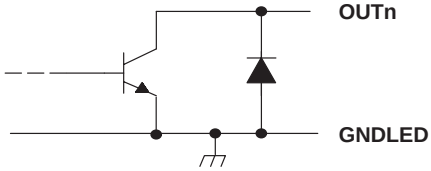
SOUT, GSOUT, BOUT



XDOWN1, XDOWN2



OUTn



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BCENA	55	I	Brightness control enable. When BCENA is low, the brightness control latch is set to the default value. The output current value in this status is 100% of the value set by an external resistor. The frequency division ratio of GSCLK is1/1. When BCENA is high, writing to brightness control latch is enabled.
BLANK	45	I	Blank(Light off). When BLANK is high, all the output of the constant current driver is turned off. The constant current output is turned on (LED on) when synchronized to the falling edge of GCLK after next rising edge of GCLK when BLANK goes from high to low.
BOUT	34	O	Blank signal delay. BOUT is an output with the addition of delay time to BLANK.
GSCLK	46	I	Clock input for gray scale. The gray scale display is accomplished by lighting the LED on until the number of GSCLK counted is equal to data latched.
GNDANA	28		Analog ground (internally connected to GNDLOG and GNDLED)
GNDLED	3,6,11,14, 19,22,59,62		LED driver ground (internally connected to GNDANA and GNDLOG)
GNDLOG	54		Logic ground (internally connected to GNDANA and GNDLED)
GSOUT	33	O	Clock delay for gray scale. GSOUT is an output with the addition of delay time to GSCLK.
IREF	25	I/O	Constant current value setting. LED current is set to the desired value by connecting an external resistor between IREF and GND. The 37 times current is compared to current across the external resistor sink on the output terminal.
MCENA	31	I	OVM enable. When MCENA is low, the OVM latch is set to the default value. The comparison voltage in this status is 0.3 V. When MCENA is high, writing to OVM latch is enabled.
MODE	53	I	8/16 bits select. When MODE is high, the 16 bits output is selected. When MODE is low, the 8 bits output is selected.
NC	1,7,10,16,17,24, 29,50,56,57,64		No internal connection
OUT0 – OUT15	58,60,61,63, 2,4,5,8,9,12,13 15,18,20,21,23	O	Constant current output
RSEL0 RSEL1	43 44	I	Shift register data latch switching. When RSEL1 is low and RESL0 is low, gray scale data shift register latch is selected. When RSEL1 is low and RESL0 is high, the brightness control register latch is selected. When RSEL1 is high and RSEL0 is low, the OVM register latch is selected. When RSEL1 is high and RSEL0 high, no register latch is selected.
SCLK	42	I	Clock input for data transfer. The input data is from SIN. All data on the shift register selected by RSEL0 and RSEL1, and output data at SOUT are sifted by 1 bit synchronizing to SCLK. The data except the SOUT is synchronized to the rising edge. The edge for data from SOUT is determined by the level of SOMODE.
SIN	49	I	Input for 1 bit serial data. These terminals are inputs for shift register for gray scale data, brightness control and OVM. The register selected is determined by RSEL0, 1.
SOMODE	47	I	Timing select for data output. When SOMODE is low, SOUT is changed by synchronizing to the rising edge of SCLK. When SOMODE is high, SOUT is changed by synchronizing to the falling edge of SCLK.
SOUT	32	O	Output for 1 bit serial data with 3–state. These terminals are outputs for shift register for gray scale data, brightness control and OVM. The register selected is determined by RSEL0, 1.
TEST1 TEST2	35 48	I	TEST. Factory test terminal. TEST1 and TEST2 should be connected to GND for normal operation.
THERMAL PAD	package bottom		Heat sink pad. This pad is connected to the lowest potential IC or thermal layer.
TSENA	51	I	TSD (thermal shutdown) enable. When TSENA is high, TSD is enabled. When TSENA is low, TSD is disabled.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
V_{CCANA}	30		Analog power supply voltage
V_{CCLOG}	52		Logic power supply voltage
V_{CCLED}	26		LED driver power supply voltage
WDCAP	27	I	WDT (watchdog timer) detection time adjustment. WDT detection time is adjusted by connecting a capacitor between WDCAP and GND. When WDCAP is directly connected to GND, the WDT function is disabled. In this case, WDTRG should be tied to a high or low level.
WDTRG	39	I	WDT (watchdog timer) trigger input. By applying a scan signal to this terminal, the scan signal can be monitored by turning the constant current output off and protecting the LED from damage by burning when the scan signal is stopped during constant period designed.
XDOWN1	37	O	Shutdown. XDOWN1 is configured as an open collector. It goes low when constant current output is shut down by the WDT or TSD function.
XDOWN2	36	O	OVM comparator output. XDOWN2 is configured as open collector. It monitors terminal voltage when constant current output is turned on. XDOWN2 goes low when this voltage is lower than the level selected by the OVM latch. When BLANK is set high, the previous level is held.
XENABLE	41	I	SCLK enable. When XENABLE is low, data transfer is enabled. Data transfer starts on the rising edge of SCLK after XENABLE goes low. During XENABLE high, no data is transferred.
XLATCH	38	I	Latch. When XLATCH is high, data on shift register goes through latch. When XLATCH is low, data is latched. Accordingly, if data on shift register is changed during XLATCH high, this new value is latched (level latch).
XOE	40	I	Data output enable. When XOE is low, the SOUT terminal is drived. When XOE is high, the SOUT terminal goes to high-impedance state.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Logic supply voltage, $V_{CC(LOG)}$ . . . . . – 0.3 V to 7 V
Supply voltage for constant current circuit, $V_{CC(LED)}$ . . . . . – 0.3 V to 7 V
Analog supply voltage, $V_{CC(ANA)}$ . . . . . – 0.3 V to 7 V
Output current (DC), $I_{OL(C)}$ . . . . . 90 mA
Input voltage range, V_I . . . . . – 0.3 V to $V_{CC(LOG)}$ + 0.3 V
Output voltage range, $V_{(SOUT)}$, $V_{(BOUT)}$ and $V_{(GSOUT)}$ . . . . . – 0.3 V to $V_{CC(LOG)}$ + 0.3 V
Output voltage range, $V_{(OUTn)}$ and $V_{(XDOWNn)}$ . . . . . – 0.3 V to 18 V
Storage temperature range, T_{stg} . . . . . –40°C to 125°C
Continuous total power dissipation at (or below) T_A = 25°C . . . . . 4.9 W
Power dissipation rating at (or above) T_A = 25°C . . . . . 39.4 mW/°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GNDLOG terminal.

recommended operating conditions

dc characteristics

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Logic supply voltage, $V_{CC(LOG)}$		4.5	5	5.5	V
Supply voltage for constant current circuit, $V_{CC(LED)}$		4.5	5	5.5	V
Analog power supply, $V_{CC(ANA)}$		4.5	5	5.5	V
Voltage between V_{CC}, $V_{(DIFF1)}$	$V_{(DIFF1)} = V_{CC(LOG)} - V_{CC(ANA)}$ $V_{CC(LOG)} - V_{CC(LED)}$, $V_{CC(ANA)} - V_{CC(LED)}$	– 0.3	0	0.3	V
Voltage between GND, $V_{(DIFF2)}$	$V_{(DIFF2)}$ = GNDLOG – GND(ANA) GND(LOG) – GND(LED), GND(ANA) – GND(LED)	– 0.3	0	0.3	V
Voltage applied to constant current output, $V_{(OUTn)}$	OUT0 to OUT15 off			17	V
High-level input voltage, V_{IH}		0.8 $V_{CC(LOG)}$		$V_{CC(LOG)}$	V
Low-level input voltage, V_{IL}		GNDLOG		0.2 $V_{CC(LOG)}$	V
High-level output current, I_{OH}	$V_{CC(LOG)}$ = 4.5V, SOUT, BOUT, GSOUT			– 1.0	mA
Low-level output current, I_{OL}	$V_{CC(LOG)}$ = 4.5V, SOUT, BOUT, GSOUT			1.0	mA
	$V_{CC(LOG)}$ = 4.5V, XDOWN1, XDOWN2			5	mA
Constant output current, $I_{OL(C)}$	OUT0 to OUT15	5		80	mA
Operating free–air temperature range, T_A		– 20		85	°C

ac characteristics, $V_{CC(LOG)} = V_{CC(ANA)} = V_{CC(LED)}$ = 4.5 V to 5.5 V, T_A = – 20 to 85°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCLK clock frequency, $f_{(SCLK)}$	At single operation			15	MHz
	At cascade operation (SOMODE = L)			10	MHz
SCLK pulse duration (high or low level), $t_{w(h)}/t_{w(l)}$		20			ns
GSCLK clock frequency, $f_{(GSCLK)}$	Frequency division ratio 1/1			8	MHz
	No GSOUT operation (see Note 2)			20	MHz
GSCLK pulse duration (high or low level), $t_{w(h)}/t_{w(l)}$	Frequency division ratio 1/1	40			ns
	No GSOUT operation (see Note 2)	20			ns
WDTRG clock frequency, $f_{(WDT)}$				8	MHz
WDTRG pulse duration (high or low level), $t_{w(h)}/t_{w(l)}$		40			ns
XLATCH pulse duration (high), $t_{w(h)}$		50			ns
Rise/fall time, t_r/t_f				100	ns
Setup time, t_{su}	SIN – SCLK	10			ns
	BLANK – GSCLK	20			ns
	XENABLE – SCLK	15			ns
	XLATCH – SCLK	15			ns
	XLATCH – GSCLK	10			ns
	RSEL – SCLK	10			ns
	RSEL – XLATCH	20			ns
Hold time, t_h	SIN – SCLK	10			ns
	XENABLE – SCLK	20			ns
	XLATCH – SCLK	30			ns
	RSEL – SCLK	20			ns
	RSEL – XLATCH	20			ns

NOTE 2: When GSCLK is operated with >8 MHz, GSOUT operation can not be assured.

electrical characteristics,
MIN/MAX: $V_{CC(LOG)}$ = $V_{CC(ANA)}$ = $V_{CC(LED)}$ = 4.5 V to 5.5 V, T_A = –20 to 85°C
TYP: $V_{CC(LOG)}$ = $V_{CC(ANA)}$ = $V_{CC(LED)}$ = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA, SOUT, GSOUT, BOUT	$V_{CC(LOG)}$ –0.5			V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA, SOUT, GSOUT, BOUT			0.5	V
		I_{OL} = 5 mA, XDOWN1, XDOWN2			0.5	
I_I	Input current	V_I = $V_{CC(LOG)}$ or GND(LOG)			±1	µA
$I_{(LOG)}$	Supply current (logic)	Input signal is static, TSENA = H, WDCAP = OPEN			1	mA
		Data transfer, SCLK = 15 MHz, GSCLK = 8 MHz		18	30	mA
$I_{(ANA)}$	Supply current (analog)	LED turnon, $R_{(IREF)}$ = 590 Ω		3	5	mA
		LED turnoff, $R_{(IREF)}$ = 590 Ω		3	5	
$I_{(LED)}$	Supply current (constant current driver)	LED turnoff, $R_{(IREF)}$ = 1180 Ω		15	20	mA
		LED turnoff, $R_{(IREF)}$ =590 Ω		30	40	
		V_O = 1 V, $R_{(IREF)}$ = 1180 Ω All output bits turn on		25	35	
		V_O = 1 V, $R_{(IREF)}$ = 590 Ω All output bits turn on		50	70	
$I_{O(LC1)}$	Constant output current	V_O = 1 V, $V_{(IREF)}$ = 1.24 V, $R_{(IREF)}$ = 1180 Ω	35	40	45	mA
$I_{O(LC2)}$	Constant output current	V_O = 1, $V_{(IREF)}$ = 1.24V, $R_{(IREF)}$ = 590 Ω	70	80	90	mA
$I_{O(LK)}$	Constant output leakage current	OUT0 to OUT15 ($V_{(OUTn)}$ = 15 V)			0.1	µA
		XDOWN1,2 ($V_{(XDOWNn)}$ = 15 V)			1	µA
		SOUT (V_{OUTn} = $V_{CC(LOG)}$ or GND)			1	µA
$\Delta I_{O(LC)}$	Constant output current error between bits	$V_{CC(LOG)}$ = $V_{CC(ANA)}$ = $V_{CC(LED)}$ = 5 V, V_O = 1V, $R_{(IREF)}$ = 590 Ω, All output bits turnon		±1%	±4%	
$I_{\Delta O(LC1)}$	Changes in constant output current depend on supply voltage	V_O = 1 V, $R_{(IREF)}$ = 1180 Ω, $V_{(IREF)}$ = 1.24 V, 1 bit output turnon		±1%	±4%	%/V
$I_{\Delta O(LC2)}$	Changes in constant output current depend on output voltage	V_O= 1 V to 3 V, $R_{(IREF)}$ = 1180 Ω, $V_{(IREF)}$ = 1.24 V, 1 bit output turnon		±1%	±2%	%/V
$T_{(tsd)}$	TSD detection temperature	Junction temperature	150	160	170	°C
$T_{(wdt)}$	WDT detection temperature	No external capacitor	5	10	15	ms
$V_{(IREF)}$	Voltage reference	BCENA = L, $R_{(IREF)}$ = 590 Ω		1.24		V

switching characteristics, C_L = 15pF, MIN/MAX: $V_{CC(LOG)}$= $V_{CC(ANA)}$ = $V_{CC(LED)}$ = 4.5 V to 5.5 V, T_A = –20 to 85°C TYP: $V_{CC(LOG)}$ = $V_{CC(ANA)}$ = $V_{CC(LED)}$ = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	SOUT		12	30	ns
		GSOUT, BOUT		13	30	
		OUTn (see Figure 1)		250		
t_f	Fall time	SOUT		8	20	ns
		GSOUT, BOUT		10	25	
		OUTn (see Figure 1)		200		
t_d	Propagation delay time	OUTn+1 – OUTn		35	60	ns
		BLANK↑ – OUT0		350	500	
		BLANK – BOUT	20	40	70	
		GSCLK↓ – OUT0		350	500	
		GSCLK – GSOUT	20	40	70	
		SCLK – SOUT	15	30	50	
		XOE↓ – SOUT (see Note 3)	10	20	35	
		XOE↑ – SOUT (see Note 3)	10	15	25	
		GSCLK – XDOWN2			5000	

NOTE 3: Until SOUT will be turned on (drive) or turned off (Hi–Z).

PARAMETER MEASUREMENT INFORMATION

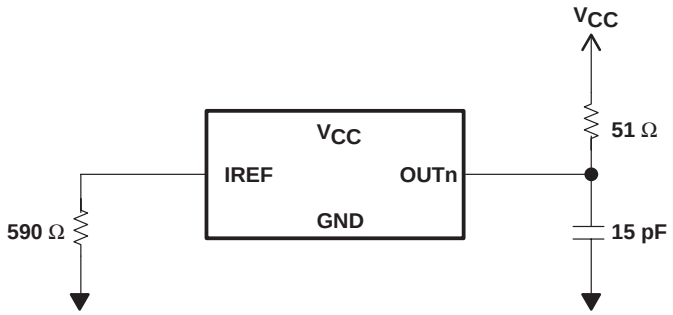


Figure 1. Rise Time and Fall Time Test Circuit for OUTn

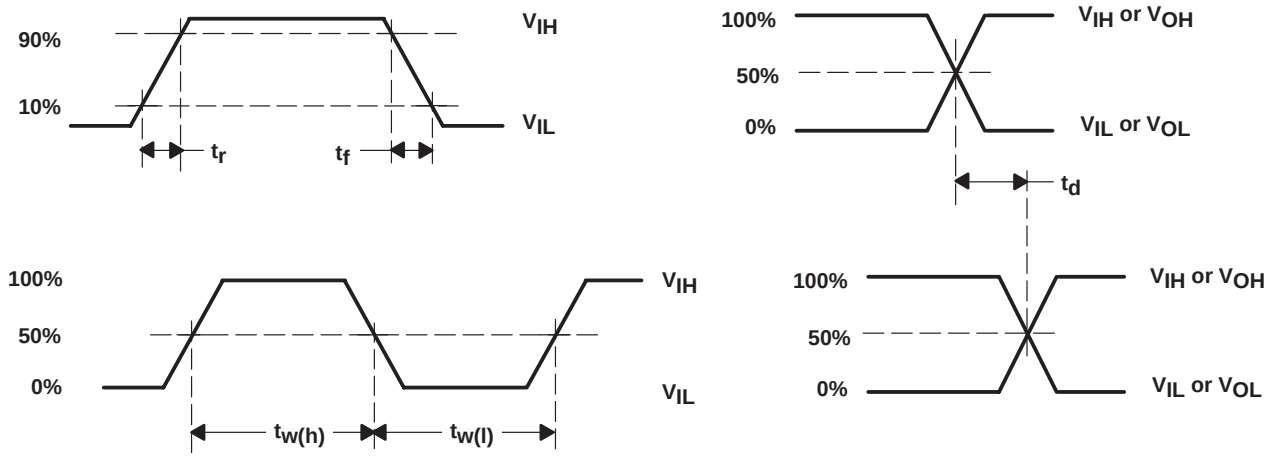


Figure 2. Timing Requirements

PRINCIPLES OF OPERATION

constant current output selection by user (80 mA x16 bits or 120 mA x 8 bits)

When the MODE terminal is set to high, output is selected as 80 mA x 16 bits. When the MODE terminal is set to low, output is selected as 120 mA x 8 bits. By this setting, the shift register latch for gray scale data is changed to the configuration corresponding to the bit selected. Note that two constant output terminals should be tied to LED such as OUT0-to-OUT1 and OUT2-to-OUT3 because they operate in pairs when the 8-bit output mode is selected. Also, in this case, the current value on constant current output is the same as in 16-bit output mode. Therefore, when output current of 120 mA is desired, the resister connected to the IREF terminal should be set to the same value as the output current of 60 mA.

Table 1. Operation Mode Selection

MODE	OUTPUT
H	80 mA × 16 bits
L	120 mA × 8 bits

On the constant current output terminals (OUT0–15), approximately 37 times the current that flows through external resistor, R_{IREF} (connected between IREF and GND), can flow. The external resistor value is calculated using the following equation.

$R_{(IREF)}\ (\Omega) \cong 37 \times 1.24\ (V) / I_{OL(C)}(A)$ where BCENA is low.

Note that more current flows if IREF is connected directly to GND.

constant output current operation

The constant current output turns on (sink constant current), if all the gray scale data latched into the gray scale latch is not zero on the falling edge of the gray scale clock after the next rising edge of the gray scale clock when BLANK goes from high to low. After that, the number of the falling edge is counted by the 8-bit gray scale counter. Then, output counted corresponding to the gray scale data is turned off (stop to sink constant current). If the shift register for gray scale is updated during XLATCH high, data on the gray scale data latch is also updated affecting the number of the gray scale of constant current output. Accordingly, during on-state of constant current output, XLATCH should be kept at a low level and the gray scale data latch should be held. If there are constant current output terminals unconnected (includes LED disconnection), the LED should be turned on after writing zero to the gray scale data latch corresponding to the output unconnected. Unless this action is taken, supply current on the constant current driver will increase resulting in influencing the current value for the constant current output when turned on.

shift register latch

The device provides three kinds of shift register latchs including the gray scale data, brightness control, and OVM. To write data into the shift register, SCLK and SIN are utilized. The selection of the shift register will be done by RSEL0 and RSEL1 as shown in Table 2. Note that RSEL0 and RSEL1 should be changed when both SCLK and XLATCH are low.

Table 2. Shift Register Latch Selection

RSEL0	RSEL1	SHIFT REGISTER LATCH SELECTED
L	L	Shift register latch for gray scale data
L	H	Shift register latch for brightness control
H	L	Shift register latch for OVM
H	H	N/A (SOUT is tied to low level)

PRINCIPLES OF OPERATION

shift register latch for gray scale data

The shift register latch for gray scale data is set as a 64 x 1 bit configuration in the 8-bit mode, and as a 128 x 1 bit configuration in the 16-bit mode. The gray scale data, configured as 8 bits, represents the time when constant current output is being turned on, and the data range is 0 to 255 (00h to FFh). When the gray scale data is 0, the time is shortest, and the output is not turned on(light off). On the other hand, when the gray scale data is 255, the time is longest, and it turns on during time of 255 clocks from GSCLK. The configuration of shift register and latch for gray scale data is shown in Figure 3.

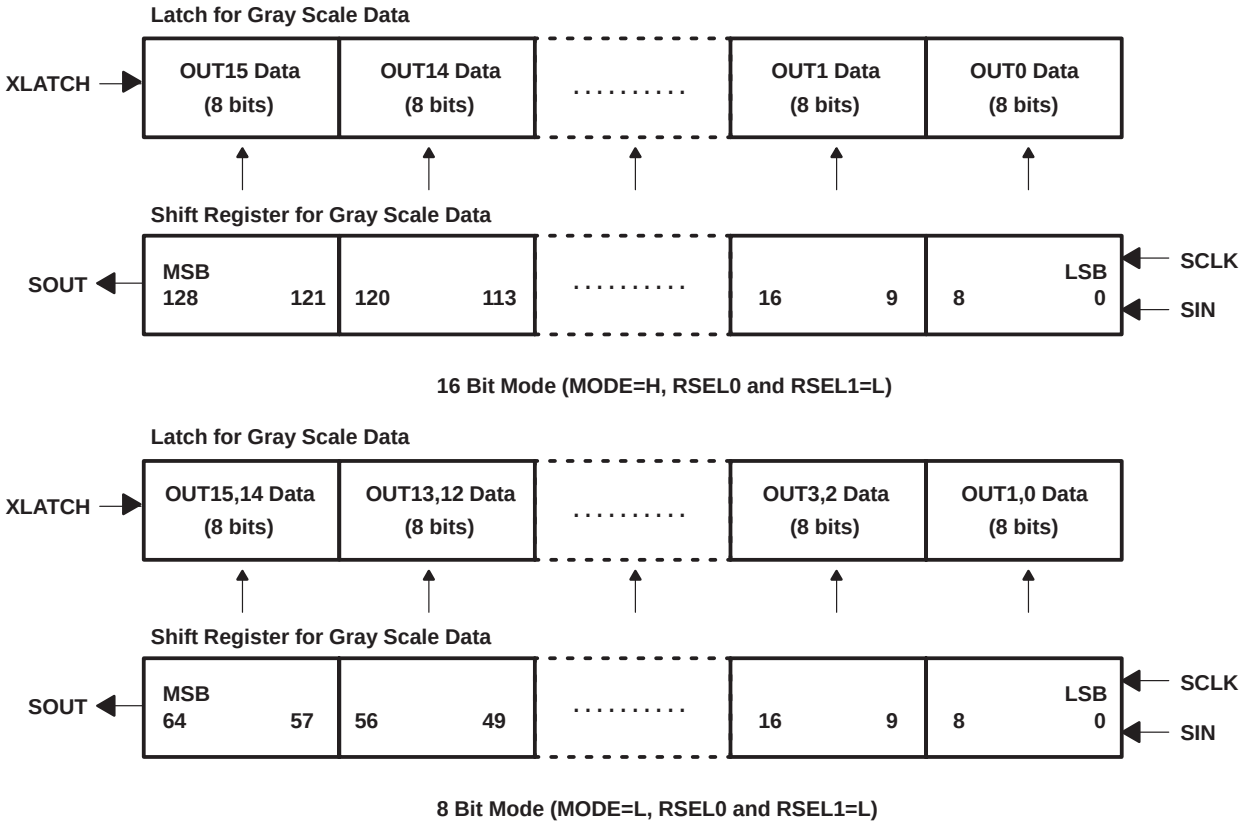
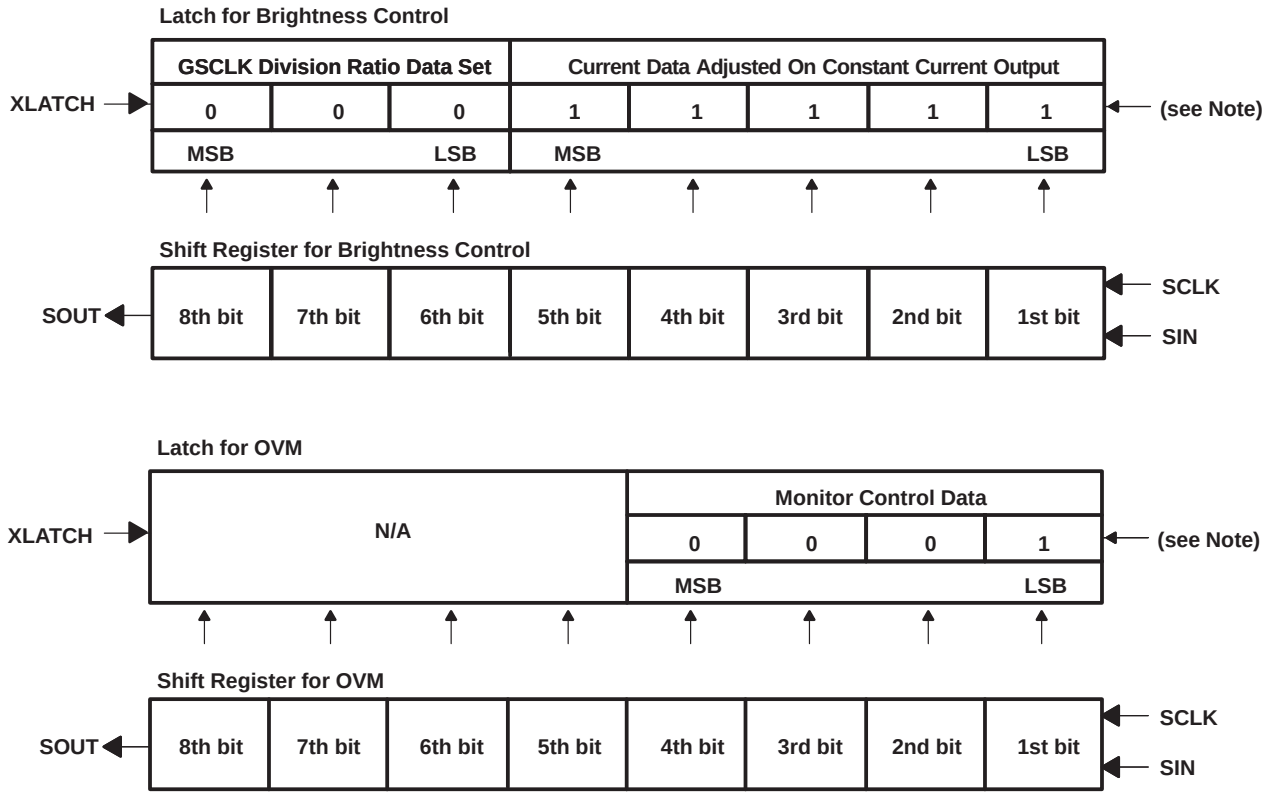


Figure 3. Relationship Between Shift Register and Latch for Gray Scale Data

PRINCIPLES OF OPERATION

shift register latch for brightness control and OVM

The shift register latch for both the brightness control and OVM (output voltage monitor) is configured with a 1 x 1 byte. In the shift register latch for brightness control, the division ratio of GSCLK can be set and the output current value on constant current output can be adjusted. In the shift register latch for OVM, the comparison voltage at the OVM comparator on constant current output terminals (OUT0 to OUT15) can be set and the output signal for both XDOWN1 and XDOWN2 can be forced to a low level. When powered up, the latch data is indeterminate and shift register is not initialized. When these functions are used, data should be written to the shift register latch prior to turning the constant current output on (BLANK=L). Also, it is inhibited from rewriting the latch value for brightness control when the constant current output is turned on. When these functions are not used, latch value can be set to the default value setting of BCENA or MCENA or to low level (tied to GND). The configuration of the shift register and latch for brightness control and monitor control is shown in Figure 4.



NOTE: Indicates default value at BCENA low if brightness control latch, at MCENA low if OVM latch.

Figure 4. Relationship Between Shift Register and Latch for Brightness Control and OVM

write data to shift register latch

The shift register latch written is selected using the RSEL0 and RSEL1 terminal. The data is applied to the SIN data input terminal and clocked into the shift register synchronizing to the rising edge of SCLK after XENABLE is pulled low. The shift register for gray scale data is 64 bit length in the 8 bit mode resulting in 64 times of SCLK, and 128 bit length in the16 bit mode resulting in 128 times of SCLK. Brigtness control and monitor control results in eight times the SCLK input. At number of SCLK input for each case, data can be written into the shift register. In this condition, when XLATCH is pulled high, data in the shift register is clocked into latch (data through), and when XLATCH is pulled low, data is held (latch).

PRINCIPLES OF OPERATION

brightness control function

By writing data into the brightness control latch, current on all constant current outputs can be adjusted to control the variation of brightness between ICs and the division ratio for the gray scale clock can be set to control the variation of brightness for the total panel system.

output current adjustment on all constant current outputs – brightness adjustment between ICs

By using the lower 5 bits of the brightness control latch, output current can be adjusted to 32 steps as 1 step of 1.6% current ratio between 100% and 51.6% when the output current is set to 100% of an external resistor. By using this function, the brightness control between modules (ICs) can be adjusted, sending the desired data externally even if ICs are mounted on a print-circuit board. When BCENA is pulled low, the output current is set to 100%.

Table 3. Relative Current Ratio For Total Constant Current Output

CODE	CURRENT RATIO%	20 (mA)	80 (mA)	V_{IREF} (TYP)
MSB 00000 LSB	51.6	10.3	41.3	0.63
. . . .	. . . .	. . . .	. . . .	. . . .
11110	98.4	19.3	78.7	1.22
11111†	100	20.0	80.0	1.24

† BCENA is low.

frequency division ratio setting for gray scale clock – panel brightness adjustment

By using the upper 3 bits of the brightness control latch, the gray scale clock can be divided into 1/1 to 1/8. If the gray scale clock is set to 8 times the speed ($256 \times 8 = 2048$) of frequency during horizontal scanning time, the brightness can be adjusted to 8 steps by selecting the frequency division ratio. Therefore, the total panel brightness can be adjusted at once, and applied to the brightness of day or night. When BCENA is pulled low, the gray scale clock is not divided. When BCENA is pulled high, the brightness can be adjusted as shown in Table 4.

Table 4. Relative Brightness Ratio For Total Constant Current Output

CODE	FREQUENCY DIVISION RATIO	RELATIVE BRIGHTNESS RATIO (%)
MSB 000 LSB†	1/1	12.5
. . . .	. . . .	. . . .
110	1/7	87.5
111	1/8	100

† BCENA is low.

OVM (output voltage monitor) function

By writing data into the OVM latch, the comparison voltage for voltage comparator of OUT0 to OUT15 can be set and the output signal for XDOWN1 and XDOWN2 can be checked.

PRINCIPLES OF OPERATION

OVM (output voltage monitor) function (continued)

OVM comparator

The OVM comparator compares the voltage on the constant current output terminal during turnon with comparison voltage set by the OVM latch. When the voltage on the constant current output terminal is lower, XDOWN2 goes low. As shown in Figure 5, the comparator is provided in every output portion, and the comparison result corresponding to the output to be turned on appears in the XDOWN2 terminal. Since the XDOWN2 terminal is an open-collector output, outputs of multiple ICs are brought together.

The output terminal for comparison result is XDOWN2 only. The voltage on all the constant current output can be checked to monitor XDOWN2, turning output on in turn. The voltage on the constant current output, when turned on, can also be measured, resulting in a change to the comparison voltage set by the OVM latch. Using this function, the sensing (LOD function) LED disconnection (output voltage is below 0.3 V) and short circuit (output voltage is extremely high) can be detected and specifies which LED has encountered this failure. Also, by monitoring the output voltage and controlling the voltage across anode of the LED to minimize the voltage on the constant current output (approximately 0.7 V at I_O = 80 mA), the rising temperature of the chip can be minimized. Furthermore, by setting BLANK to low during LED on, the previous comparison result can be held. Thus, synchronizing timing to check XDOWN2 from the system to the LED lighting timing is not required. Note that the gray scale data being turned on should be a minimum of 5 μs since the XDOWN2 output is required approximately 5 μs after the constant current output is turned on. The comparison result is also required approximately 5 μs after latch data is changed.

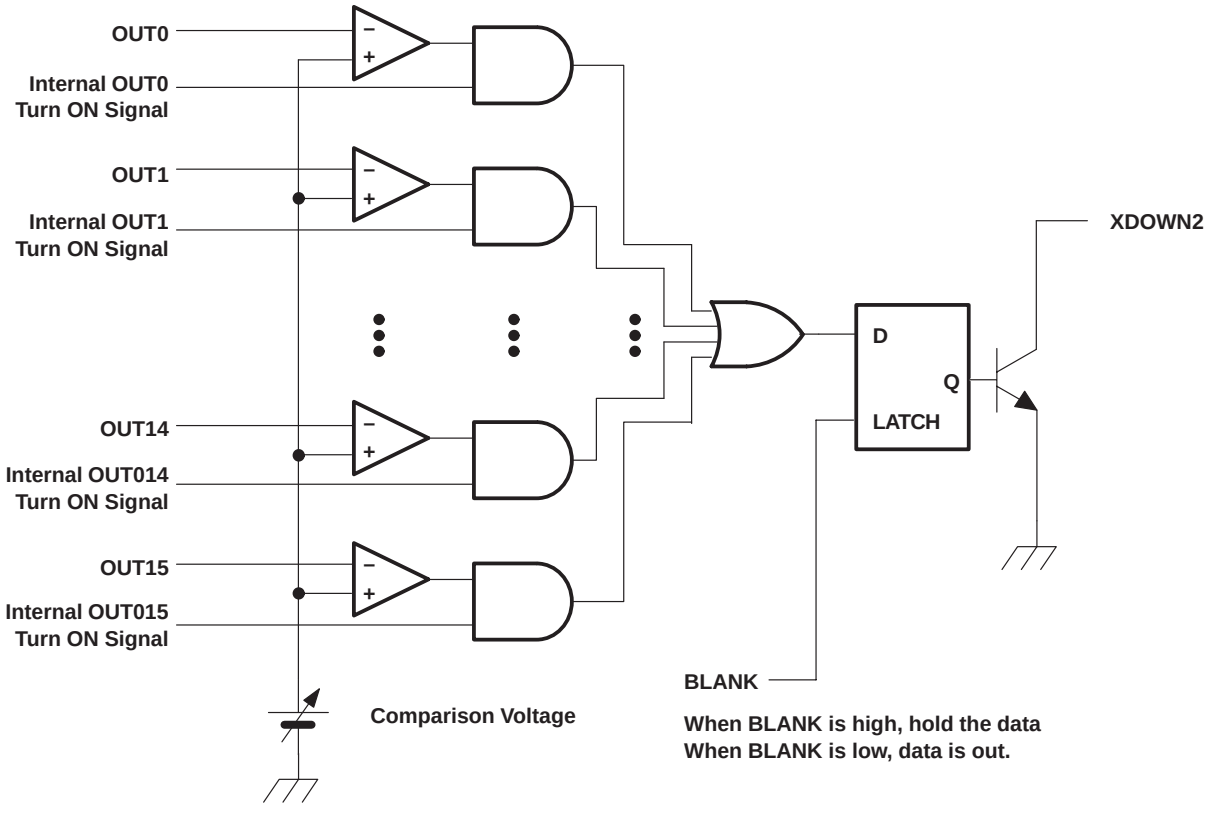


Figure 5. OVM Functional Diagram

PRINCIPLES OF OPERATION

OVM (output voltage monitor) function (continued)

output signal check for XDOWN1, XDOWN2

XDOWN1 or XDOWN2 can be forced to a low level by setting the appropriate latch value for OVM. This allows investigation of the correct connection of XDOWN1 or XDOWN2 to the external system. Since both XDOWN1 and XDOWN2 terminal are open-collector outputs, outputs of multiple ICs are brought together.

OVM comparator setting

Setting the OVM latch is shown in Table 5. Note that the comparison voltage is set to the default value of 0.3 V when MCENA tied to a low level.

Table 5. OVM Setting

MONITOR CONTROL DATA	COMPARISON VOLTAGE	XDOWN1	XDOWN2
MSB LSB			
0000	NO COMPARISON	DEPEND ON TSD/WDT	HI–Z
0001†	0.3 V	DEPEND ON TSD/WDT	DEPEND ON OVM COMPARATOR
0010	0.4 V	DEPEND ON TSD/WDT	DEPEND ON OVM COMPARATOR
0011	0.5 V	DEPEND ON TSD/WDT	DEPEND ON OVM COMPARATOR
0100	0.6 V	DEPEND ON TSD/WDT	DEPEND ON OVM COMPARATOR
0101	0.7 V	DEPEND ON TSD/WDT	DEPEND ON OVM COMPARATOR
0110	0.8 V	DEPEND ON TSD/WDT	DEPEND ON OVM COMPARATOR
0111	0.9 V	DEPEND ON TSD/WDT	DEPEND ON OVM COMPARATOR
1000	1.0 V	DEPEND ON TSD/WDT	DEPEND ON OVM COMPARATOR
1001	1.1 V	DEPEND ON TSD/WDT	DEPEND ON OVM COMPARATOR
1010	1.2 V	DEPEND ON TSD/WDT	DEPEND ON OVM COMPARATOR
1011	$1/3 \times V_{CC(ANA)}$	DEPEND ON TSD/WDT	DEPEND ON OVM COMPARATOR
1100	$1/2 \times V_{CC(ANA)}$	DEPEND ON TSD/WDT	DEPEND ON OVM COMPARATOR
1101	$2/3 \times V_{CC(ANA)}$	DEPEND ON TSD/WDT	DEPEND ON OVM COMPARATOR
1110	0.3 V	L	DEPEND ON OVM COMPARATOR
1111	0.3 V	DEPEND ON TSD/WDT	L

† MCENA is low.

SOUT output timing selection

The timing for the SOUT output can be switched by selecting the SOMODE level. When SOMODE is low, SOUT is clocked out synchronizing to the rising edge of SCLK. When SOMODE is high, SOUT is clocked out synchronizing to the falling edge of SCLK. When the shift operation with SOMODE high, data can be protected from shift error even if the SCLK signal is buffered in serial externally. In this case, when ICs are connected in cascade, the maximum data transfer speed will be slower than the case of SOMODE low.

protection

This device incorporates WDT and TSD functions. If the WDT or TSD is turned on, then the constant current output is stopped and XDOWN1 goes low. Therefore, by monitoring XDOWN1 terminal, these failures can be detected immediately. Since the XDOWN1 output is configured as an open collector, outputs of multiple ICs are brought together.

PRINCIPLES OF OPERATION

protection (continued)

WDT (watchdog timer)

The constant current output is forced to turn off and XDOWN1 goes low when the fixed period elapsed after the signal applied to WDTRG has not been changed. Therefore, by a connecting scan signal (signal to control line displayed) to WDTRG, the stop of the scan signal can be detected and the constant current output is turned off preventing the LED from burning and damage by continuous LED turnon at the dynamic scanning operation. The detection time can be set using an external capacitor, Cext. The typical value is approximately 10 ms without a capacitor, 160 ms with a1000 pF capacitor and 1500 ms with a 0.01 μF capacitor. During static operation, the WDT function is disabled connecting WDCAP to GND (high or low level should be applied to WDTRG). Note that normal operation will be resumed changing the WDTRG level when WDT functions.

WDT operational time T (ms) ≅ 10 + 0.15 x Cext (pF)

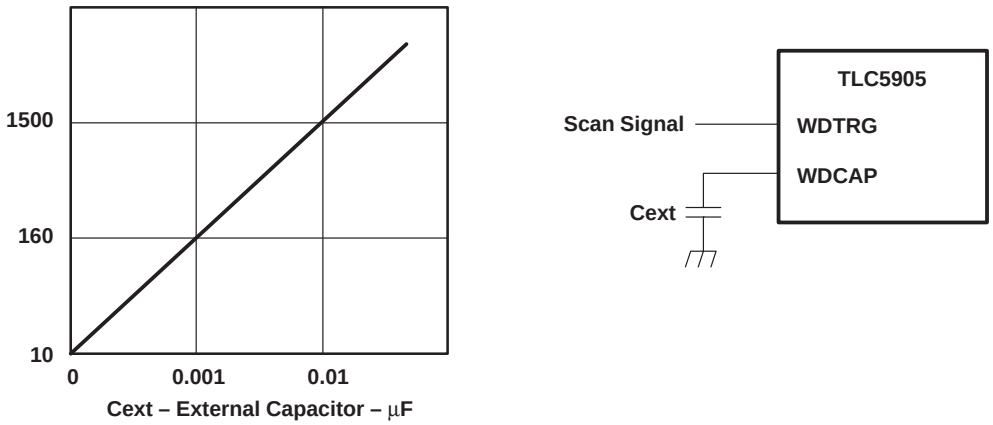


Figure 6. WDT Operational Time and Usage Example

TSD (thermal shutdown)

When the junction temperature exceeds the limit, TSD functions and turns the constant current output off, and XDOWN1 goes low. When TSD is used, TSENA is pulled high. When TSD is not used, TSENA is pulled low. To recover from constant current output off-state to normal operation, the power supply should be turned off or TSENA should be pulled low once.

PRINCIPLES OF OPERATION

noise reduction

concurrent switching noise reduction

The concurrent switching noise has potential to occur when multiple outputs turn on or off at the same time. To prevent this noise, the device has delay output terminals such as XGSOUT and BOUT for GSCLK (gray scale clock) and BLANK (blanking signal) respectively. By connecting these outputs to GSCLK and BLANK terminals of next stage IC, it allows differences in the switching time between ICs to be made. When GSCLK is output to GSOUT through the device, duty will be changed between input and output, and the number of stages to be connected will be limited depending on frequency.

output slope

When output current is 80 mA, the time to change constant current output to turnon and turnoff is approximately 150 ns and 250 ns respectively. It is effective in reducing concurrent switching noise that occurrs when multiple outputs turn or off at the same time.

delay between constant current output

The constant current output has a delay time of approximately 30 ns between outputs. It means approximately 450 ns delay time exists between OUT0 and OUT15. This time difference by delay is effective for reduction of concurrent switching noise as well as the output slope. This delay time has the same value in 8 bits or 16 bits operation mode.

power supply

The followings should be taken into consideration.

- $V_{CC(LOG)}$, $V_{CC(ANA)}$ and $V_{CC(LED)}$ should be supplied by a single power supply to minimize voltage differences between these terminals.
- The bypass capacitor should be located between power the supply and GND to eliminate the variation of power supply voltage.

GND

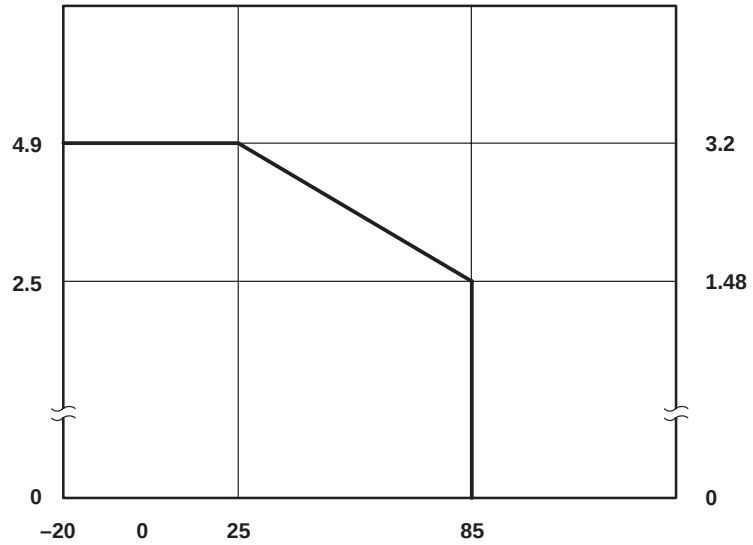
Although GNDLOG, GNDANA and GNDLED are internally tied together, these terminals should be externally connected to reduce noise influence.

thermal pad

The thermal pad should be connected to GND to eliminate the noise influence since it is connected to the bottom side of IC chip. Also, desired thermal effect will be obtained by connecting this pad to the PCB pattern with better thermal conductivity.

PRINCIPLES OF OPERATION

noise reduction (continued)



NOTES: A. This is based on simulation. When a TI recommended PCB is used, derate linearly at the rate of 39.4 mW/°C for operation above 25°C free-air temperature.
$V_{CC(LOG)}$=$V_{CC(ANA)}$=$V_{CC(LED)}$= 5 V, $I_{O(LC)}$ = 80 mA, $I_{C(C)}$ is typical value.

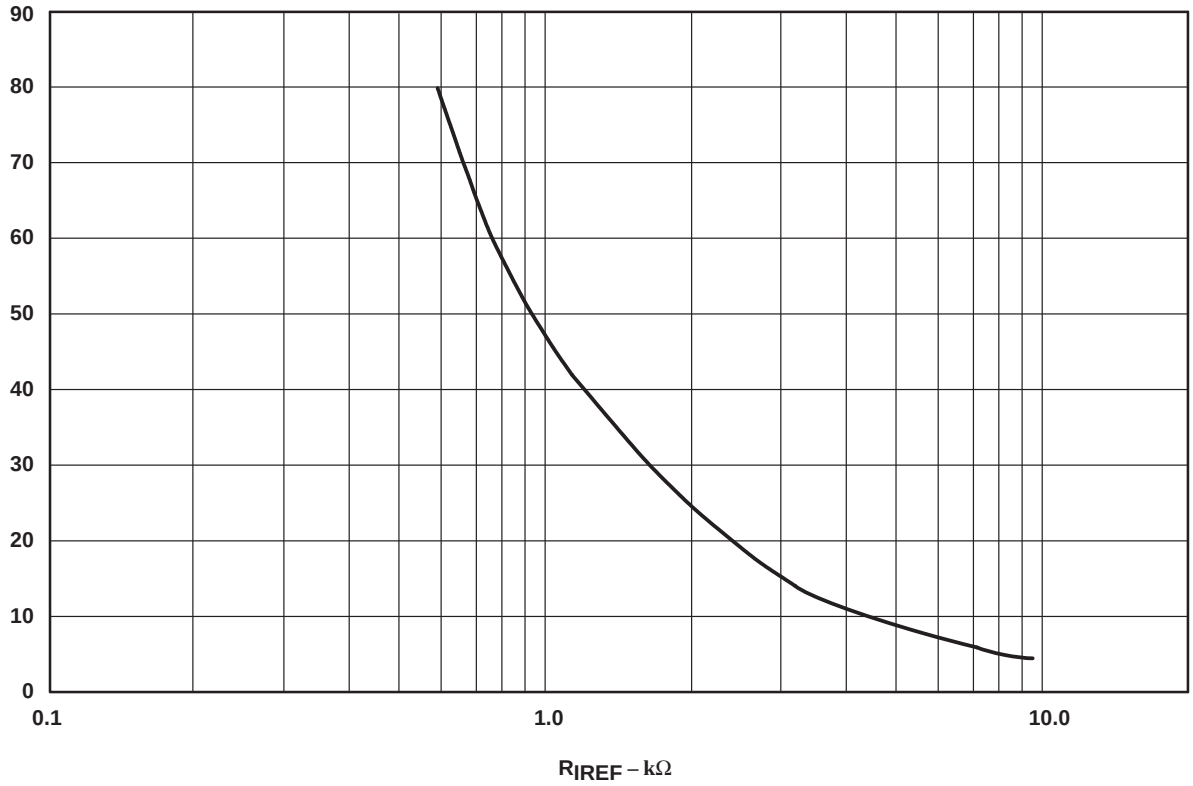
B. The thermal impedance will be varied depending on mounting conditions. Since PAP package established low thermal impedance by radiating heat from the thermal pad, the thermal pad should be soldered to the pattern with a low thermal impedance.

C. The material for PCB should be selected considering the thermal characteristics since the temperature will rise around the thermal pad.

Figure 7. Power Rating – Free-Air Temperature

PRINCIPLES OF OPERATION

noise reduction (continued)



Conditions : V_O = 1 V, $V_{(IREF)}$ = 1.24 V

$$I_{OLC}(mA) \cong \frac{V_{(IREF)}(V)}{R_{(IREF)}(k\Omega)} \times 37$$

$$R_{(IREF)}\ (k\Omega) \cong \frac{47}{I_{O(LC)}(mA)}$$

NOTE: The output current is in 16 bit mode. When in 8 bit mode (MODE=L), the output current is the sum of both outputs. This sum current should be set from 10 mA to 120 mA. The resistor, $R_{(IREF)}$, should be located as close to the IREF terminal as possible to avoid the noise influence.

Figure 8. Current on Constant Current Output vs External Resistor

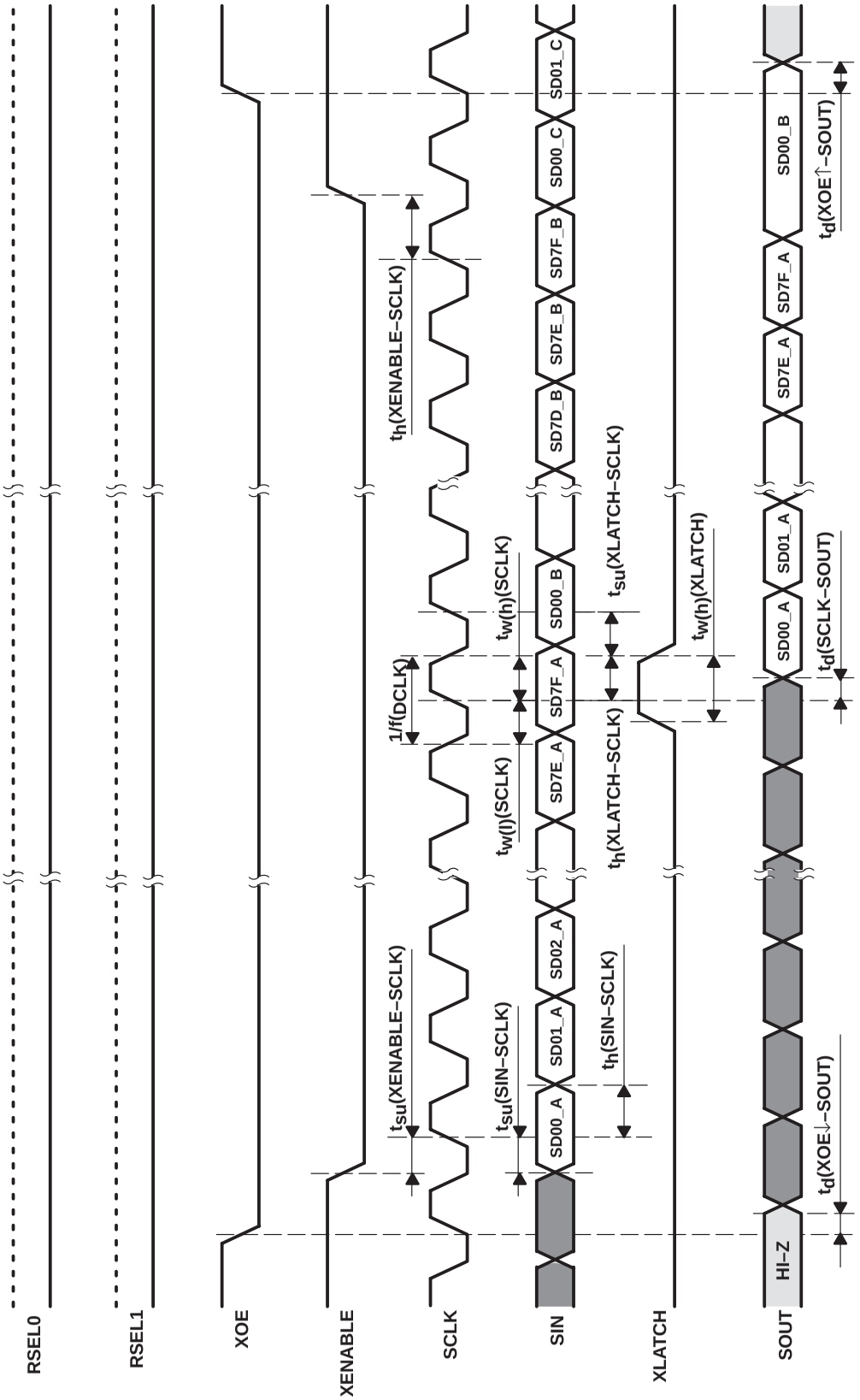


Figure 9. Timing Diagram (Shift Register for Gray Scale Data)

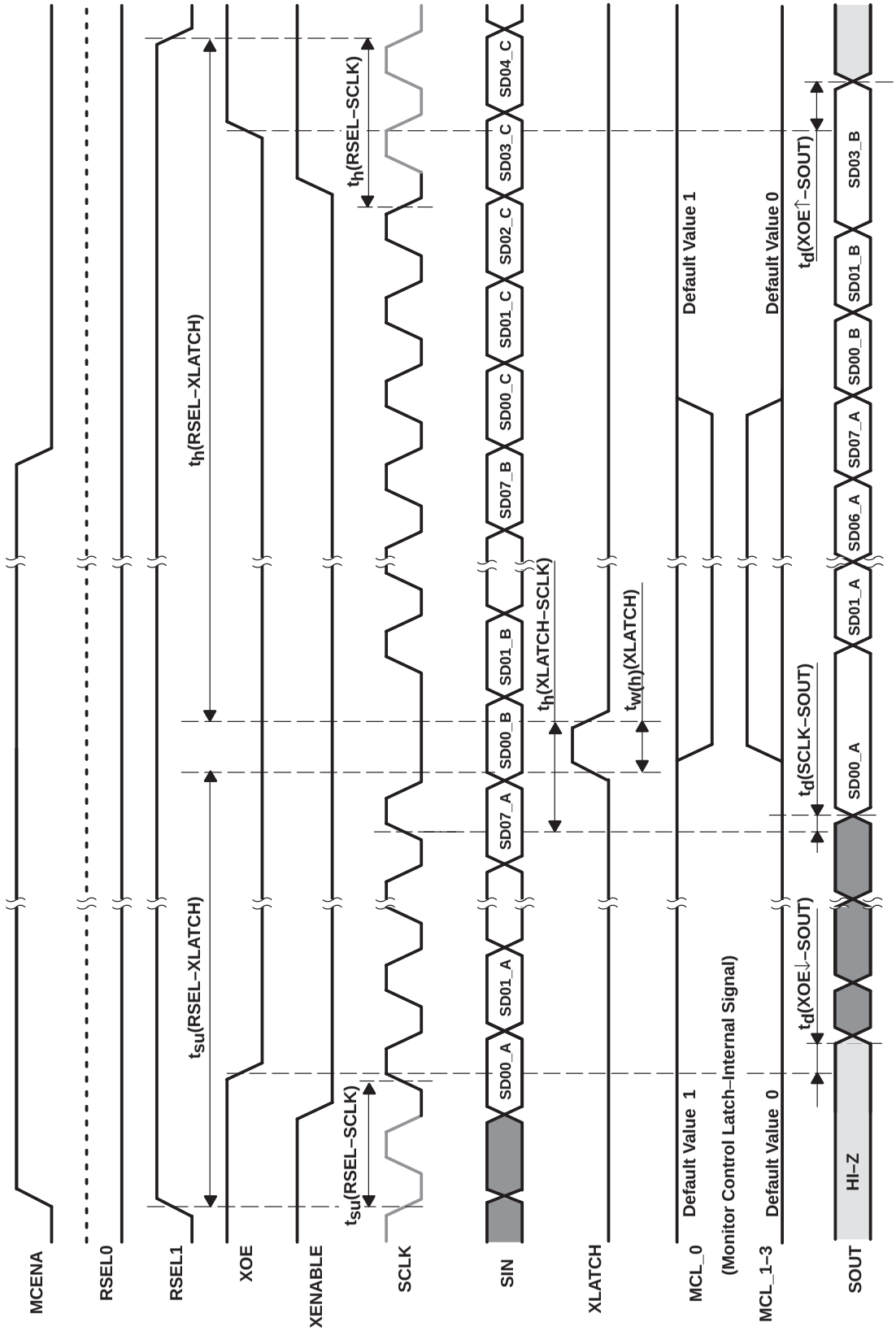


Figure 10. Timing Diagram (Shift Register for Monitor Control)

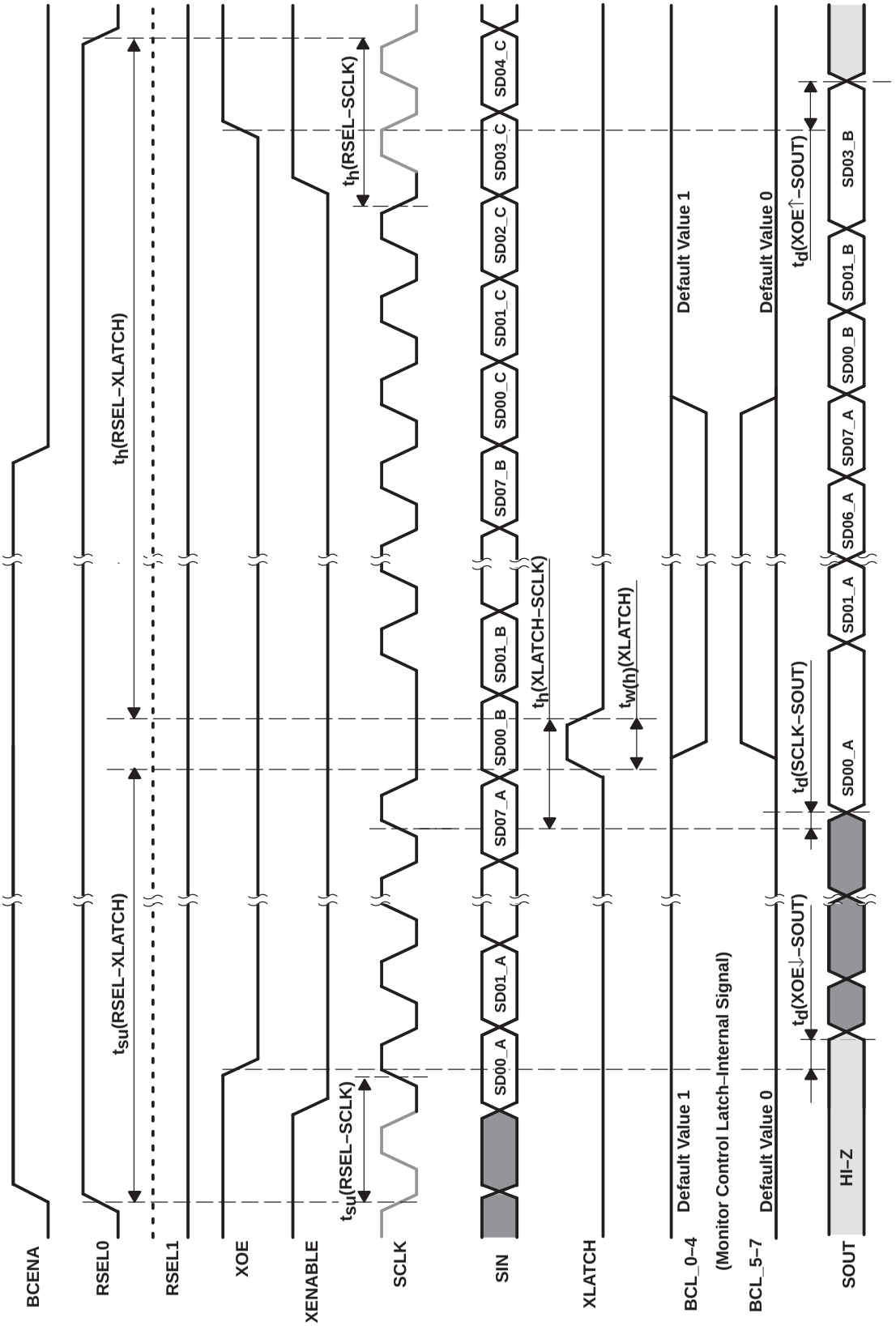


Figure 11. Timing Diagram (Shift Register for Brightness Control)

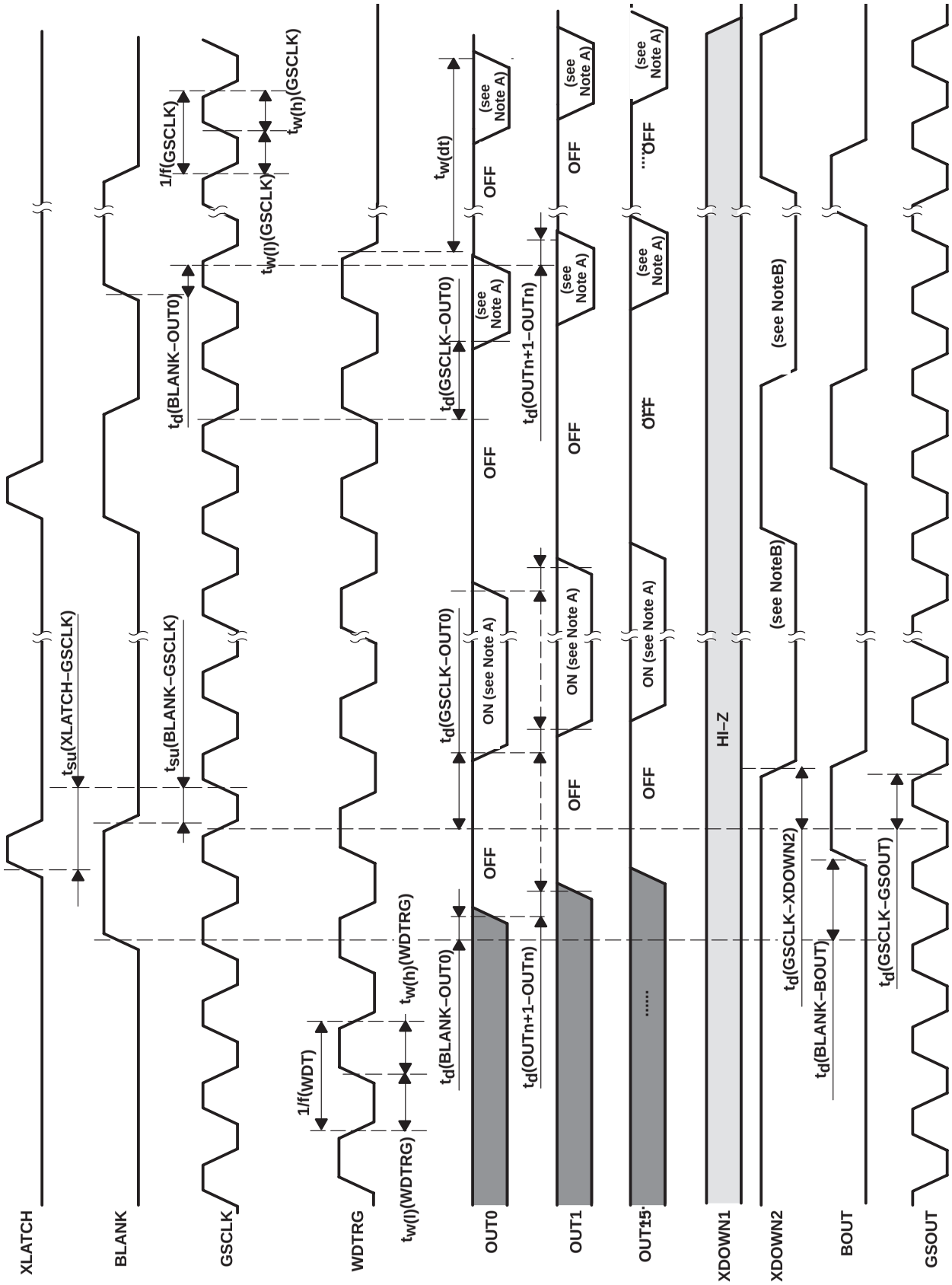
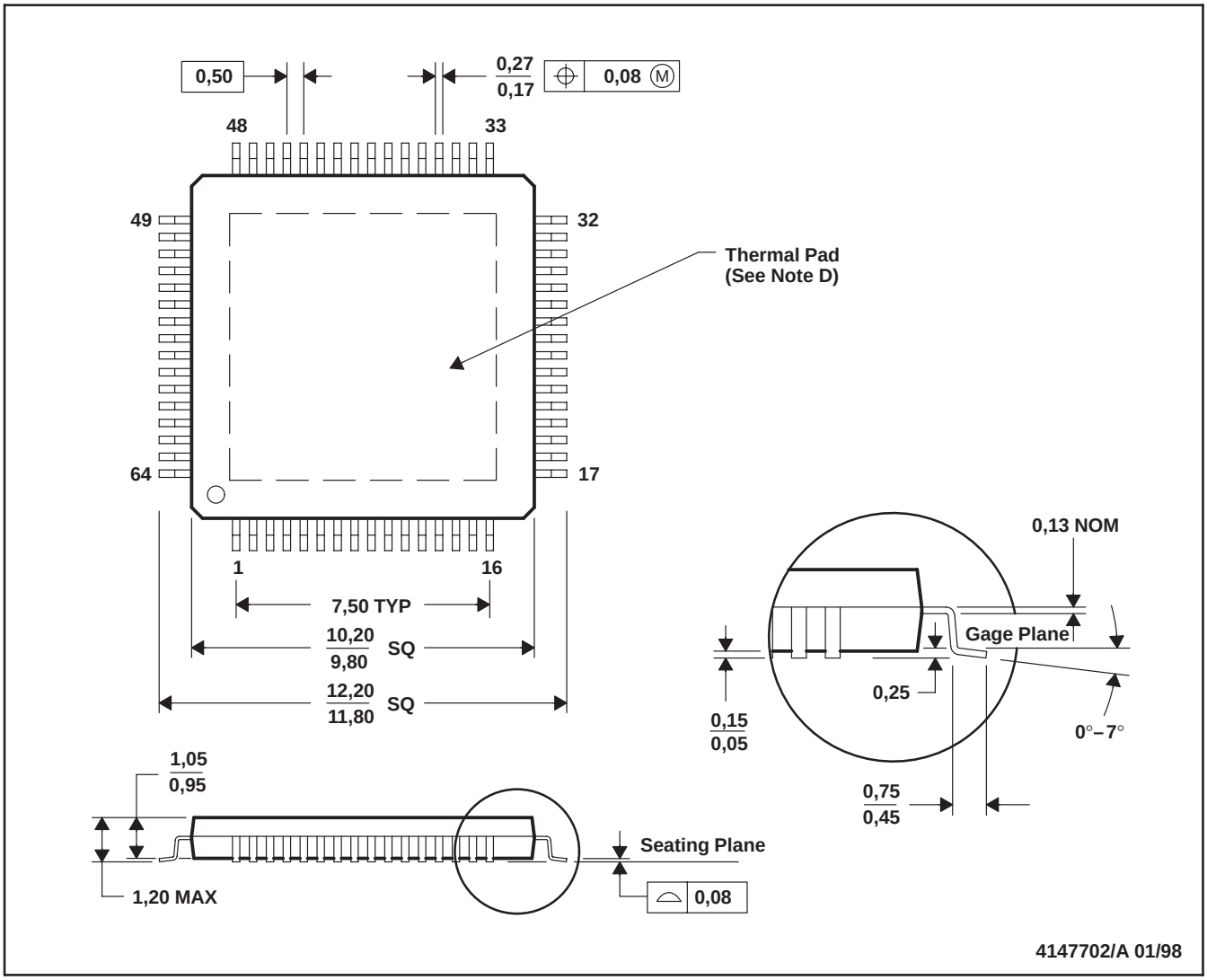


Figure 12. Timing Diagram (Constant Current Output)

NOTES: A. ON or OFF, or ON time is varied dpend on the gray scale data and BLANK.
B. LED disconnection

MECHANICAL DATA

PAP (S-PQFP-G64) **PowerPAD™ PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC5905PAP	Active	Production	HTQFP (PAP) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-20 to 85	TLC5905
TLC5905PAP.A	Active	Production	HTQFP (PAP) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-20 to 85	TLC5905

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

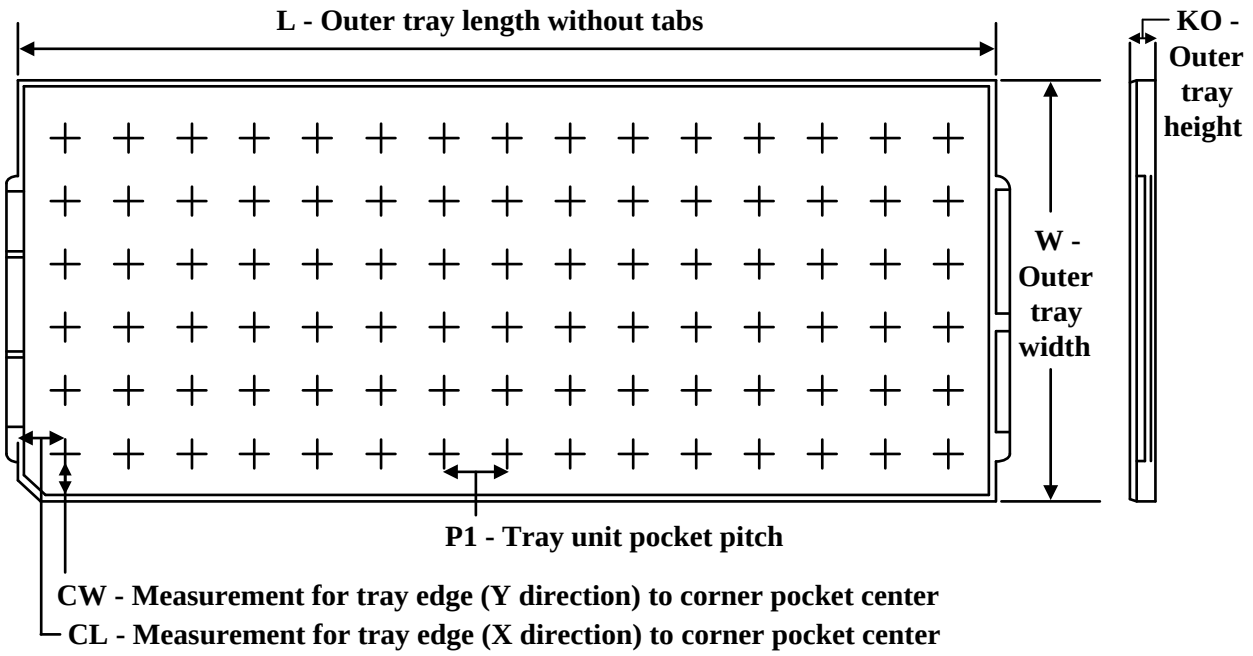
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TLC5905PAP	PAP	HTQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
TLC5905PAP.A	PAP	HTQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13

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