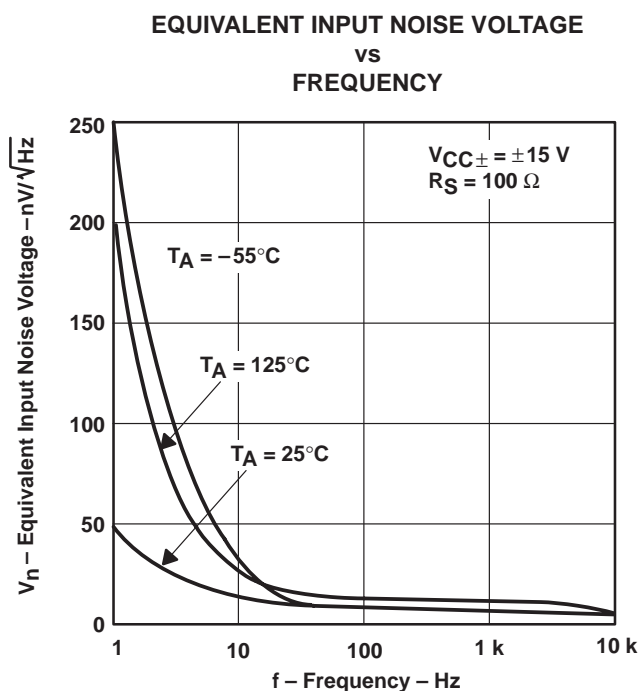
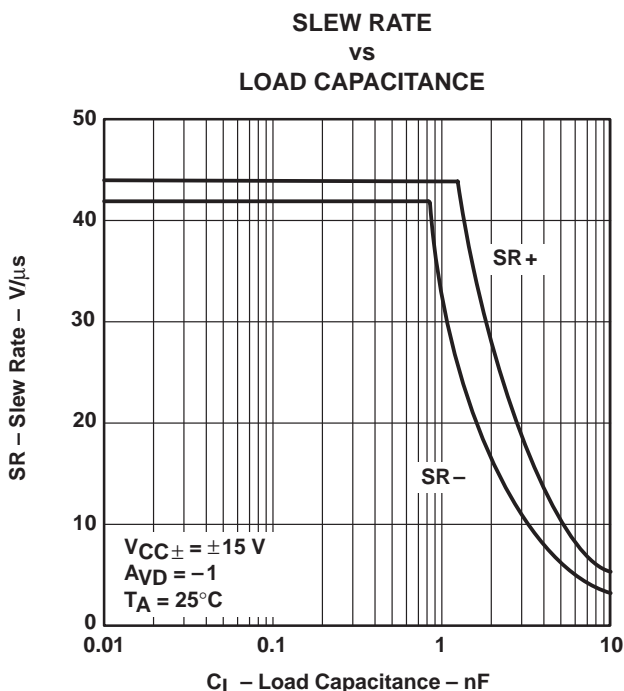


# TLE2141M, TLE2141AM EXCALIBUR LOW-NOISE HIGH-SPEED PRECISION OPERATIONAL AMPLIFIERS

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## available features

- Low Noise:  
10 Hz ... 15 nV/√Hz  
1 kHz ... 10.5 nV/√Hz
- 10000-pF Load Capability
- 20-mA Min Short-Circuit Output Current
- 30-V/μs Min Slew Rate
- High Gain-Bandwidth Product ... 5.9 MHz
- Low  $V_{IO}$  ... 500 μV Max at 25°C
- Single or Split Supply ... 4 V to 44 V
- Fast Settling Time  
340 ns to 0.1%  
400 ns to 0.01%
- Saturation Recovery ... 150 ns
- Large Output Swing ...  $V_{CC-} + 0.1$  V  
to  $V_{CC+} - 1$  V



## description

The TLE2141M and TLE2141AM are high-performance, internally compensated operational amplifiers built using Texas Instruments complementary bipolar Excalibur process. The TLE2141AM is a tighter offset voltage grade of the TLE2141M. Both are pin-compatible upgrades to standard industry products.

The design incorporates a patent-pending input stage that simultaneously achieves low audio band noise of 10.5 nV/√Hz with a 10-Hz 1/f corner and symmetrical 40-V/μs slew rate typically with loads up to 800 pF. The resulting low distortion and high power bandwidth are important in high-fidelity audio applications. A fast settling time of 340 ns to 0.1% of a 10-V step with a 2-kΩ/100-pF load is useful in fast actuator/positioning drivers. Under similar test conditions, settling time to 0.01% is 400 ns.

### AVAILABLE OPTIONS

$T_A$	$V_{IO}$ max AT 25°C	PACKAGE		CHIP FORM (Y)
		CHIP CARRIER (FK)	CERAMIC DIP (JG)	
-55°C to 125°C	500 μV	TLE2141AMFK	TLE2141AMJG	TLE2141Y
	900 μV	TLE2141MFK	TLE2141MJG	

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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## description (continued)

The devices are stable with capacitive loads up to 10 nF, although the 6-MHz bandwidth decreases to 1.8 MHz at this high loading level. As such, the TLE2141M and TLE2141AM are useful for low-droop sample and holds and direct buffering of long cables, including four 20-mA current loops.

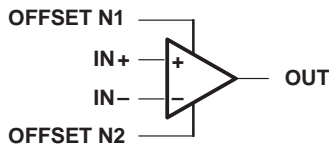
The special design also exhibits an improved insensitivity to inherent IC component mismatches as is evidenced by a 500- $\mu$ V maximum offset voltage and 1.7- $\mu$ V/ $^{\circ}$ C typical drift. Minimum common-mode rejection ratio and supply-voltage rejection ratio are 85 dB and 90 dB, respectively.

Device performance is relatively independent of supply voltage over the  $\pm 2$ -V to  $\pm 22$ -V range. Inputs can operate between  $V_{CC-} - 0.3$  to  $V_{CC+} - 1.8$  V without inducing phase reversal, although excessive input current may flow out of each input exceeding the lower common-mode input range. The all NPN output stage provides a nearly rail-to-rail output swing of  $V_{CC-} + 0.1$  to  $V_{CC+} - 1$  V under light current loading conditions. The device can sustain shorts to either supply since output current is internally limited, but care must be taken to ensure that maximum package power dissipation is not exceeded.

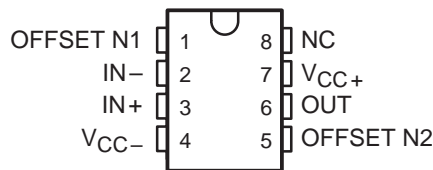
Both versions can also be used as comparators. Differential inputs of  $V_{CC\pm}$  can be maintained without damage to the device. Open-loop propagation delay with TTL supply levels is typically 200 ns. This gives a good indication as to output stage saturation recovery when the device is overdriven beyond the limits of recommended output swing.

Both the TLE2141M and TLE2141AM are available in a wide variety of packages, including both the industry-standard 8-pin small-outline version and chip form for high-density system applications. The M-suffix is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to  $125^{\circ}$ C.

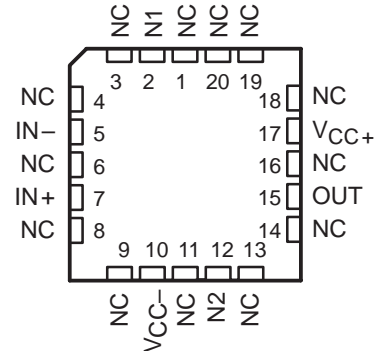
## symbol



JG PACKAGE  
(TOP VIEW)



FK PACKAGE  
(TOP VIEW)



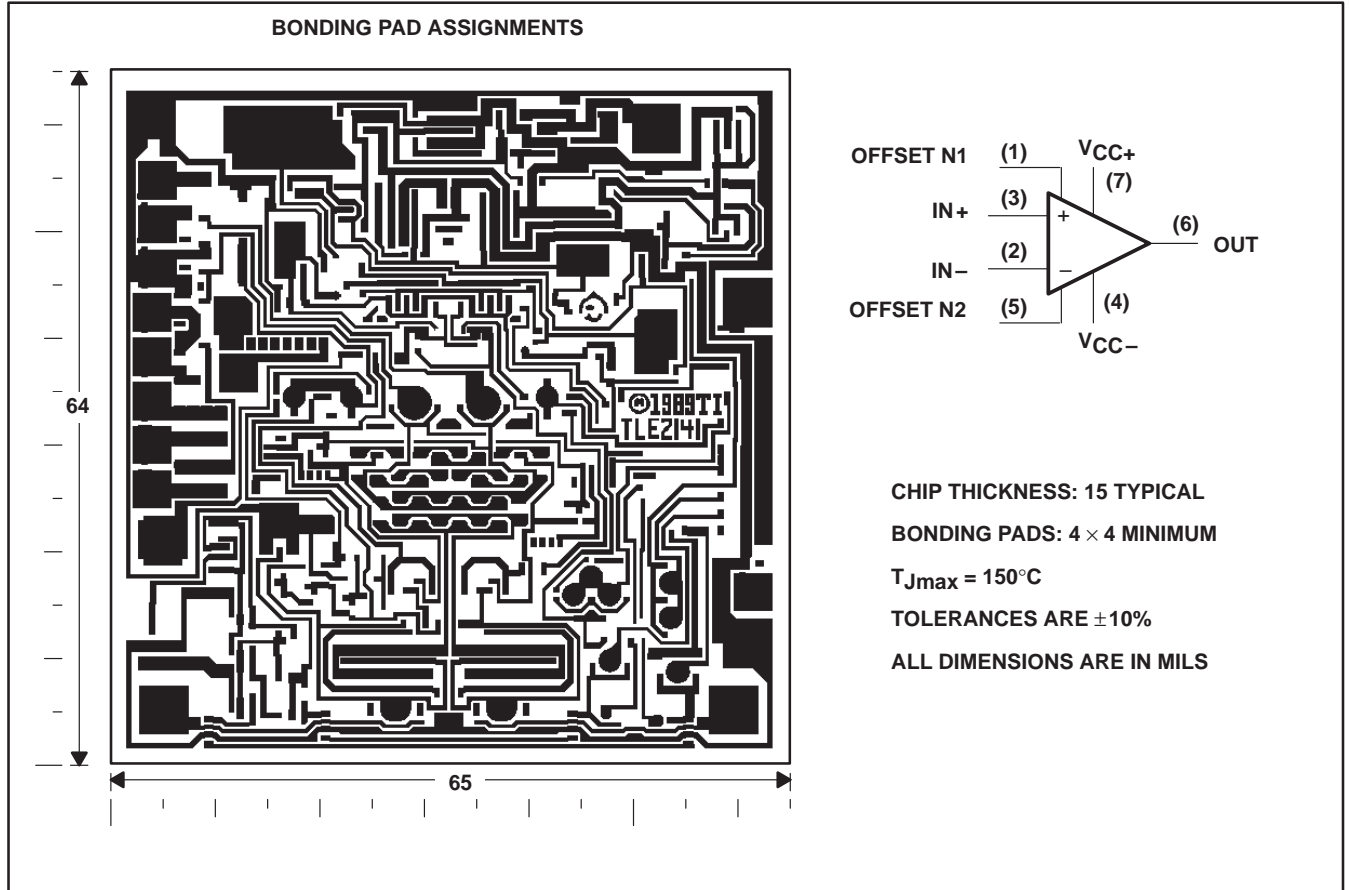
NC – No internal connection

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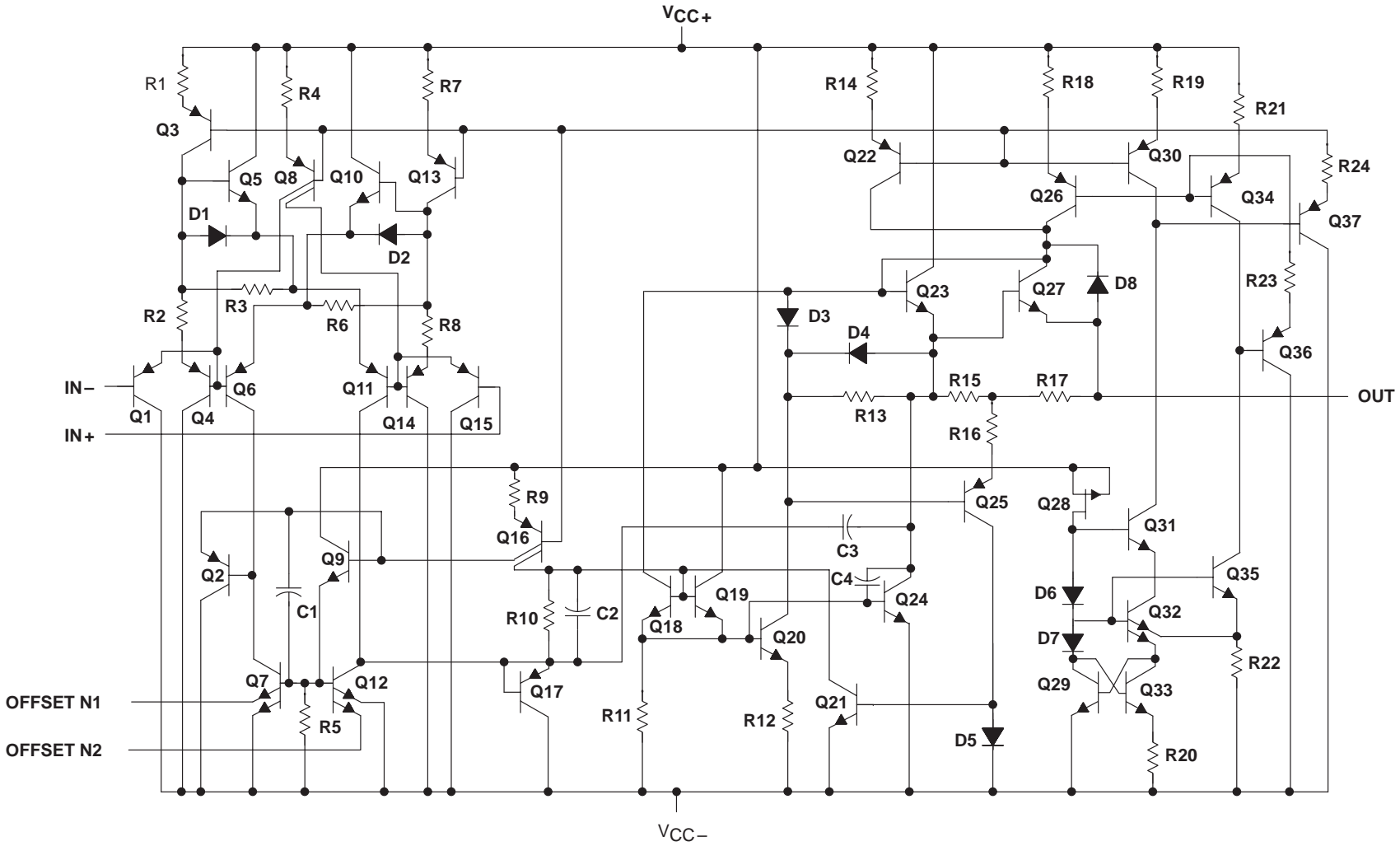
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**chip information**

These chips, when properly assembled, display characteristics similar to the TLE2141M. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



equivalent schematic



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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC+}$ (see Note 1)	22 V
Supply voltage, $V_{CC-}$ (see Note 1)	–22 V
Differential input voltage (see Note 2)	±44 V
Input voltage range, $V_I$ (any input)	$V_{CC+}$ to $V_{CC-} - 0.3$ V
Input current, $I_I$ (each input)	±1 mA
Output current, $I_O$	±80 mA
Total current into $V_{CC+}$	80 mA
Total current out of $V_{CC-}$	80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$	–55°C to 125°C
Storage temperature range	–65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package	300°C

- NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between  $V_{CC+}$  and  $V_{CC-}$ .
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current will flow if input voltage is brought below  $V_{CC-} - 0.3$  V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 105^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
FK	1375 mW	11.0 mW/°C	880 mW	495 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	378 mW	210 mW

**recommended operating conditions**

		MIN	MAX	UNIT
Supply voltage, $V_{CC\pm}$		±2	±22	V
Common-mode input voltage, $V_{IC}$	$V_{CC} = 5$ V	0	2.7	V
	$V_{CC\pm} = \pm 15$ V	–15	12.7	
Operating free-air temperature, $T_A$		–55	125	°C



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**electrical characteristics at specified free-air temperature,  $V_{CC} = 5\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLE2141M			TLE2141AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_O = 2.5\text{ V}$ , $R_S = 50\ \Omega$ , $V_{IC} = 2.5\text{ V}$	25°C	225	1400		200	1000	$\mu\text{V}$	
		Full range			2100		1700		
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		Full range		1.7			1.7	$\mu\text{V}/^\circ\text{C}$	
$I_{IO}$ Input offset current		25°C		8	100		8	100	nA
		Full range			250			250	
$I_{IB}$ Input bias current		25°C		-0.8	-2		-0.8	-2	$\mu\text{A}$
	Full range			-2.3			-2.3		
$V_{ICR}$ Common-mode input voltage range	$R_S = 50\ \Omega$	25°C	0 to 3	-0.3 to 3.2		0 to 3	-0.3 to 3.2	V	
		Full range	0 to 2.7	-0.3 to 2.9		0 to 2.7	-0.3 to 2.9		
$V_{OH}$ High-level output voltage	$I_{OH} = -150\ \mu\text{A}$	25°C		3.9	4.1		3.9	4.1	V
	$I_{OH} = -1.5\text{ mA}$			3.8	4		3.8	4	
	$I_{OH} = -15\text{ mA}$			3.2	3.7		3.2	3.7	
	$I_{OH} = -100\ \mu\text{A}$	Full range		3.75			3.75		
	$I_{OH} = -1\text{ mA}$			3.65			3.65		
	$I_{OH} = -10\text{ mA}$			3.25			3.25		
$V_{OL}$ Low-level output voltage	$I_{OL} = 150\ \mu\text{A}$	25°C		75	125		75	125	mV
	$I_{OL} = 1.5\text{ mA}$			150	225		150	225	
	$I_{OL} = 15\text{ mA}$			1.2	1.4		1.2	1.4	V
	$I_{OL} = 100\ \mu\text{A}$	Full range		200			200		
	$I_{OL} = 1\text{ mA}$			250			250		
	$I_{OL} = 10\text{ mA}$			1.25			1.25		
$A_{VD}$ Large-signal differential voltage amplification	$V_{CC} = \pm 2.5\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $V_O = 1\text{ V to } -1.5\text{ V}$	25°C	50	220		50	220	V/mV	
		Full range		5			5		
$r_i$ Input resistance		25°C		70			70	M $\Omega$	
$c_i$ Input capacitance		25°C		2.5			2.5	pF	
$z_o$ Open-loop output impedance	$f = 1\text{ MHz}$	25°C		30			30	$\Omega$	
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR}\text{ min}$ , $R_S = 50\ \Omega$	25°C	85	118		85	118	dB	
		Full range		80			80		
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC\pm} = \pm 2.5\text{ V to } \pm 15\text{ V}$ , $R_S = 50\ \Omega$	25°C	90	106		90	106	dB	
		Full range		85			85		
$I_{CC}$ Supply current	$V_O = 2.5\text{ V}$ , No load, $V_{IC} = 2.5\text{ V}$	25°C		3.4	4.4		3.4	4.4	mA
		Full range			4.6			4.6	

† Full range is  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ .



**TLE2141M, TLE2141AM**  
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operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TLE2141M			TLE2141AM			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$A_{VD} = -1$ , $C_L = 500\text{ pF}$		$R_L = 2\text{ k}\Omega^\dagger$		45		V/ $\mu\text{s}$
SR-	Negative slew rate					42		
	Settling time	$A_{VD} = -1$ , 2.5-V step	To 0.1%		0.16		$\mu\text{s}$	
			To 0.01%		0.22			
$V_n$	Equivalent input noise voltage	$R_S = 100\ \Omega$ , $f = 10\text{ Hz}$		15		nV/ $\sqrt{\text{Hz}}$		
		$R_S = 100\ \Omega$ , $f = 1\text{ kHz}$		10.5				
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$		0.48		$\mu\text{V}$		
		$f = 0.1\text{ Hz to }10\text{ Hz}$		0.51				
$I_n$	Equivalent input noise current	$f = 10\text{ Hz}$		1.92		pA/ $\sqrt{\text{Hz}}$		
		$f = 1\text{ kHz}$		0.5				
THD + N	Total harmonic distortion plus noise	$V_O = 1\text{ V to }3\text{ V}$ , $A_{VD} = 2$		$R_L = 2\text{ k}\Omega^\dagger$ , $f = 10\text{ kHz}$		0.0052%		
B1	Unity-gain bandwidth	$R_L = 2\text{ k}\Omega^\dagger$ , $C_L = 100\text{ pF}$		5.9		MHz		
	Gain-bandwidth product	$R_L = 2\text{ k}\Omega^\dagger$ , $f = 100\text{ kHz}$		5.8		MHz		
B <sub>OM</sub>	Maximum output-swing bandwidth	$R_L = 2\text{ k}\Omega^\dagger$ , $A_{VD} = 1$		$V_{O(PP)} = 2\text{ V}$		6.6 MHz		
$\phi_m$	Phase margin at unity gain	$R_L = 2\text{ k}\Omega^\dagger$ , $C_L = 100\text{ pF}$		57°		57°		

$^\dagger R_L$  terminates at 2.5 V.

**TLE2141M, TLE2141AM**  
**EXCALIBUR LOW-NOISE HIGH-SPEED**  
**PRECISION OPERATIONAL AMPLIFIERS**

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**electrical characteristics at specified free-air temperature,  $V_{CC\pm} = \pm 15$  V (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$T_A$ †	TLE2141M			TLE2141AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = 0, R_S = 50 \Omega$	25°C	200	900		175	500	$\mu$ V	
		Full range			1700		1200		
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		Full range		1.7			1.7	$\mu$ V/°C	
$I_{IO}$ Input offset current		25°C		7	100		7	100	nA
		Full range			250			250	
$I_{IB}$ Input bias current		25°C		-0.7	-1.5		-0.7	-1.5	$\mu$ A
	Full range			-1.8			-1.8		
$V_{ICR}$ Common-mode input voltage range	$R_S = 50 \Omega$	25°C	-15 to 13	-15.3 to 13.2		-15 to 13	-15.3 to 13.2	V	
		Full range			-15 to 12.7				-15.3 to 12.9
$V_{OM+}$ Maximum positive peak output voltage swing	$I_O = -150 \mu$ A	25°C		13.8	14.1		13.8	14.1	V
	$I_O = -1.5$ mA			13.7	14		13.7	14	
	$I_O = -15$ mA			13.1	13.7		13.1	13.7	
	$I_O = -100 \mu$ A	Full range		13.7			13.7		
	$I_O = -1$ mA			13.6			13.6		
	$I_O = -10$ mA			13.1			13.1		
$V_{OM-}$ Maximum negative peak output voltage swing	$I_O = 150 \mu$ A	25°C		-14.7	-14.9		-14.7	-14.9	V
	$I_O = 1.5$ mA			-14.5	-14.8		-14.5	-14.8	
	$I_O = 15$ mA			-13.4	-13.8		-13.4	-13.8	
	$I_O = 100 \mu$ A	Full range		-14.6			-14.6		
	$I_O = 1$ mA			-14.5			-14.5		
	$I_O = 10$ mA			-13.4			-13.4		
$A_{VD}$ Large-signal differential voltage amplification	$V_O = \pm 10$ V, $R_L = 2$ k $\Omega$	25°C	100	450		100	450	V/mV	
		Full range		20			20		
$r_i$ Input resistance		25°C		65			65	M $\Omega$	
$c_i$ Input capacitance		25°C		2.5			2.5	pF	
$z_o$ Open-loop output impedance	$f = 1$ MHz	25°C		30			30	$\Omega$	
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, $R_S = 50 \Omega$	25°C	85	108		85	108	dB	
		Full range		80			80		
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC\pm} / \Delta V_{IO}$ )	$V_{CC\pm} = \pm 2.5$ V to $\pm 15$ V, $R_S = 50 \Omega$	25°C	90	106		90	106	dB	
		Full range		85			85		
$I_{OS}$ Short-circuit output current	$V_O = 0$	25°C	$V_{ID} = 1$ V	-25	-50		-25	-50	mA
			$V_{ID} = -1$ V	20	31		20	31	
$I_{CC}$ Supply current	$V_O = 0, V_{IC} = 2.5$ V	25°C	No load,		3.5	4.5	3.5	4.5	mA
			Full range		4.7		4.7		

† Full range is -55°C to 125°C.



**TLE2141M, TLE2141AM**  
**EXCALIBUR LOW-NOISE HIGH-SPEED**  
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**operating characteristics,  $V_{CC\pm} = \pm 15$ ,  $T_A = 25^\circ\text{C}$**

PARAMETER		TEST CONDITIONS		TLE2141M			TLE2141AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate	$A_{VD} = -1$ , $C_L = 500\text{ pF}$ $R_L = 2\text{ k}\Omega$ ,		30	45		30	45		V/ $\mu\text{s}$
SR-	Negative slew rate			30	42		30	42		
Settling time		$A_{VD} = -1$ , 10-V step		To 0.1%			0.34			$\mu\text{s}$
				To 0.01%			0.4			
$V_n$	Equivalent input noise voltage	$R_S = 100\ \Omega$ , $f = 10\text{ Hz}$		15			15			nV/ $\sqrt{\text{Hz}}$
		$R_S = 100\ \Omega$ , $f = 1\text{ kHz}$		10.5			10.5			
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$		0.48			0.48			$\mu\text{V}$
		$f = 0.1\text{ Hz to }10\text{ Hz}$		0.51			0.51			
$I_n$	Equivalent input noise current	$f = 10\text{ Hz}$		1.89			1.89			pA/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		0.47			0.47			
THD + N	Total harmonic distortion plus noise	$V_{O(PP)} = 20\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $A_{VD} = 10$ , $f = 10\text{ kHz}$		0.01%			0.01%			
$B_1$	Unity-gain bandwidth	$R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$		6			6			MHz
	Gain-bandwidth product	$R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , $f = 100\text{ kHz}$		5.9			5.9			MHz
$B_{OM}$	Maximum output-swing bandwidth	$V_{O(PP)} = 20\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $A_{VD} = 1$ , $C_L = 100\text{ pF}$		668			668			kHz
$\phi_m$	Phase margin at unity gain	$R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$		58°			58°			

**TLE2141Y**  
**EXCALIBUR LOW-NOISE HIGH-SPEED**  
**PRECISION OPERATIONAL AMPLIFIER**

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**electrical characteristics,  $V_{CC\pm} = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IO}$	Input offset voltage	$V_{IC} = 0$ , $R_S = 50\ \Omega$ , $V_O = 0$		200	1000	$\mu\text{V}$
$I_{IO}$	Input offset current			7	100	nA
$I_{IB}$	Input bias current			-0.7	-1.5	$\mu\text{A}$
$V_{ICR}$	Common-mode input voltage range	$R_S = 50\ \Omega$	-15 to 13	-15.3 to 13.2		V
$V_{OM+}$	Maximum positive peak output voltage swing	$I_O = -150\ \mu\text{A}$	13.8	14.1		V
		$I_O = -1.5\ \text{mA}$	13.7	14		
		$I_O = -15\ \text{mA}$	13.3	13.7		
$V_{OM-}$	Maximum negative peak output voltage swing	$I_O = 150\ \mu\text{A}$	-14.7	-14.9		V
		$I_O = 1.5\ \text{mA}$	-14.5	-14.8		
		$I_O = 15\ \text{mA}$	-13.4	-13.8		
$A_{VD}$	Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}$ , $R_L = 2\ \text{k}\Omega$	100	450		V/mV
$r_i$	Input resistance			65		M $\Omega$
$c_i$	Input capacitance			2.5		pF
$z_o$	Open-loop output impedance	$f = 1\ \text{MHz}$		30		$\Omega$
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR\ \text{min}}$ , $R_S = 50\ \Omega$	80	108		dB
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{CC\pm} / \Delta V_{IO}$ )	$V_{CC\pm} = \pm 2.5\ \text{V}$ to $\pm 15\ \text{V}$ , $R_S = 50\ \Omega$	85	106		dB
$I_{OS}$	Short-circuit output current	$V_O = 0$	$V_{ID} = 1\ \text{V}$	-25	-50	mA
			$V_{ID} = -1\ \text{V}$	20	31	
$I_{CC}$	Supply current	$V_O = 0$ , No load		3.5	4.5	mA

## TYPICAL CHARACTERISTICS

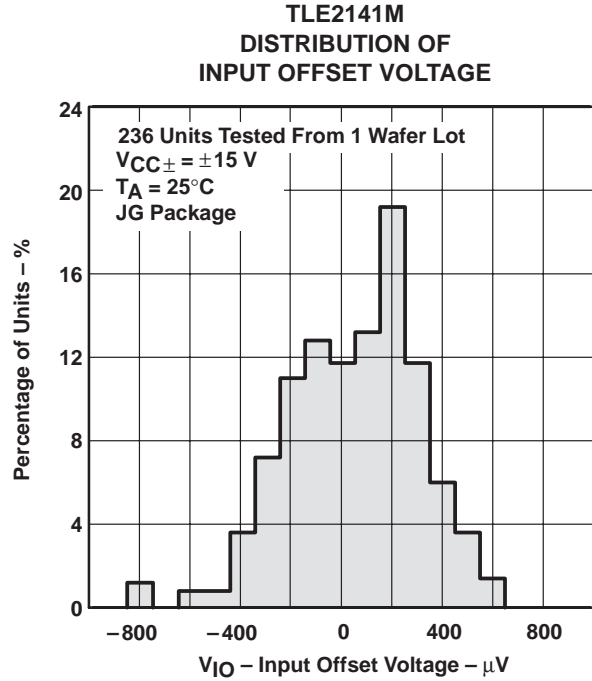
**Table of Graphs**

		<b>FIGURE</b>	
$V_{IO}$	Input offset voltage	Distribution	1
$I_{IO}$	Input offset current	vs Temperature	2
$I_{IB}$	Input bias current	vs Temperature	3
		vs Common-mode input voltage	4
$V_{OM+}$	Maximum positive peak output voltage	vs Supply voltage	5
		vs Temperature	6
		vs Output current	7
		vs Setting time	9
$V_{OM-}$	Maximum negative peak output voltage	vs Supply voltage	5
		vs Temperature	6
		vs Output current	8
		vs Setting time	9
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	vs Frequency	10
$V_{OH}$	High-level output voltage	vs Output current	11
$V_{OL}$	Low-level output voltage	vs Output current	12
$A_{VD}$	Differential voltage amplification	vs Temperature	13
		vs Frequency	14
$z_o$	Closed loop output impedance	vs Frequency	15
$I_{OS}$	Short-circuit output current	vs Supply current	16
CMRR	Common-mode rejection ratio	vs Supply current	17
		vs Temperature	18
$k_{SVR}$	Supply-voltage rejection ratio	vs Frequency	19
		vs Temperature	20
$I_{CC}$	Supply current	vs Temperature	21
		vs Supply voltage	22
$V_n$	Equivalent input noise voltage	vs Frequency	23
$V_{N(PP)}$	Equivalent input noise voltage	Over a 10-second period	24
$I_n$	Noise current	vs Frequency	25
THD+N	Total harmonic distortion plus noise	vs Frequency	26
SR	Slew rate	vs Temperature	27
		vs Load capacitance	28
Pulse response	Noninverting large signal	vs Time	29
	Inverting large signal	vs Time	30
	Small signal	vs Time	31
$B_1$	Unity-gain-bandwidth	vs Load capacitance	32
	Gain margin	vs Load capacitance	33
$\phi_m$	Phase margin	vs Load capacitance	34
	Phase shift	vs Frequency	14

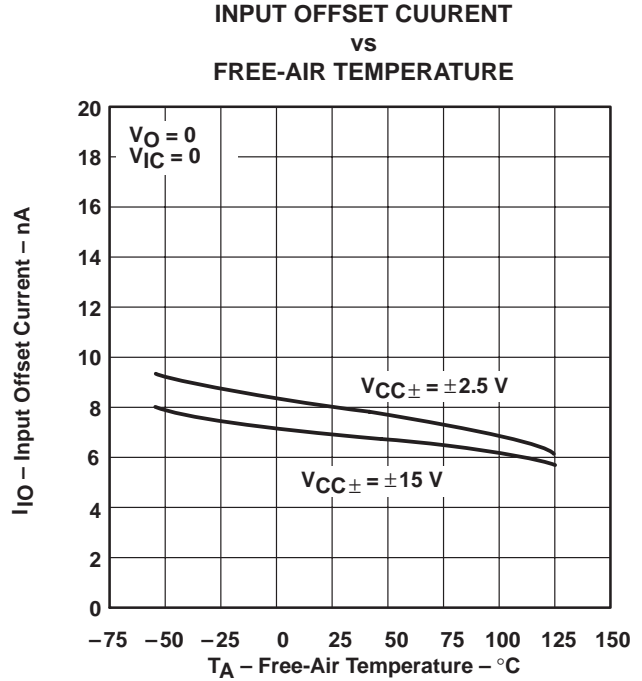
**TLE2141M, TLE2141AM**  
**EXCALIBUR LOW-NOISE HIGH-SPEED**  
**PRECISION OPERATIONAL AMPLIFIERS**

SGLS059 – NOVEMBER 1990 – REVISED OCTOBER 1991

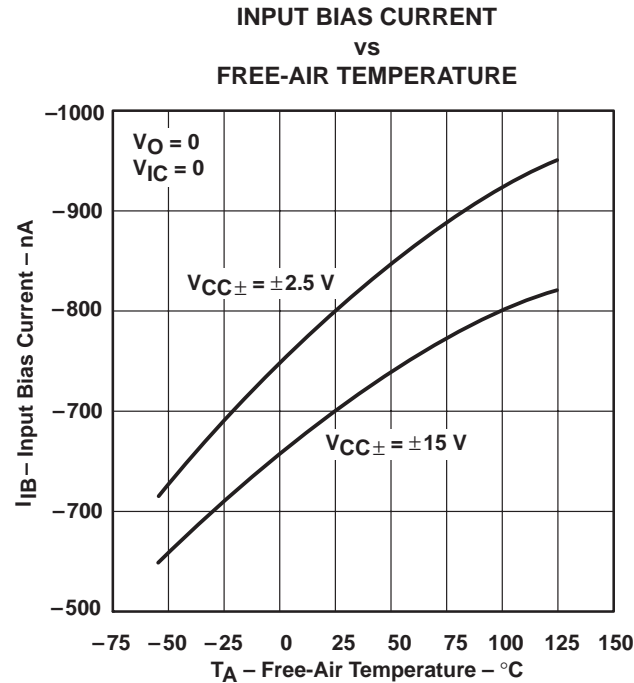
**TYPICAL CHARACTERISTICS**



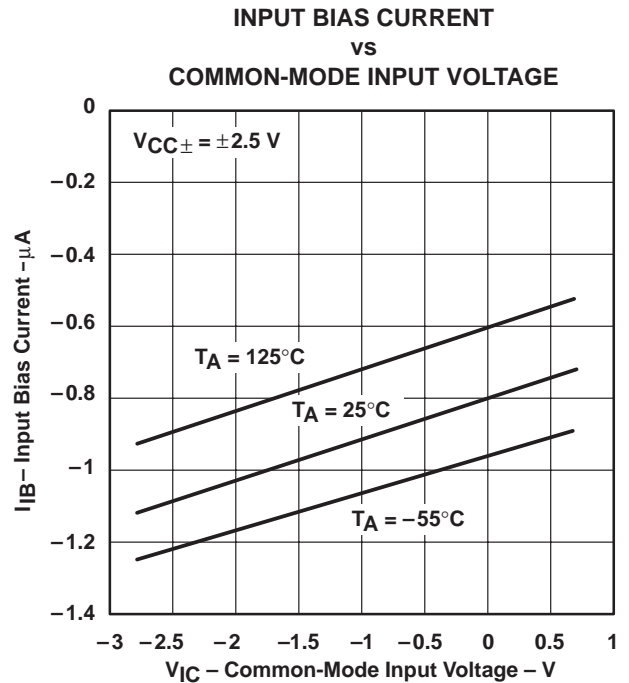
**Figure 1**



**Figure 2**



**Figure 3**



**Figure 4**

TYPICAL CHARACTERISTICS

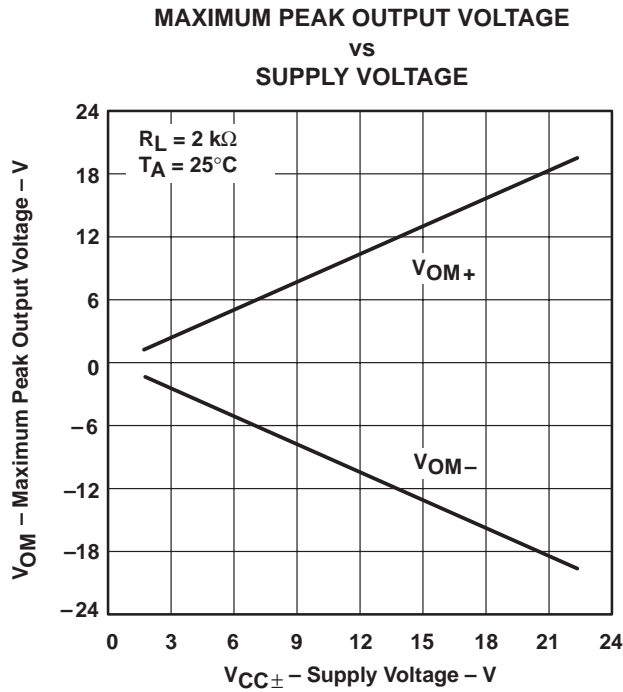


Figure 5

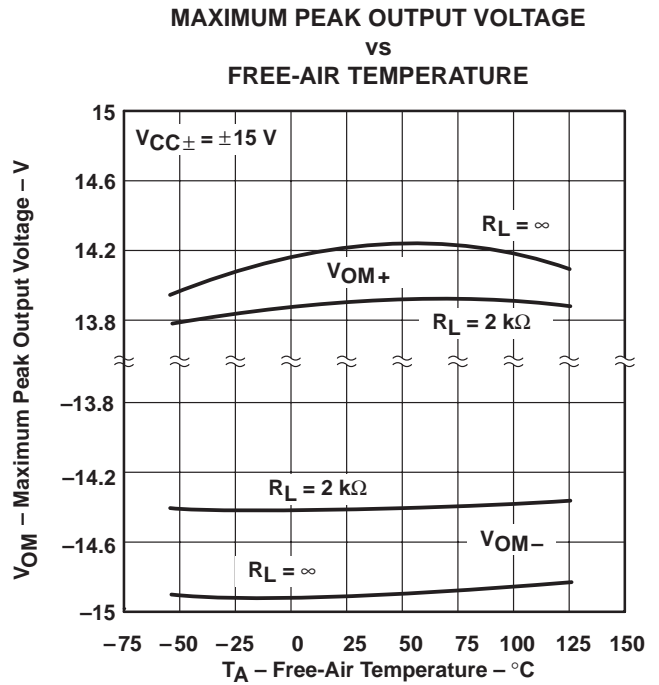


Figure 6

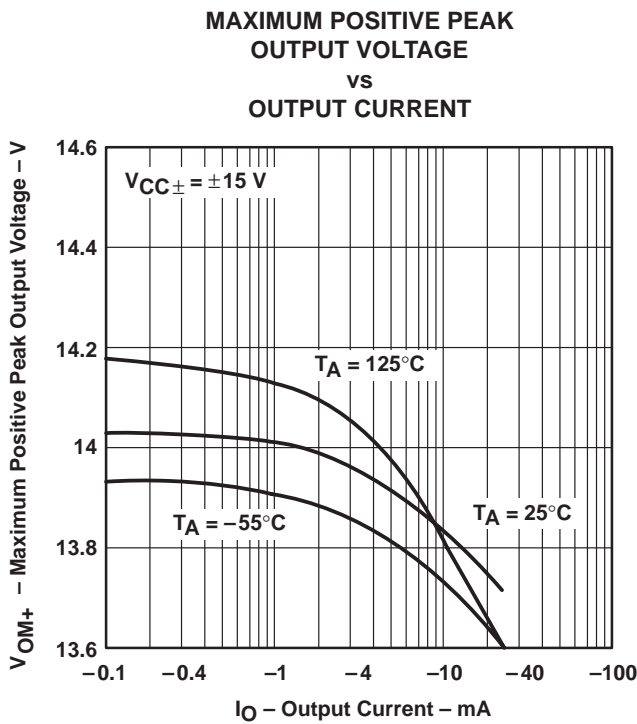


Figure 7

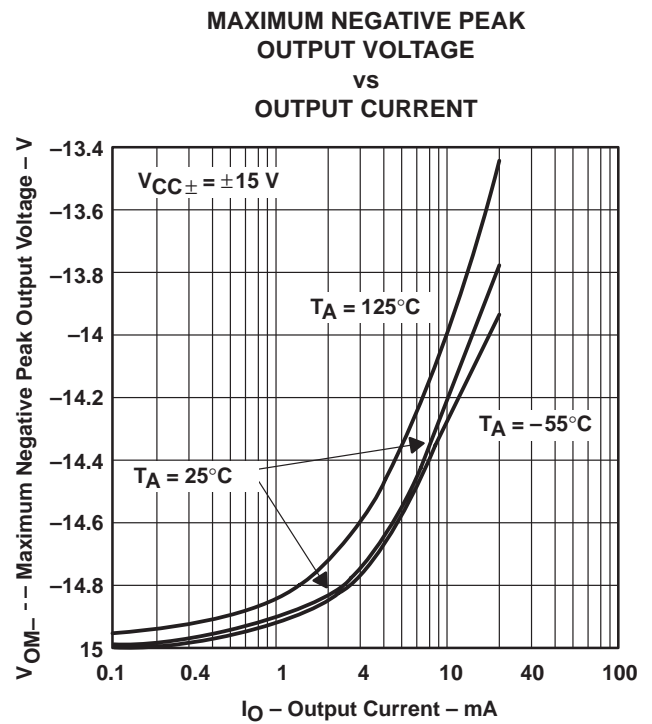


Figure 8

**TLE2141M, TLE2141AM**  
**EXCALIBUR LOW-NOISE HIGH-SPEED**  
**PRECISION OPERATIONAL AMPLIFIERS**

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**TYPICAL CHARACTERISTICS**

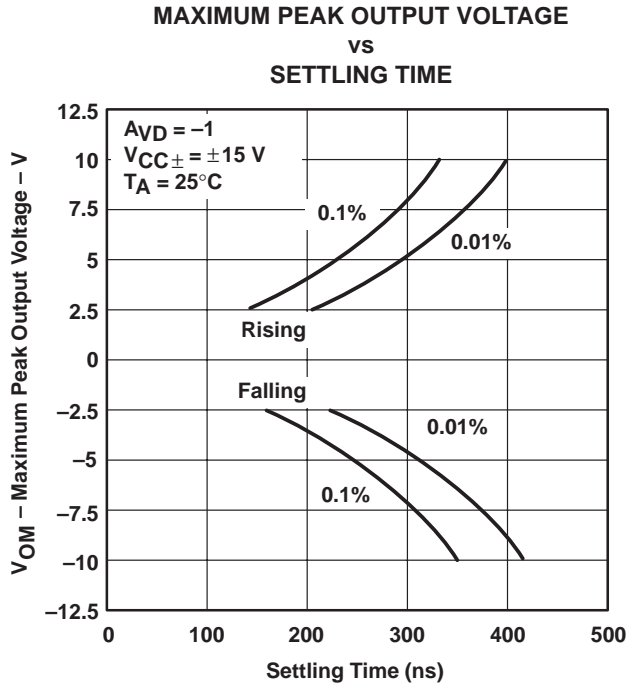


Figure 9

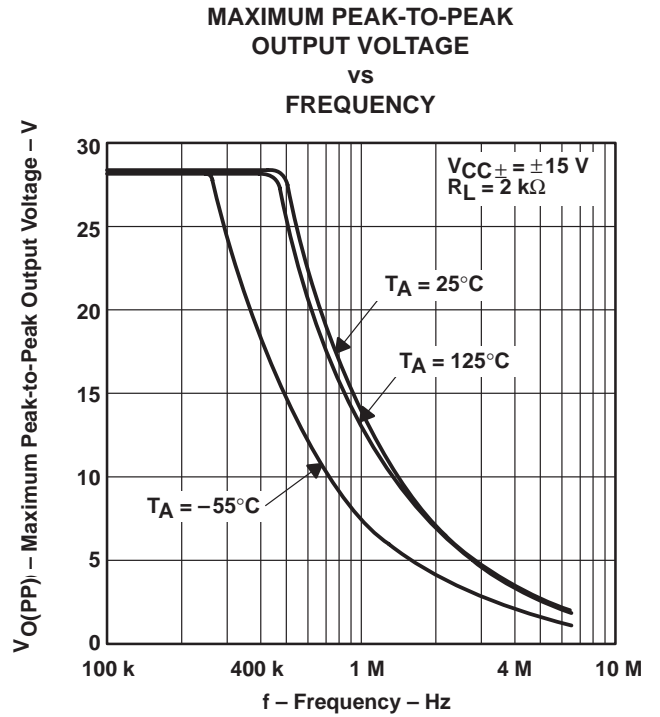


Figure 10

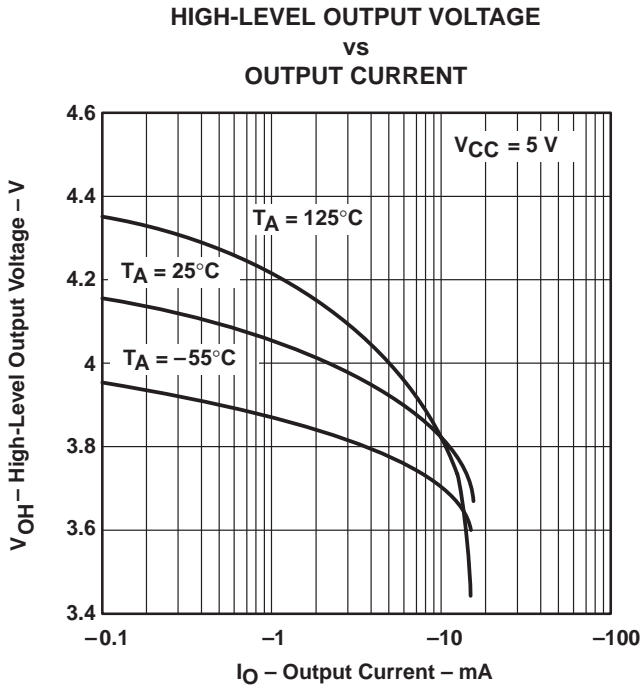


Figure 11

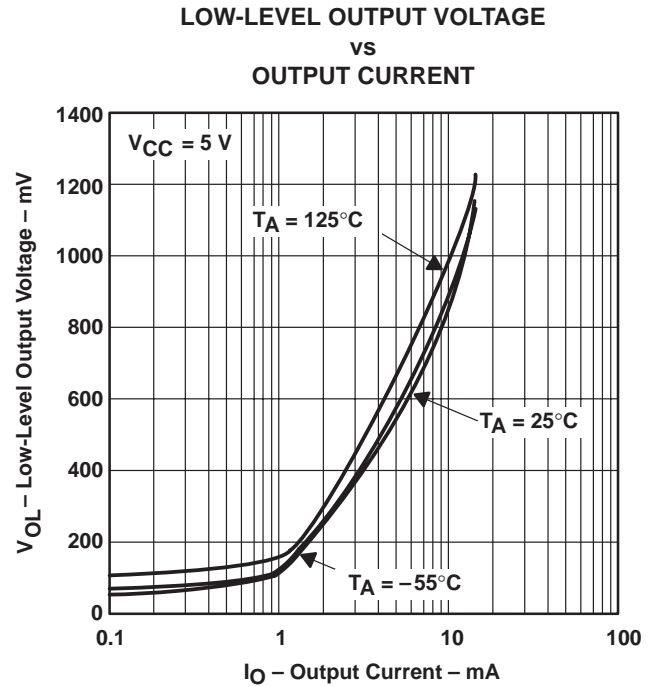


Figure 12



TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL  
 VOLTAGE AMPLIFICATION  
 VS  
 FREE-AIR TEMPERATURE

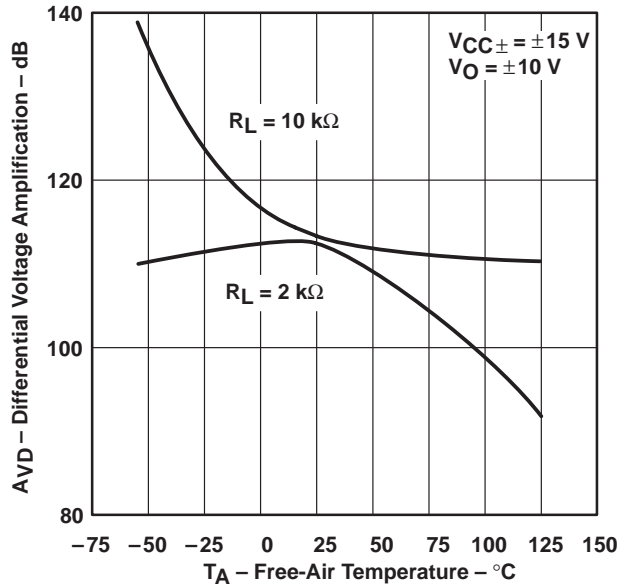


Figure 13

LARGE-SIGNAL DIFFERENTIAL VOLTAGE  
 AMPLIFICATION AND PHASE SHIFT  
 VS  
 FREQUENCY

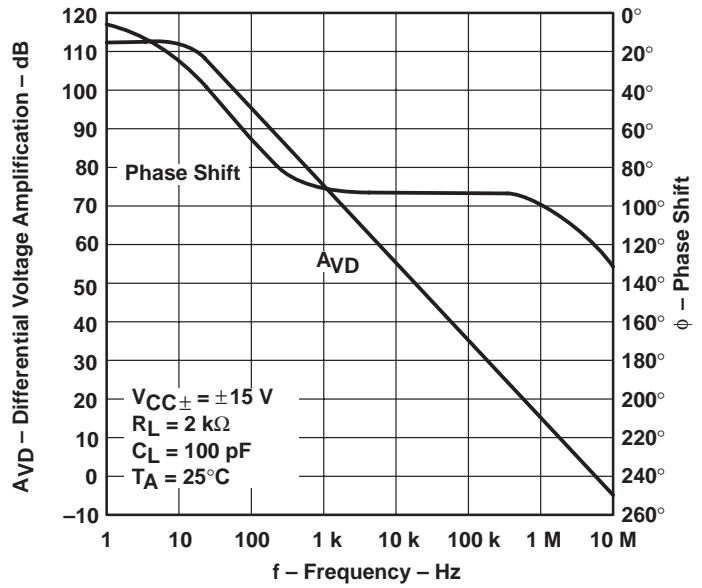


Figure 14

CLOSED-LOOP OUTPUT IMPEDANCE  
 VS  
 FREQUENCY

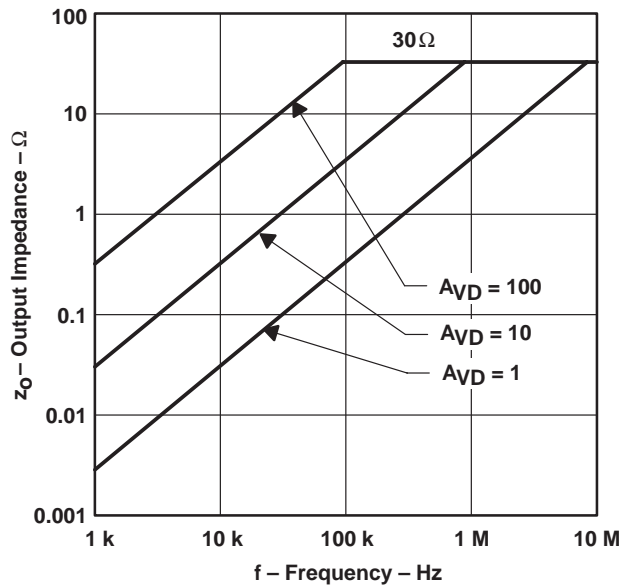


Figure 15

SHORT-CIRCUIT OUTPUT CURRENT  
 VS  
 FREE-AIR TEMPERATURE

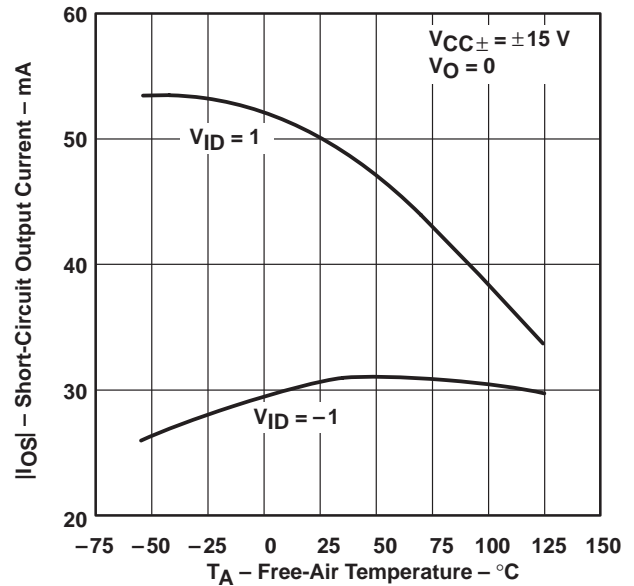
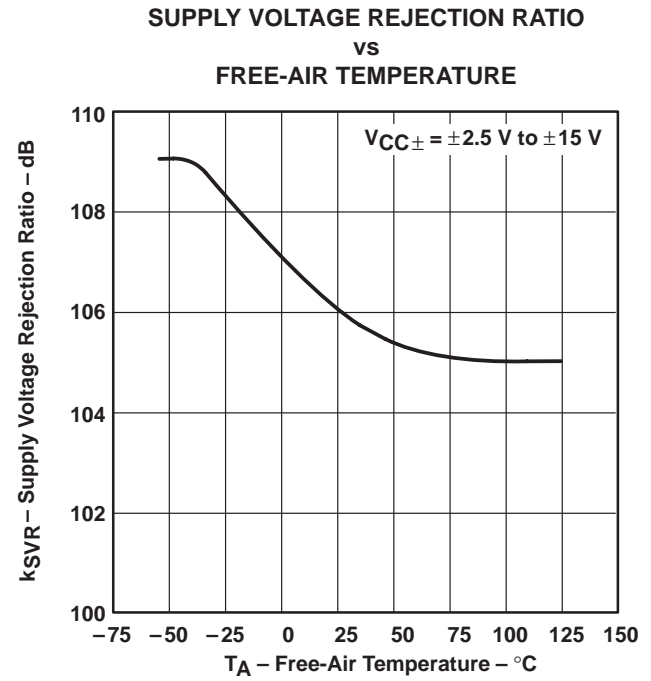
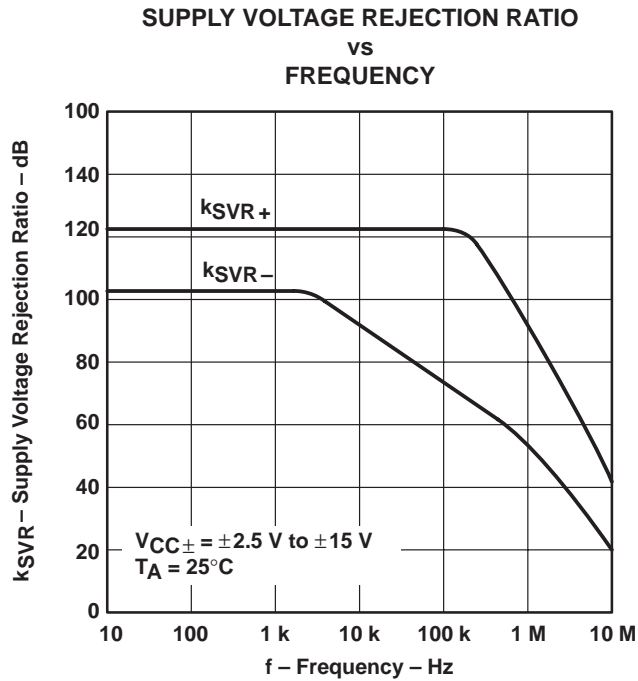
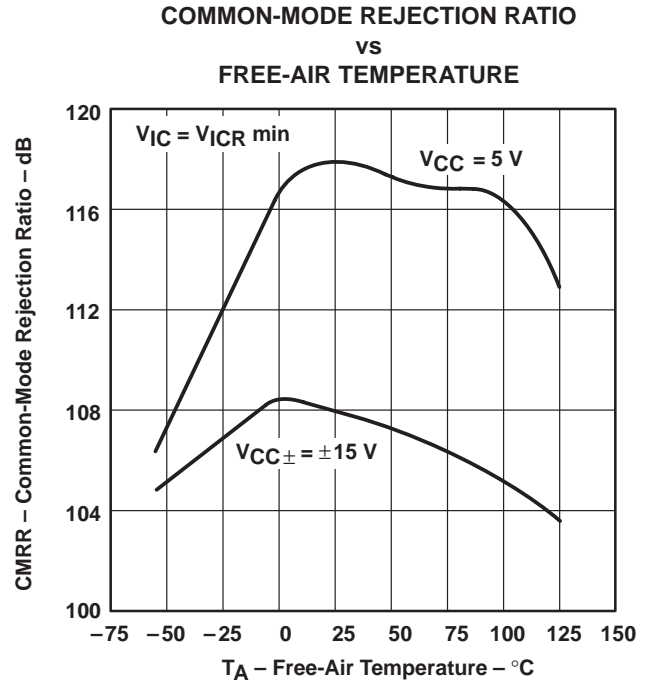
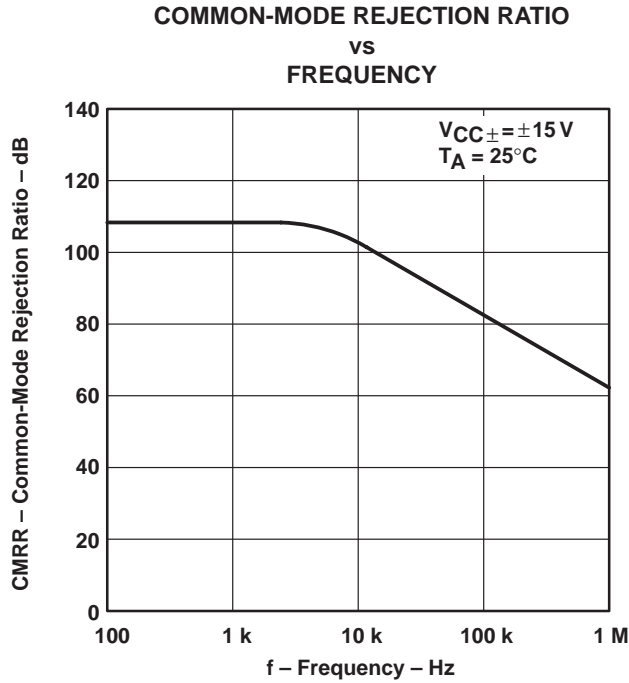


Figure 16

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

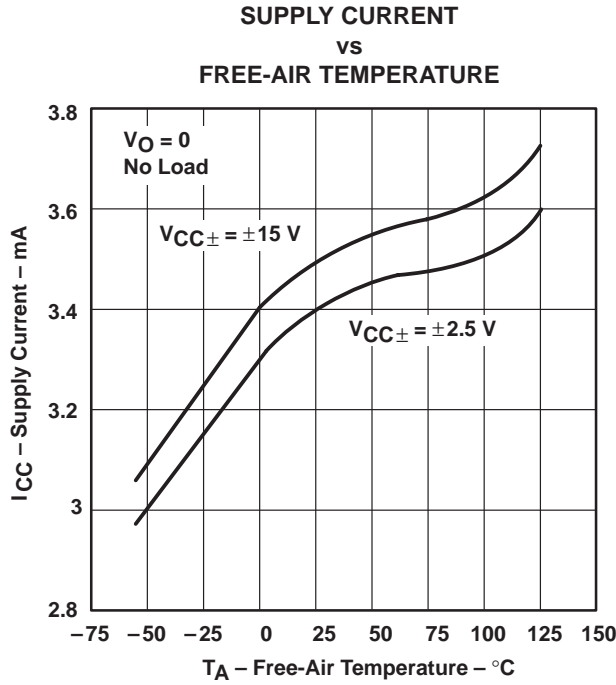


Figure 21

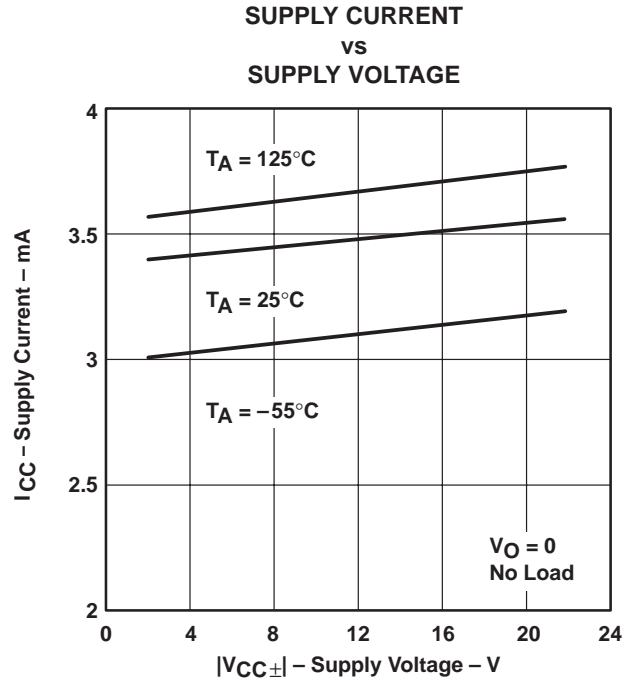


Figure 22

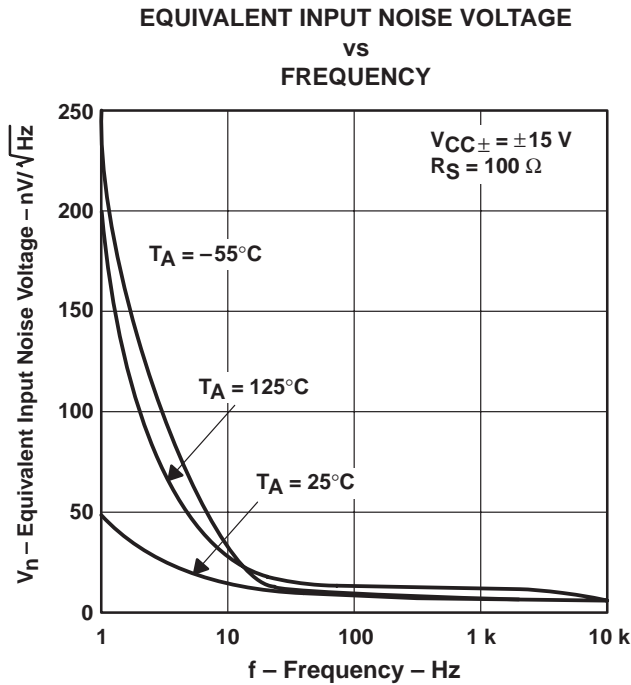


Figure 23

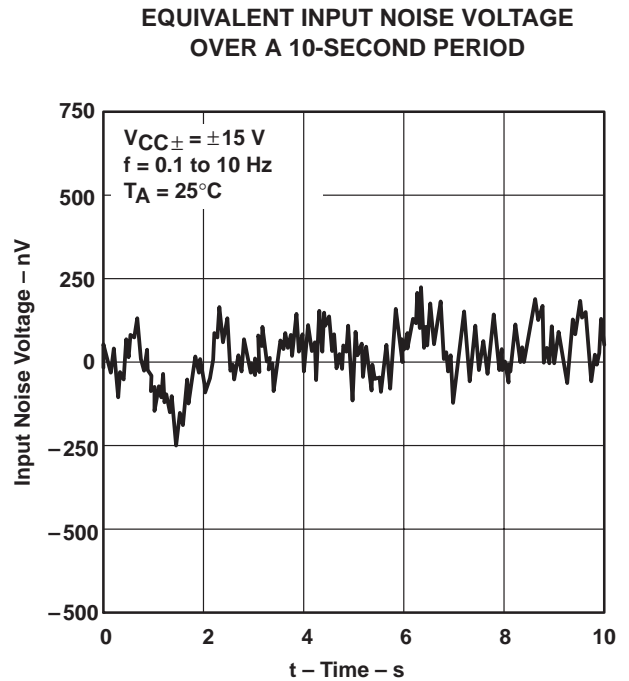
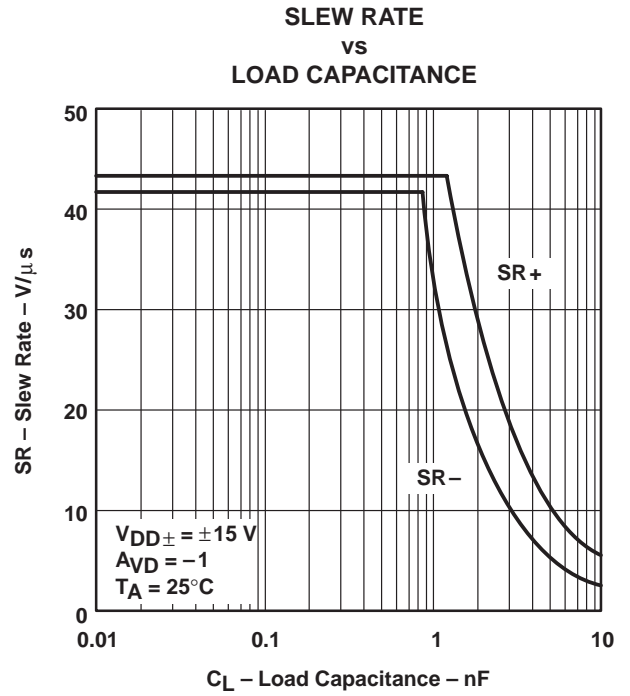
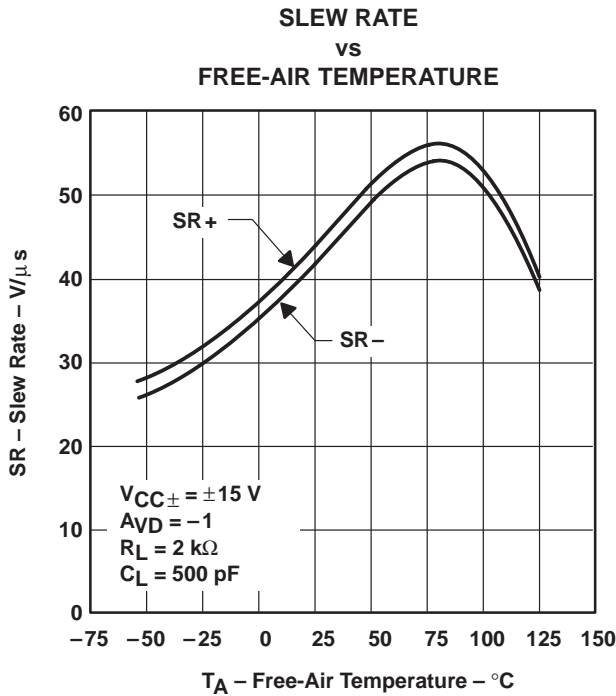
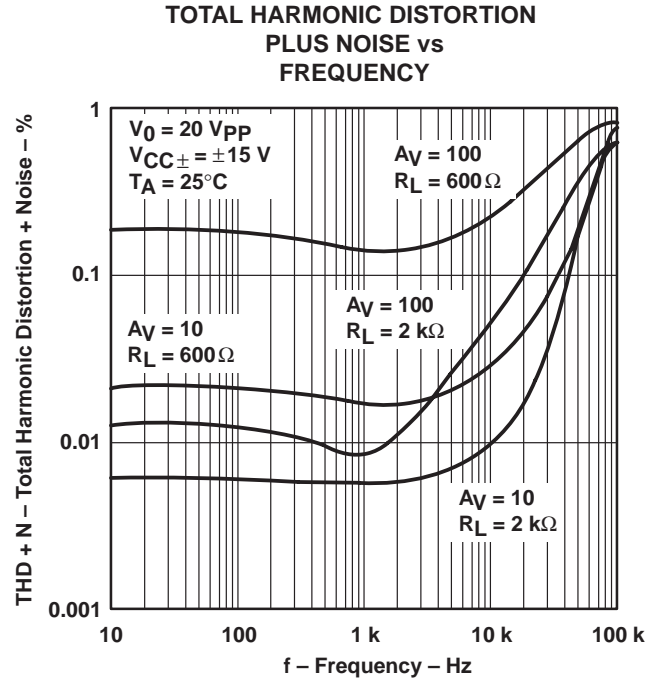
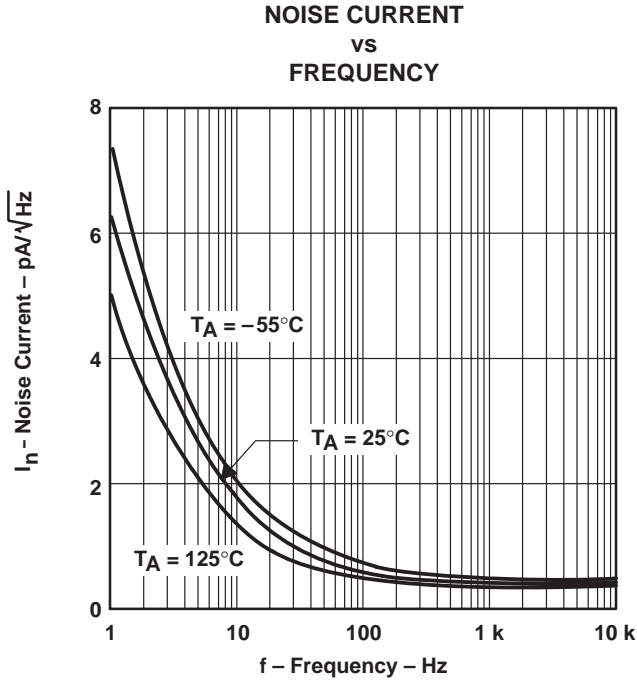
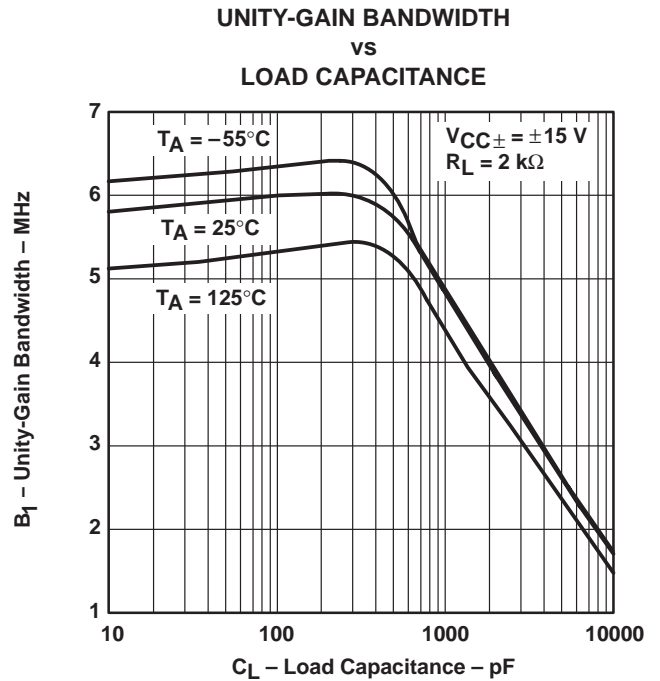
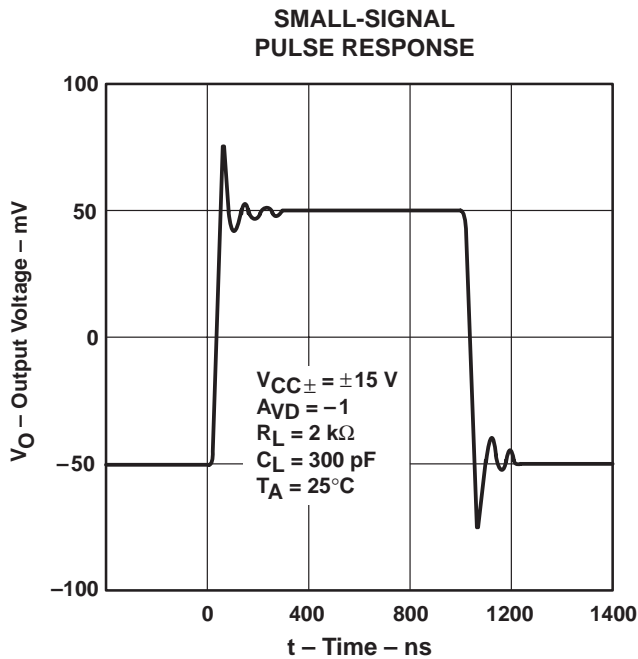
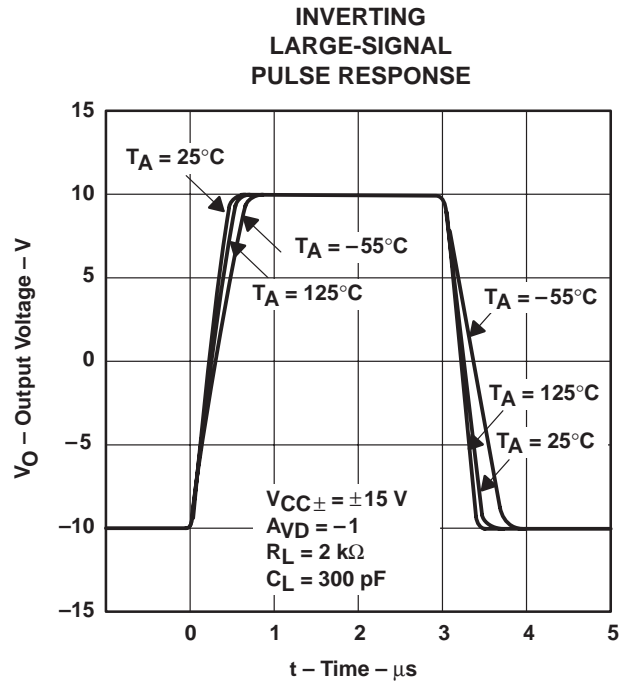
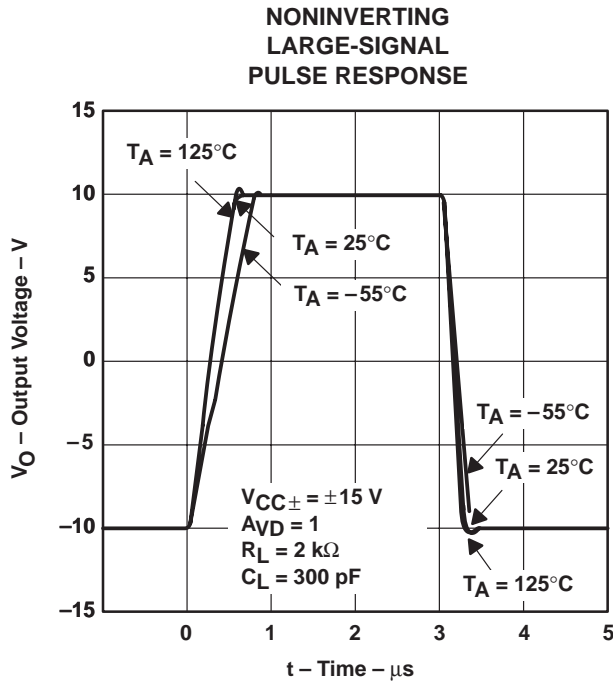


Figure 24

TYPICAL CHARACTERISTICS



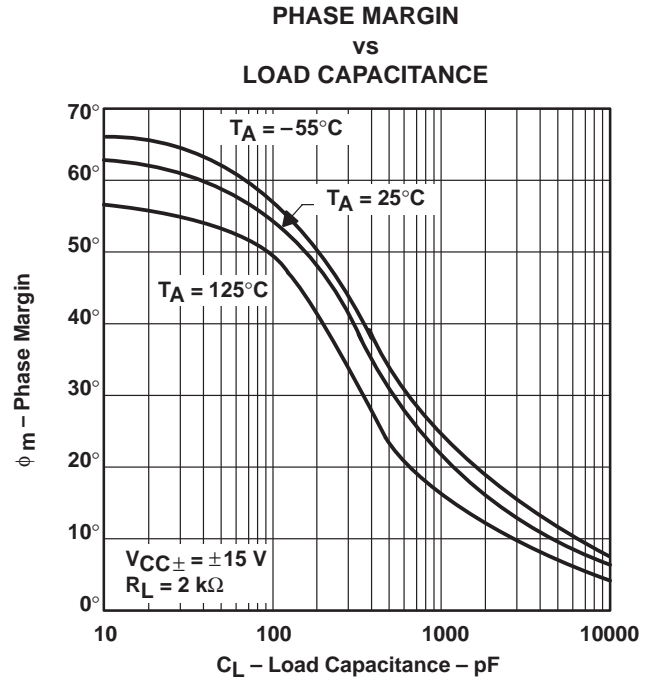
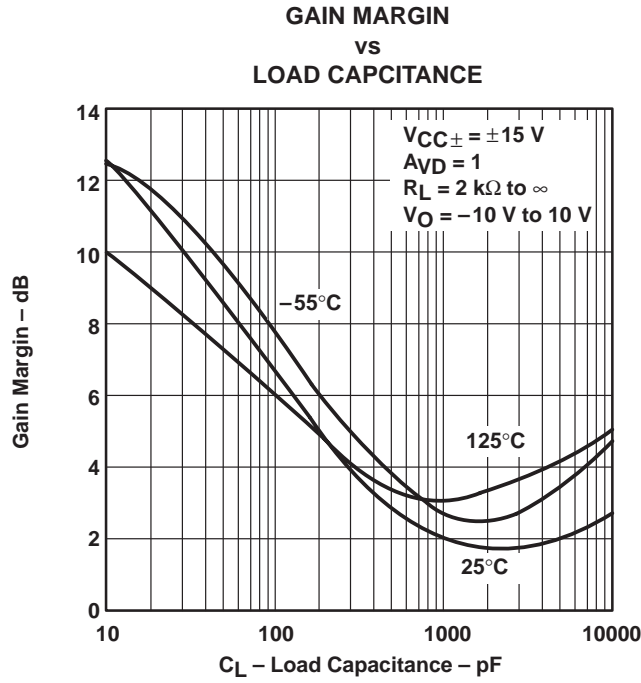
TYPICAL CHARACTERISTICS



**TLE2141M, TLE2141AM**  
**EXCALIBUR LOW-NOISE HIGH-SPEED**  
**PRECISION OPERATIONAL AMPLIFIERS**

SGLS059 – NOVEMBER 1990 – REVISED OCTOBER 1991

**TYPICAL CHARACTERISTICS**



**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">5962-9321601QPA</a>	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9321601QPA TLE2141M
<a href="#">5962-9321602QPA</a>	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9321602QPA TLE2141AM
<a href="#">TLE2141AMJGB</a>	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9321602QPA TLE2141AM
TLE2141AMJGB.A	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9321602QPA TLE2141AM
<a href="#">TLE2141MDG4</a>	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2141M
TLE2141MDG4.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2141M
<a href="#">TLE2141MDRG4</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2141M
TLE2141MDRG4.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2141M
<a href="#">TLE2141MJGB</a>	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9321601QPA TLE2141M
TLE2141MJGB.A	Active	Production	CDIP (JG)   8	50   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9321601QPA TLE2141M

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF TLE2141AM, TLE2141M :**

- Catalog : [TLE2141A](#), [TLE2141](#)
- Automotive : [TLE2141-Q1](#)
- Enhanced Product : [TLE2141-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLE2141MDG4	D	SOIC	8	75	505.46	6.76	3810	4
TLE2141MDG4.A	D	SOIC	8	75	505.46	6.76	3810	4



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

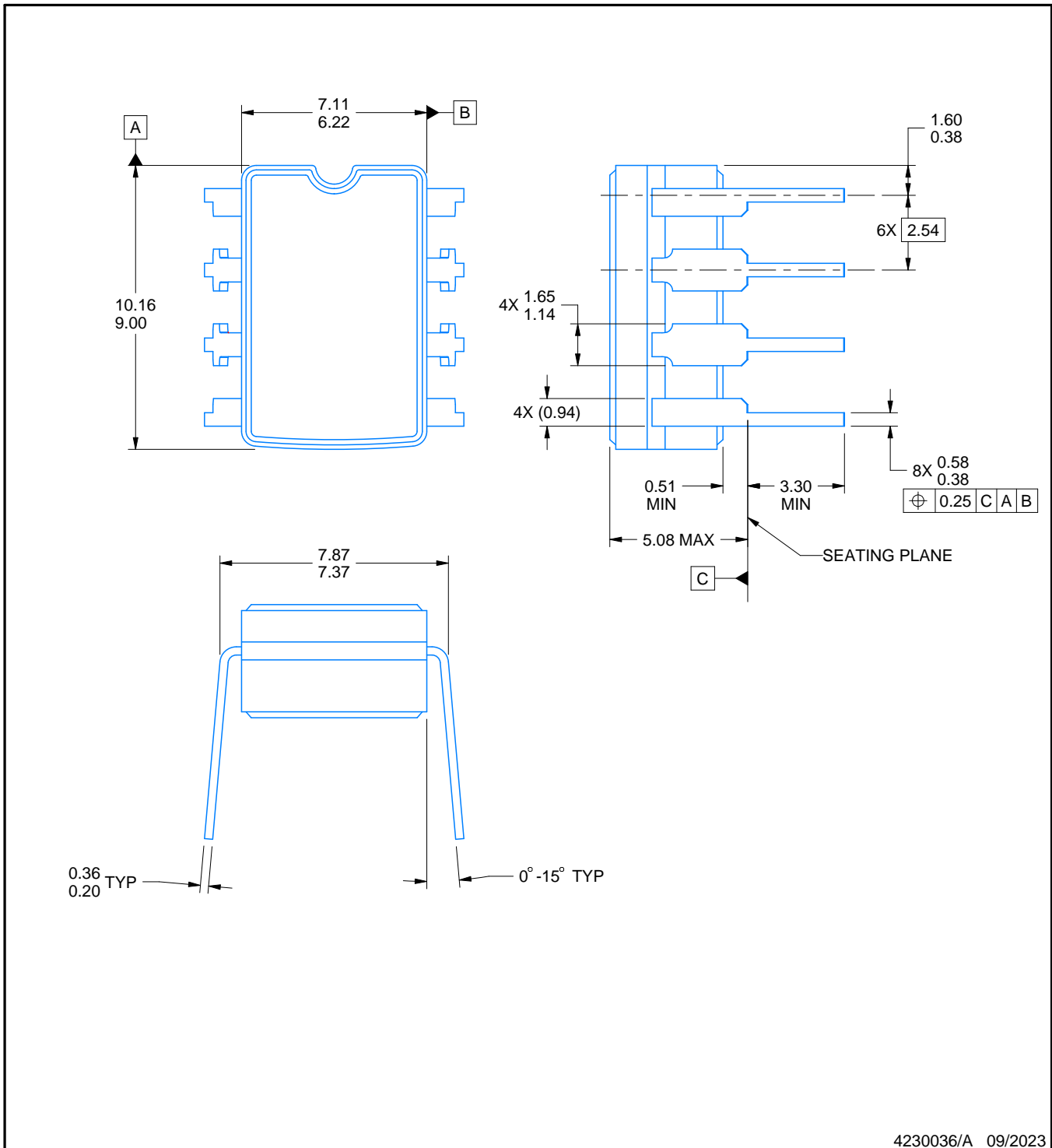
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## JG0008A

### CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

#### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8



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