TLV904xD 3.1MHz, 16µA Micro-Power, 1.2V Low Voltage, Decompensated RRIO Amplifier for Power Conscious Applications

1 Features

- Wide Gain bandwidth product: 3.1MHz
- Low quiescent current: 16µA/ch
- Operational from supply voltage as low as 1.2V
- Low integrated noise (0.1Hz - 10Hz): 4.5µV_{p-p}
- Low input offset voltage: ±0.5mV
- Low input bias current: 1pA
- Rail-to-rail input and output
- Decompensated, Gain ≥ 10V/V (Stable)
- Integrated RFI and EMI filters
- Extended industrial temperature range: –40°C to 125°C
- For unity gain stable version, see: TLV9041/TLV9042/TLV9044

2 Applications

- Portable Electronics
- Flow Transmitter
- Smoke Detector
- Active Filters
- Audio Microphone Preamplifier
- Low Side Current Sensing
- Temperature Transmitter
- Pressure Transmitter
- Motion detector (PIR, uWave, etc.)
- Pulse Oximeter

3 Description

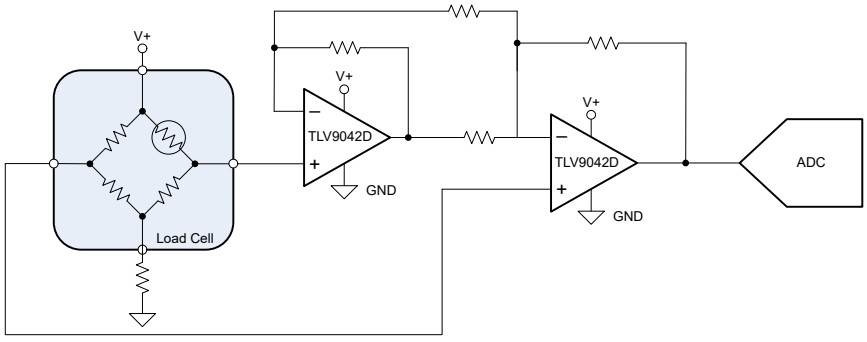
The TLV904xD family includes single (TLV9041D) and dual (TLV9042D) decompensated operational amplifiers optimized for high efficiency in ultra-low-voltage applications. Operating from 1.2V to 5.5V with rail-to-rail input and output swing, this family of amplifiers deliver an exceptional gain bandwidth of 3.1MHz with only 16µA of quiescent current. The TLV904xD enables high gain circuit configurations and longevity in battery powered systems. The availability of miniature packages also allow this amplifier family to be used effectively in high density board applications.

The TLV904xD is among the few amplifiers in the industry capable of operating at supply voltages as low as 1.2V, making the family well suited for 1.5V coin cell applications. The high gain bandwidth eliminates the need for cascaded amplifier stages in signal conditioning and filtering applications such as field transmitters, motion detectors, and personal electronics, simplifying design while reducing both board space and overall system power consumption.

Package Information

PART NUMBER	CHANNEL COUNT	PACKAGE(2)	PACKAGE SIZE(3)
TLV9041D	Single	DBV (SOT-23, 5) (1)	2.9mm × 2.8mm
		DCK (SC70, 5)	2mm × 1.25mm
		DQN (SOT-5X3, 5) (1)	1mm × 1mm
TLV9042D	Dual	D (SOIC, 8)	4.9mm × 6mm
		DSG (WSON, 8) (1)	2mm × 2mm
		DGK (VSSOP, 8)	3mm × 4.9mm

(1) Part number is preview only.
(2) For more information, see Section 12.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



Bridge Amplifier Circuit

Table of Contents

4 Pin Configuration and Functions

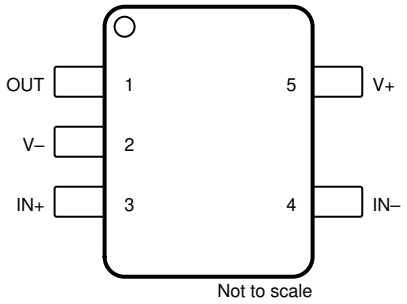


Figure 4-1. TLV9041D DBV Package
5-Pin SOT-23
Top View

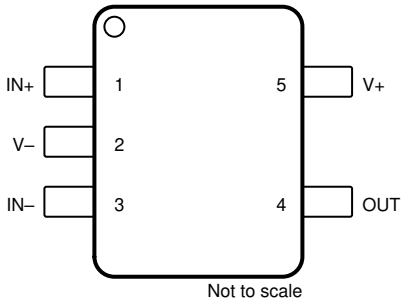


Figure 4-2. TLV9041 DCK Package
5-Pin SC70
Top View

Pin Functions: TLV9041D

PIN			I/O	DESCRIPTION
NAME	NO.			
	SOT-23	SC70		
IN–	4	3	I	Inverting input
IN+	3	1	I	Noninverting input
OUT	1	4	O	Output
V–	2	2	I	Negative (low) supply or ground (for single-supply operation)
V+	5	5	I	Positive (high) supply

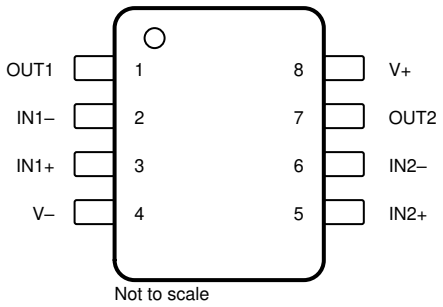
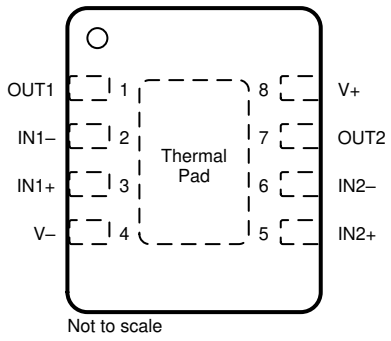


Figure 4-3. TLV9042D D and DGK Packages
8-Pin SOIC and VSSOP
Top View



Connect exposed thermal pad to V–. See Figure 4-4 for more information.

Figure 4-4. TLV9042D DSG Package
8-Pin WSON With Exposed Thermal Pad
Top View

Pin Functions: TLV9042D

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V–	4	I	Negative (low) supply or ground (for single-supply operation)
V+	8	I	Positive (high) supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	6.0	V
Signal input pins	Common-mode voltage (2)	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage (2)		V_S + 0.2	V
	Current (2)	–10	10	mA
Output short-circuit (3)		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.
(3) Short-circuit to ground, one amplifier per package.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	1.2	5.5	V
V_I	Input voltage range	(V–)	(V+)	V
T_A	Specified temperature	–40	125	°C

5.4 Thermal Information for Single Channel

THERMAL METRIC (1)		TLV9041D DBV (SOT-23) 5 PINS	TLV9041D DCK (SC70) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	228.0	259.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	127.7	159.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	93.6	107.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	63.3	63.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	93.4	106.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the application note, *Semiconductor and IC Package Thermal Metrics*

5.5 Thermal Information for Dual Channel

THERMAL METRIC (1)		TLV9042D			UNIT
		D (SOIC)	DSG (WSON)	DGK (VSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	147.0	98.9	160.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	86.5	117.7	77.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	92.3	35.5	97.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	32.2	11.5	14.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	91.7	60.1	97.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	41.5	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the application note, *Semiconductor and IC Package Thermal Metrics*.

5.6 Electrical Characteristics

For V_S = (V+) – (V–) = 1.2 V to 5.5 V (±0.6 V to ±2.75 V) at T_A = 25°C, R_F = 180kΩ, G = 10 V/V, R_L = 100 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±0.5	±1.8	mV
			T_A = –40°C to 125°C			±2	
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to 125°C		±0.4		µV/°C
PSRR	Input offset voltage versus power supply	V_S = ±0.6V to ±2.75V , V_{CM} = V–		80	95		dB
INPUT BIAS CURRENT							
I_B	Input bias current (1)				±0.5	±12	pA
I_{OS}	Input offset current (1)				±0.5	±2.5	pA
NOISE							
E_N	Input voltage noise	f = 0.1 to 10Hz			4.5		μV_{PP}
e_N	Input voltage noise density	f = 100Hz			55		nV/√Hz
		f = 1kHz			36		
		f = 10kHz			33		
i_N	Input current noise (2)	f = 1kHz			10		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–)		(V+)	V
CMRR	Common-mode rejection ratio	(V–) < V_{CM} < (V+) – 0.7V, V_S = 1.2V	T_A = –40°C to 125°C	65	80		dB
		(V–) < V_{CM} < (V+) – 0.7V, V_S = 5.5V		76	89		
		(V–) < V_{CM} < (V+), V_S = 1.2V			60		
		(V–) < V_{CM} < (V+), V_S = 5.5V		58	72		
INPUT IMPEDANCE							
Z_{ID}	Differential				80 || 2		GΩ || pF
Z_{ICM}	Common-mode				100 || 1		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 1.2V, (V–) + 0.2V < V_O < (V+) – 0.2V, R_L = 10kΩ to V_S / 2	T_A = –40°C to 125°C		100		dB
		V_S = 5.5V, (V–) + 0.2V < V_O < (V+) – 0.2V, R_L = 10kΩ to V_S / 2			127		
		V_S = 1.2V, (V–) + 0.1V < V_O < (V+) – 0.1V, R_L = 100kΩ to V_S / 2			110		
		V_S = 5.5V, (V–) + 0.1V < V_O < (V+) – 0.1V, R_L = 100kΩ to V_S / 2		109	125		
FREQUENCY RESPONSE							
THD+N	Total harmonic distortion + noise (3)	V_S = 5.5V, V_{CM} = 2.75V, V_O = 1V_{RMS}, G = +10, f = 1kHz, R_L = 100kΩ to V_S / 2			0.02		%
GBW	Gain-bandwidth product	G = 100V/V, R_F = 1.8MΩ, R_L = 1MΩ connected to V_S/2			3.1		MHz
SR	Slew rate	V_S = 5.5V, G = +10, C_L = 10pF, TLV9041D	V_S = 5.5 V, G = +10, C_L = 10 pF		1.5		V/µs
SR	Slew rate	V_S = 5.5 V, G = +10, C_L = 10 pF, TLV9042D			0.8		V/µs
t_S	Settling time	To 0.1%, V_S = 5.5V, V_{STEP} = 400mV, G = +10, C_L = 10 pF			23		µs
		To 0.1%, V_S = 5.5V, V_{STEP} = 200mV, G = +10, C_L = 10pF			22		
		To 0.01%, V_S = 5.5V, V_{STEP} = 400mV, G = +10, C_L = 10pF			32		
		To 0.01%, V_S = 5.5V, V_{STEP} = 200mV, G = +10, C_L = 10pF			31		
	Phase margin	C_L = 10pF			72		°
	Overload recovery time	V_{IN} × gain > V_S (TLV9041D)	V_{IN} × gain > V_S		5		µs

For V_S = (V+) – (V–) = 1.2 V to 5.5 V (±0.6 V to ±2.75 V) at T_A = 25°C, R_F = 180kΩ, G = 10 V/V, R_L = 100 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Overload recovery time	V_{IN} × gain > V_S (TLV9042D)			11		µs
EMIRR	Electro-magnetic interference rejection ratio	f = 1GHz, V_{IN_EMIRR} = 100mV			89		dB
OUTPUT							
	Voltage output swing from rail	Positive rail headroom	V_S = 1.2V, R_L = 100kΩ to V_S / 2		0.75	7	mV
			V_S = 5.5V, R_L = 10kΩ to V_S / 2		9	21	
			V_S = 5.5V, R_L = 100kΩ to V_S / 2		1	8	
		Negative rail headroom	V_S = 1.2V, R_L = 100kΩ to V_S / 2		0.75	5	
			V_S = 5.5V, R_L = 10kΩ to V_S / 2		8	21	
			V_S = 5.5V, R_L = 100kΩ to V_S / 2		0.85	8	
I_{SC}	Short-circuit current (4)	V_S = 5.5 V			±40		mA
Z_O	Open-loop output impedance	f = 10kHz			8250		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_S = 5.5V, I_O = 0A, , TLV9041D			16.5	21	µA
			T_A = –40°C to 125°C			22	
	Quiescent current per amplifier	V_S = 5.5V, I_O = 0A, TLV9042D			16	19.5	
			T_A = –40°C to 125°C			20	
	Power-on time	At T_A = 25°C, V_S = 5.5V, V_S ramp rate > 0.3V/µs			90		µs

(1) Max I_B and I_{OS} limits are specified based on characterization results. Input differential voltages greater than 2.5V can cause increased I_B
(2) Typical input current noise data is specified based on design simulation results
(3) Third-order filter; bandwidth = 80 kHz at –3 dB.
(4) Short circuit current is average of sourcing and sinking short circuit currents

5.7 Typical Characteristics

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, G = 10V/V, R_F= 180kΩ, R_L = 100kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

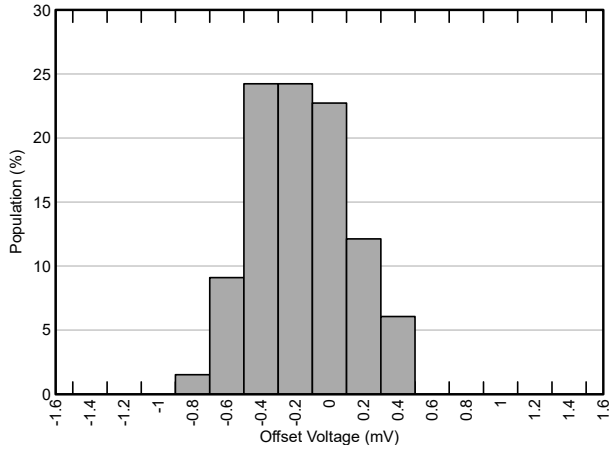


Figure 5-1. Offset Voltage Distribution Histogram

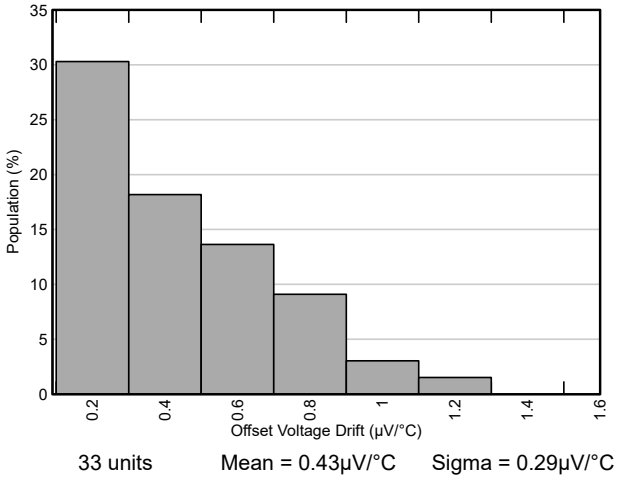


Figure 5-2. Offset Voltage Drift Distribution Histogram

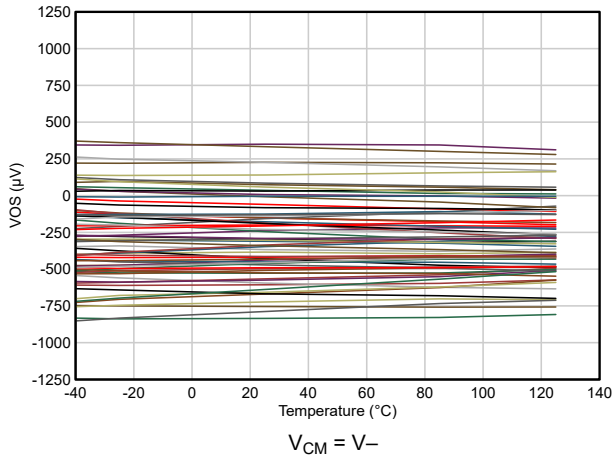


Figure 5-3. Input Offset Voltage vs Temperature

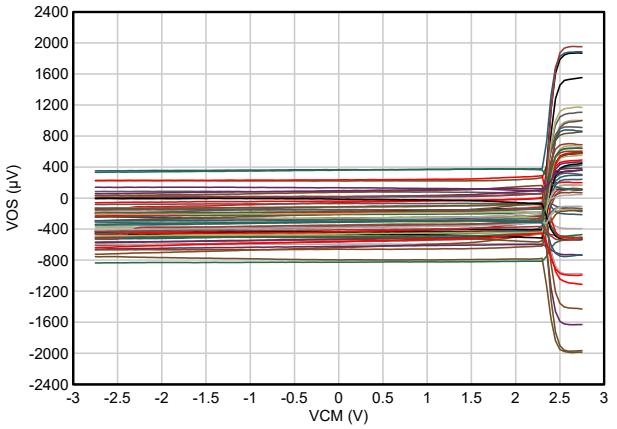
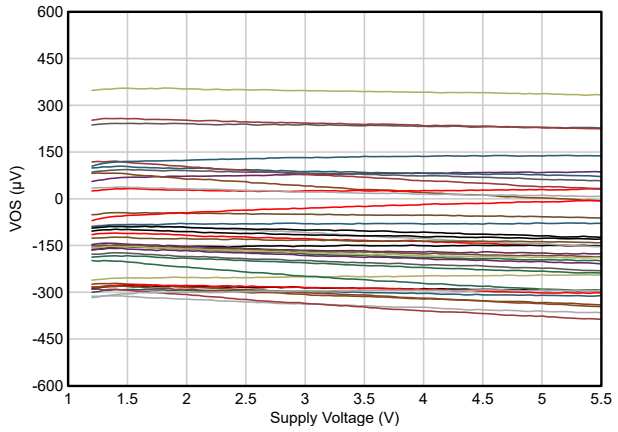


Figure 5-4. Offset Voltage vs Common-Mode

5.7 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, G = 10V/V, R_F= 180kΩ, R_L = 100kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V_{CM} = (V–)

Figure 5-5. Offset Voltage vs Supply Voltage

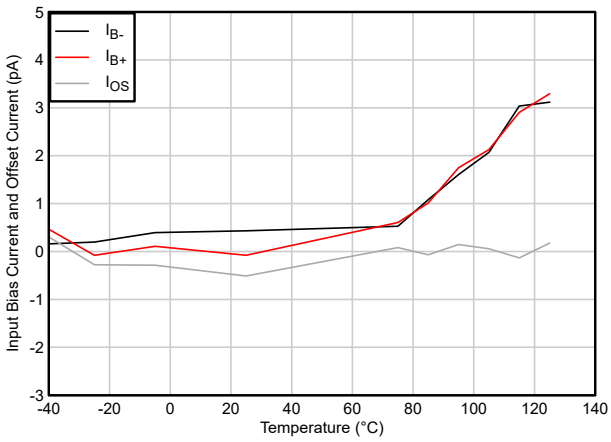


Figure 5-6. I_B and I_{OS} vs Temperature

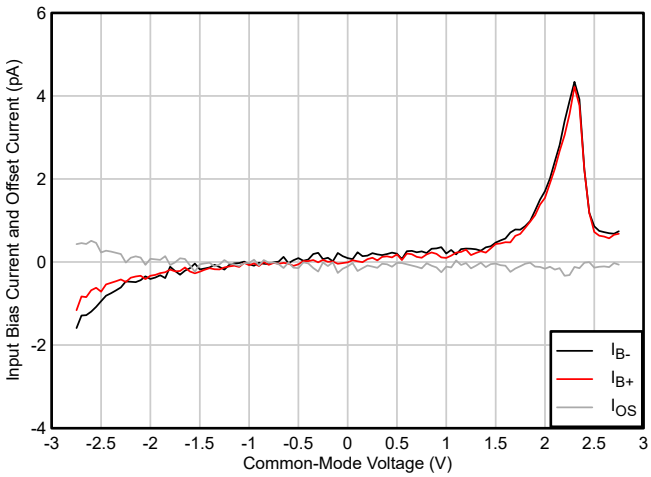


Figure 5-7. I_B and I_{OS} vs Common-Mode Voltage

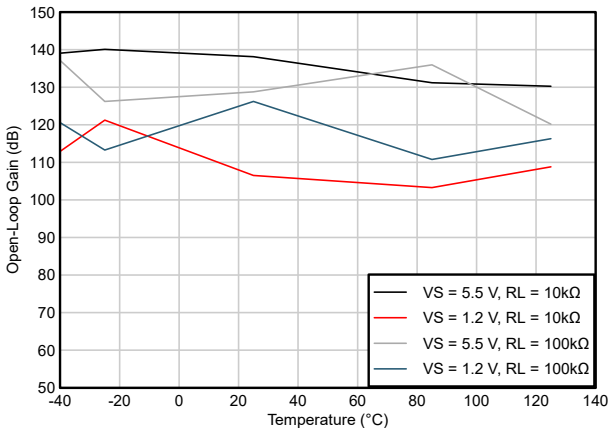
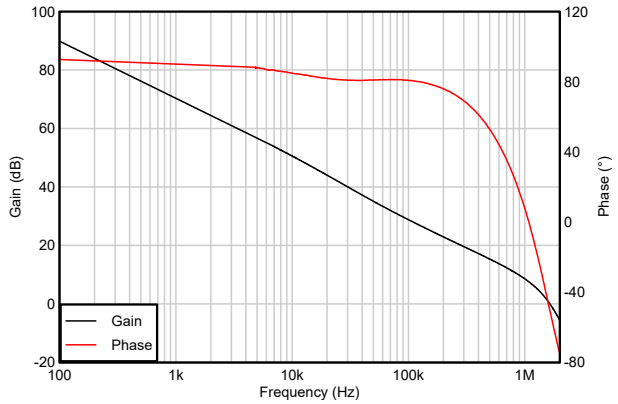


Figure 5-8. Open-Loop Gain vs Temperature



R_L = 1MΩ, C_L = 20pF

Figure 5-9. Open-Loop Gain and Phase vs Frequency

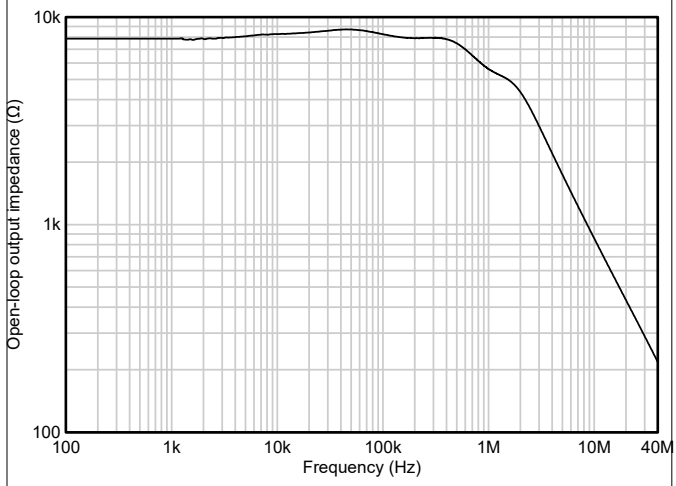
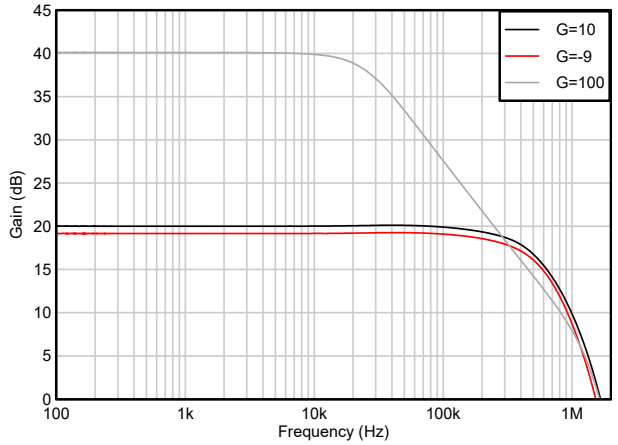


Figure 5-10. Open-Loop Output Impedance vs Frequency

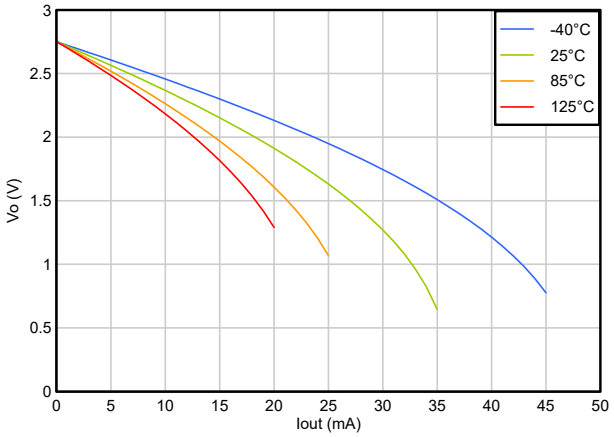
5.7 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, G = 10V/V, R_F= 180kΩ, R_L = 100kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



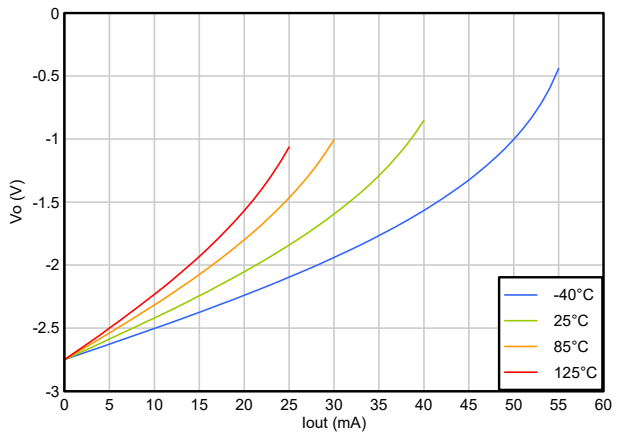
R_L = 100kΩ, C_L = 20pF

Figure 5-11. Closed-Loop Gain vs Frequency



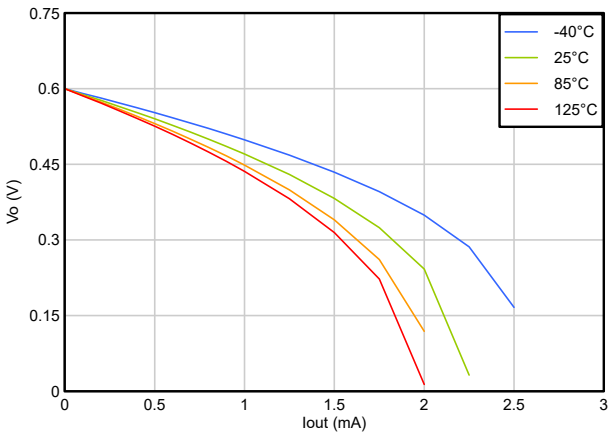
V+ = 2.75V, V– = –2.75V

Figure 5-12. Output Voltage vs Output Current (Claw)



V+ = 2.75V, V– = –2.75V

Figure 5-13. Output Voltage vs Output Current (Claw)

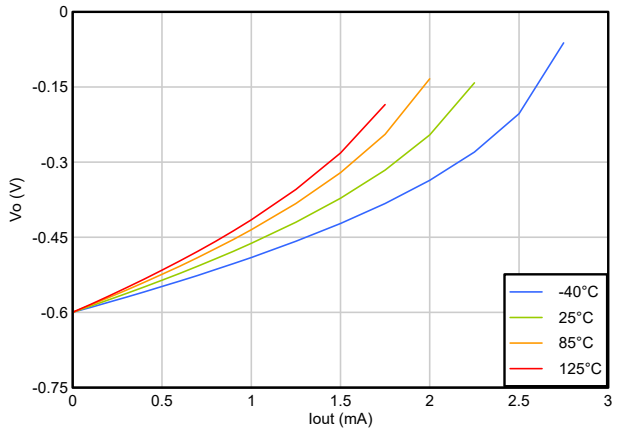


V+ = 0.6V, V– = –0.6V

Figure 5-14. Output Voltage vs Output Current (Claw)

5.7 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, G = 10V/V, R_F= 180kΩ, R_L = 100kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V+ = 0.6V, V– = –0.6V

Figure 5-15. Output Voltage vs Output Current (Claw)

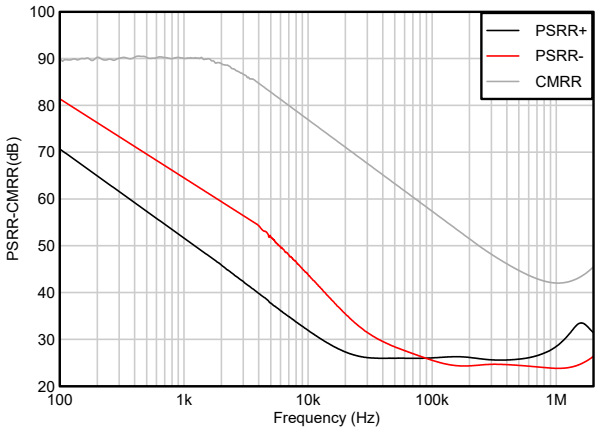
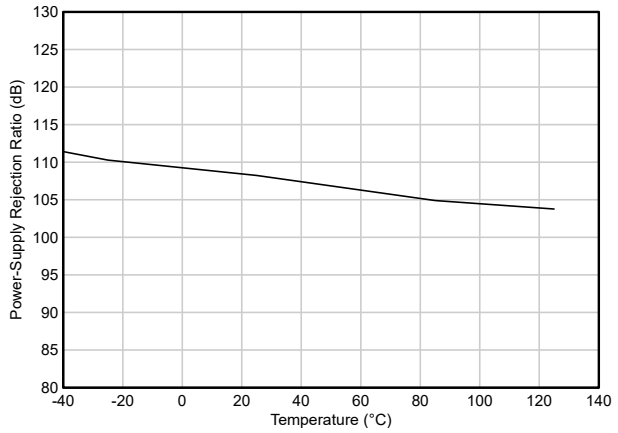


Figure 5-16. CMRR and PSRR vs Frequency



V_S = 1.2V to 5.5V

Figure 5-17. DC PSRR vs Temperature

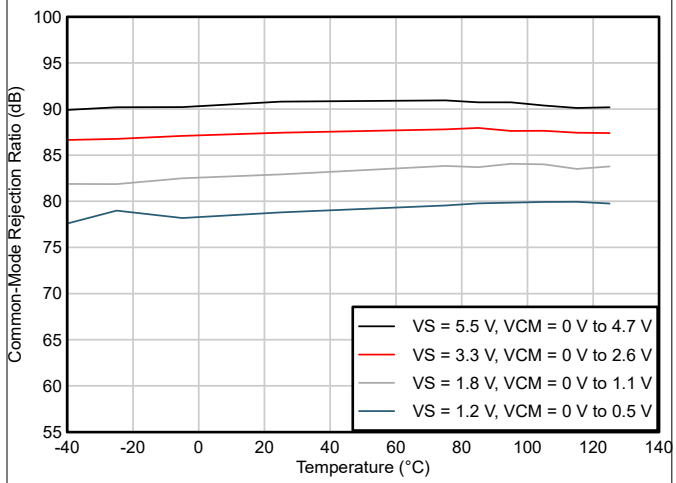


Figure 5-18. DC CMRR vs Temperature

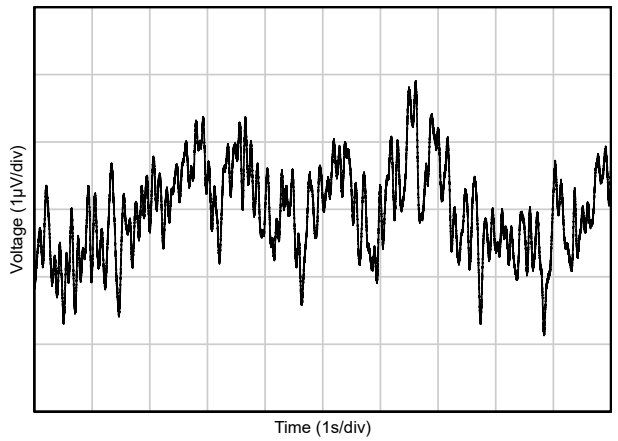


Figure 5-19. 0.1Hz to 10Hz Voltage Noise in Time Domain

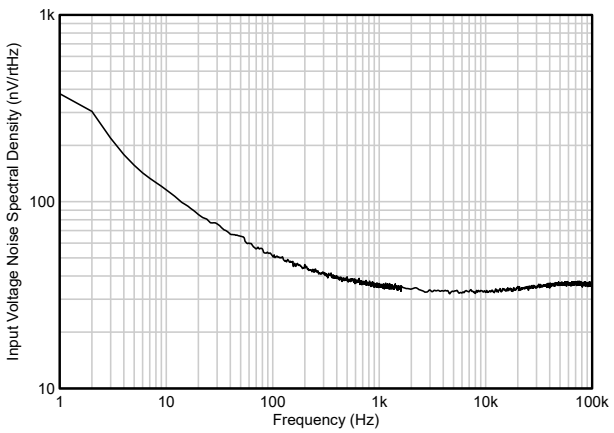
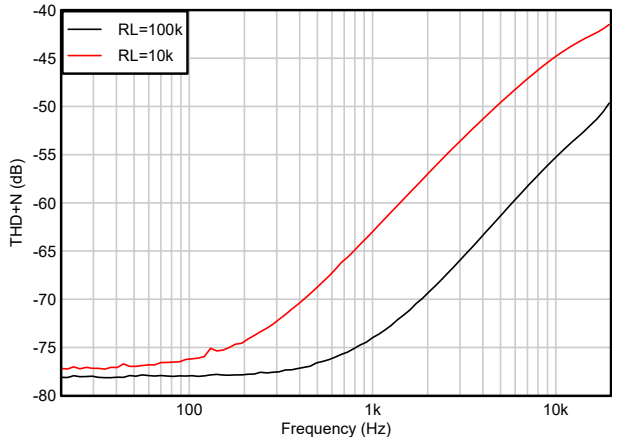


Figure 5-20. Input Voltage Noise Spectral Density

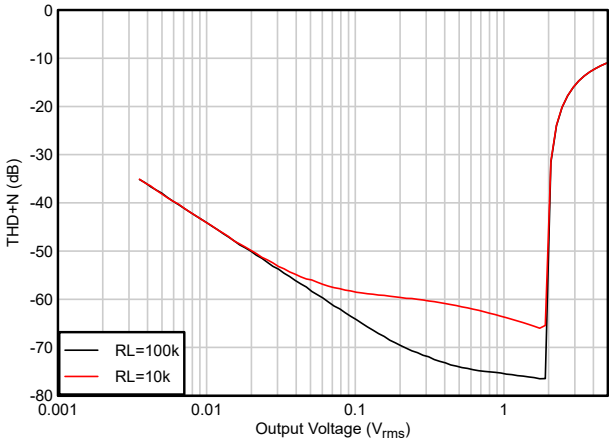
5.7 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, G = 10V/V, R_F= 180kΩ, R_L = 100kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



BW = 80kHz V_{OUT} = 1V_{RMS}

Figure 5-21. THD + N vs Frequency



BW = 80kHz f = 1kHz

Figure 5-22. THD + N vs Amplitude

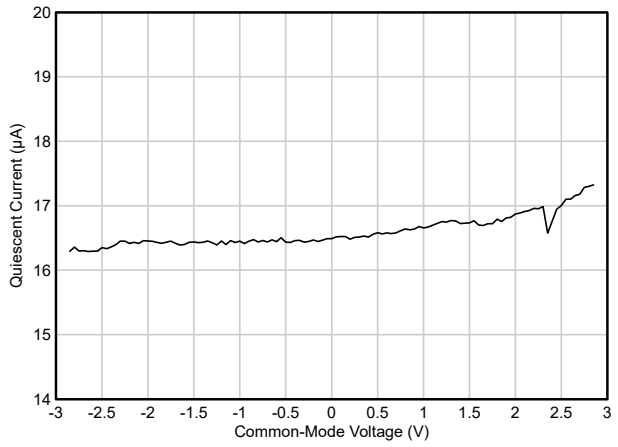


Figure 5-23. Quiescent Current vs Common-Mode

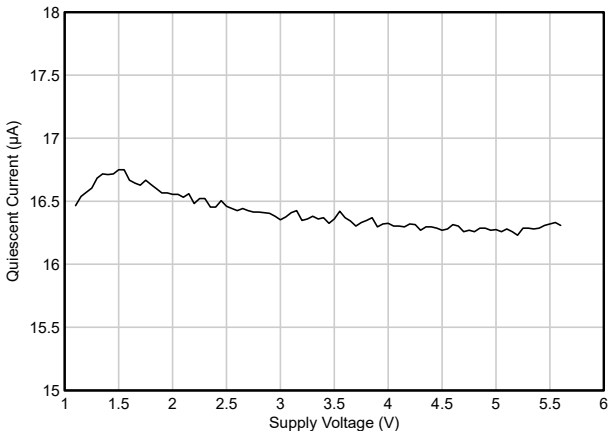


Figure 5-24. Quiescent Current vs Supply Voltage

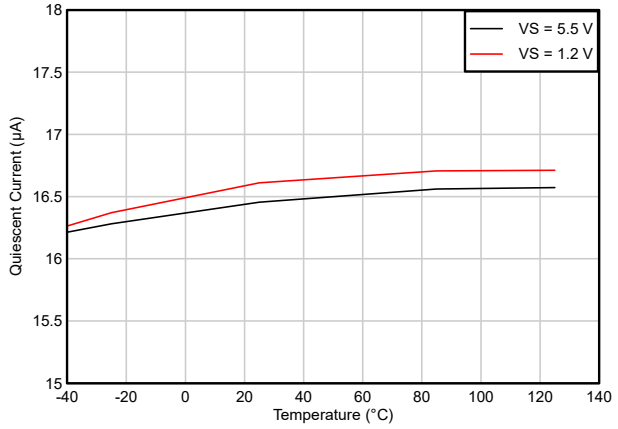


Figure 5-25. Quiescent Current vs Temperature

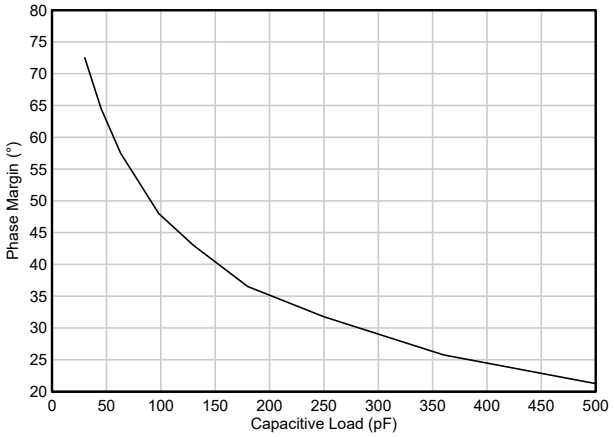
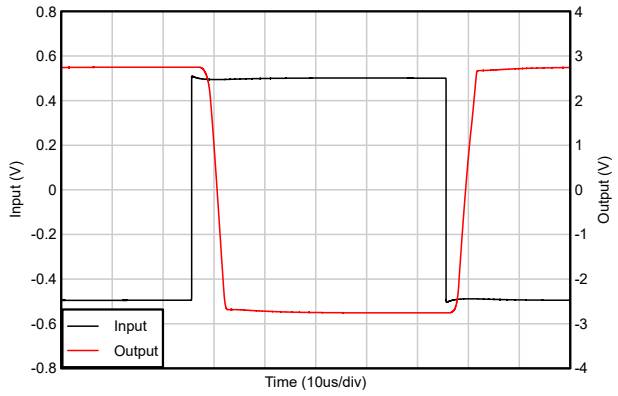


Figure 5-26. Phase Margin vs Capacitive Load

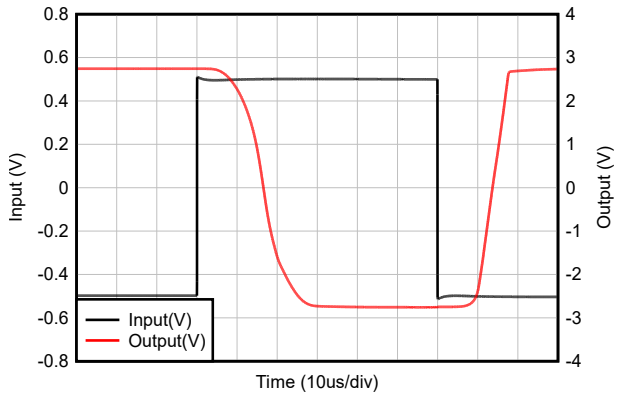
5.7 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, G = 10V/V, R_F= 180kΩ, R_L = 100kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



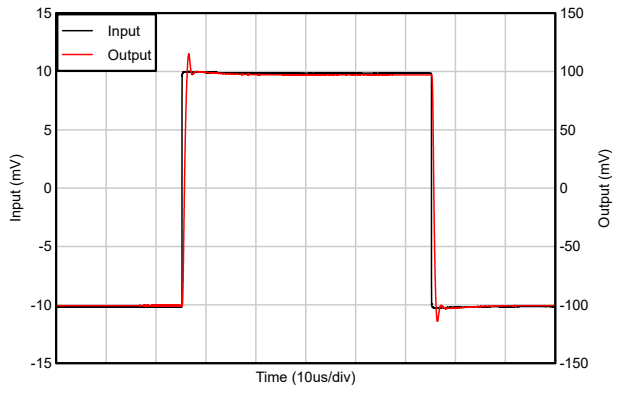
G = –10 V_{IN} = 500mV_{PP}

Figure 5-27. Overload Recovery (TLV9041D)



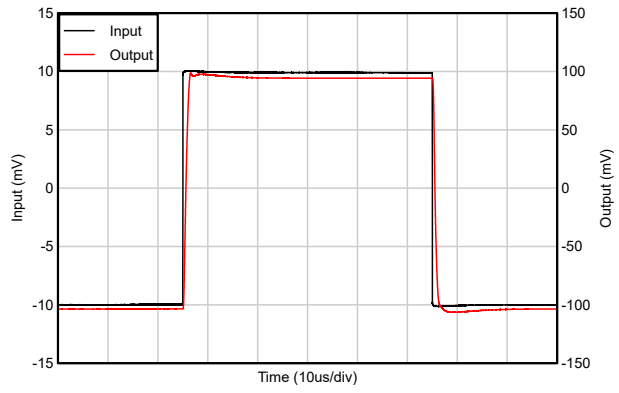
G = –10 V_{IN} = 500mV_{PP}

Figure 5-28. Overload Recovery (TLV9042D)



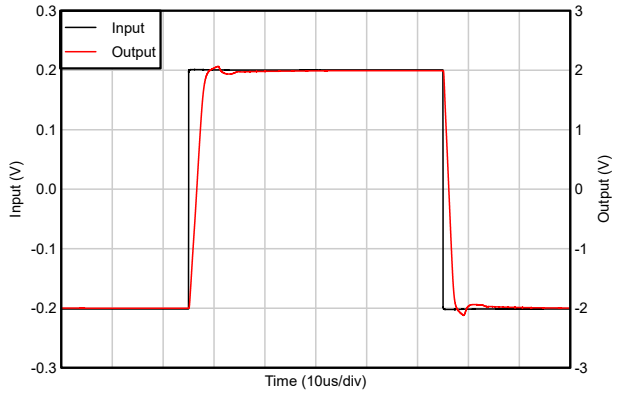
V_{IN} = 20mV_{PP}

Figure 5-29. Small-Signal Step Response (TLV9041D)



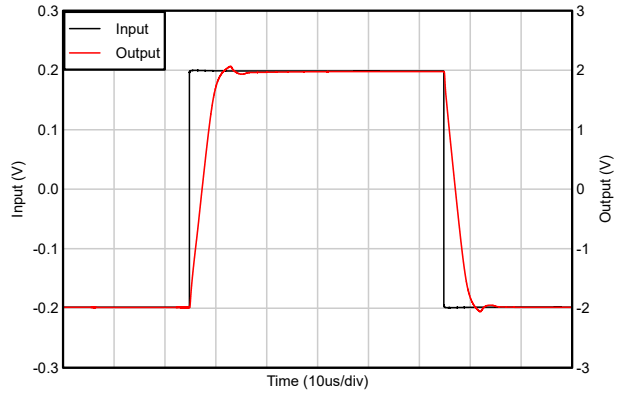
V_{IN} = 20mV_{PP}

Figure 5-30. Small-Signal Step Response (TLV9042D)



V_{IN} = 4V_{PP}

Figure 5-31. Large-Signal Step Response (TLV9041D)



V_{IN} = 4V_{PP}

Figure 5-32. Large-Signal Step Response (TLV9042D)

5.7 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, G = 10V/V, R_F= 180kΩ, R_L = 100kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

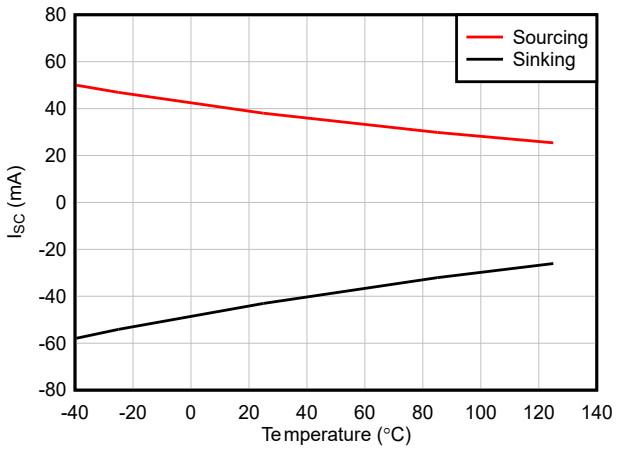


Figure 5-33. Short-Circuit Current vs Temperature

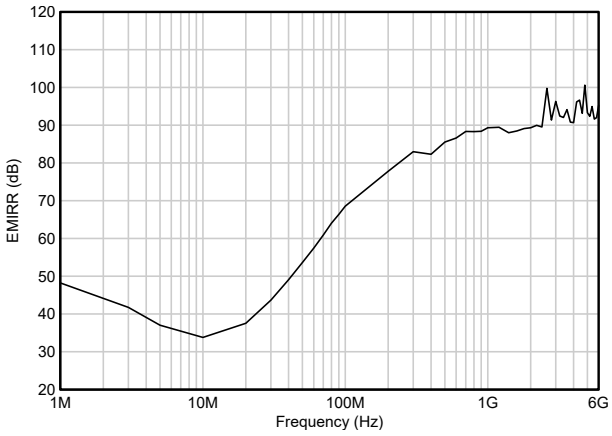


Figure 5-34. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

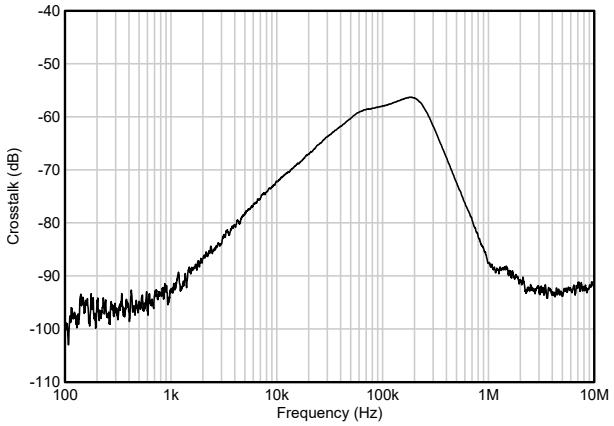


Figure 5-35. Channel Separation

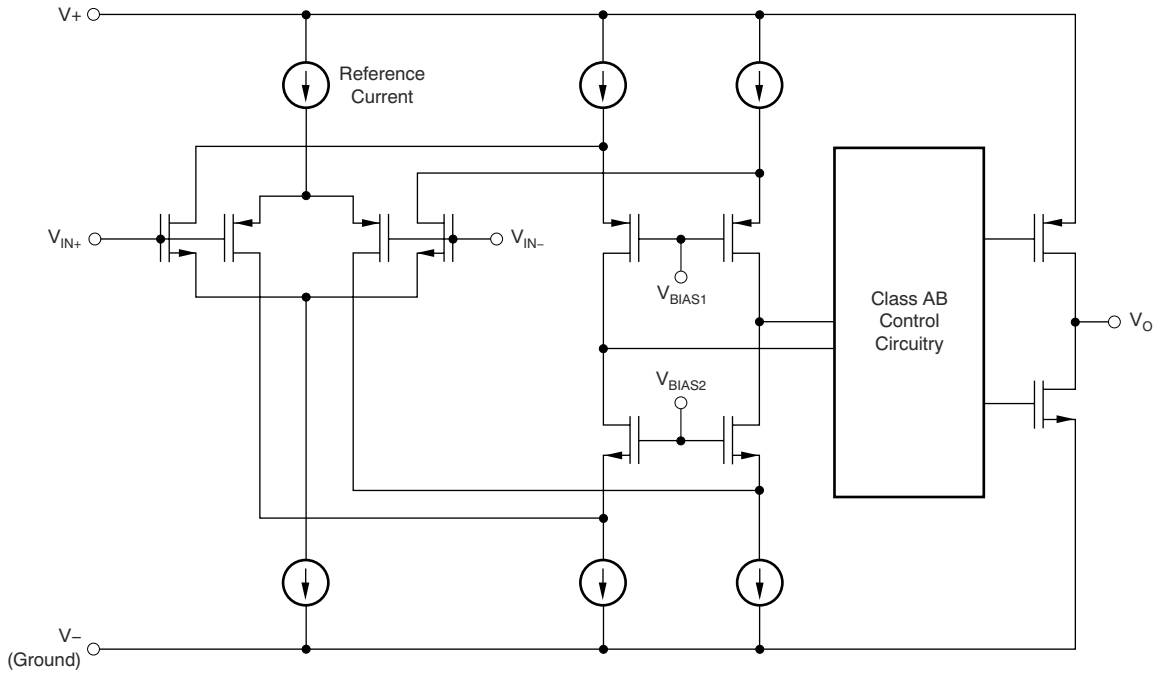
6 Detailed Description

6.1 Overview

The TLV904xD family of low-power, rail-to-rail input and output operational amplifiers is specifically designed for high-gain, battery-powered applications. This family of amplifiers utilizes a decompensated architecture that enables operation from an ultra-low supply voltage of 1.2V to a standard supply voltage of 5.5V and are optimized for use in noise gains of 10V/V or higher. The decompensated architecture provides 3.1MHz of gain-bandwidth product and up to 1.5V/µs of slew rate with around 16µA of quiescent current per channel, delivering superior AC performance compared to unity-gain stable architectures with similar power consumption. This eliminates the need for multiple cascaded amplifier stages in sensor signal conditioning and filtering applications, reducing both component count and total system power consumption.

The input common-mode voltage range includes both rails, allowing the TLV904xD series to be used in many single-supply or dual-supply configurations. The TLV904xD can drive capacitive loads up to 100pF at a gain of 10V/V and features 4.5µVp-p integrated noise (0.1Hz to 10Hz), enabling designers to achieve both improved AC performance and lower power consumption. The design also delivers good DC performance with 0.5mV input offset voltage (typical) and 0.5pA of input bias current (typical), along with good PSRR, CMRR, and AOL and features an integrated RFI and EMI rejection filter for reliable operation in electrically noisy environments.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Operating Voltage

The TLV904xD series of operational amplifiers is fully specified and ensured for operation from 1.2V to 5.5V. In addition, many specifications apply from –40°C to 125°C. Parameters that vary significantly with operating voltages or temperature are provided in Section 5.7. It is highly recommended to bypass power-supply pins with at least 0.01µF ceramic capacitors.

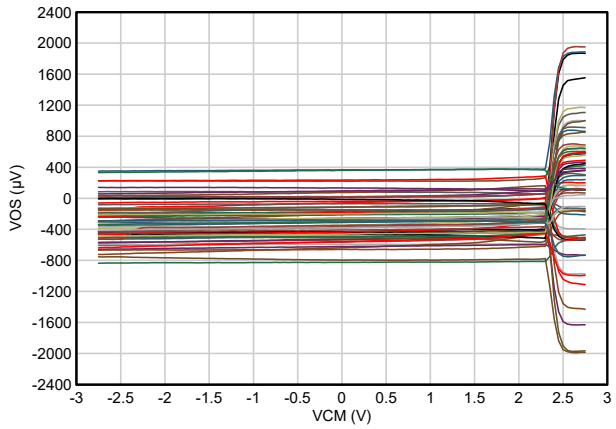
6.3.2 Rail-to-Rail Input and Output

The input common-mode voltage range of the TLV904xD extends to either supply rail, even when operating at ultra-low supply voltages as low as 1.2V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. Refer to Section 6.2 for more details.

For the TLV904xD, the P-channel pair is typically active for input voltages from the negative rail to (V+) – 0.4V and the N-channel pair is typically active for input voltages from the positive supply to (V+) – 0.4V. The transition region occurs typically from (V+) – 0.5V to (V+) – 0.3V, in which both pairs are on. These voltage levels can vary with process variations, and the transition region can range from (V+) – 0.7V to (V+) – 0.5V on the low end, up to (V+) – 0.3V to (V+) – 0.1V on the high end.

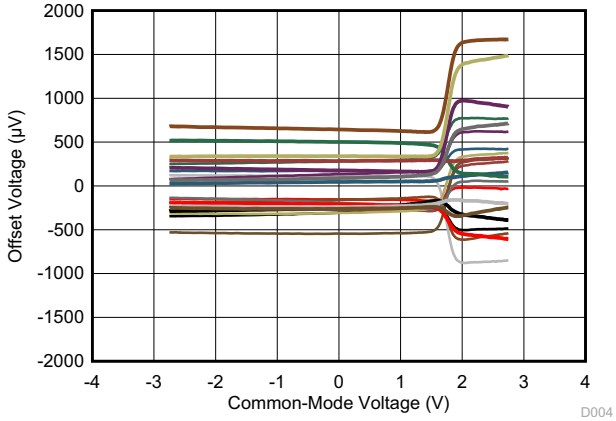
For most amplifiers with a complementary input stage, the P-channel input pair is designed to deliver better performance in terms of input offset voltage and offset drift over the N-channel pair. Within the transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region. The TLV904xD guarantees P-channel pair operation until 0.7V from the positive rail, providing a much wider P-channel input range compared to most complementary input amplifiers. This extended range is particularly useful when operating at lower supply voltages (1.2V, 1.8V, etc.), allowing wide common-mode swing of input signals to be accommodated within the P-channel input pair while avoiding the transition region and maintaining linearity.

Designed as a micro-power, low-noise operational amplifier, the TLV904xD also delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 5kΩ, the output typically swings to within 20mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails.



V+ = 2.75V, V– = –2.75V

Figure 6-1. TLV904xD Offset Voltage vs Common-Mode



V+ = 2.75V, V– = –2.75V

Figure 6-2. TLV900x Offset Voltage vs Common-Mode

6.3.3 Decompensated Architecture with Wide Gain-Bandwidth Product

Amplifiers such as the TLV904xD family are not unity-gain stable and are referred to as *decompensated amplifiers*. The decompensated architecture typically allows for higher GBW, higher slew rate, and lower noise compared to a unity-gain stable amplifier with similar quiescent currents. The increased available bandwidth reduces the rise time and settling time of the op amp, allowing for sampling at faster rates in an ADC-based signal chain.

As shown in Figure 6-3, the dominant pole of a unity-gain stable amplifier, f_d, is moved to the frequency f_1 in the case of a decompensated op amp. The solid A_{OL} plot is the open-loop gain plot of a traditional unity-gain stable op amp. The change in internal compensation in a decompensated amp such as the TLV904xD increases the bandwidth for the same amount of power. Besides the advantages in the above mentioned parameters, an increased slew rate and a better distortion value is achieved because of the higher available loop-gain, compared to its unity-gain counterpart. The most important factor to consider is ensuring that the op amp is in a noise gain (NG) greater than G_{min}. A value of NG lower than G_{min} results in instability, as shown in Figure 6-3, because the 1/ß curve intersects the A_{OL} curve at 40dB/decade. This method of analyzing stability is called the *rate of closure method*. See TI precision labs for a better understanding on device stability and for different techniques of ensuring stability.

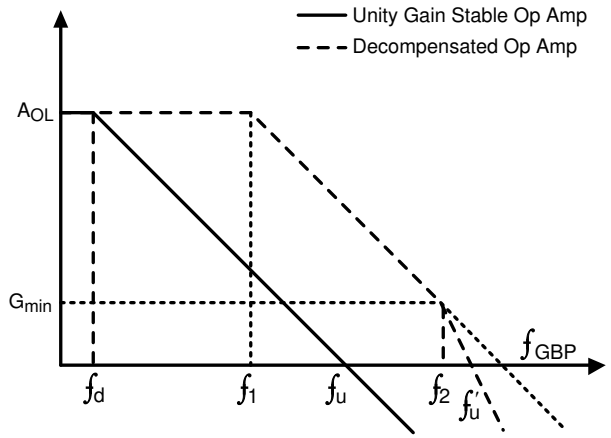


Figure 6-3. Gain vs Frequency Characteristics for a Unity-Gain Stable Op Amp and a Decompensated Op Amp

The TLV904xD family is stable in a noise gain of 10V/V (20dB) or higher in conventional gain circuits. The device has 3.1MHz of small-signal bandwidth (SSBW) in this gain configuration with approximately 72° of phase margin. The high GBW and low power consumption of the TLV904xD devices make them suitable for power sensitive, high-gain applications.

6.3.4 Capacitive Load and Stability

The TLV904xD is designed to be used in applications where driving a capacitive load is required. As with all operational amplifiers, there may be specific instances where the TLV904xD can become unstable. The particular operational amplifier circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. The capacitive load, in conjunction with the operational amplifier open-loop output impedance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases when capacitive loading increases. When operating in a gain of 10V/V, the TLV904xD remains stable with a pure capacitive load up to approximately 100pF with a good phase margin of 48° typical. The equivalent series resistance (ESR) of some very large capacitors (C_L greater than 1µF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when measuring the overshoot response of the amplifier at higher voltage gains.

One technique for increasing the capacitive load drive capability of the amplifier is to insert a small resistor (typically 10Ω to 20Ω) in series with the output, as shown in Figure 6-4. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique, however, is that a voltage divider is created with the added series resistor and any resistive load connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.

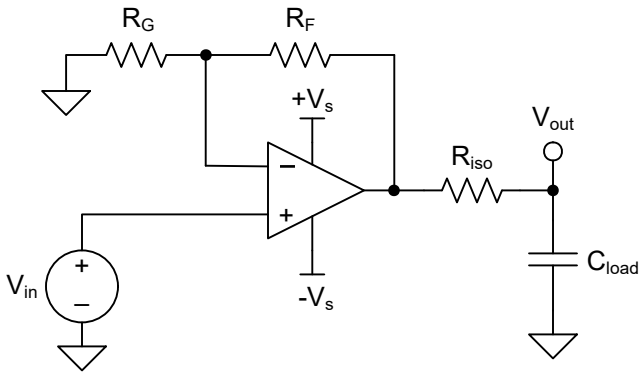


Figure 6-4. Improving Capacitive Load Drive

6.3.5 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or high gain. Once one of the output devices enters the saturation region, the output stage requires additional time to return to the linear operating state which is referred to as overload recovery time. After the output stage returns to its linear operating state, the amplifier begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time of the TLV9041D and TLV9042D is approximately 5µs and 11µs respectively.

6.3.6 EMI Rejection

The TLV904xD uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV904xD benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. Figure 6-5 shows the results of this testing on the TLV904xD. Table 6-1 shows the EMIRR IN+ values for the TLV904xD at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

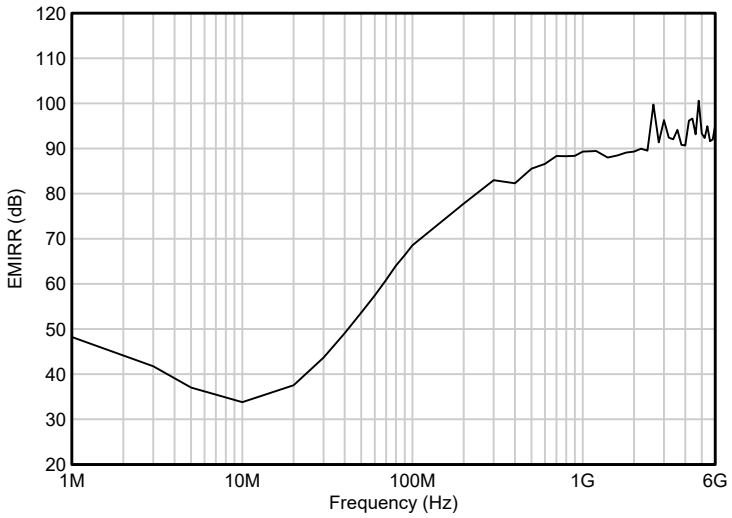


Figure 6-5. EMIRR Testing

Table 6-1. TLV904xD EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	60dB
900MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications	70dB
1.8GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1GHz to 2GHz)	75dB
2.4GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz)	79.0dB
3.6GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	82dB
5GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz)	85dB

6.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 6-6 shows the ESD circuits contained in the TLV904xD devices. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

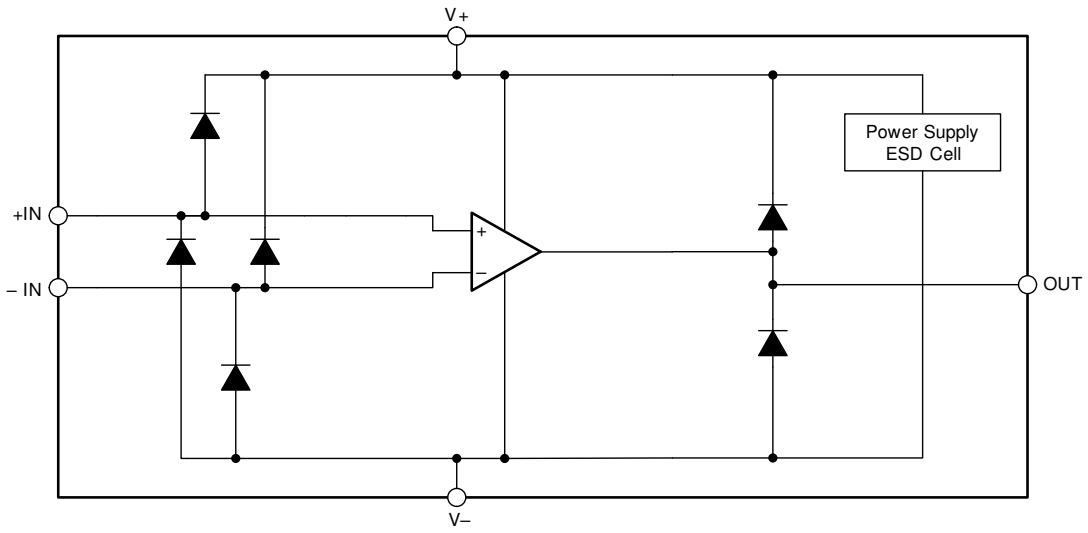


Figure 6-6. Equivalent Internal ESD Circuitry

6.3.8 Input and ESD Protection

The TLV904xD family incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10mA. Figure 6-7 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

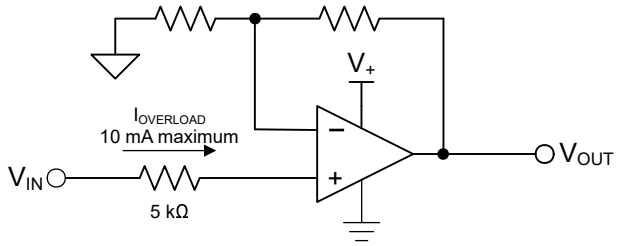


Figure 6-7. Input Current Protection

6.4 Device Functional Modes

The TLV904xD family haa a single functional mode. These devices are powered on as long as the power-supply voltage is between 1.2V (±0.6V) and 5.5V (±2.75V).

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TLV904xD family of low-power, rail-to-rail input and output operational amplifiers is specifically designed for portable, high gain applications. The devices operate from 1.2V to 5.5V, are stable above 10V/V and are suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving resistive loads greater than 2kΩ connected to any point between V+ and V–. The input common-mode voltage range includes both rails and allows the TLV904xD series to be used in many single-supply or dual supply configurations.

7.2 Typical Application

7.2.1 TLV904xD Low-Side, Current Sensing Application

Figure 7-1 shows the TLV904xD configured in a low-side current sensing application.

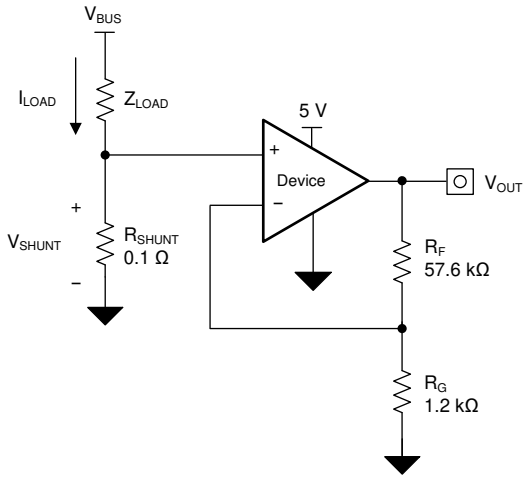


Figure 7-1. TLV904xD in a Low-Side, Current-Sensing Application

7.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0A to 1A
- Maximum output voltage: 4.9V
- Maximum shunt voltage: 100mV

7.2.1.2 Detailed Design Procedure

The transfer function of the circuit in Figure 7-1 is given in Equation 1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0A to 1A. To keep the shunt voltage below 100mV at maximum load current, the largest shunt resistor is shown using Equation 2.

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100mV}{1A} = 100m\Omega \quad (2)$$

Using Equation 2, R_{SHUNT} is calculated to be 100mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TLV904xD to produce an output voltage of approximately 0V to 4.9V. The gain needed by the TLV904xD to produce the necessary output voltage is calculated using Equation 3.

$$Gain = \frac{V_{OUT\_MAX} - V_{OUT\_MIN}}{V_{IN\_MAX} - V_{IN\_MIN}} \quad (3)$$

Using Equation 3, the required gain is calculated to be 49V/V, which is set with resistors R_F and R_G. Equation 4 sizes the resistors R_F and R_G, to set the gain of the TLV904xD to 49V/V.

$$Gain = 1 + \frac{R_F}{R_G} \quad (4)$$

Selecting R_F as 57.6kΩ and R_G as 1.2kΩ provides a combination that equals 49V/V. Figure 7-2 shows the measured transfer function of the circuit shown in Figure 7-1. Notice that the gain is only a function of the feedback and gain resistors. This gain is adjusted by varying the ratio of the resistors and the actual resistors values are determined by the impedance levels that the designer wants to establish. The impedance level determines the current drain, the effect that stray capacitance has, and a few other behaviors. There is no optimal impedance selection that works for every system; you must choose an impedance that is ideal for your system parameters.

7.2.1.3 Application Curve

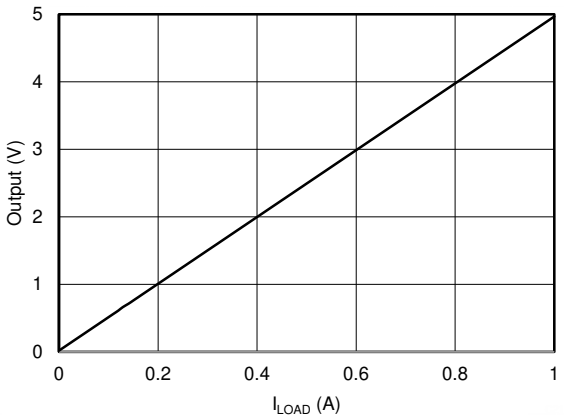


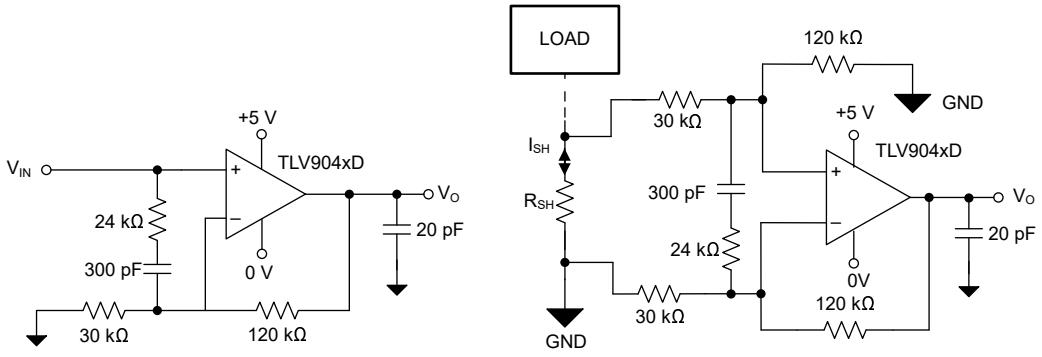
Figure 7-2. Low-Side, Current-Sense Transfer Function

7.2.2 Noninverting Gain of 3V/V

The TLV904xD devices are normally stable in noise gain configurations of greater than 10V/V when conventional feedback networks are used. The TLV904xD devices can be configured in noise gains of less than 10V/V by using capacitors in the feedback path and between the inputs to maintain the desired gain at lower frequencies and increase the gain greater that 10V/V at higher frequencies such that the amplifier is stable. Configuration (a) in Figure 7-3 shows TLV904xD devices configured in a gain of 5V/V by using capacitors and resistors to shape the noise gain and achieve a target phase margin of approximately 60° as shown in Figure 7-3.

The key benefit of using a decompensated amplifier (such as the TLV904xD) below the minimum stable gain, is that it takes advantage of the lower noise, lower distortion and higher slew rate performance at quiescent powers smaller than comparable unity-gain stable architectures. By reducing the 300pF input capacitor, higher closed-loop bandwidth and improved total noise can be achieved at the expense of increased peaking and reduced phase margin. Ensure that low parasitic capacitance layout techniques on the IN– pin are as small as 1pF to 2pF of parasitic capacitance on the inverting input, which will require tweaking the noise-shaping component values to get a flat frequency response and the desired phase margin. Configurations in Figure 7-3 does not take into account this parasitic capacitance but it must be considered for practical purposes. Details on this stabilizing technique and the benefits of decompensated architectures are discussed in *Decompensated Operational Amplifiers*.

In a difference amplifier circuit, typically used for low side current sensing applications, the (noise gain) = (signal gain + 1).



(a) G = 5 V/V **(c) G = 4 V/V**

Figure 7-3. Noninverting Gain of 5V/V, and Difference Amplifier in Signal Gain of 4V/V

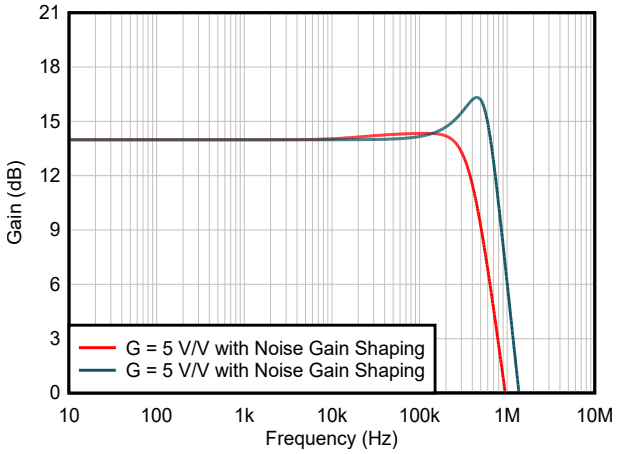


Figure 7-4. Small-Signal Frequency Response in Gains of 5V/V

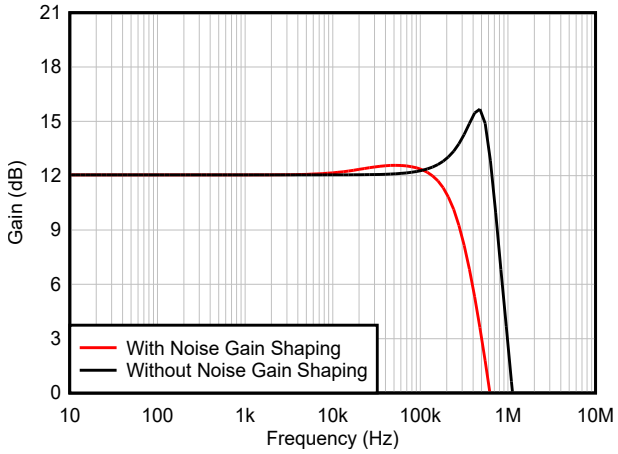


Figure 7-5. Small-Signal Frequency Response of Difference Amplifier With and Without Noise Gain Shaping

7.2.3 250kΩ Gain Transimpedance Design

The combination of GBW low input offset voltage and current noise for the TLV904xD devices make it an excellent option for moderate speed transimpedance amplifier applications.

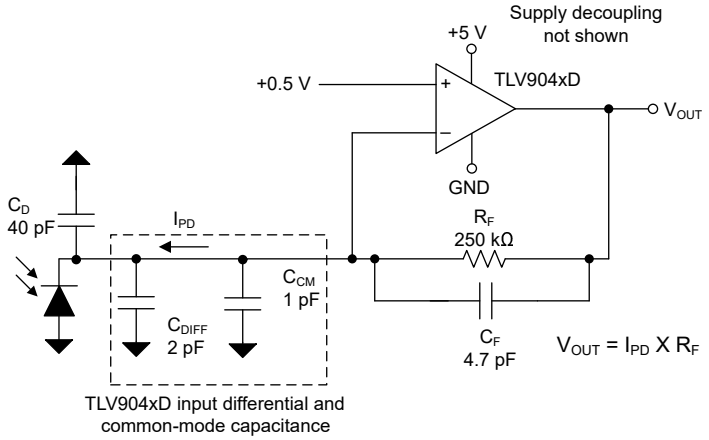


Figure 7-6. Low Power, High-Sensitivity, Transimpedance Amplifier

7.2.3.1 Design Requirements

Design a 200kHz, high-transimpedance-gain amplifier with the design requirements shown in Table 7-1.

Table 7-1. Design Requirements

TARGET BANDWIDTH (kHz)	TRANSIMPEDANCE-GAIN (kΩ)	PHOTODIODE CAPACITANCE (pF)
200	250	40

7.2.3.2 Detailed Design Procedure

Designs that require a low power solution with a relatively high transimpedance-gain can utilize the TLV904xD family. Use the Excel™ calculator available at *What You Need to Know About Transimpedance Amplifiers* to help with the component selection based on total input capacitance and C_{TOT}. C_{TOT} is referred as C_{IN} in the calculator. C_{TOT} is the sum of C_D, C_{DIFF}, and C_{CM} which is 43pF. Using this value of C_{TOT}, and the targeted closed-loop bandwidth (f_{-3dB}) of 200kHz and transimpedance gain of 250kΩ results in amplifier GBW of approximately 3MHz and a feedback capacitance (C_F) of 4.4pF as shown in Figure 7-7. These results are for a Butterworth response with a Q = 0.707 and a phase margin of approximately 65°.

Closed-loop TIA Bandwidth (f_{-3dB})	0.200	***MHz***
Feedback Resistance (R_F)	250.000	***kOhm***
Input Capacitance (C_{IN})	43.000	***pF***
Opamp Gain Bandwidth Product (GBP)	2.9807	***MHz***
Feedback Capacitance (C_F)	4.4395	***pF***

Figure 7-7. Results of Inputting Design Parameters in the TIA Calculator

The TLV904xD's 3.1MHz GBW, is suitable for the above design requirements. If the required feedback capacitance C_F comes out to be a very low value capacitor to be practically achievable, a T-Network capacitor circuit as shown below can be used. A very low capacitor value (C_{EQ}) can be achieved between $Port_1$ and $Port_2$ using standard value capacitors in a T-Network circuit as shown in Figure 7-8.

$$C_{EQ} = \frac{C_1 \times C_2}{C_1 + C_2 + C_T} \quad (5)$$

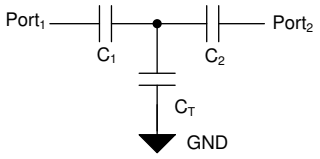


Figure 7-8. T-Network

7.2.3.3 Application Curves

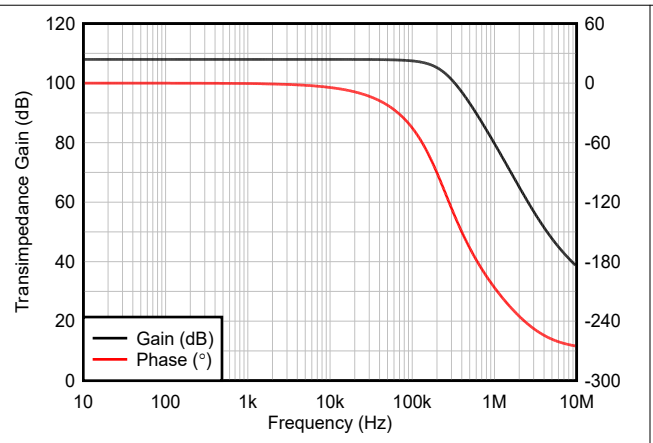


Figure 7-9. Simulated Closed-Loop Bandwidth of TIA

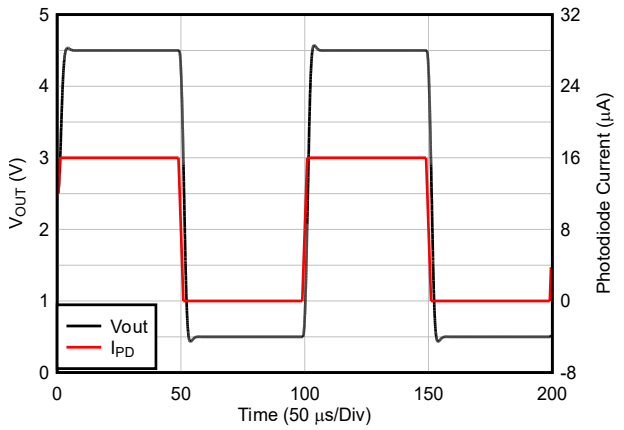


Figure 7-10. Simulated Time Domain Response

8 Power Supply Recommendations

The TLV904xD family is specified for operation from 1.2V to 5.5V (±0.6V to ±2.75V); many specifications apply from –40°C to 125°C. *Section 5.6* presents parameters that may exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 6V may permanently damage the device; see the *Section 5.1* table.

Place 0.1µF bypass capacitors close to the power-supply pins to reduce coupling errors from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Section 9.1*.

9 Layout

9.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power connections of the board and propagate to the power pins of the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing a low-impedance path to ground.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is adequate for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace at a 90 degree angle is much better as opposed to running the traces in parallel with the noisy trace.
- Place the external components as close to the device as possible, as shown in Figure 9-2. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring may significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

9.2 Layout Example

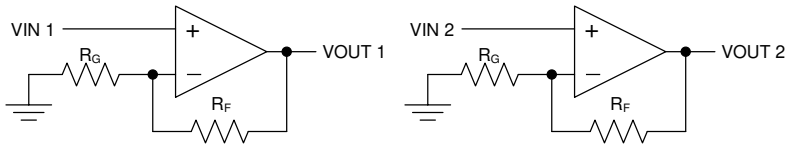


Figure 9-1. Schematic Representation

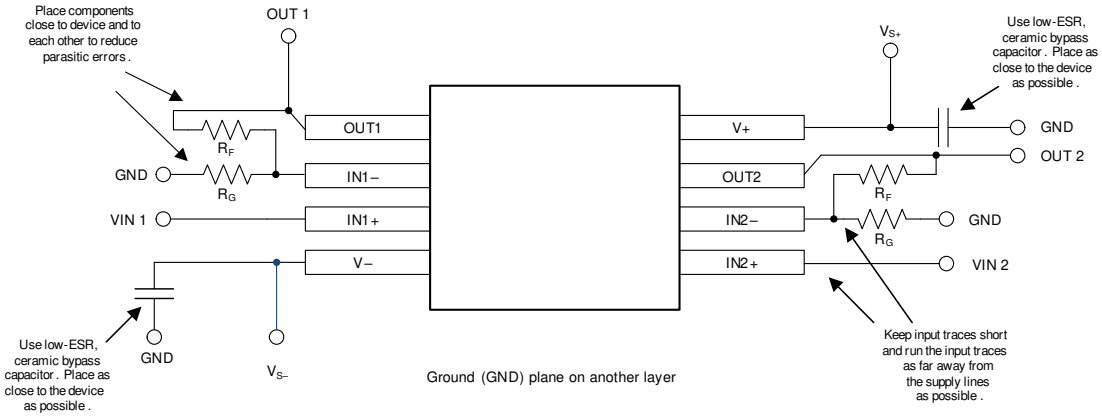


Figure 9-2. Layout Example

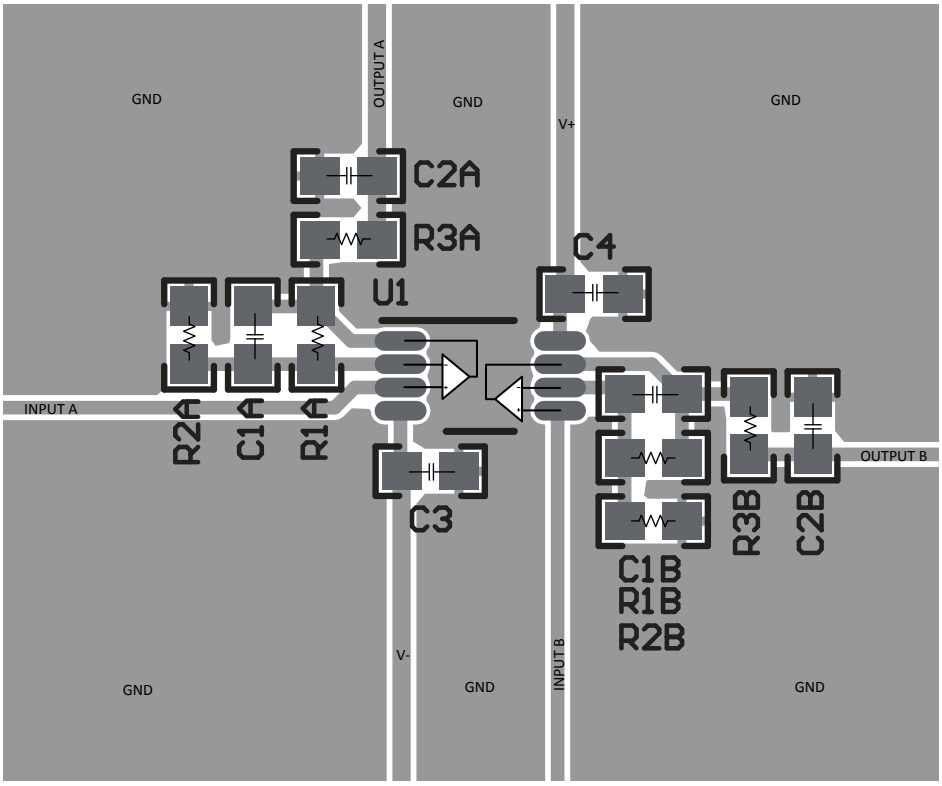


Figure 9-3. Example Layout for VSSOP-8 (DGK) Package

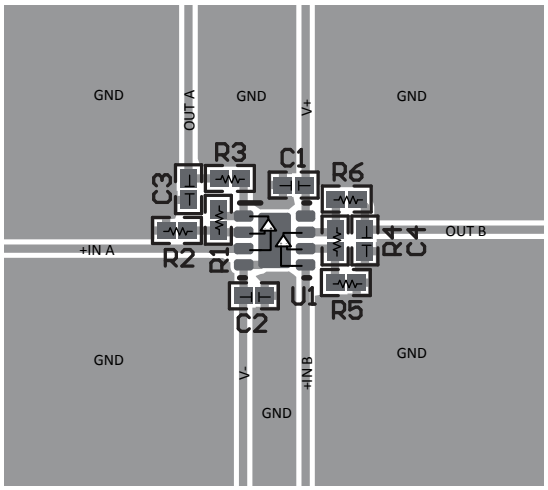


Figure 9-4. Example Layout for WSON-8 (DSG) Package

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *EMI rejection ratio of operational amplifiers*
- Texas Instruments, *QFN/SON PCB attachment*
- Texas Instruments, *Quad flatpack no-lead logic packages*

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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TI E2E™ is a trademark of Texas Instruments.
Bluetooth® is a registered trademark of Bluetooth SIG, Inc.
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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV9041DDCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	-	SN	Level-1-260C-UNLIM	-40 to 125	3Z3H
TLV9042DDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3XRS
TLV9042DDR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3XPT

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

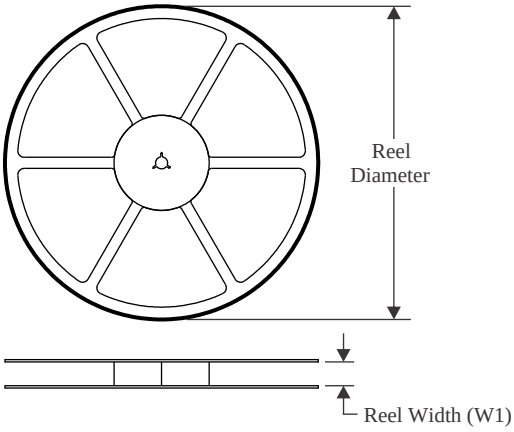
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

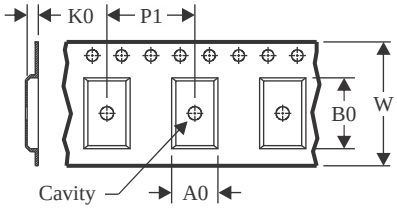
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

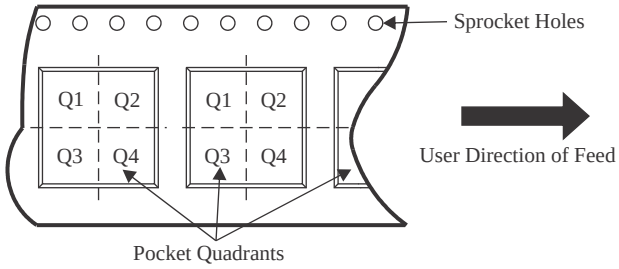


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

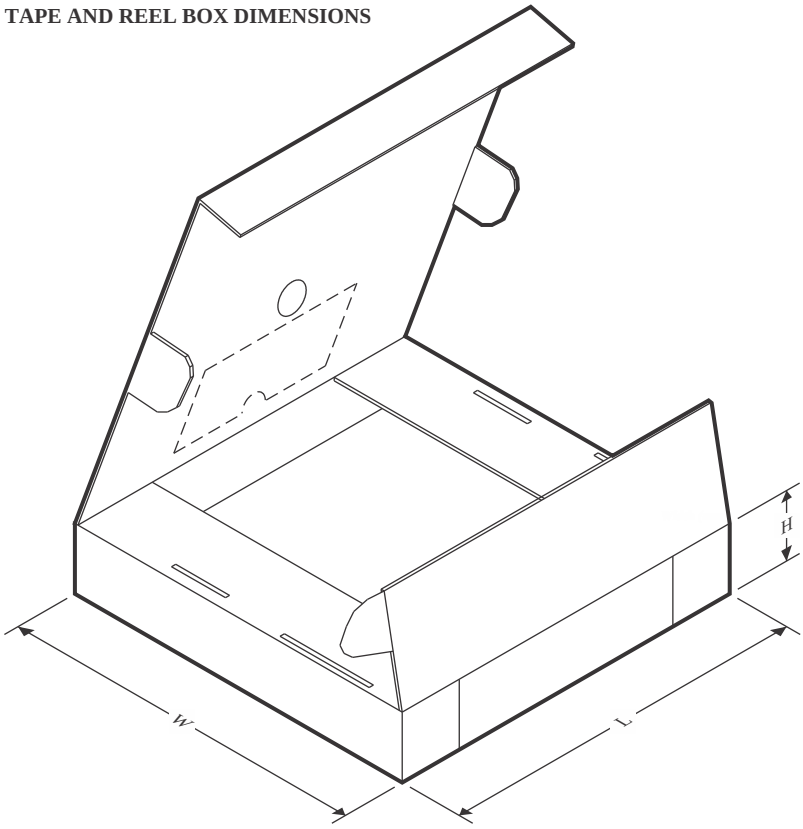
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9041DDCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
TLV9042DDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9042DDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

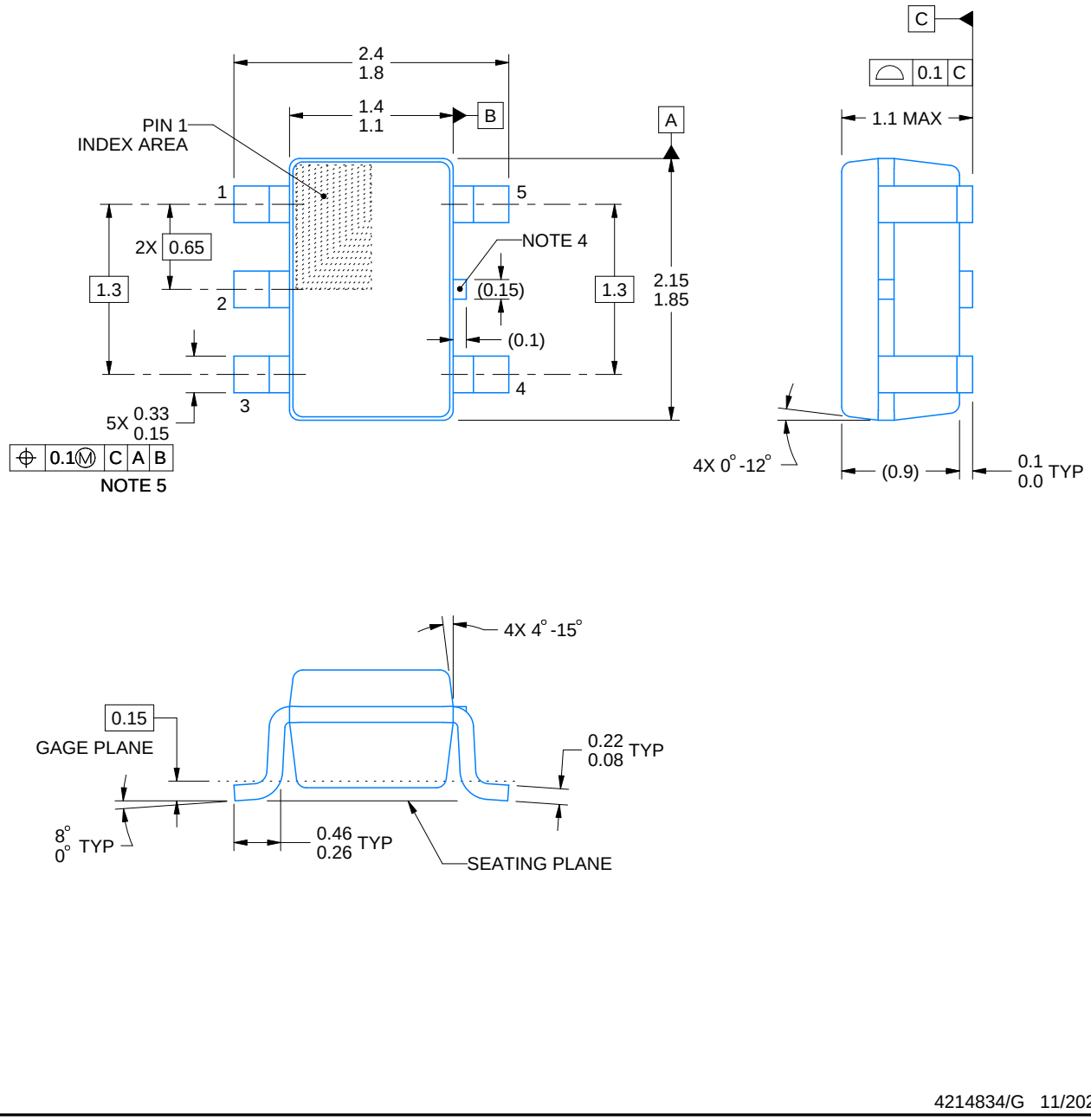
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9041DDCKR	SC70	DCK	5	3000	210.0	185.0	35.0
TLV9042DDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV9042DDR	SOIC	D	8	3000	353.0	353.0	32.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

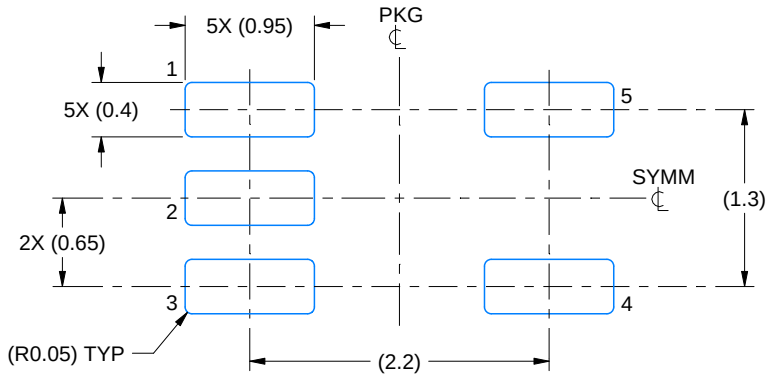
SMALL OUTLINE TRANSISTOR



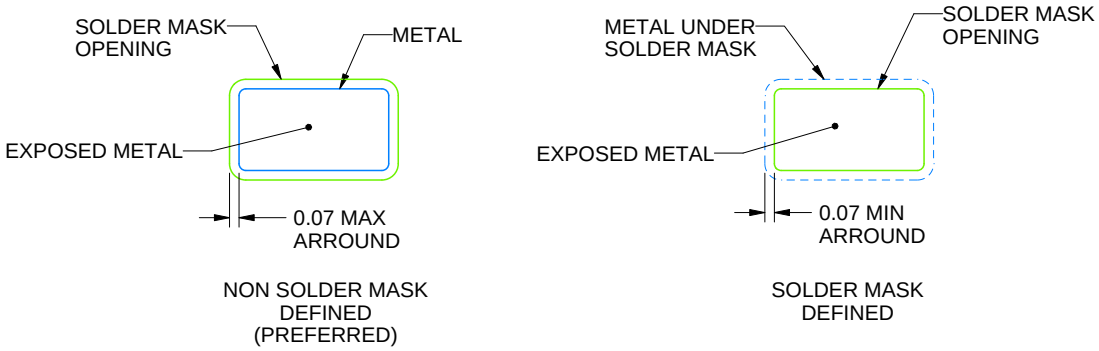
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

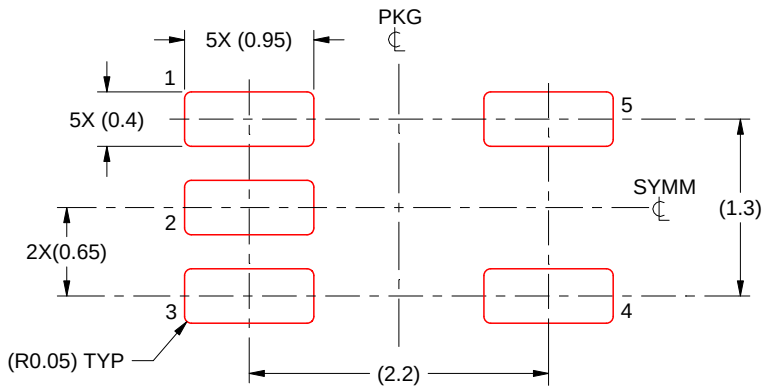


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

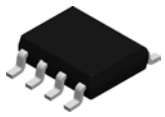


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

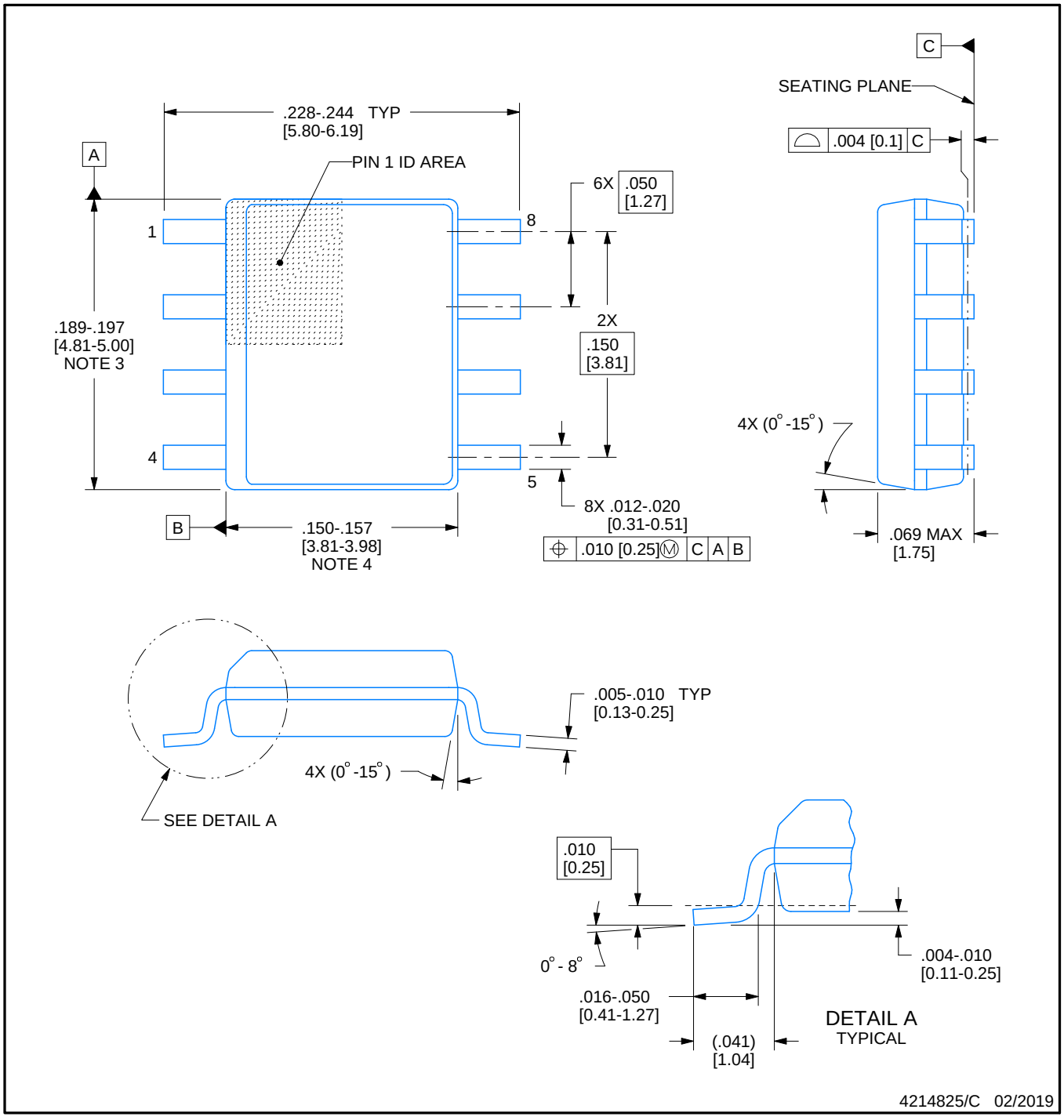


PACKAGE OUTLINE

D0008A

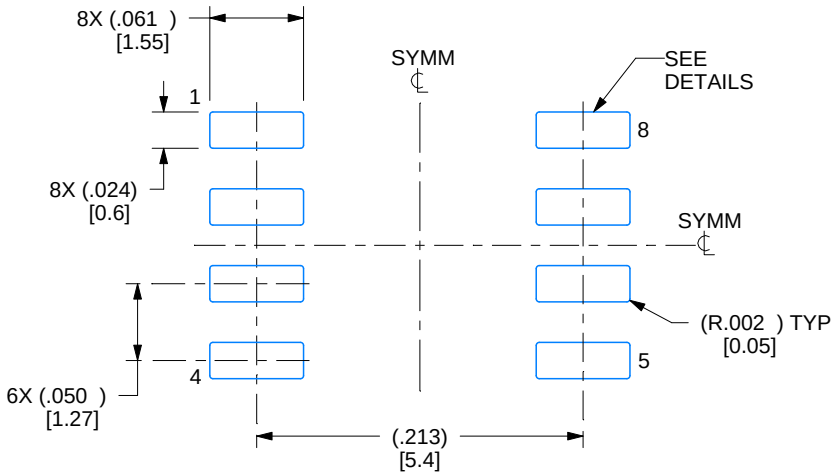
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

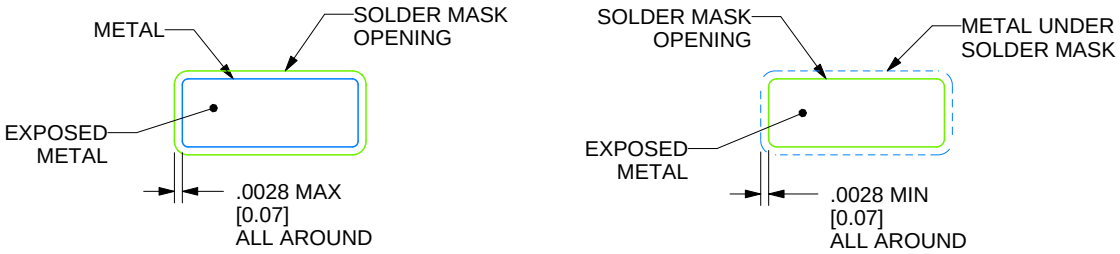


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

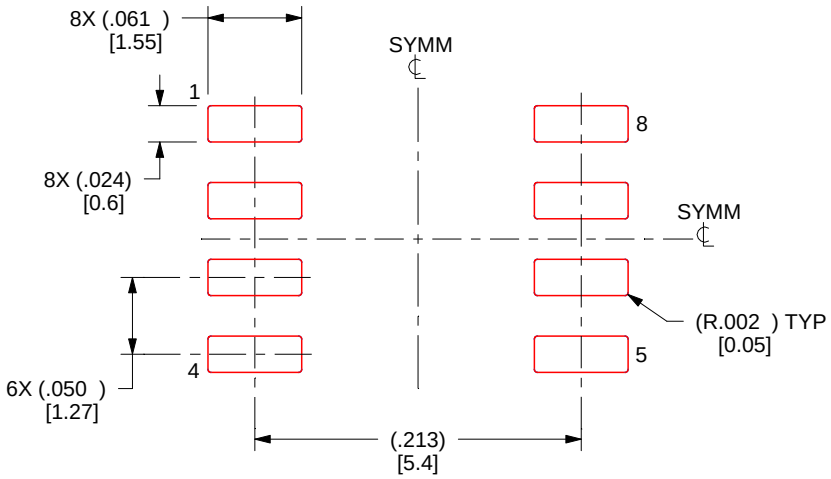
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

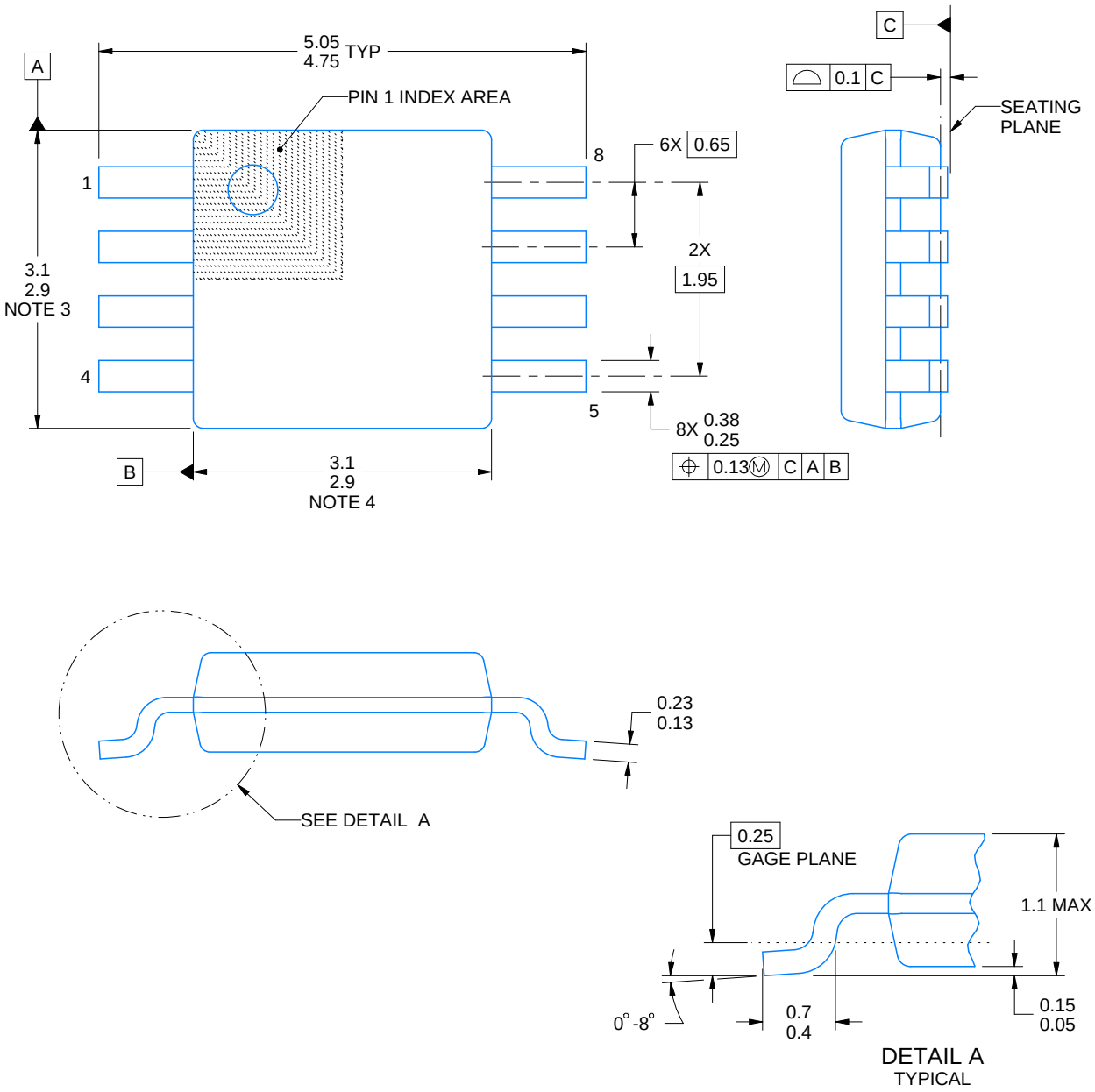
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

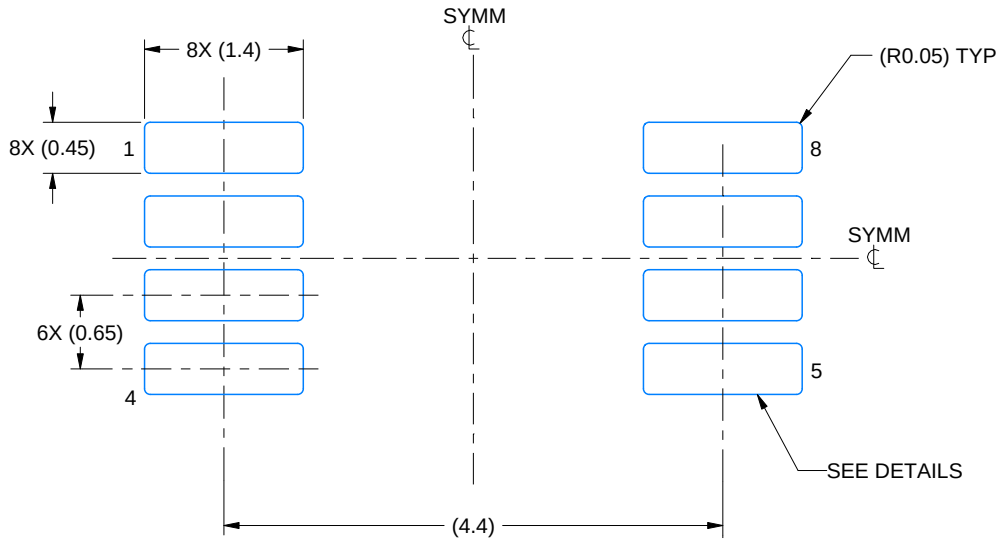
SMALL OUTLINE PACKAGE



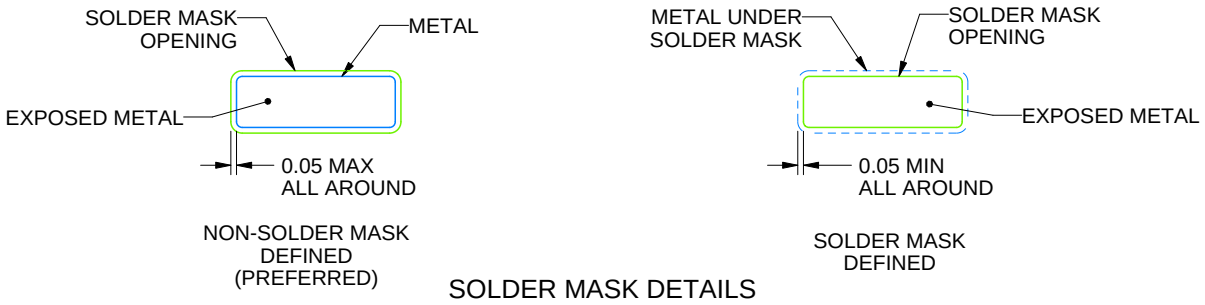
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

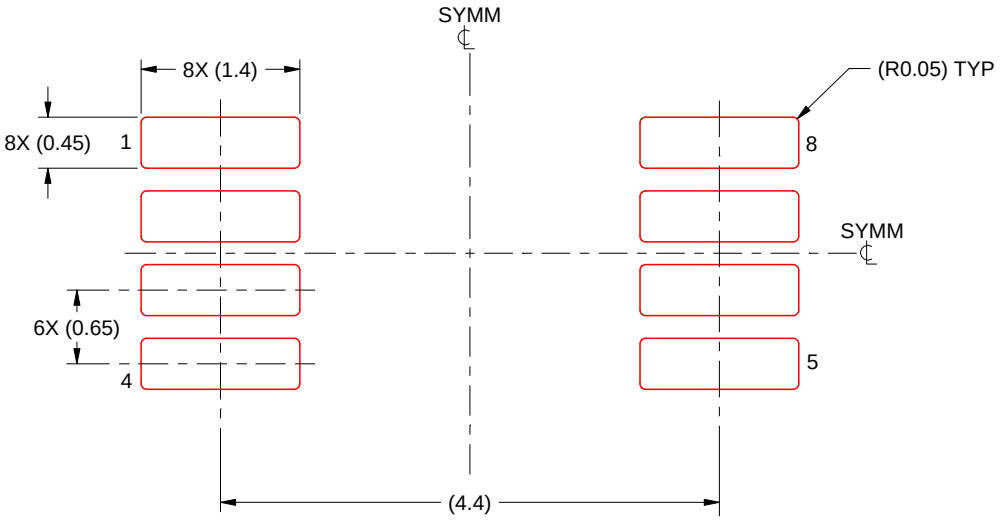


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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