TPS25868-Q1 and TPS25869-Q1 USB Type-A and Type-C® Charging Ports Controller With Sync DC/DC Converter and Programmable Current Limit

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: T_A range –40°C to +125°C
  - HBM ESD classification level H2
  - CDM ESD classification level C5
- Optimized for ultra-low EMI requirements:
  - Meets CISPR25 class 5 standard
  - HotRod™ package minimizes switch node ringing
  - Spread spectrum reduces peak emissions
- Synchronous buck regulator
  - High efficiency at 400 KHz: 95% at V_{IN} = 12 V, I_{PA_BUS} = 3 A and I_{PB_BUS} = 2.4 A
  - 18-mΩ/10-mΩ low $R_{DS(ON)}$ buck regulator MOSFETs
  - Operating voltage range: 5.5 V to 26 V, withstand 36-V input
  - Adjustable frequency: 200 kHz to 800 kHz
  - FPWM with spread-spectrum dithering
  - Selectable output voltage: 5.1 V, 5.17 V, 5.3 V, 5.4 V
- Internal power path:
  - 7-mΩ/7-mΩ low $R_{DS(ON)}$ internal USB power MOSFETs
  - Programmable current limit for USB ports with high accuracy: ±10% at 3.4 A
  - OUT: 5.1 V, 200 mA supply for auxiliary loads
- Line drop compensation: 90 mV at 2.4-A load
- Compliant to USB-IF standards
  - Type-C rev 1.3
    - 3-A capability advertisement on CC
    - V_{BUS} application and discharge
    - V_{CONN} source: 200 mA
  - Automatic DCP modes (TPS25868-Q1):
    - Shorted mode per BC1.2 and YD/T 1591 2009
    - 1.2-V mode
    - 2.7-V divider 3 mode
- Load shedding versus programmable T_A
- Device T_J range: –40°C to +150°C
- FAULT flag reports (TPS25869-Q1): USB overcurrent, thermal shutdown
- USB ports ON/OFF control (TPS25869-Q1)

2 Applications

- Automotive USB charging ports
- Automotive USB media hubs

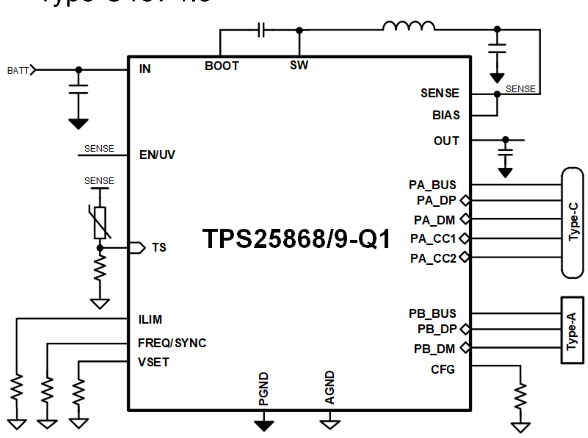
3 Description

The TPS2586x-Q1 is an integrated USB charging port solution, which includes a synchronous, high efficiency DC/DC converter and integrated detection and control for implementing USB Battery Charging 1.2 and Type-C ports.

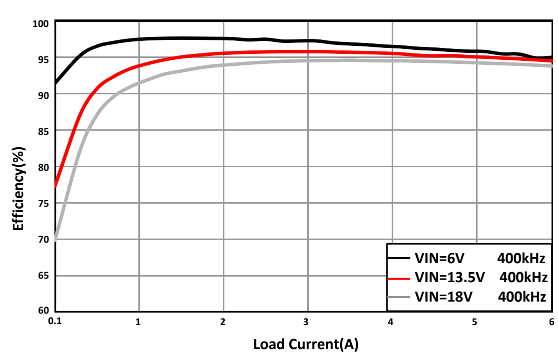
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS25868-Q1	VQFN-HR (25)	3.50 mm × 4.50 mm
TPS25869-Q1	VQFN-HR (25)	3.50 mm × 4.50 mm

(1) For detail part numbers for all available different options, see the orderable addendum at the end of the data sheet.



Simplified Schematic: TPS2586x-Q1



Efficiency vs Output Current

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4 Revision History

DATE	REVISION	NOTES
August 2021	*	Initial release

5 Description (continued)

The TPS2586x-Q1 is a family of highly-integrated USB charging controller for Type-C and Type-A dual ports application.

The device integrates a monolithic, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs and two USB current-limit switches with charging port auto-detection. The TPS2586x-Q1 offers a compact solution with excellent load and line regulation over a wide input supply range. The synchronous buck regulator operates with peak-current mode control and is internally compensated to simplify the design. A resistor on the FREQ pin sets the switching frequency between 200 kHz and 800 kHz, operating below 400 kHz results in better system efficiency.

The TPS2586x-Q1 integrates standard USB Type-C® port controller functionality including Configuration Channel (CC) logic for 3-A and 1.5-A current advertisement. Battery Charging (Rev. 1.2) integration provides the required electrical signatures necessary for non-Type-C, legacy USB devices which use USB data line signaling to determine USB port current sourcing capabilities. The TPS2586x-Q1 also has integrated VCONN power that can meet the USB3.1 power requirement. The part is especially suitable for dual-port application due to the high system integration and small footprint.

Since the TPS2586x-Q1 supports intelligent thermal regulation, the output current and voltage can be regulated according to the temperature sensing through the TS pin. It needs to connect a NTC thermistor on the TS pin to monitor the ambient temperature or PCB board temperature, depending on where the NTC thermistor is put in the USB charging module or PCB board. Select a different NTC thermistor and bottom-side series resistor can change the temperature for load shedding.

The TPS2586x-Q1 have four selectable USB output voltage settings: 5.1 V, 5.17 V, 5.3 V, and 5.4 V. The TPS2586x-Q1 integrates a precision current sense amplifier for cable droop compensation and user-programmable current limit tuning. The cable compensation is only available when the output voltage is set to 5.17 V. The cable compensation voltage is 90 mV at 2.4-A output current. Cable compensation aids portable devices in charging at optimum current and voltage under heavy loads by changing the buck regulator output voltage linearly with load current to counteract the voltage drop due to wire resistance in automotive cabling. The BUS voltage measured at a connected portable device remains approximately constant, regardless of load current, allowing the battery charger of the portable device to work optimally.

The TPS2586x-Q1 provides various safety features for USB charging and system operations, including external negative thermistor monitoring, cycle-by-cycle current limit, hiccup short-circuit protection, undervoltage lockout, BUS overcurrent, OUT overcurrent, and die overtemperature protection.

The device family is available in 25-pin, 3.5-mm × 4.5-mm QFN package.

6 Device Comparison Table

DEVICE NUMBER	TPS25868-Q1	TPS25869-Q1
USB ports Number	Dual	Dual
Support Type-C Protocol	Yes, only Port A	Yes, only Port A
NTC Thermistor Input (TS)	Yes	Yes
USB Load Switch ON/OFF Control	No	Yes
Fault Event Indication	No	Yes
Support MFi new OCP	Yes	Yes
External Clock Synchronization	Yes, range 200 kHz to approximately 800 KHz	Yes, range 200 kHz to approximately 800 KHz
BC1.2 DCP	Yes	No
Apple/Samsung charging scheme	Yes	No
Cable Compensation	Yes(1)	Yes(1)
Selectable Output Voltage	Yes	Yes
Adjustable Output Short Current Limit	Yes	Yes
FPWM/PFM	FPWM	FPWM
DCDC always ON (EN pull High)	Yes	Yes
Spread Spectrum	Yes	Yes
Package	QFN-25 3.5 mm × 4.5 mm	QFN-25 3.5 mm × 4.5 mm

(1) VSET short to GND to set 5.17-V output voltage. Compensation voltage is 90 mV when either USB port A or USB port B output 2.4-A current.

7 Pin Configuration and Functions

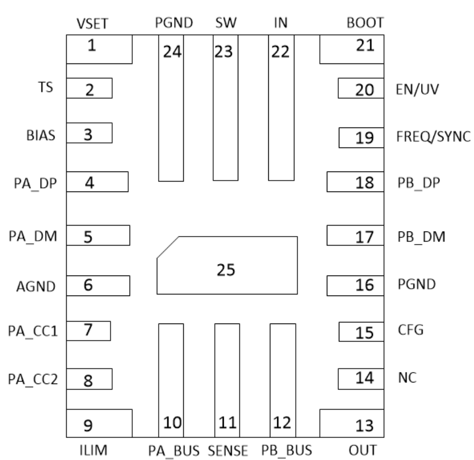


Figure 7-1. TPS25868 RPQ Package 25-Pin (QFN) Top View

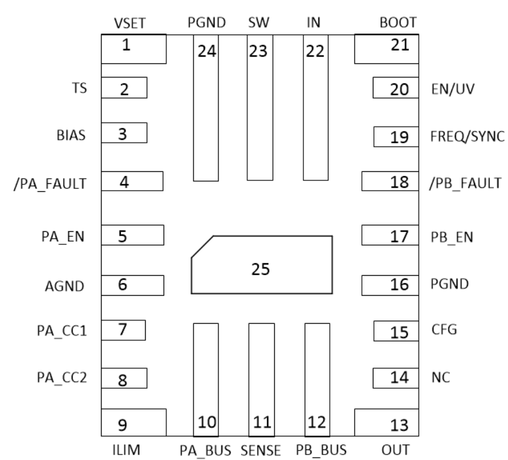


Figure 7-2. TPS25869 RPQ Package 25-Pin (QFN) Top View

Table 7-1. Pin Functions for TPS25868 RPQ Package

NAME	NO.	TYPE (1)	DESCRIPTION
VSET	1	A	Output Voltage Setting. Short to GND to set the 5.17-V output voltage. Float or pull up to V_{SENSE} to set 5.1-V output voltage. Tie to GND through a 40.2-KΩ resistor to set 5.3-V output voltage. Tie to GND through a 80.6-KΩ resistor to set 5.4-V output voltage.
TS	2	A	Temperature Sense terminal. Connect the TS input to the NTC thermistor.
BIAS	3	P	Input of internal bias supply. Must connect to the SENSE pin directly. Power the internal circuit.
PA_DP	4	A	D+ data line. Connect to USB Port A connector.

Table 7-1. Pin Functions for TPS25868 RPQ Package (continued)

NAME	NO.	TYPE (1)	DESCRIPTION
PA_DM	5	A	D- data line. Connect to USB Port A connector.
AGND	6	P	Analog ground terminal. Connect AGND to PGND.
PA_CC1	7	A	Connect to Type-C Port A CC1 pin. Analog Input/Output
PA_CC2	8	A	Connect to Type-C Port A CC2 pin. Analog Input/Output
ILIM	9	A	Current Limit program. Connect a resistor to set the current limit threshold. Short to GND to set the default 3.55-A current limit for Port A, and 2.84-A current limit for Port B.
PA_BUS	10	P	Port A BUS output
SENSE	11	P	Output Voltage Sensing. External load on this pin is strictly prohibited. Connect to the other side of the external inductor.
PB_BUS	12	P	Port B BUS output
OUT	13	P	Output pin. Provide 5.1-V voltage to power external load with max 200-mA capability. The voltage follows the VSET setting.
NC	14	A	Makes no electrical connection.
CFG	15	A	Configuration pin. For internal circuit, must connect a 5.1-KΩ resistor to AGND.
PGND	16,24,25	P	Power Ground terminal. Connected to the source of LS FET internally. Connect to system ground, AGND, and the ground side of the C_{IN} and C_{OUT} capacitors. The path to C_{IN} must be as short as possible.
PB_DM	17	A	D- data line. Connect to USB port B connector.
PB_DP	18	A	D+ data line. Connect to USB port B connector.
FREQ/ SYNC	19	A	Switching Frequency Program and External Clock Input. Connect a resistor from FREQ to GND to set the switching frequency.
EN/UV	20	A	Enable pin. Precision enable controls the regulator switching action and type-C. Do not float. High = on, Low = off. Can be tied to SENSE directly. Precision enable input allows adjustable UVLO by external resistor divider if tie to IN pin.
BOOT	21	P	Bootstrap capacitor connection. Internally, the BOOT is connected to the cathode of the boost-strap diode. Connect the 0.1-µF bootstrap capacitor from SW to BOOT
IN	22	P	Input power. Connected to external DC supply. Expected range of bypass capacitors is 1 µF to 10 µF, connect from IN to PGND. Can withstand up to 36 V without damage but operating is suspended if VIN is above the 26-V OVP threshold.
SW	23	P	Switching output of the regulator. Internally connected to source of the HS FET and drain of the LS FET. Connect to output inductor.

(1) A = Analog, P = Power, G = Ground.

Table 7-2. Pin Functions for TPS25869 RPQ Package

NAME	NO.	TYPE (1)	DESCRIPTION
VSET	1	A	Output Voltage Setting. Short to GND to set the 5.17-V output voltage. Float or pull up to V_{SENSE} to set 5.1-V output voltage. Tie to GND through a 40.2-KΩ resistor to set 5.3-V output voltage. Tie to GND through a 80.6-KΩ resistor to set 5.4-V output voltage.
TS	2	A	Temperature Sense terminal. Connect the TS input to the NTC thermistor.
BIAS	3	P	Input of internal bias supply. Must connect to the SENSE pin directly. Power the internal circuit.
$\overline{\text{PA\_FAULT}}$	4	A	USB Port A Fault Indication. /PA_FAULT indicates overcurrent on PA_BUS or overtemperature conditions. /PA_FAULT is an open drain in normal conditions. Pull / PA_FAULT low during fault conditions.
PA_EN	5	A	USB Port A Enable pin. To control the USB port A channel load switch ON/OFF. When pull-low, the pin turns off the port A USB power and CC1/2 current and voltage. When pull-high, the pin turns on the port A USB power and CC1/2 current and voltage. Can be tied to SENSE directly to automatically turn on USB port.
AGND	6	P	Analog ground terminal. Connect AGND to PGND.
PA_CC1	7	A	Connect to Type-C Port A CC1 pin. Analog Input/Output
PA_CC2	8	A	Connect to Type-C Port A CC2 pin. Analog Input/Output

Table 7-2. Pin Functions for TPS25869 RPQ Package (continued)

NAME	NO.	TYPE [1]	DESCRIPTION
ILIM	9	A	Current Limit program. Connect a resistor to set the current limit threshold. Short to GND to set the default 3.55-A current limit for Port A, and 2.84-A current limit for Port B.
PA_BUS	10	P	Port A BUS output
SENSE	11	P	Output Voltage Sensing, external load on this pin is strictly prohibited. Connect to the other side of the external inductor.
PB_BUS	12	P	Port B BUS output
OUT	13	P	Output pin. Provide 5.1-V voltage to power external load with max 200-mA capability. The voltage follows the VSET setting.
NC	14	A	Makes no electrical connection.
CFG	15	A	Configuration pin. For internal circuit, must connect a 5.1-KΩ resistor to AGND.
PGND	16,24,25	P	Power Ground Terminal. Connected to the source of LS FET internally. Connect to system ground, AGND, and the ground side of C_{IN} and C_{OUT} capacitors. Path to C_{IN} must be as short as possible.
PB_EN	17	A	USB Port B Enable pin. To control the USB port B channel load switch ON/OFF. When pull-low, the pin turns off the port B USB power. When pull-high, the pin turns on the port B USB power. Can be tied to SENSE directly to automatically turn on USB port.
$\overline{\text{PB\_FAULT}}$	18	A	USB Port B Fault Indication. /PB_FAULT indicates overcurrent on PB_BUS or overtemperature conditions. /PB_FAULT is an open drain in normal conditions. Pull /PB_FAULT low during fault conditions.
FREQ/ SYNC	19	A	Switching Frequency Program and External Clock Input. Connect a resistor from FREQ to GND to set the switching frequency.
EN/UV	20	A	Enable pin. Precision enable controls the regulator switching action and type-C. Do not float. High = on, Low = off. Can be tied to SENSE directly. Precision enable input allows adjustable UVLO by external resistor divider if tie to IN pin.
BOOT	21	P	Bootstrap capacitor connection. Internally, the BOOT is connected to the cathode of the booststrap diode. Connect the 0.1-µF bootstrap capacitor from SW to BOOT.
IN	22	P	Input power. Connected to external DC supply. Expected range of bypass capacitors is 1 µF to 10 µF. Connect from IN to PGND. Withstand up to 36 V without damage but operating is suspended if VIN is above the 26-V OVP threshold.
SW	23	P	Switching output of the regulator. Internally connected to source of the HS FET and drain of the LS FET. Connect to output inductor.

(1) A = Analog, P = Power, G = Ground.

8 Specifications

8.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of -40°C to +150°C and AGND = PGND (unless otherwise noted)[(1)]

PARAMETER		MIN	MAX	UNIT
Input voltage	IN to PGND	–0.3	40[(2)]	V
	IN to SW	–0.3	35	
	SENSE to PGND	–0.3	6	
	EN to AGND	–0.3	11	
	FREQ/SYNC to AGND	–0.3	6	
	PA_EN, PB_EN to AGND	–0.3	6	
	VSET, ILIM to AGND	-0.3	6	
	AGND to PGND	–0.3	0.3	
Input voltage	$\overline{\text{PA\_FAULT}}$, $\overline{\text{PB\_FAULT}}$, $\overline{\text{FAULT}}$ to AGND	–0.3	6	V
Output voltage	SW to PGND	–0.3	26	V
	SW to PGND (less than 10 ns transients)	–3.5	35	
	BOOT to SW	–0.3	6	
	PA_BUS, PB_BUS to PGND	–0.3	6	
Voltage range	CC1, CC2, CFG to AGND	–0.3	6	V
	DP, DM to AGND	–0.3	6	
	$\overline{\text{PA\_FAULT}}$, $\overline{\text{PB\_FAULT}}$ to AGND	–0.3	6	
	TS to AGND	–0.3	6	
Pin positive sink current, I_{SNK}	CC1, CC2 (while applying VCONN)		1	A
I/O current	DP to DM in BC1.2 DCP Mode	–35	35	mA
T_J	Junction temperature	-40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) VIN rising slew rate below 20 V/ms if in 0 V to 36 V or above transient.

8.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[(1)]		±2000[(2)]	V
		Charged device model (CDM), per AEC Q100-011	Corner pins	±750[(3)]	
			Other pins	±750[(3)]	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) The passing level per AEC-Q100 Classification H2.
(3) The passing level per AEC-Q100 Classification C5.

8.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of -40°C to 150°C. Voltages are with respect to GND (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_I	Input voltage	IN to PGND	5.5		26	V
		EN	0		VSENSE	
		TS	0		VSENSE	
		PA_EN, PB_EN	0		VSENSE	
		FREQ/SYNC when driven by external clock	0		3.3	
V_{PU}	Pull up voltage	$\overline{\text{PA\_FAULT}}$, $\overline{\text{PB\_FAULT}}$	0		VSENSE	
V_O	Output voltage	PA_BUS, PB_BUS	5		5.5	
I_O	Output current	PA_BUS	0		3	A
		PB_BUS	0		2.84	A
		OUT	0		0.2	A
		DP to DM Continuous current in BC1.2 DCP Mode	–15		15	mA
I_{SRC}	Source current	CC1 or CC2 source current when supplying VCONN			250	
I_{SNK}	Sink current	$\overline{\text{PA\_FAULT}}$, $\overline{\text{PB\_FAULT}}$			10	
R_{EXT}	External resistnace	R_{VSET}	0		100	kΩ
		R_{ILIM}	0		100	kΩ
		R_{FREQ}	0		100	kΩ
C_{EXT}	External capacitance	C_{BOOT}		0.1		uF
T_J		Operating junction temperature	–40		150	°C

8.4 Thermal Information

THERMAL METRIC[(1)] [(2)]		TPS2586x-Q1 RPQ (VQFN) 25 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	7.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Power rating at a specific ambient temperature T_A should be determined with a maximum junction temperature of 150 °C.

8.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of -40°C to +150°C; V_{IN} = 13.5 V, f_{SW} =400kHz, VSET short to GND unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTATE (IN PIN)						
I_{SD}	Shutdown quiescent current; measured at IN pin.	VEN/UV = 0, –40°C ≤ T_J ≤ 85°C		21	50	uA
V_{OVLO_R}	Voltage on VIN pin when buck regulator stops switching		26.6	27.5	28.4	V
V_{OVLO_HYS}	Hysteresis			0.5		V
ENABLE AND UVLO (EN/UVLO PIN)						
$V_{EN/UVLO\_R}$	Rising threshold for not in External UVLO	$V_{EN/UV}$ rising threshold	1.26	1.3	1.34	V
$V_{EN/UVLO\_HYS}$	Hysteresis	$V_{EN/UVLO}$ falling		100		mV
V_{PA/B_EN_H}	PA_EN, PB_EN input level required to turn on PA_BUS and PB_BUS Load Switch	V_{PA_EN} or V_{PB_EN} rising threshold		1.6	1.98	V
V_{PA/B_EN_L}	PA_EN, PB_EN input level required to turn off PA_BUS and PB_BUS Load Switch	V_{PA_EN} or V_{PB_EN} falling threshold	0.97	1.5		V
$V_{EN1/2\_HYS}$	Hysteresis	V_{PA_EN} or V_{PB_EN} falling threshold		100		mV
BOOTSTRAP						
V_{BTST_UVLO}	Bootstrap voltage UVLO threshold			2.2		V
R_{BOOT}	Bootstrap pull-up resistence	VSENSE-BOOT = 0.1 V, Need a test mode		7.7		Ω
BUCK REGULATOR						
$I_{L-SC-HS}$	High-side current limit	BOOT-SW = 5 V	10.2	11.4	12.6	A
$I_{L-SC-LS}$	Low-side current limit	SENSE = 5 V	8.5	10	11.5	A
$I_{L-NEG-LS}$	Low-side negative current limit	SENSE = 5 V		–5		A
I_{ZC}	Zero current detector threshold			0.01		A
V_{SENSE}	BUCK Output voltage	CC1 or CC2 pulldown resistance = R_d, VSET float or pull up to V_{SENSE}, T_J = 25℃	-1%	5.1	+1%	V
		CC1 or CC2 pulldown resistance = R_d, VSET short to AGND, T_J = 25℃	-1%	5.17	+1%	V
		CC1 or CC2 pulldown resistance = R_d, R_{VSET} = 40.2 KΩ, T_J = 25℃	-1%	5.3	+1%	V
		CC1 or CC2 pulldown resistance = R_d, R_{VSET} = 80.6 KΩ, T_J =25℃	-1%	5.4	+1%	V
V_{SENSE}	BUCK Output voltage accuracy	CC1 or CC2 pulldown resistance = R_d, –40℃ ≤ T_J ≤ 150℃	–2		2	%
$V_{DCDC\_UVLO\_R}$	SENSE input level to enable DCDC switching	V_{SENSE} rising, CC1 or CC2 pull down resistance = R_d	3.85	4	4.15	V
$V_{DCDC\_UVLO\_HYS}$	Hysteresis	V_{SENSE} falling, CC1 or CC2 pull down resistance = R_d		0.4		V
V_{DROP}	Dropout voltage (V_{IN}-V_{SENSE})	V_{IN} = V_{SENSE} + V_{DROP}, V_{SENS} = 5.1V, I_{PA_BUS} = 3 A, I_{PB_BUS}= 2.4 A		300		mV
$R_{DS-ON-HS}$	High-side MOSFET ON-resistance	I_{PA_BUS}=3A, I_{PB_BUS} = 2.4 A, BOOT-SW = 5 V, –40℃ ≤ T_J ≤ 150℃		18	34	mΩ
$R_{DS-ON-LS}$	Low-side MOSFET ON-resistance	I_{PA_BUS} = 3 A, I_{PB_BUS} = 2.4 A, V_{SENSE} = 5 V, –40℃≤ T_J ≤ 150℃		9.5	18.5	mΩ

8.5 Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature (T_J) range of -40°C to +150°C; V_{IN} = 13.5 V, f_{SW} =400kHz, VSET short to GND unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCH AND CURRENT LIMIT						
R_{DS-ON_USB}	USB Load Switch MOSFET ON-resistance	I_{PA_BUS} = 3 A, I_{PB_BUS} = 2.4 A; -40℃ ≤ T_J ≤ 150℃		6.8	11.73	mΩ
R_{DS-ON_OUT}	OUT Load Switch MOSFET ON-resistance	I_{OUT} = 0.3 A		230		mΩ
R_{DS-ON_VCONN}	On-state resistance	T_J = 25°C, I_{CCn} = 0.25 A		410	550	mΩ
R_{DS-ON_VCONN}	On-state resistance	–40°C ≤T_J ≤ 150°C, I_{CCn} = 0.25 A		410	740	mΩ
$V_{USBLS\_UVLO\_R}$	Voltage on SENSE pin that will enable the USB Load Switch		3.95	4.1	4.25	V
$V_{USBLS\_UVLO\_HYS}$	Hysteresis			200		mV
R_{BUS_DCHG}	Discharge resistance for Port A or Port B BUS	Apply 5 V on PA_BUS or PB_BUS, PA_EN or PB_EN pull low	250	500	750	Ω
$V_{TH\_R\_BUS\_DCHGb}$	Rising threshold voltage for BUS not discharged		670	700	730	mV
$V_{TH\_HYS\_BUS\_DCHG}$	Hysteresis			100		mV
$V_{BUS\_DCHG\_BLEED}$	BUS bleed resistance	V_{PA_BUS} = 4 V, No sink termination on CC lines, Time>$t_{W\_BUS\_DCHG}$	100	150	200	KΩ
I_{OS_HI} (USB Port B)	Port B BUS output short-circuit secondary current limit	R_{ILIM} = 48.7 KΩ	679	849	1018	mA
		R_{ILIM} = 19.1 KΩ	1947	2163	2379	mA
		R_{ILIM} = 15.4 KΩ	2415	2683	2951	mA
		R_{ILIM} = 12.4 KΩ	2999	3332	3665	mA
		R_{ILIM} = 11.5 KΩ	3233	3592	3951	mA
		RILIM = 9.53 KΩ	3901	4334	4767	mA
		R_{ILIM}= 0 Ω (short to GND)	3862	4544	5225	mA
		R_{ILIM}= 11.5 KΩ, T_J = 25℃	3412	3592	3771	mA
I_{OS_BUS} (USB Port B)	Port B BUS output short-circuit current limit	R_{ILIM} = 48.7 KΩ	424	530	636	mA
		R_{ILIM} = 19.1 KΩ	1217	1352	1487	mA
		R_{ILIM}= 15.4 KΩ	1509	1677	1844	mA
		R_{ILIM} = 12.4 KΩ	1874	2082	2290	mA
		R_{ILIM} = 11.5 KΩ	2020	2245	2469	mA
		RILIM = 9.53 KΩ	2438	2709	2980	mA
		R_{ILIM}= 0 Ω (short to GND)	2414	2840	3266	mA
		R_{ILIM} = 11.5 KΩ, T_J = 25℃	2133	2245	2357	mA
I_{OS_HI} (USB Port A)	Port A BUS output short-circuit secondary current limit	R_{ILIM}= 48.7 KΩ	849	1061	1273	mA
		R_{ILIM} = 19.1 KΩ	2434	2704	2974	mA
		R_{ILIM} = 15.4 KΩ	3018	3354	3689	mA
		R_{ILIM} = 12.4 KΩ	3748	4165	4581	mA
		R_{ILIM} = 11.5 KΩ	4040	4490	4938	mA
		R_{ILIM} = 9.53 KΩ	4876	5418	5960	mA
		R_{ILIM}= 0 Ω (short to GND)	4828	5680	6532	mA
		R_{ILIM} = 11.5 KΩ, T_J = 25℃	4265	4490	4714	mA

8.5 Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature (T_J) range of -40°C to +150°C; V_{IN} = 13.5 V, f_{SW} =400kHz, VSET short to GND unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OS_BUS} (USB Port A)	Port A BUS output short-circuit current limit	R_{ILIM} = 48.7 KΩ	530.4	663	795.6	mA
		R_{ILIM} = 19.1 KΩ	1521	1690	1859	mA
		R_{ILIM} = 15.4 KΩ	1886.4	2096	2305.6	mA
		R_{ILIM} = 12.4 KΩ	2342.7	2603	2863.3	mA
		R_{ILIM} = 11.5 KΩ	2525.4	2806	3086.6	mA
		RILIM = 9.53 KΩ	3047.4	3386	3724.6	mA
		R_{ILIM} = 0 Ω (short to GND)	3017.5	3550	4082.5	mA
		R_{ILIM} = 11.5 KΩ, T_J = 25℃	2666	2806	2946	mA
I_{OS_OUT}	OUT output short-circuit current limit	Short circuit current limit	390	450	495	mA
I_{OS_VCONN}	VCONN output short-circuit current limit	Short circuit current limit	240	300	360	mA
CABLE COMPENSATION VOLTAGE						
V_{DROP_COM}	Cable compensation voltage	I_{PA_BUS} or I_{PB_BUS} = 2.4 A, VSET = GND (set 5.17-V output)	70	90	110	mV
CC CONNECT MANAGEMENT						
$I_{SRC\_CC\_3A}$	Sourcing current	CC pin voltage: 0 V ≤ V_{CCn} ≤ 2.45 V	304	330	356	µA
$I_{SRC\_CC\_1.5A}$	Sourcing current in thermal management(Temp warm)	CC pin voltage: 0 V ≤ V_{CCn} ≤ 1.5 V , T_A > 85℃	167	180	194	µA
$I_{SRC\_CC\_DFLT}$	Sourcing current in thermal management(Temp hot)	CC pin voltage: 0 V ≤ V_{CCn} ≤ 1.5 V , T_A > 85℃	64	80	105	µA
I_{REV}	Reverse leakage current	CCx is the CC pin under test, CCy is the other CC pin. CC pin voltage VCCx = 5.5 V, CCy floating, V_{EN_UV} = 0 V or V_{SENSE}, 0 V ≤ V_{IN} ≤ 26 V I_{REV} is current into CCx pin		2.75	10	µA
V_{TH_R}	Rising threshold voltage for VCONN not discharged	CC pin that was providing VCONN in previous SINK state	670	700	730	mV
V_{TH_HYS}	Hysteresis			100		mV
$\overline{\text{FAULT}}$						
V_{OL}	$\overline{\text{PA\_FAULT}}$, $\overline{\text{PB\_FAULT}}$ Output low voltage	I_{SNK_PIN} = 1 mA			250	mV
I_{OFF}	$\overline{\text{PA\_FAULT}}$, $\overline{\text{PB\_FAULT}}$ Off-state leakage	V_{PIN} = 5.5 V			2.2	µA
BC 1.2 DOWNSTREAM CHARGING PORT						
R_{DPM_SHORT}	DP and DM shorting resistance			70	200	Ω
DIVIDER 3 MODE						
V_{DP_DIV3}	DP output voltage		2.57	2.7	2.84	V
V_{DM_DIV3}	DM output voltage		2.57	2.7	2.84	V
R_{DP_DIV3}	DP output impedance	I_{DP_IN} = –5 µA	24	30	36	kΩ
R_{DM_DIV3}	DM output impedance	I_{DM_IN} = –5 µA	24	30	36	kΩ
1.2-V MODE						
$V_{DP\_1.2V}$	DP output voltage		1.12	1.2	1.26	V
$V_{DM\_1.2V}$	DM output voltage		1.12	1.2	1.26	V
$R_{DP\_1.2V}$	DP output impedance	I_{DP_IN} = –5 µA	84	100	126	kΩ
$R_{DM\_1.2V}$	DM output impedance	I_{DM_IN} = –5 µA	84	100	126	kΩ

8.5 Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature (T_J) range of -40°C to +150°C; V_{IN} = 13.5 V, f_{SW} =400kHz, VSET short to GND unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQ/SYNC THRESHOLD						
$V_{IH\_FREQ/SYNC}$	FREQ/SYNC high threshold for external clock synchronization	Amplitude of SYNC clock AC signal (measured at FREQ/SYNC pin)	2			V
$V_{IL\_FREQ/SYNC}$	FREQ/SYNC low threshold for external clock synchronization	Amplitude of SYNC clock AC signal (measured at FREQ/SYNC pin)			0.8	V
TEMPERATURE SENSING						
V_{WARN_HIGH}	Temperature warning threshold rising	As percentage to V_{SENSE}	0.475	0.5	0.525	V/V
V_{WARN_HYS}	Hysteresis	As percentage to V_{SENSE}		0.1		V/V
V_{HOT_HIGH}	Temperature Hot assert threshold rising to reduce SENS voltage	As percentage to V_{SENSE}	0.6175	0.65	0.6825	V/V
V_{HOT_HYS}	Hysteresis	As percentage to V_{SENSE}		0.1		V/V
V_{R_VSENS}	V_{SENSE} voltage decay when Temperature Hot assert	TS pin voltage rise above 0.65*V_{SENSE}		4.77		V
THERMAL SHUTDOWN						
T_{LS_SD}	USB Load Switch Over Temperature	OTSD2&3 threshold		160		°C
		Recovery threshold		150		°C
T_{SD}	Thermal shutdown	Shutdown threshold		166		°C
		Recovery threshold		154		°C

8.6 Timing Requirements

Over the recommended operating junction temperature range of -40 °C to 150 °C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$\overline{FAULT}$ DUE TO BUS OC AND THERMAL SD						
t_{DEGLA_FAULT}	Asserting deglitch time	(Thermal SD Fault assertion is instantaneous, not subject to this timing)	2.94	4.1	5.42	ms
t_{DEGLD_FAULT}	De-asserting deglitch time		11.09	16.38	23.03	ms
BUS DISCHARGE						
$t_{DEGA\_BUS\_DCHG}$	Discharge asserting deglitch		5.6	12.3	21.2	ms
$t_{W\_BUS\_DCHG}$	V_{BUS} discharge time after sink termination removed from CC lines	V_{BUS} = 1 V, time I_{SNK_OUT} > 1 mA after sink termination removed from CC lines	170	260	360	ms
POWER SWITCH TIMING						
$t_{IOS\_HI\_DEG}$	Deglitch time for USB power switch current limit enable	USB port enter overcurrent (per ILIM setting)	1.228	2.048	2.867	ms
$t_{IOS\_HI\_RST}$	MFi OCP reset timing		9.6	16	22.4	ms
t_{r_USB}	PA_BUS, PB_BUS voltage rise time	C_L = 1 µF, R_L = 100 Ω (measured from 10% to 90% of final value)		1.67		ms
t_{f_USB}	PA_BUS, PB_BUS voltage fall time	C_L = 1 µF, R_L = 100 Ω (measured from 90% to 10% of final value)		0.49		ms
t_{on_USB}	PA_BUS, PB_BUS voltage turnon-time	C_L = 1 µF, R_L = 100 Ω		2.59		ms
t_{off_USB}	PA_BUS, PB_BUS voltage turnoff-time	C_L = 1 µF, R_L = 100 Ω		2.07		ms
t_{IOS_USB}	PA_BUS, PB_BUS short-circuit response time	C_L = 1 µF, R_L = 1 Ω		1		us
t_{r_OUT}	OUT voltage rise time	C_L = 1 µF, R_L = 100 Ω (measured from 10% to 90% of final value)	0.12	0.2	0.28	ms

8.6 Timing Requirements (continued)

Over the recommended operating junction temperature range of -40 °C to 150 °C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
t_{f_OUT}	OUT voltage fall time	C_L = 1 µF, R_L = 100 Ω (measured from 90% to 10% of final value)	0.16	0.22	0.28	ms
t_{on_OUT}	OUT voltage turnon-time	C_L = 1 µF, R_L = 100 Ω	0.6	1.1	1.65	ms
t_{off_OUT}	OUT voltage turnoff-time	C_L = 1 µF, R_L = 100 Ω	0.22	0.38	0.55	ms
t_{IOS_OUT}	OUT short-circuit response time	C_L = 1 µF, R_L = 1 Ω		1.4	4	us
t_{IOS_VCONN}	CC-VCONN short circuit response time	C_L = 1 µF, R_L = 1 Ω		1	3.5	µs
t_{r_VCONN}	VCONN output voltage rise time	C_L = 1 µF, R_L = 100 Ω (measured from 10% to 90% of final value); 5.1 KΩ on CC1 and 1 KΩ on CC2	0.2	0.28	0.35	ms
t_{f_VCONN}	VCONN output voltage fall time	C_L = 1 µF, R_L = 100 Ω (measured from 90% to 10% of final value); 5.1 KΩ on CC1 and 1KΩ on CC2	0.18	0.23	0.28	ms
t_{on_VCONN}	VCONN output voltage turnon time	C_L = 1 µF, R_L = 100 Ω; 5.1KΩ on CC1 and 1KΩ on CC2	0.7	1.2	1.7	ms
t_{off_VCONN}	VCONN output voltage turnoff time	C_L = 1 µF, R_L = 100 Ω; 5.1 KΩ on CC1 and 1 KΩ on CC2	0.37	0.44	0.51	ms
HICCUP MODE						
T_{HICP_ON}	OUT, PA_BUS, PB_BUS output hiccup mode ON time	OC, V_{OUT}, V_{PA_BUS}, V_{PB_BUS} drop 10%	2.94	4.1	5.42	ms
T_{HICP_OFF}	OUT, PA_BUS, PB_BUS output hiccup mode OFF time	OC, OUT, PA_BUS, PB_BUS connect to GND	367	524	715	ms

8.7 Switching Characteristics

Over the recommended operating junction temperature range of -40 °C to 150 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SW (SW PIN)						
T_{ON_MIN}	Minimum turnon-time			84		ns
T_{ON_MAX}	Maximum turnon-time, HS timeout in dropout			6		µs
T_{OFF_MIN}	Minimum turnoff time			81		ns
D_{max}	Maximum switch duty cycle. While in frequency fold-back			98		%
TIMING RESISTOR AND INTERNAL CLOCK						
f_{SW_RANGE}	Switching frequency range using FREQ mode	9 kΩ ≤ R_{FREQ} ≤ 99 kΩ	200		800	kHz
f_{SW}	Switching frequency	R_{FREQ} = 80.6 kΩ	228	253	278	kHz
		R_{FREQ} = 49.9 kΩ	360	400	440	kHz
FS_{SS}	Frequency span of spread spectrum operation			±6		%
EXTERNAL CLOCK(SYNC)						
$f_{FREQ/SYNC}$	Switching frequency using external clock on FREQ/SYNC pin		200		800	kHz
T_{SYNC_MIN}	Minimum SYNC input pulse width	f_{SYNC} = 400kHz, $V_{FREQ/SYNC}$ > $V_{IH\_FREQ/SYNC}$, $V_{FREQ/SYNC}$ < $V_{IL\_FREQ/SYNC}$		100		ns
T_{LOCK_IN}	PLL lock time			100		µs
CC - CONNECT MANAGEMENT - ATTACH AND DETACH DEGLITCH						
$t_{DEGA\_CC\_ATT\_DETM}$	Attach asserting deglitch in the Detached Mode		1.29	2.05	3.05	ms

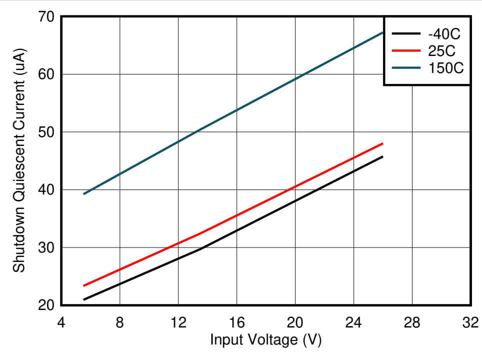
8.7 Switching Characteristics (continued)

Over the recommended operating junction temperature range of -40 °C to 150 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{DEGA\_CC\_DETACH\_SINKM}$	Detach asserting deglitch for exiting SINK Mode		8.2	12.5	18	ms
$t_{DEGA\_CC\_SHORT}$	Detach, Rd and Ra asserting deglitch		92	192	339	µs
$t_{DEGA\_CC\_LONG}$	Long deglitch		103	148	200	ms

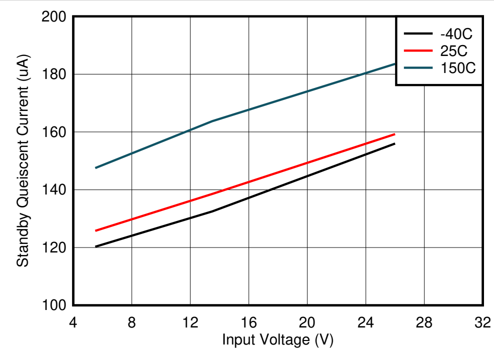
8.8 Typical Characteristics

Unless otherwise specified the following conditions apply: V_{IN} = 13.5 V, f_{SW} = 400 kHz, L = 3.3 µH, C_{SENSE} = 141 µF, C_{PA_BUS} = 1 µF, C_{PB_BUS} = 1 µF, T_A = 25 °C.



$V_{EN/EULVO}$ = 0 V PA_CC1 = R_d

Figure 8-1. Shutdown Quiescent Current



$V_{EN/UVLO}$ = V_{SENSE} PA_CC1/2 = OPEN

Figure 8-2. Standby Quiescent Current

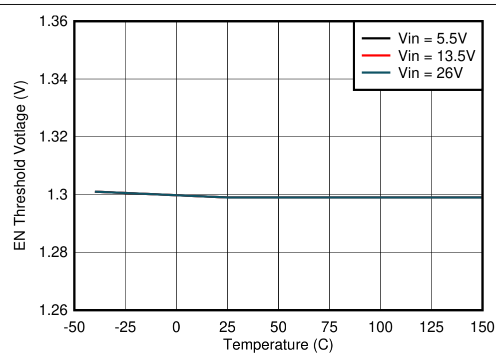
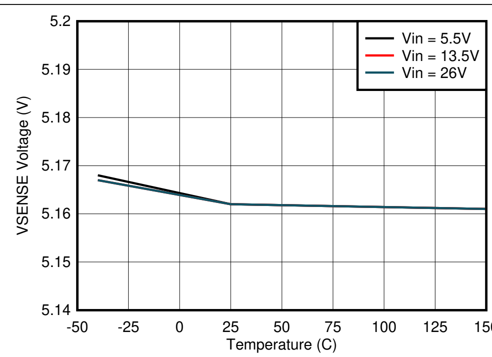
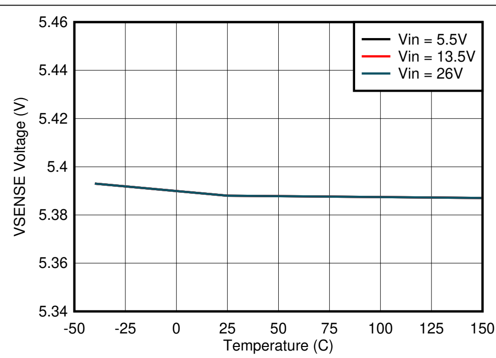


Figure 8-3. Precision Device Enable Threshold



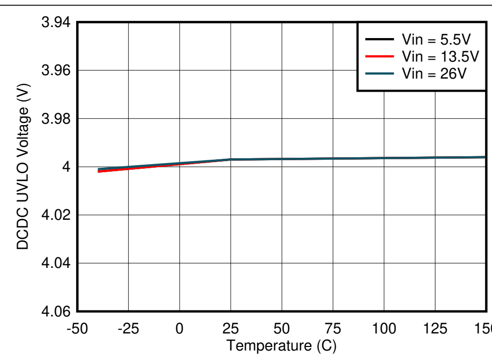
VSET = GND

Figure 8-4. V_{SENSE} Voltage vs Junction Temperature



R_{VSET} = 80.6 kΩ

Figure 8-5. V_{SENSE} Voltage vs Junction Temperature



$V_{EN/EULVO}$ = V_{SENSE} PA_CC1= R_d

Figure 8-6. DCDC UVLO Threshold

8.8 Typical Characteristics (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 13.5 V, f_{SW} = 400 kHz, L = 3.3 µH, C_{SENSE} = 141 µF, C_{PA_BUS} = 1 µF, C_{PB_BUS} = 1 µF, T_A = 25 °C.

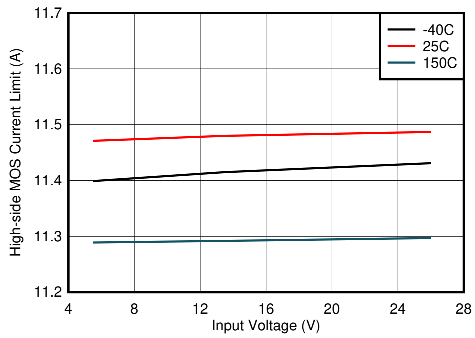


Figure 8-7. High-side Current Limit vs Input Voltage

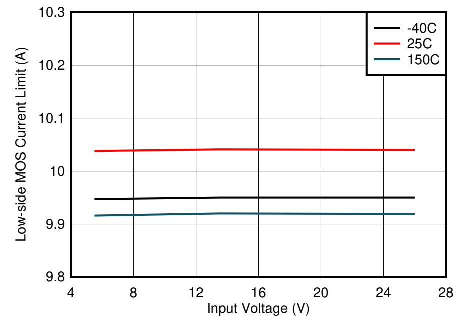
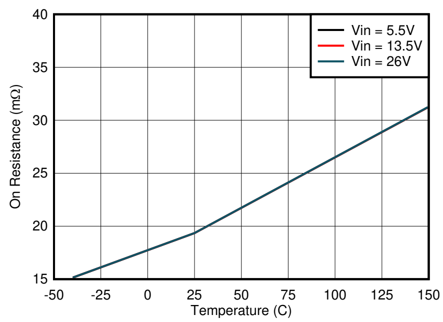
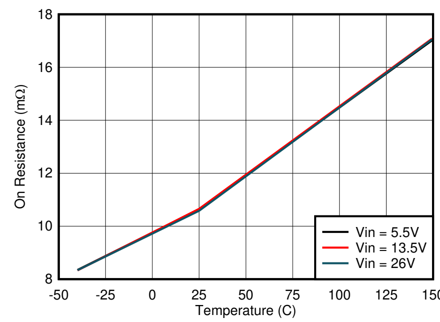


Figure 8-8. Low-side Current Limit vs Input Voltage



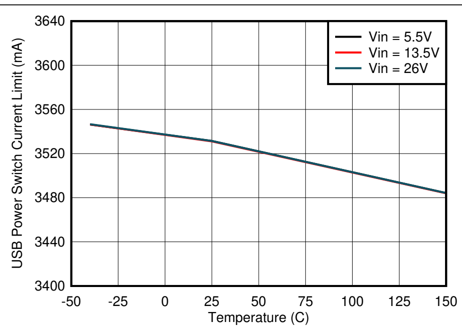
I_{PA_BUS} = 3 A I_{PB_BUS} = 2.4 A

Figure 8-9. High-side MOSFET on Resistance vs Junction Temperature



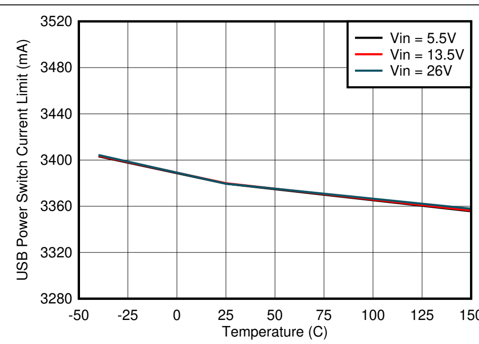
I_{PA_BUS} = 3 A I_{PB_BUS} = 2.4 A

Figure 8-10. Low-side MOSFET on Resistance vs Junction Temperature



ILIM = GND

Figure 8-11. USB Power Switch Current Limit vs Junction Temperature

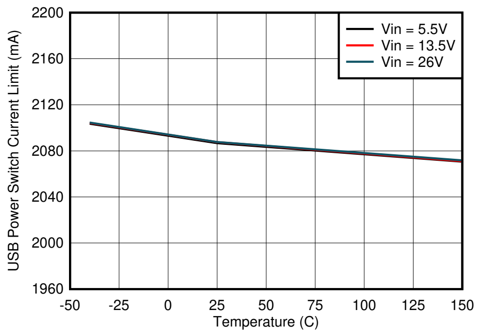


R_{ILIM} = 9.53 kΩ

Figure 8-12. USB Power Switch Current Limit vs Junction Temperature

8.8 Typical Characteristics (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 13.5 V, f_{SW} = 400 kHz, L = 3.3 µH, C_{SENSE} = 141 µF, C_{PA_BUS} = 1 µF, C_{PB_BUS} = 1 µF, T_A = 25 °C.



R_{ILIM} = 15.4 kΩ

Figure 8-13. USB Power Switch Current Limit vs Junction Temperature

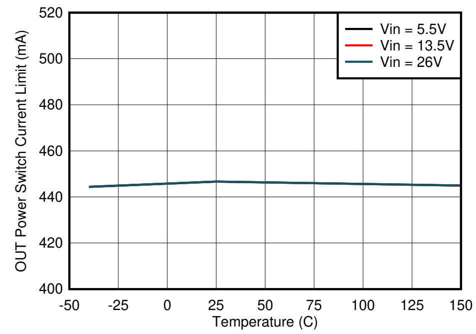


Figure 8-14. OUT Power Switch Current Limit vs Junction Temperature

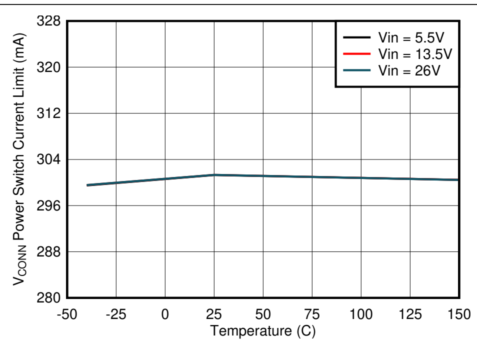
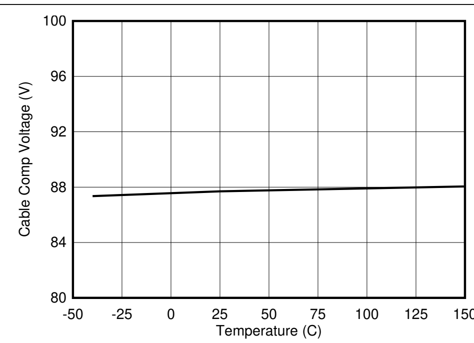


Figure 8-15. V_{CONN} Power Switch Current Limit vs Junction Temperature



I_{PA/B_BUS} = 2.4 A   VSET = GND

Figure 8-16. Cable Compensation Voltage vs Junction Temperature

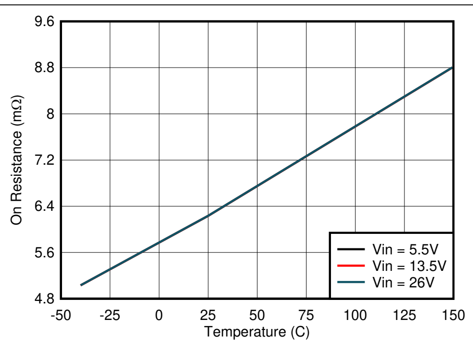


Figure 8-17. USB Power Switch On Resistance vs Junction Temperature

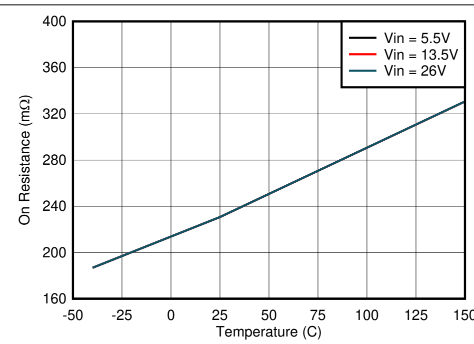


Figure 8-18. OUT Power Switch On Resistance vs Junction Temperature

8.8 Typical Characteristics (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 13.5 V, f_{SW} = 400 kHz, L = 3.3 µH, C_{SENSE} = 141 µF, C_{PA_BUS} = 1 µF, C_{PB_BUS} = 1 µF, T_A = 25 °C.

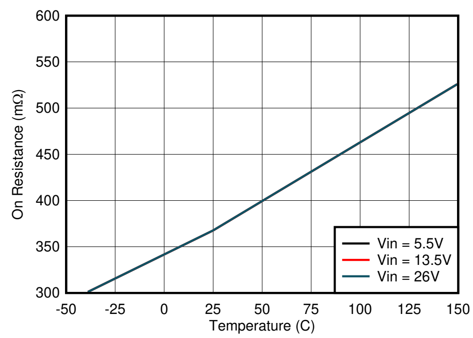
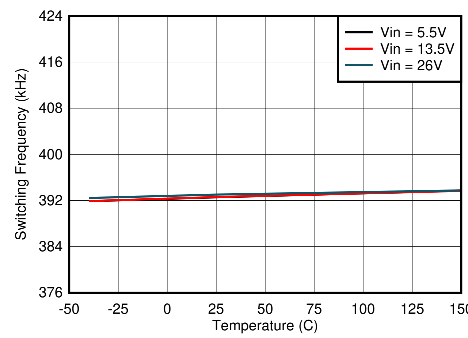
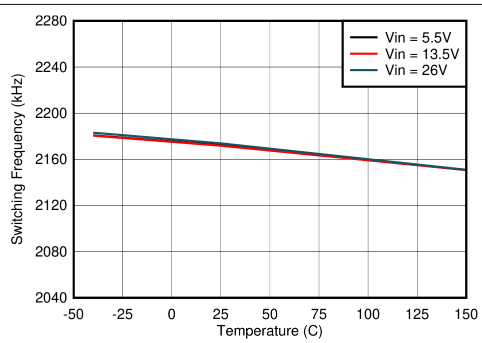


Figure 8-19. V_{CONN} Power Switch On Resistance vs Junction Temperature



R_{FREQ} = 49.9 kΩ

Figure 8-20. Switching Frequency vs Junction Temperature



R_{FREQ} = 8.45 kΩ

Figure 8-21. Switching Frequency vs Junction Temperature

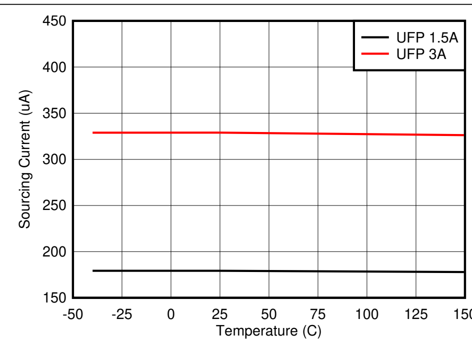


Figure 8-22. CC Sourcing Current vs Junction Temperature

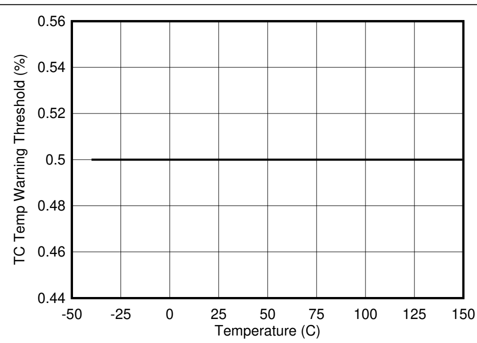


Figure 8-23. TS Temperature Wam Threshold vs Junction Temperature

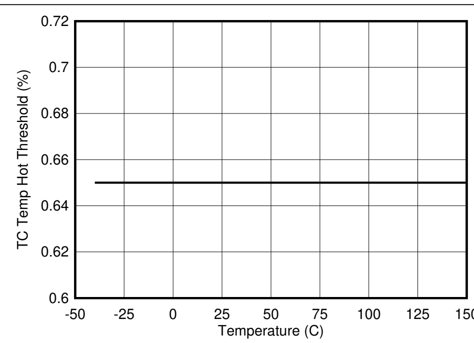


Figure 8-24. TS Temperature Hot Threshold vs Junction Temperature

8.8 Typical Characteristics (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 13.5 V, f_{SW} = 400 kHz, L = 3.3 µH, C_{SENSE} = 141 µF, C_{PA_BUS} = 1 µF, C_{PB_BUS} = 1 µF, T_A = 25 °C.

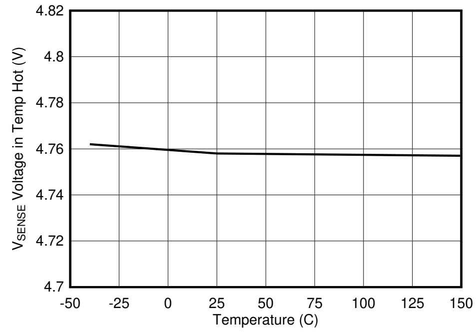


Figure 8-25. SENSE Voltage in Temperature Hot vs Junction Temperature

9 Parameter Measurement Information

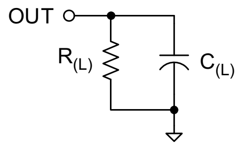


Figure 9-1. OUT Rise-Fall Test Load Figure

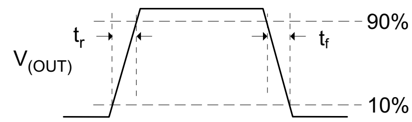


Figure 9-2. Power-On and Power-Off Timing

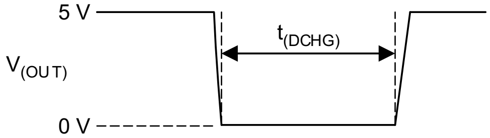


Figure 9-3. OUT Discharge During Mode Change

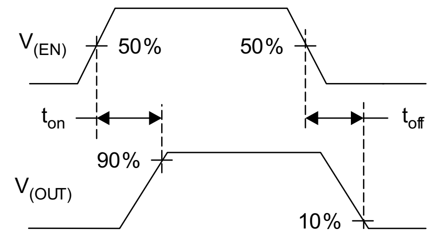


Figure 9-4. Enable Timing, Active-High Enable

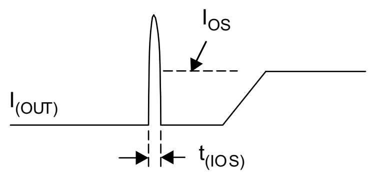


Figure 9-5. Output Short-Circuit Parameters

10 Detailed Description

10.1 Overview

The TPS2586x-Q1 is a full-featured solution for implementing a compact USB charging port with support for both Type-C and BC1.2 standards. Both devices contain an efficient buck regulator power source. For Type-C and Type-A dual ports, the TPS2586x-Q1 is capable of providing 6 A of output current at 5.17 V (nominal), 3 A for Type-C port, 2.4A for Type-A port, 200 mA for the OUT pin, and 200 mA for Port A VCONN power. The TPS2586x-Q1 is an automotive-focused USB charging controller and offers a robust solution, so it is recommend to add adequate protection (TVS3300 equivalent or better but auto qualified) on the IN pin to protect systems from high-power transients or lightning strikes.

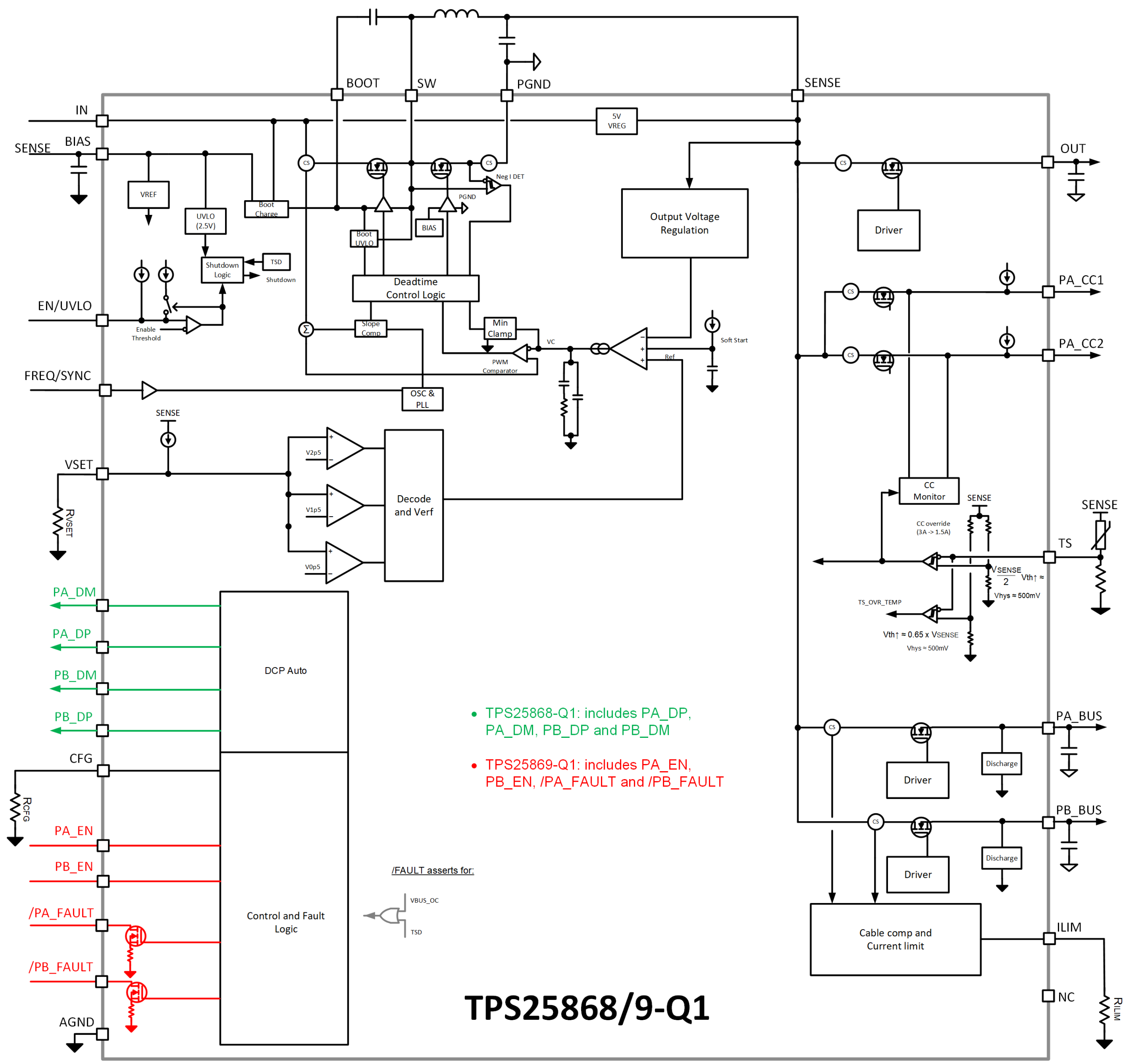
System designers can optimize efficiency or solution size through careful selection of switching frequency in the range of 200 KHz - 800 KHz with sufficient margin to operate below the AM radio frequency band. In the TPS2586x-Q1, the buck regulator operates in forced PWM mode, ensuring fixed switching frequency regardless of load current. Spread-spectrum frequency dithering reduces harmonic peaks of the switching frequency, potentially simplifying EMI filter design and easing compliance.

Current sensing through a precision FET current sense amplifier on the USB port enables an accurate, user-programmable overcurrent limit setting, and linear cable compensation to overcome IR losses when powering remote USB ports.

The TPS2586x-Q1 includes a TS input for user-programmable thermal protection using a negative temperature coefficient (NTC) resistor.

Both devices can support the USB Type-C protocol on the port A. For the TPS25868-Q1, it also supports the legacy Battery Charging Specification Rev 1.2 (BC1.2) DCP mode with an auto-detect feature to charge not only BC1.2-compliant hand-held devices, but also popular phones and tablets that incorporate their own propriety charging algorithm.

10.2 Functional Block Diagram



10.3 Feature Description

10.3.1 Power-Down or Undervoltage Lockout

The device is in power down mode if the IN terminal voltage is less than VUVLO, so the part is considered "dead" and all the terminals are high impedance. Once the IN voltage rises above the VUVLO threshold, the IC enters Sleep Mode or Active Mode, depending on the EN/UVLO voltage.

The voltage on the EN/UVLO pin controls the ON/OFF operation of the TPS2586x-Q1. An EN/UVLO pin voltage higher than $V_{EN/UVLO-H}$ is required to start the internal regulator and begin monitoring the CCn lines for a valid Type-C connection. The internal USB monitoring circuitry is on when V_{IN} is within the operation range and the EN/UVLO threshold is cleared. The buck regulator starts to operate, however, the USB ports load switch remains OFF until a valid Type-C detection has been made. This feature ensures the "cold socket" (0 V) USB Type-C V_{BUS} requirement is met.

The EN/UVLO pin is an input and cannot be left open or floating. The simplest way to enable the operation of the TPS2586x-Q1 is to connect EN to SENSE. This connection allows self-start-up of the TPS2586x-Q1 when V_{IN} is within the operation range. Note that you cannot connect the EN to IN pin directly for self-start-up.

Many applications benefit from the employment of enable dividers R_{ENT} and R_{ENB} to establish a precision system UVLO level for the TPS2586x-Q1 shown in Figure 10-1. The system UVLO can be used for sequencing, ensuring reliable operation, or supply protection, such as a battery discharge level. To ensure the USB port V_{BUS} is within the 5-V operating range as required for USB compliance (refer to USB.org for the latest USB specifications and requirements), it is suggested that the R_{ENT} and R_{ENB} resistors be chosen such that the TPS2586x-Q1 enables when V_{IN} is approximately 6 V. Considering the dropout voltage of the buck regulator and IR losses in the system, 6 V provides adequate margin to maintain V_{BUS} within USB specifications. If system requirements, such as a warm crank (start) automotive scenario, require operation with V_{IN} < 6 V, the values of R_{ENT} and R_{ENB} can be calculated assuming a lower V_{IN}. An external logic signal can also be used to drive the EN/UVLO input when a microcontroller is present and it is desirable to enable or disable the USB port remotely for other reasons.

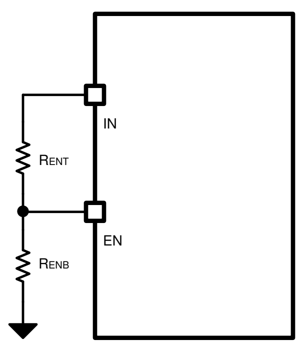


Figure 10-1. System UVLO by Enable Divider

UVLO configuration using external resistors is governed by the following equations:

$$R_{ENT} = \left(\frac{V_{IN(ON)}}{V_{EN/UVLO\_H}} - 1\right) \times R_{ENB} \quad (1)$$

$$V_{IN(OFF)} = V_{IN(ON)} \times \left(1 - \frac{V_{EN/UVLO\_HYS}}{V_{EN/UVLO\_H}}\right) \quad (2)$$

For example:

$V_{IN(ON)}$ = 6 V

R_{ENT} = 20 kΩ

$$R_{ENB} = [(V_{EN\text{-}VOUT\text{-}H}) / (V_{IN(ON)} – V_{EN})] \times R_{ENT} \quad (3)$$

R_{ENB} = 5 kΩ

Therefore, $V_{IN(OFF)}$ = 5.5 V

10.3.2 Input Overvoltage Protection (OVP) - Continuously Monitored

The operation voltage range of the TPS2586x-Q1 is up to 26 V. If the input source applies an overvoltage, the buck regulator HSFET/LSFET turns off immediately. Thus, the USB ports and OUT pin loses their power as well. Once the overvoltage returns to a normal voltage, the buck regulator continues switching and provides power on the USB ports and OUT pin.

During the overvoltage condition, the internal regulator regulates the SENSE voltage at 5 V, so the SENSE always has power for the internal bias circuit and external NTC pullup reference.

10.3.3 Buck Converter

The following operating description of the TPS2586x-Q1 refers to the *Functional Block Diagram*. The TPS2586x-Q1 integrates a monolithic, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs and USB current-limit switches with charging ports auto-detection. The TPS2586x-Q1 offers a compact and high efficiency solution with excellent load and line regulation over a wide input supply range. The TPS2586x-Q1 supplies a regulated output voltage by turning on the high-side (HS) and low-side (LS) NMOS switches with controlled duty cycle. During high-side switch ON time, the SW pin voltage swings up to approximately V_{IN}. The inductor current i_L increases with linear slope (V_{IN} – V_{OUT}) / L. When the HS switch is turned off by the control logic, the LS switch is turned on after an anti-shoot-through dead time. Inductor current discharges through the LS switch with a slope of $–V_{OUT}$ / L. The control parameter of a buck converter is defined as Duty Cycle D = t_{ON} / T_{SW}, where t_{ON} is the high-side switch ON time and T_{SW} is the switching period, shown in Figure 10-2. The regulator control loop maintains a constant output voltage by adjusting the duty cycle D. In an ideal buck converter, where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: D = V_{OUT} / V_{IN}.

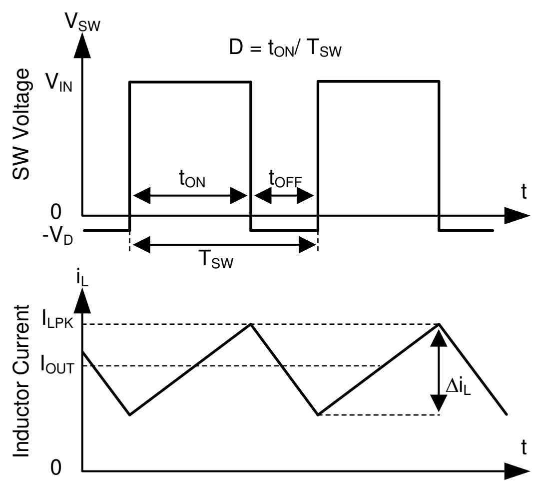


Figure 10-2. SW Node and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

The TPS2586x-Q1 operates in a fixed-frequency, peak-current-mode control to regulate the output voltage. A voltage feedback loop is used to get accurate DC voltage regulation by adjusting the peak current command based on voltage offset. The peak inductor current is sensed from the high-side switch and compared to the peak current threshold to control the ON time of the high-side switch. The voltage feedback loop is internally compensated, which allows for fewer external components, making it easy to design, and provides stable operation with a reasonable combination of output capacitors. The TPS2586x-Q1 operates in FPWM mode for low output voltage ripple, tight output voltage regulation, and constant switching frequency.

The TPS2586x-Q1 also has variants to support PFM mode. In PFM mode, the high-side FET is turned on in a burst of one or more cycles to provide energy to the load. The frequency of these bursts is adjusted to regulate the output, while diode emulation is used to maximize efficiency. This mode provides high light-load efficiency by reducing the amount of input supply current required to regulate the output voltage at small loads. A small increase in the output voltage occurs in PFM. This trades off very good light load efficiency for larger output voltage ripple and variable switching frequency.

10.3.4 FREQ/SYNC

The switching frequency of the TPS2586x-Q1 can be programmed by the resistor R_{FREQ} from the FREQ/SYNC pin and AGND pin. To determine the FREQ resistance, for a given switching frequency, use Equation 4:

$$R_{FREQ}(k\Omega) = 26660 \times f_{SW}^{-1.0483}(kHz) \quad (4)$$

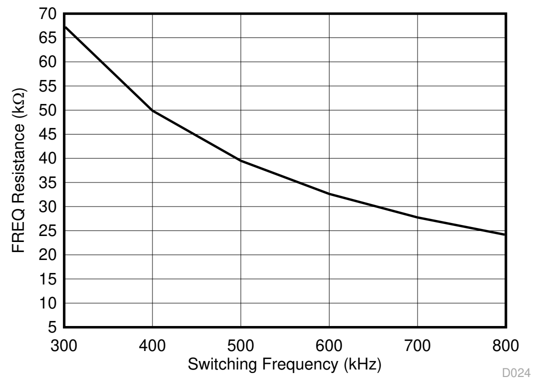


Figure 10-3. FREQ Set Resistor vs Switching Frequency

The normal method of setting the buck regulator switching frequency is by selecting an appropriate value FREQ resistor as shown in Table 10-1.

Table 10-1. Setting the Switching Frequency with FREQ

FREQ (KΩ)	SWITCHING FREQUENCY (KHz)
80.6	253
49.9	400

The FREQ/SYNC pin can be used to synchronize the internal oscillator to an external clock. The internal oscillator can be synchronized by AC coupling a positive edge into the FREQ/SYNC pin. When using a low impedance signal source, the frequency setting resistor FREQ is connected in parallel with an AC coupling capacitor, C_{COUP}, to a termination resistor, R_{TERM} (for example, 50 Ω). The two resistors in series provide the default frequency setting resistance when the signal source is turned off. A 10-pF ceramic capacitor can be used for C_{COUP}. The AC coupled peak-to-peak voltage at the FREQ/SYNC pin must exceed the SYNC amplitude threshold of 1.2 V (typical) to trip the internal synchronization pulse detector, and the minimum SYNC clock HIGH and LOW time must be longer than 100 ns (typical). A 2.5 V or higher amplitude pulse signal coupled through a 1-nF capacitor, C_{SYNC}, is a good starting point. Figure 10-4 shows the device synchronized to an external system clock. The external clock must be off before start-up to allow proper start-up sequencing.

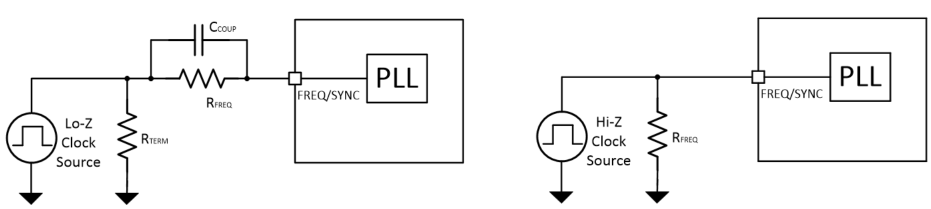


Figure 10-4. Synchronize to External Clock

The TPS2586x-Q1 switching action can be synchronized to an external clock from 200 KHz to 800 KHz.

10.3.5 Bootstrap Voltage (BOOT)

The TPS2586x-Q1 provides an integrated bootstrap voltage regulator. A small capacitor between the BOOT and SW pins provides the gate drive voltage for the high-side MOSFET. The BOOT capacitor is refreshed when the high-side MOSFET is off and the low-side switch conducts. The recommended value of the BOOT capacitor is 100 nF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended for stable performance over temperature and voltage. The BOOT rail has a UVLO to protect the chip from operation with too little bias, and is typically 2.2 V. If the BOOT capacitor voltage drops below the UVLO threshold, the device initiates a charging sequence using the low-side FET before attempting to turn on the high-side device.

10.3.6 Minimum ON-Time, Minimum OFF-Time

Minimum ON-time, T_{ON_MIN}, is the smallest duration of time that the HS switch can be on. T_{ON_MIN} is typically 84 ns in the TPS2586x-Q1. Minimum OFF-time, T_{OFF_MIN}, is the smallest duration that the HS switch can be off. T_{OFF_MIN} is typically 81 ns in the TPS2586x-Q1. In CCM (FPWM) operation, T_{ON_MIN} and T_{OFF_MIN} limit the voltage conversion range given in a selected switching frequency.

The minimum duty cycle allowed is:

$$D_{MIN} = T_{ON\_MIN} \times f_{SW} \tag{5}$$

And the maximum duty cycle allowed is:

$$D_{MAX} = 1 - T_{OFF\_MIN} \times f_{SW} \tag{6}$$

Given fixed T_{ON_MIN} and T_{OFF_MIN}, the higher the switching frequency, the narrower the range of the allowed duty cycle.

Given an output voltage, the choice of the switching frequency affects the allowed input voltage range, solution size, and efficiency. The maximum operation supply voltage can be found by:

$$V_{IN\_MAX} = \frac{V_{OUT}}{\left(f_{SW} \times T_{ON\_MIN}\right)} \tag{7}$$

At lower supply voltage, the switching frequency is limited by T_{OFF_MIN}. The minimum V_{IN} can be approximated by:

$$V_{IN\_MIN} = \frac{V_{OUT}}{\left(1 - f_{SW} \times T_{OFF\_MIN}\right)} \tag{8}$$

Considering power losses in the system with heavy load operation, V_{IN_MAX} is higher than the result calculated in Equation 7.

If minimum ON-time or minimum OFF-time do not support the desired conversion ratio, frequency is reduced, automatically allowing regulation to be maintained during load dump and with very low dropout during cold crank even with high operating-frequency setting.

10.3.7 Internal Compensation

The TPS2586x-Q1 is internally compensated. The internal compensation is designed such that the loop response is stable over the specified operating frequency and output voltage range. The TPS2586x-Q1 is optimized for transient response over the range of 200 kHz ≤ fsw ≤ 3000 kHz.

10.3.8 Selectable Output Voltage (VSET)

The TPS2586x-Q1 provides four different output voltage options. The voltage can be set by an external resistor across the VSET pin. The normal method of setting the buck output voltage is by selecting an appropriate value VSET resistor as shown in Table 10-2.

Table 10-2. VSET Configuration vs BUS Output Voltage

VSET CONFIGURATION	V_{SENSE}
Float or pull up to V_{SENSE}	5.1 V
Short to GND	5.17 V
R_{VSET} = 40.2 KΩ	5.3 V
R_{VSET} = 80.6 KΩ	5.4 V

Note that the VSET has an internal weak 20-µA current source to overdrive the pin to SENSE. If this pin is floated, the voltage on this pin approaches the SENSE voltage, and sets the output voltage to 5.1 V. It is not recommend to float this pin if there is external noise from the PCB board, since the noise interferes with the VSET internal logic block.

10.3.9 Current Limit and Short Circuit Protection

For maximum versatility, the TPS2586x-Q1 includes both a precision, programmable current limit as well cycle-by-cycle current limit to protect the USB port from extreme overload conditions. The R_{ILIM} resistor determines the overload threshold on the USB ports in the event ILIM is shorted to ground to set the default USB current limit. The cycle-by-cycle current limit serves as a backup means of protection.

10.3.9.1 USB Switch Programmable Current Limit (ILIM)

Since the TPS2586x-Q1 integrates two USB current-limit switches, it provides adjustable current limit to prevent USB port overheating. It engages the Two-Level current limit scheme, which has one typical current limit, I_{OS_BUS}, and the secondary current limit, I_{OS_HI}. The secondary current limit, I_{OS_HI}, is 1.6x the primary current limit, I_{OS_BUS}. The secondary current limit acts as the current limit threshold for a deglitch time, $t_{IOS\_HI\_DEG}$, then the USB power switch current limit threshold is set back to I_{OS_BUS}. Equation 9 calculates the value of resistor for adjusting the port A typical current limit.

$$R_{ILIM}(K\Omega) = \frac{32273}{I_{OS\_BUS(Port\ A)}(mA)} \tag{9}$$

Note in TPS25860/2-Q1, the Port A is the Type-C port, and Port B is the Type-A port, the Port B current limit is the ration of Port A, which fix at 80% internally. R_{ILIM} is the resistor that can be changed to achieve different current limit for Port A and Port B. Typical R_{ILIM} resistors value are listed in Table 10-3:

Table 10-3. Setting the Current Limit with R_{ILIM}

R_{ILIM} (kΩ)	I_{OS_BUS}: Current-Limit Threshold (mA)	
	Port A	Port B (= 0.8 × Port A)
12.4	2603	2082
9.53	3386	2709
0 (ILIM short to GND)	3550	2840

This equation assumes an ideal-no variation-external adjusting resistor. To take resistor tolerance into account, first determine the minimum and maximum resistor values based on its tolerance specifications and use these values in the equations. Because of the inverse relationship between the current limit and the adjusting resistor, use the maximum resistor value in the $I_{OS(min)}$ equation and the minimum resistor value in the $I_{OS(max)}$ equation.

For the normal application, the ILIM pin can short to GND directly, which sets a default 3.55-A and 2.84-A current limit with a maximum ±15% variation on USB port A and port B separately to follow the USB specification. The TPS2586x-Q1 provides built-in soft-start circuitry that controls the rising slew rate of the output voltage to limit inrush current and voltage surges.

The secondary current limit, I_{OS_HI}, allows the USB port pull out a larger current for a short time, which can benefit USB port MFi OCP testing. In a normal application, once the device is powered on and USB port is not in UVLO, the USB port current limit threshold is overridden by the secondary current limit, I_{OS_HI}, so the USB port can output as high as a 1.6 × I_{OS_BUS} current for typically 2 ms. After the deglitch time, $t_{IOS\_HI\_DEG}$, the current limit threshold is set back to the typical current with I_{OS_BUS}. The secondary current limit threshold does not resume until after the $t_{IOS\_HI\_RST}$ deglitch time, which is typically 16 ms. If there is an inrush current higher than the I_{OS_HI} threshold, the current limit is set back to I_{OS_BUS} immediately, without waiting for a $t_{IOS\_HI\_DEG}$.

The TPS2586x-Q1 responds to overcurrent conditions by limiting output current to I_{OS_BUS} as shown in previous equation. When an overload condition occurs, the device maintains a constant output current and the output voltage reduces accordingly. Three possible overload conditions can occur:

- The first condition is when a short circuit or overload is applied to the USB output when the device is powered up or enabled. There can be inrush current and once it triggers the approximate 8-A threshold, a fast turnoff circuit is activated to turn off the USB power switch within t_{IOS_USB} before the current limit control loop is able to respond (shown in Figure 10-5). After the fast turnoff is triggered, the USB power switch turns off for approximately 200 µs, and restarts with a soft start. If the USB port is still in overcurrent condition, the short circuit and overload hold the output near zero potential with respect to ground and the power switch ramps the output current to I_{OS_BUS}. If the overcurrent limit condition lasts longer than 4.1 ms, the corresponding USB channel enters hiccup mode with 524 ms of off-time and 4.1 ms of on-time.

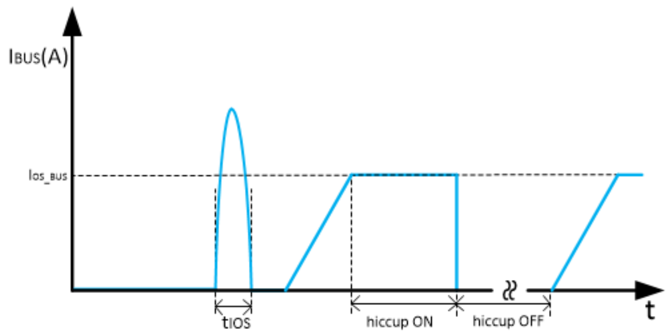


Figure 10-5. Response Time to BUS Short-Circuit

- The second condition is the load current increases above I_{OS_BUS} but below the I_{OS_HI} setting. The device allows the USB port to output this large current for $t_{IOS\_HI\_DEG}$, without limiting the USB port current to I_{OS_BUS}. After the $t_{IOS\_HI\_DEG}$ deglitch time, device will limit the output current to I_{OS_BUS} and works in a constant current-limit mode. If the load demands a current greater than I_{OS_BUS}, the USB output voltage decreases to $I_{OS\_BUS} \times R_{LOAD}$ for a resistive load, which is shown in Figure 10-6. If the overcurrent limit condition lasts longer than 4.1 ms, the corresponding USB channel enters hiccup mode with 524 ms of off-time and 4.1 ms of on-time. Another USB channel still works normally.

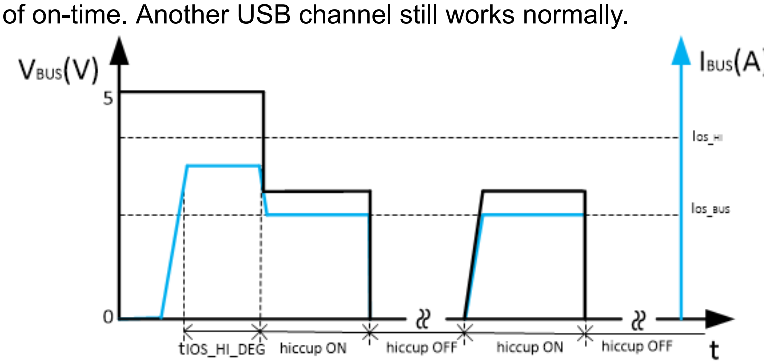


Figure 10-6. BUS Overcurrent Protection

- The third condition is the load current increases above the I_{OS_HI} setting. In this case, the USB power switch current limit threshold is set back to the primary current limit, I_{OS_BUS}, immediately. If the load still demands a current greater than I_{OS_BUS}, the USB output voltage decreases to $I_{OS\_BUS} \times R_{LOAD}$ for a resistive load, which is shown in Figure 10-7. If the overcurrent limit condition lasts longer than 4.1 ms, the corresponding USB channel enters hiccup mode with 524 ms of off-time and 4.1 ms of on-time. Another USB channel still works normally.

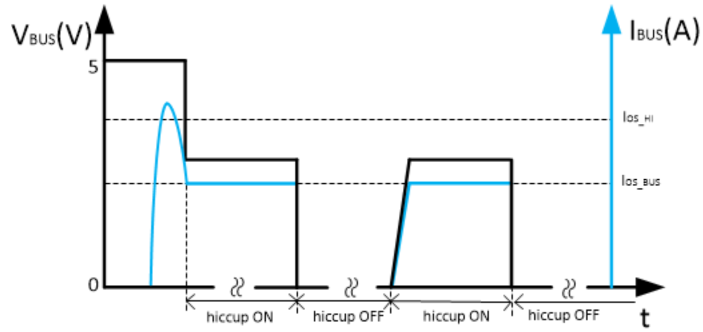


Figure 10-7. BUS Overcurrent Protection: Two-Level Current Limit

The TPS2586x-Q1 thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the previously mentioned cases. Thermal limiting turns off the internal NFET and starts when the NFET junction temperature exceeds 160°C (typical). The device remains off until the NFET junction temperature cools 10°C (typical) and then restarts. This extra thermal protection mechanism can help prevent further junction temperature rise, which can cause the device to turn off due to junction temperature exceeding the main thermal shutdown threshold, T_{SD}.

10.3.9.2 Interlocking for Two-Level USB Switch Current Limit

The TPS2586x-Q1 has two USB ports. Since the secondary current limit, I_{OS_HI}, is 1.6x of the primary current limit, I_{OS_BUS}, if the two USB ports pull out larger current at the same time, then the DC-DC regulator is overloaded, and DC-DC regulator output voltage can be crashed. To avoid these potential issues, the TPS2586x-Q1 adopts the interlocking scheme to manage the current limits of the two USB ports.

For interlocking, if one USB port current is beyond the primary current limit threshold, I_{OS_BUS}, then another USB port current limit threshold will be overridden to the primary current limit, I_{OS_BUS}, immediately. With this control scheme, the TPS2586x-Q1 only allows one USB port to output a large current, which can as high as 1.6x of the primary current limit, I_{OS_BUS}, at the same time. Ensure the DC-DC regulator has enough energy to sustain its output voltage.

10.3.9.3 Cycle-by-Cycle Buck Current Limit

There is a buck regulator cycle-by-cycle current limit on both the peak and valley of the inductor current.

High-side MOSFET overcurrent protection is implemented by the nature of the Peak Current Mode control. The HS switch current is sensed when the HS is turned on after a set blanking time. The HS switch current is compared to the output of the Error Amplifier (EA) minus slope compensation every switching cycle. The peak current of HS switch is limited by a clamped maximum peak current threshold, I_{HS_LIMIT}, which is constant. The peak current limit of the high-side switch is not affected by the slope compensation and remains constant over the full duty cycle range.

The current going through LS MOSFET is also sensed and monitored. When the LS switch turns on, the inductor current begins to ramp down. The LS switch is turned OFF at the end of a switching cycle if its current is above the LS current limit, I_{LS_LIMIT}. The LS switch is kept ON so that the inductor current keeps ramping down until the inductor current ramps below the LS current limit, I_{LS_LIMIT}. Then, the LS switch is turned OFF and the HS switch is turned on after a dead time. This action is somewhat different than the more typical peak current limit, and results in Equation 10 for the maximum load current.

$$I_{OUT\_MAX} = I_{LS\_LIMIT} + \frac{(V_{IN} - V_{OUT})}{2 \times f_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}} \quad (10)$$

10.3.9.4 OUT Current Limit

The TPS2586x-Q1 can provide 200-mA current at the OUT pin to power the auxiliary loads, such as USB HUB, LEDs. The OUT regulator input comes from the buck output, so the voltage is the same with the SNESE pin, which depends on the VSET setting.

If the OUT current reaches the current limit level, the OUT pin MOSFET works in a constant current-limit mode. If the overcurrent limit condition lasts longer than 4.1 ms, it enters hiccup mode with 4.1 ms of on-time and 524 ms of off-time.

10.3.10 Cable Compensation

When a load draws current through a long or thin wire, there is an IR drop that reduces the voltage delivered to the load. In the vehicle from the voltage regulator output V_{OUT} to V_{BUS} (input voltage of portable device), the total resistance of PCB trace, connector, and cable resistances causes an IR drop at the portable device input, so the charging current of most portable devices is less than their expected maximum charging current. The voltage drop is shown in Figure 10-8.

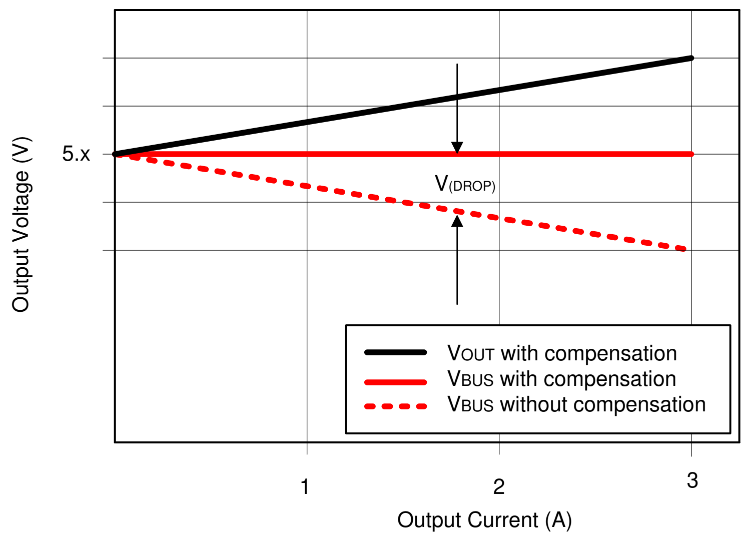


Figure 10-8. Voltage Drop

To handle this case, the TPS2586x-Q1 has a built-in cable compensation function where the droop compensation linearly increases the voltage at the SENSE pin of the TPS2586x-Q1 as load current increases, to maintain a fairly constant output voltage at the load-side voltage.

For the TPS2586x-Q1, the internal comparator compares the current-sense output voltage of the two current-limit switches and uses the larger current-sense output voltage to compensate for the line drop voltage. The cable compensation amplitude increases linearly as the load current increases. It also has an upper limitation. The cable compensation at output currents greater than 2.4 A is 90 mV and is shown in Figure 10-9. Note the cable compensation only works when you short the VSET to GND. For the other VSET configuration, the cable compensation is not available.

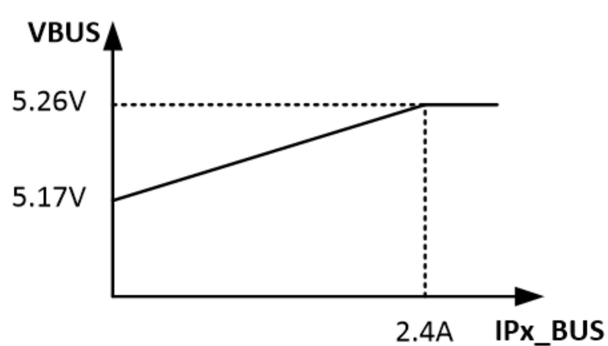


Figure 10-9. Dual Ports Cable Compensation

10.3.11 Thermal Management with Temperature Sensing (TS) and OTSD

The TS input pin allows for user-programmable thermal protection, see the Electrical Characteristics for the TS pin thresholds. The TS input pin threshold is ratiometric with V_{SENSE}. The external resistor divider setting, V_{TS}, must be connected to the TPS2586x-Q1 SENSE pin to achieve accurate results (refer to the Figure 10-10). When $V_{TS} = 0.5 \times V_{SENSE}$, the TPS2586x-Q1 performs two actions:

- If you are operating with 3-A Type-C advertisement, the PA_CC1, PA_CC2 pin automatically reduces advertisement to the 1.5-A level.

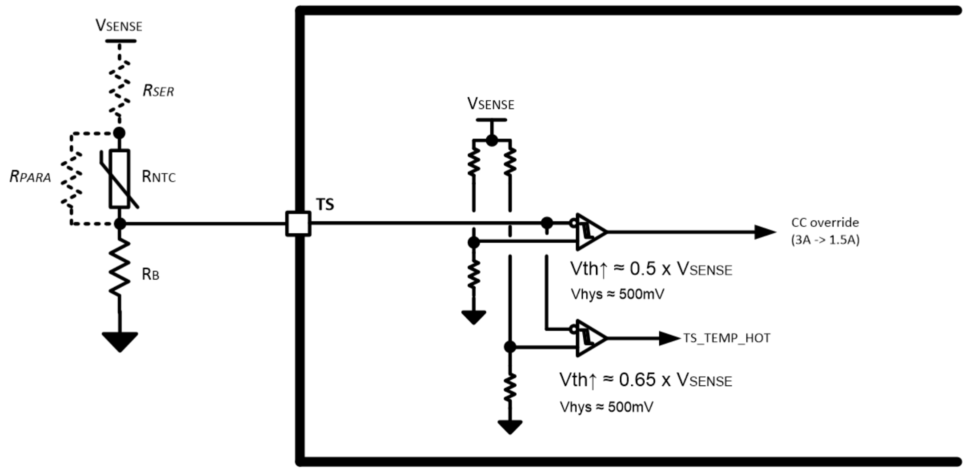


Figure 10-10. TS Input

If the overtemperature condition persists, causing $V_{TS} = 0.65 \times V_{SENSE}$, the TPS2586x-Q1 operates at default USB mode, which means it broadcasts the Default USB Power mode, and the output voltage at the SENS pin is reduced to 4.77 V.

In Default USB Power, the charging is ideally reduced further per the USB2.0 and USB3.0 specification.

If the overtemprature condition persists, causing T_J to reach the OTSD threshold, then the device thermal shuts down.

If the overtemprature condition persists, causing T_J to reach the OTSD threshold, then the device thermal shuts down.Figure 10-11 shows the TPS2586x-Q1 behavior when TS pin voltge trigger the Temp Warm and Temp Hot threshold.

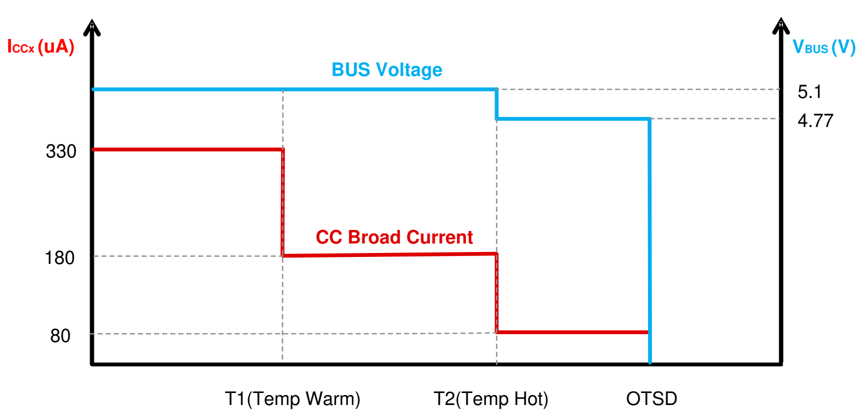


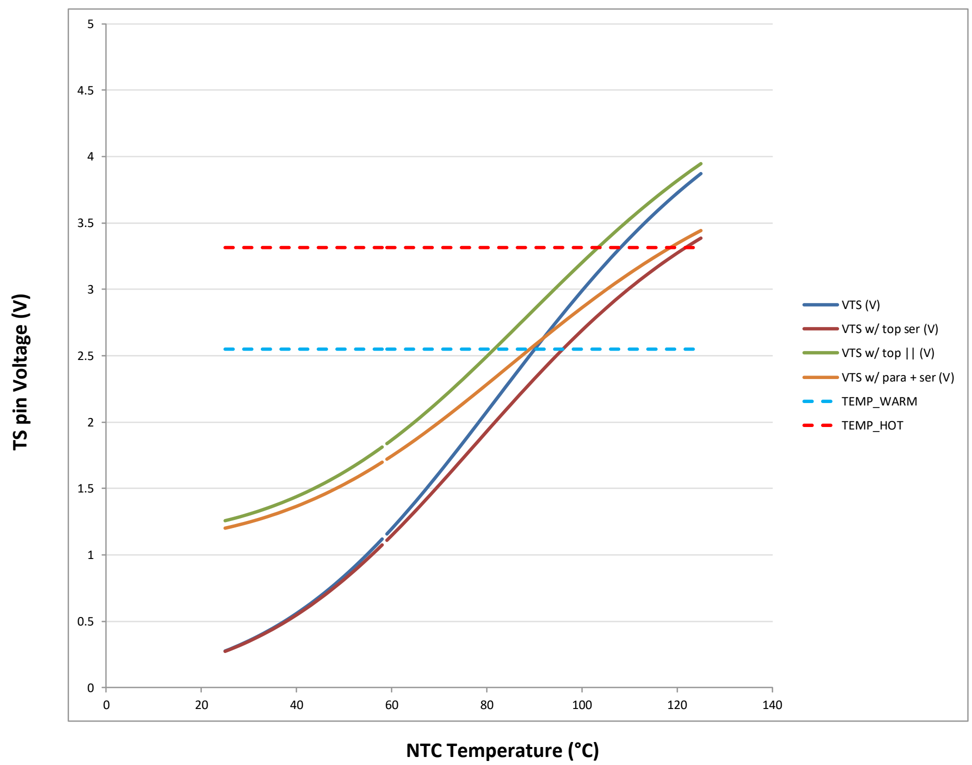
Figure 10-11. TPS2586x-Q1 Behavior When Trigger Temp Warm and Hot threshold

The NTC thermistor must be placed near the hottest point on the PCB. In most cases, this is close to the SW node of the TPS2586x-Q1, near the buck inductor.

Tuning the V_{NTC} threshold levels of V_{TEMP_WARM} and V_{TEMP_HOT} is achieved by adding R_{SER}, R_{PARA}, or both R_{SER} and R_{PARA} in conjunction with R_{NTC}. Figure 10-12 is an example illustrating how to set the V_{TEMP_WARM} threshold between 81°C and 90°C with a ΔT between TEMP_WARM assertion and TEMP_HOT assertion of 18°C to 29°C. Consult the chosen NTC manufacturer's specification for the value of β. It may take some iteration to establish the desired warning and shutdown thresholds.

Below is NTC spec and resistor value used in Figure 10-12 example.

- R_0 = 470 kΩ. β = 4750. $R_{NTC} = R_0 \times \exp \beta \times (1/T - 1/T_0)$.
- R_{PARA} = 100 kΩ.
- R_{SER} = 5.1 kΩ.
- $R_B = R_{NTC}$(at TEMP_WARM) = 27 kΩ.



Rising Thresholds		V (V)	T NTC (°C)	T NTC || (°C)	T NTC ser (°C)	T NTC || + ser (°C)
Temp Warm	=VSENSE * 0.5	2.55	90	81	95	89
Temp Hot	=VSENSE * 0.65	3.315	108	103	121	118
TEMP_HOT - TEMP_WARM			18	22	26	29

Figure 10-12. V_{TS} Threshold Design Examples

10.3.12 Thermal Shutdown

The device has an internal overtemperature shutdown threshold, T_{SD}, to protect the device from damage and overall safety of the system. When the device temperature exceeds T_{SD}, the device is turned off when thermal shutdown activates. Once the die temperature falls below 154°C (typical), the device re-initiates the power-up sequence controlled by the internal soft-start circuitry.

10.3.13 USB Enable On/Off Control (TPS25869-Q1)

The PA_EN and PB_EN are the on/off control input pins for PA_USB and PB_USB, respectively. The USB switch is active when Px_EN is pulled high. Pull the Px_EN voltage to logic low to shut down the USB switch with an output discharge. Connect Px_EN to SENSE for automatic start-up, or control them by an external on/off signal from the microcontroller or USB HUB.

10.3.14 FAULT Indication

For the TPS25869-Q1, $\overline{\text{PA\_FAULT}}$ and $\overline{\text{PB\_FAULT}}$ are the fault indication pins for PA_USB and PB_USB, respectively. FAULT is in an open-drain state during shutdown, start-up, or normal condition. When the USB switch enters hiccup mode, or overtemperature thermal shutdown (OTSD) is triggered, $\overline{\text{Px\_FAULT}}$ is pulled low. $\overline{\text{FAULT}}$ asserts (logic low) on an individual USB switch during an overcurrent or overtemperature condition. $\overline{\text{Px\_FAULT}}$ switches high after the fault condition is removed, and the USB output voltage goes high again.

The device features an active-low, open-drain fault output. Connect a 100-kΩ pullup resistor from $\overline{\text{Px\_FAULT}}$ to SENSE or other suitable I/O voltage. $\overline{\text{Px\_FAULT}}$ can be left open or tied to GND when not used.

Table 10-4 summarizes the conditions that generate a fault and actions taken by the device.

Table 10-4. Fault Conditions

EVENT	CONDITION	ACTION
Overcurrent on Px_BUS	I_{Px_BUS} > Programmed I_{ILIM}	Px_BUS load switch enter hiccup mode. The fault indicator asserts with a 4.1-ms deglitch and de-asserts with a 16.4-ms deglitch. The fault indicator remains asserted during the Px_BUS overload condition.
TPS2586x-Q1 overtemperature	$T_J > T_{SD}$	The device immediately disables and asserts fault indicator with no deglitch. The device attempts to power up once the die temperature decreases below the thermal hysteresis threshold as specified

10.3.15 USB Specification Overview

All USB ports are capable of providing a 5-V output, making them a convenient power source for operating and charging portable devices. USB specification documents outline specific power requirements to ensure interoperability. In general, a USB 2.0 port host port is required to provide up to 500 mA; a USB 3.0 or USB 3.1 port is required to provide up to 900 mA; ports adhering to the USB Battery Charging 1.2 Specification provide up to 1500 mA; newer Type-C ports can provide up to 3000 mA. Though USB standards governing power requirements exist, some manufacturers of popular portable devices created their own proprietary mechanisms to extend allowed available current beyond the 1500 mA maximum per BC 1.2. While not officially part of the standards maintained by the USB-IF, these proprietary mechanisms are recognized and implemented by manufacturers of USB charging ports.

The TPS2586x-Q1 device supports five of the most-common USB-charging schemes found in popular hand-held media and cellular devices:

- USB Type-C (1.5-A and 3-A advertisement)
- USB Battery Charging Specification BC1.2 DCP mode
- Chinese Telecommunications Industry Standard YD/T 1591-2009
- Divider 3 mode
- 1.2-V mode

10.3.16 USB Type-C® Basics

For a detailed description of the Type-C specification, refer to the USB-IF website to download the latest released version. Some of the basic concepts of the Type-C spec that pertains to understanding the operation of the TPS2586x-Q1 (a DFP device) are described as follows.

USB Type-C removes the need for different plug and receptacle types for host and device functionality. The Type-C receptacle replaces both the Type-A and Type-B receptacles since the Type-C cable is plug-able in either direction between the host and device. A host-to-device logical relationship is maintained by the configuration channel (CC). Optionally, hosts and devices can be either providers or consumers of power when USB PD communication is used to swap roles.

All USB Type-C ports operate in one of following data modes:

- Host mode: The port can only be a host (provider of power).
- Device mode: The port can only be a device (consumer of power).

- Dual-Role mode: The port can be either a host or device.

Port types:

- DFP (Downstream Facing Port): Host
- UFP (Upstream Facing Port): Device
- DRP (Dual-Role Port): Host or Device

Valid DFP-to-UFP connections:

- Table 10-5 describes valid DFP-to-UFP connections.
- Host-to-Host or Device-to-Device have no functions.

Table 10-5. DFP-to-UFP Connections

	HOST-MODE PORT	DEVICE-MODE PORT	DUAL-ROLE PORT
Host-Mode Port	No Function	Works	Works
Device-Mode Port	Works	No Function	Works
Dual-Role Port	Works	Works	Works(1)

(1) This may be automatic or manually driven.

10.3.16.1 Configuration Channel

The function of the configuration channel is to detect connections and configure the interface across the USB Type-C cables and connectors.

Functionally, the Configuration Channel (CC) is used to serve the following purposes:

- Detect connect to the USB ports.
- Resolve cable orientation and twist connections to establish USB data bus routing.
- Establish DFP and UFP roles between two connected ports.
- Discover and configure power: USB Type-C current modes or USB Power Delivery.
- Discover and configure optional Alternate and Accessory modes.
- Enhances flexibility and ease of use.

Typical flow of DFP-to-UFP configuration is shown in Figure 10-13.

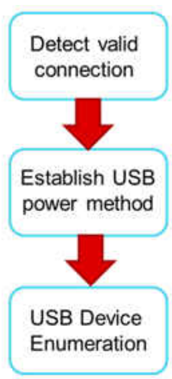


Figure 10-13. Flow of DFP-to-UFP Configuration

10.3.16.2 Detecting a Connection

DFPs and DRPs fulfill the role of detecting a valid connection over USB Type-C. Figure 10-14 shows a DFP-to-UFP connection made with a Type-C cable. As shown in Figure 10-14, the detection concept is based on being able to detect terminations in the product that have been attached. A pull-up and pull-down termination model is used. A pull-up termination can be replaced by a current source.

- In the DFP-UFP connection, the DFP monitors both CC pins for a voltage lower than the unterminated voltage.

- An UFP advertises Rd on both its CC pins (CC1 and CC2).
- A powered cable advertises Ra on only one of the CC pins of the plug. Ra is used to inform the source to apply VCONN.
- An analog audio device advertises Ra on both CC pins of the plug, which identifies it as an analog audio device. VCONN is not applied on either CC pin in this case.

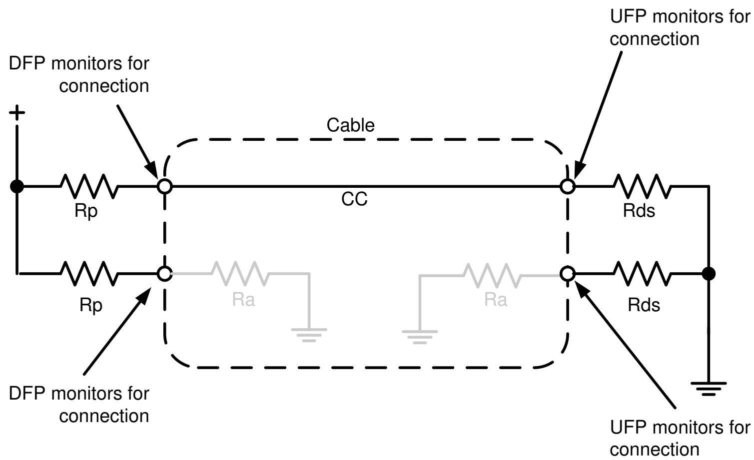


Figure 10-14. DFP-UFP Connection

For USB Type-C solutions, two pins (CC1, CC2) on the connector are used to establish and manage the source-to-sink connection. The general concept for setting up a valid connection between a source and a sink is based on being able to detect terminations residing in the product being attached. To aid in defining the functional behavior of CC, a pull-up (Rp) and pull-down (Rd 5.1 kΩ) termination model is used based on a pull-up resistor and pull-down resistor.

Initially, a source exposes independent Rp terminations on its CC1 and CC2 pins, and a sink exposes independent Rd terminations on its CC1 and CC2 pins. The source-to-sink combination of this circuit configuration represents a valid connection. To detect this, the source monitors CC1 and CC2 for a voltage lower than its unterminated voltage. The choice of Rp is a function of the pull-up termination voltage and the detection circuit of the source. This indicates that either a sink, a powered cable, or a sink connected by a powered cable has been attached. Prior to the application of VCONN, a powered cable exposes Ra (typically 1 kΩ) on its VCONN pin. Ra represents the load on VCONN plus any resistive elements to ground. In some cable plugs, this might be a pure resistance, and in others, it can simply be the load. The CC pin functional block is shown in Figure 10-15.

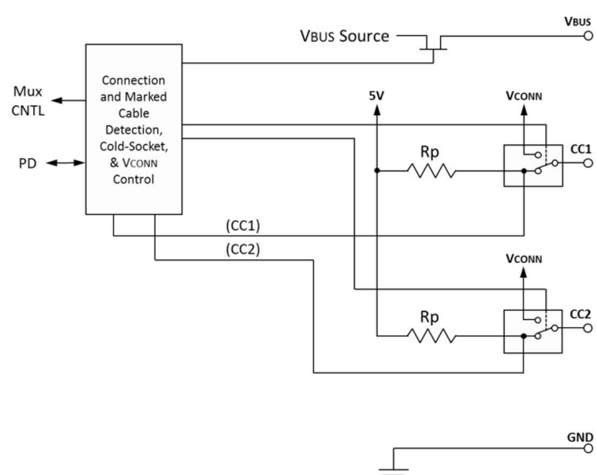


Figure 10-15. Source Functional Model for CC1 and CC2 (From Type-C Specification)

The source must be able to differentiate between the presence of Rd and Ra to know whether there is a sink attached and where to apply VCONN. The source is not required to source VCONN unless Ra is detected. Two special termination combinations on the CC pins as seen by a source are defined for directly attached accessory modes: Ra/Ra for audio adapter accessory mode and Rd/Rd for debug accessory mode.

10.3.17 USB Port Operating Modes

10.3.17.1 USB Type-C® Mode

The TPS2586x-Q1 port A is a Type-C controller that supports all Type-C functions in a downstream facing port. It is also used to manage current advertisement and protection to a connected UFP and active cable. When V_{SENSE} exceeds the undervoltage lockout threshold, the device samples the EN pin. A high level on this pin enables the device and normal operation begins. Having successfully completed its start-up sequence, the device now actively monitors its CC1 and CC2 pins for attachment to a UFP. When a UFP is detected on either the CC1 or CC2 pin the USB power switch turn-ons. If Ra is detected on the other CC pin (not connected to UFP), VCONN is applied to allow current to flow to the CC pin connected to Ra.

10.3.17.2 Dedicated Charging Port (DCP) Mode (TPS25868-Q1 Only)

A DCP only provides power and does not support data connection to an upstream port. As shown in the following sections, a DCP is identified by the electrical characteristics of the data lines. The TPS25860-Q1 only emulates one state, DCP-auto state. In the DCP-auto state, the device charge-detection state machine is activated to selectively implement charging schemes involved with the shorted, divider 3 and 1.2-V modes. The shorted DCP mode complies with BC1.2 and Chinese Telecommunications Industry Standard YD/T 1591-2009, whereas the divider 3 and 1.2-V modes are employed to charge devices that do not comply with the BC1.2 DCP standard.

10.3.17.2.1 DCP BC1.2 and YD/T 1591-2009

Both standards specify that the D+ and D– data lines must be connected together with a maximum series impedance of 200 Ω, as shown in Figure 10-16.

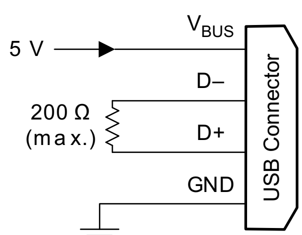


Figure 10-16. DCP Supporting BC1.2 and YD/T 1591-2009

10.3.17.2.2 DCP Divider-Charging Scheme

The device supports Divider 3, as shown in Figure 10-17. In the Divider 3 charging scheme the device applies 2.7 V and 2.7 V to D+ and D– data lines.

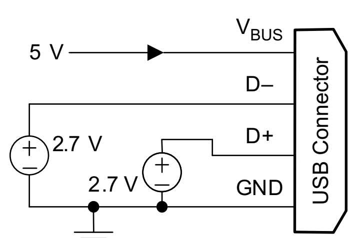


Figure 10-17. Divider 3 Mode

10.3.17.2.3 DCP 1.2-V Charging Scheme

The DCP 1.2-V charging scheme is used by some hand-held devices to enable fast charging at 2 A. The TPS25860-Q1 device supports this scheme in DCP-auto state before the device enters BC1.2 shorted mode. To simulate this charging scheme, the D+ and D– lines are shorted and pulled up to 1.2 V for a fixed duration. Then the device moves to DCP shorted mode as defined in the BC1.2 specification and as shown in Figure 10-18.

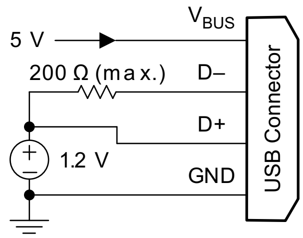


Figure 10-18. 1.2-V Mode

10.3.17.3 DCP Auto Mode (TPS25868-Q1)

The TPS25860-Q1 device integrates an auto-detect state machine that supports all the DCP charging schemes as shown in Figure 10-19. The auto-detect state machine starts in the Divider 3 scheme. If a BC1.2 or YD/T 1591-2009 compliant device is attached, the TPS25860-Q1 device responds by turning the power switch back on without output discharge and operating in 1.2-V mode briefly before entering BC1.2 DCP mode. Then, the auto-detect state machine stays in that mode until the device releases the data line, in which case, the auto-detect state machine goes back to the Divider 3 scheme. When a Divider 3-compliant device is attached, the TPS25860-Q1 device stays in the Divider 3 state.

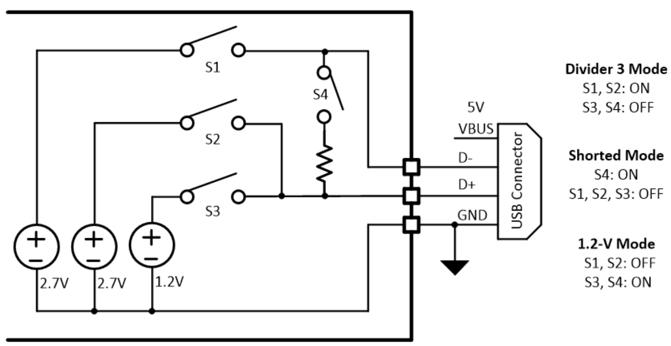


Figure 10-19. DCP Auto Mode

10.4 Device Functional Modes

10.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control for the TPS2586x-Q1. When V_{EN} is below 1.2 V (typ), the device is in shutdown mode. The TPS2586x also employs V_{IN} over voltage lock out protection and V_{SENSE} under voltage lock out protection. If V_{IN} voltage is above its respective OVLO level V_{OVLO}, or V_{SENSE} voltage is below its respective UVLO level V_{DCDC_UVLO}, the DC/DC converter will be turned off.

10.4.2 Active Mode

The TPS2586x-Q1 is in Active Mode when V_{EN} is above the precision enable threshold, V_{SENSE} is above its respective UVLO levels and a valid detection has been made on the CC lines. The simplest way to enable the TPS2586x-Q1 is to connect the EN pin to SENSE pin. This connection allows self startup when the input voltage is in the operating range (5.5 V to 26 V) and a UFP detection is made.

In Active Mode, the TPS2586x-Q1 buck regulator operates with Forced Pulse Width Modulation (FPWM), also referred to as Forced Continuous Conduction Mode (FCCM). This operation ensures the buck regulator switching frequency remains constant under all load conditions. FPWM operation provides low output voltage ripple, tight output voltage regulation, and constant switching frequency. Built-in spread-spectrum modulation aids in distributing spectral energy across a narrow band around the switching frequency programmed by the FREQ/SYNC pin. Under light load conditions the inductor current is allowed to go negative. A negative current limit of IL_NEG is imposed to prevent damage to the regulator's low side FET. During operation the TPS2586x-Q1 will synchronize to any valid clock signal on the FREQ/SYNC input.

11 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

11.1 Application Information

The TPS2586x-Q1 is a step down DC-to-DC regulator and USB charge port controller. The device is typically used in automotive systems to convert a DC voltage from the vehicle battery to 5-V DC with a maximum output current of 6 A in Type-C and Type-A dual ports applications. The TPS2586x-Q1 engages a high efficiency buck converter, letting the device operate at as high as 85°C ambient temperature with full load. The following design procedure can be used to select components for the TPS2586x-Q1.

11.2 Typical Applications

The TPS2586x-Q1 only requires a few external components to convert from a wide voltage range supply to a 5-V output to power USB devices. Figure 11-1 shows the TPS25868-Q1 typical application schematic for Dual Type-A and Type-C charging ports. Figure 11-2 shows the TPS25869-Q1 typical application schematic for Media HUB.

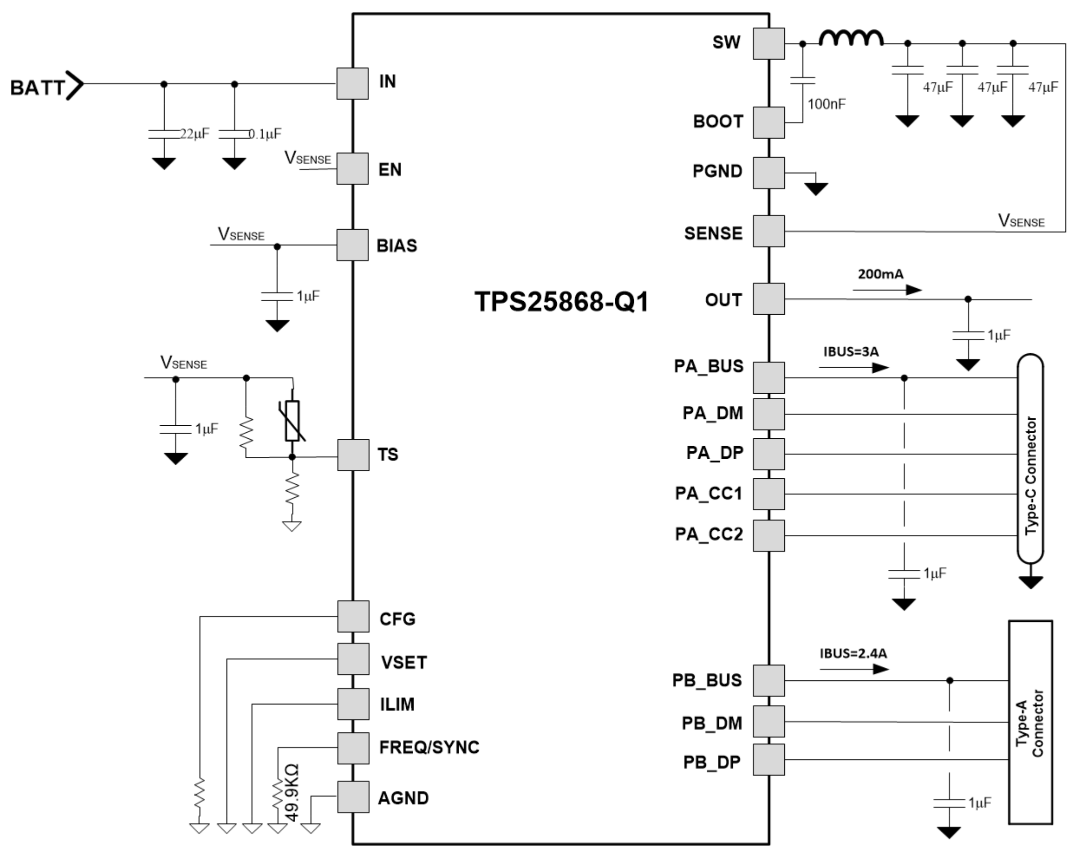


Figure 11-1. TPS25868-Q1 Typical Application Circuit for 400-kHz f_{SW}

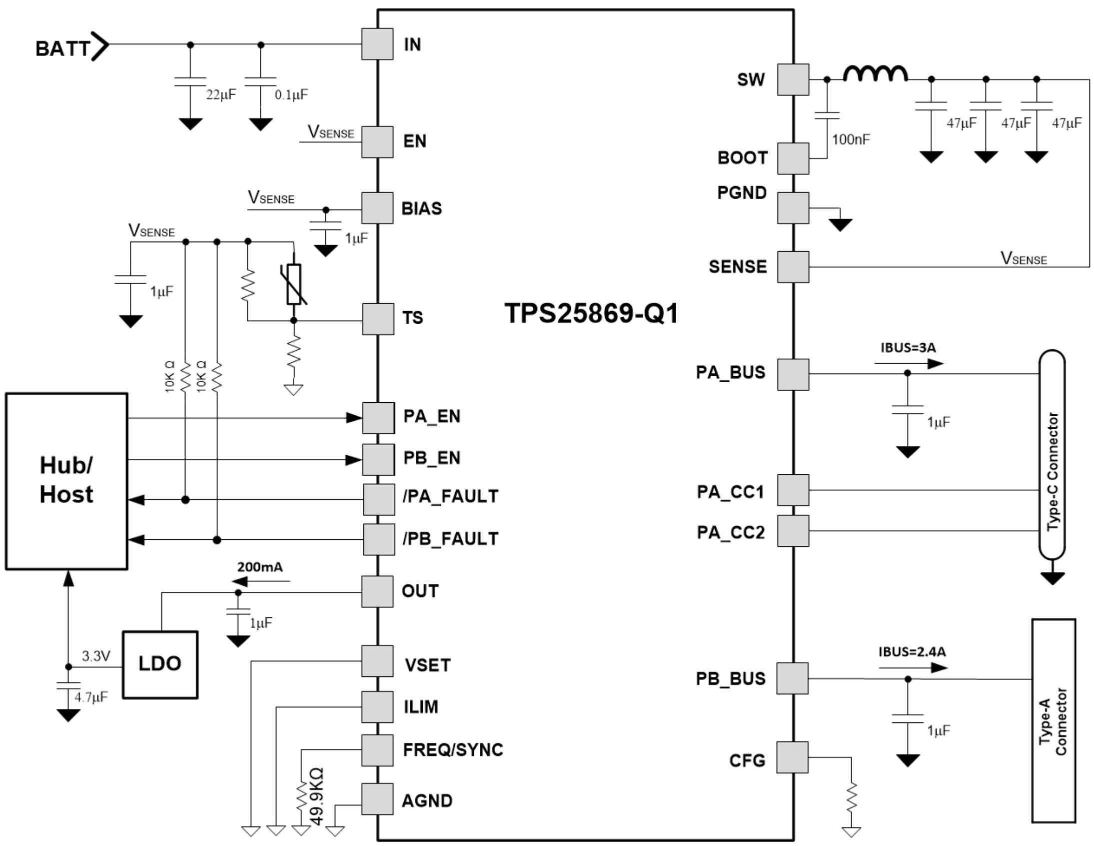


Figure 11-2. TPS25869-Q1 Typical Application Circuit for 400-kHz f_{SW}

As a quick start guide, Table 11-1 provides typical component values for some of the most common configurations. The values given in Table 11-1 are typical. Other values can be used to enhance certain performance criterion as required by the application. The integrated buck regulator of TPS2586x-Q1 is internally compensated and optimized for a reasonable selection of external inductance and capacitance. The external components have to fulfill the needs of the application, but also the stability criteria of the control loop of the device.

Table 11-1. L and C_{OUT} Typical Values

f_{SW}	V_{OUT} WITHOUT CABLE COMPENSATION	L	C_{HF} + C_{IN}	C_{BOOT}	RATED C_{OUT}
400 KHZ	5.17 V	3.3 µH	1 X 100 nF + 1 × 47 µF	1 × 100 nF	3 × 47 µF

1. The inductance value is calculated based on max V_{IN} = 18 V.
2. All the C_{OUT} values are after derating and use low ESR ceramic capacitors.
3. The C_{OUT} is the buck regulator output capacitors at the SENSE pin.

11.2.1 Design Requirements

The detailed design procedure is described based on a design example. For this design example, use the parameters listed in Table 11-2 as the input parameters.

Table 11-2. Design Example Parameters

Input Voltage, V_{IN}	13.5-V typical, range from 8 V to 18 V
Output Voltage, V_{SENSE}	5.17 V
Maximum Output Current	6 A
Switching Frequency f_{SW}	400 kHz

11.2.2 Detailed Design Procedure

11.2.2.1 Output Voltage Setting

The output voltage of TPS2586x-Q1 is programmed by the VSET pin, and if short VSET to GND, sets the output voltage at 5.17 V and enables the cable compensation function, and the output voltage increases linearly with increasing load current. Refer to Table 10-2 for more details on output voltage setting. Cable compensation can be used to increase the voltage on the SENSE pin linearly with increasing load current. Refer to *the list item in Ground Plane and Thermal Considerations* section for more details on cable compensation setting. If cable compensation is not desired, use a 0-Ω R_{IMON} resistor.

11.2.2.2 Switching Frequency

The recommended switching frequency of the TPS2586x-Q1 is in the range of 250–400 KHz for high efficiency. Choose R_{FREQ} = 49.9 kΩ for 400-KHz operation. To choose a different switching frequency, refer to Table 10-1.

The choice of switching frequency is a compromise between conversion efficiency and overall solution size. Lower switching frequency implies reduced switching losses and usually results in higher system efficiency. However, higher switching frequency allows the use of smaller inductors and output capacitors, and hence, a more compact design. In automotive USB charging applications, it tends to operate at either 400 kHz below the AM band, or 2.1 MHz above the AM band. In this example, 400 KHz is chosen.

11.2.2.3 Inductor Selection

The most critical parameters for the inductor are the inductance, saturation current, and the rated current. The inductance is based on the desired peak-to-peak ripple current, Δi_L. Since the ripple current increases with the input voltage, the maximum input voltage is always used to calculate the minimum inductance L_{MIN}. Use Equation 12 to calculate the minimum value of the output inductor. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current of the device. A reasonable value of K_{IND} should be 20% to 40%. Note that when selecting the ripple current for applications with much smaller maximum load than the maximum available from the device, the maximum device current must still be used. During an instantaneous short or overcurrent operation event, the RMS and peak inductor current can be high. The inductor current rating must be higher than the current limit of the device.

$$\Delta i_L = \frac{V_{OUT} \times \left(V_{IN\_MAX} - V_{OUT}\right)}{V_{IN\_MAX} \times L \times f_{SW}} \quad (11)$$

$$L_{MIN} = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \quad (12)$$

In general, it is preferable to choose lower inductance in switching power supplies because it usually corresponds to faster transient response, smaller DCR, and reduced size for more compact designs. Too low of an inductance can generate too large of an inductor current ripple such that overcurrent protection at the full load can be falsely triggered. It also generates more conduction loss and inductor core loss. Larger inductor current ripple also implies larger output voltage ripple with the same output capacitors. With peak current mode control, it is not recommended to have too small of an inductor current ripple. A larger peak current ripple improves the comparator signal to noise ratio.

For this design example, choose K_{IND} = 0.3, and find an inductance of approximately 3.58 µH. Select the next standard value of 3.3 µH.

11.2.2.4 Output Capacitor Selection

The output capacitor or capacitors, C_{OUT}, must be chosen with care since it directly affects the steady state output voltage ripple, loop stability, and the voltage overshoot/undershoot during load current transients.

The value of the output capacitor and its ESR, determine the output voltage ripple and load transient performance. The output capacitor is usually limited by the load transient requirements rather than the output voltage ripple if the system requires tight voltage regulation with presence of large current steps and fast slew rate. When a fast large load increase happens, output capacitors provide the required charge before the inductor current can slew up to the appropriate level. The control loop of the regulator usually needs four or more clock cycles to respond to the output voltage droop. The output capacitance must be large enough to supply the current difference for four clock cycles to maintain the output voltage within the specified range. Table 11-3 can be used to find output capacitors for a few common applications. In this example, good transient performance is desired giving 3 × 47-µF ceramic as the output capacitor.

Table 11-3. Selected Output Capacitor

FREQUENCY	C_{OUT}	SIZE/COST	TRANSIENT PERFORMANCE
400 KHz	3 × 47 µF ceramic	Small size	Good
400 KHz	2 × 47 µF ceramic	Small size	Minimum
400 KHz	4 × 22 µF + 1 × 260 µF, < 50-mΩ electrolytic	Larger size, low cost	Good
400 KHz	1 × 4.7 µF + 2 × 10 µF + 1 × 260 µF, < 50-mΩ electrolytic	Lowest cost	Minimum

where

- K_{IND} = Ripple ratio of the inductor ripple current (Δi_L / I_{OUT})
- I_{OL} = Low level output current during load transient
- I_{OH} = High level output current during load transient
- V_{US} = Target output voltage undershoot
- V_{OS} = Target output voltage overshoot

11.2.2.5 Input Capacitor Selection

The TPS2586x-Q1 device requires a high frequency input decoupling capacitor or capacitors, depending on the application. A high-quality ceramic capacitor type X5R or X7R with sufficient voltage rating is recommended. The ceramic input capacitors provide a low impedance source to the converter in addition to supplying the ripple current and isolating switching noise from other circuits. The typical recommended value for the high frequency decoupling capacitor is 10 µF of ceramic capacitance. This must be rated for at least the maximum input voltage that the application requires; preferably twice the maximum input voltage. This capacitance can be increased to help reduce input voltage ripple, maintain the input voltage during load transients, or both. In addition, a small case size 100-nF ceramic capacitor must be used at IN and PGND, immediately adjacent to the converter. This provides a high frequency bypass for the control circuits internal to the device. For this example a 10-µF, 50-V, X7R (or better) ceramic capacitor is chosen, and the 100-nF ceramic capacitor must also be rated at 50 V with an X7R or better dielectric.

Additionally, an electrolytic capacitor on the input in parallel with the ceramics can be required, especially if long leads from the automotive battery to the IN pin of the TPS2586x-Q1, cold or warm engine crank requirements, and so forth. The moderate ESR of this capacitor is used to provide damping to the voltage spike due to the lead inductance of the cable or the trace.

11.2.2.6 Bootstrap Capacitor Selection

The TPS2586x-Q1 design requires a bootstrap capacitor (C_{BOOT}). The recommended capacitor is 100 nF and rated 16 V or higher. The bootstrap capacitor is located between the SW pin and the BOOT pin. It stores energy that is used to supply the gate drivers for the power MOSFETs. The bootstrap capacitor must be a high-quality ceramic type with an X7R or X5R grade dielectric for temperature stability.

11.2.2.7 Undervoltage Lockout Set-Point

The system undervoltage lockout (UVLO) is adjusted using the external voltage divider network of R_{ENT} and R_{ENB}. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brownouts when the input voltage is falling. Equation 13 can be used to determine the V_{IN} UVLO level.

$$V_{IN\_RISING} = V_{ENH} \times \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \quad (13)$$

The EN rising threshold (V_{ENH}) for the TPS2586x-Q1 is set to be 1.3 V (typ.). Choose 10 kΩ for R_{ENB} to minimize input current from the supply. If the desired V_{IN} UVLO level is at 6.0 V, then the value of R_{ENT} can be calculated using Equation 14:

$$R_{ENT} = \left(\frac{V_{IN\_RISING}}{V_{ENH}} - 1 \right) \times R_{ENB} \tag{14}$$

Equation 14 yields a value of 36.1 kΩ. The resulting falling UVLO threshold equals 5.5 V and can be calculated by Equation 15, where EN hysteresis (V_{EN_HYS}) is 0.1 V (typ.).

$$V_{IN\_FALLING} = \left(V_{ENH} - V_{EN\_HYS} \right) \times \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \tag{15}$$

Note that it cannot connect EN to IN pin directly for self-start up. Because the voltage rating of EN pin is 11 V, tying it to VIN directly damages the device. The simplest way to enable the operation of the TPS2586x-Q1 is to connect the EN to V_{SENSE}. This allows the automatic start up when VIN is within the operation range.

11.2.2.8 Cable Compensation Set-Point

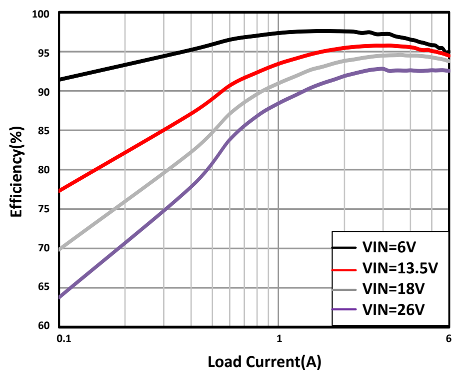
The TPS2586x-Q1 needs to short the VSET pin to ground to enable the cable compensation. With that setting, the buck regulator increases its output voltage linearly as the load current increases, and the voltage compensation at the currents of the USB ports greater than 2.4 A is 90 mV.

11.2.2.9 $\overline{\text{FAULT}}$ Resistor Selection

The $\overline{\text{FAULT}}$ pins are open-drain output flags. They can be connected to the TPS2586x-Q1 VSENSE with 100-kΩ resistors, or connected to another suitable I/O voltage supply if actively monitored by a USB HUB or MCU. They can be left floating if unused.

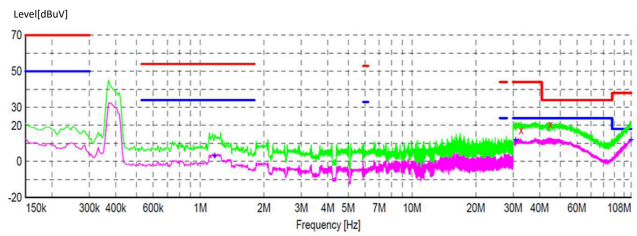
11.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 13.5 V, f_{SW} = 400 kHz, L = 3.3 µH, C_{SENSE} = 141 µF, C_{PA_BUS} = 1 µF, C_{PB_BUS} = 1 µF, ILIM = GND, T_A = 25 °C.



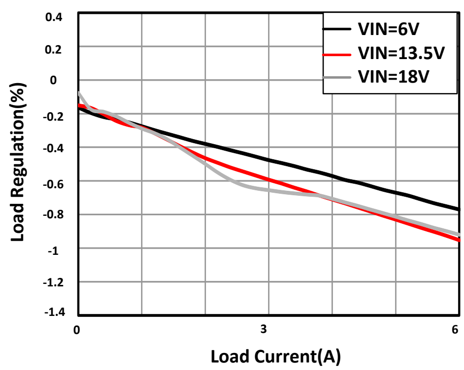
VSET = GND f_{SW} = 400 kHz L = 3.3 uH

Figure 11-3. Buck Only Efficiency



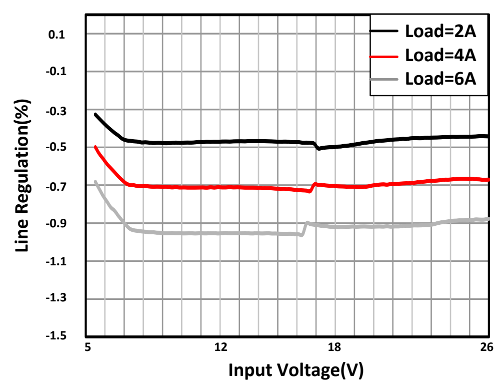
Load = 6 A f_{SW} = 400 kHz L = 3.3 uH

Figure 11-4. 400-khz EMI Results (Without CM Filter)



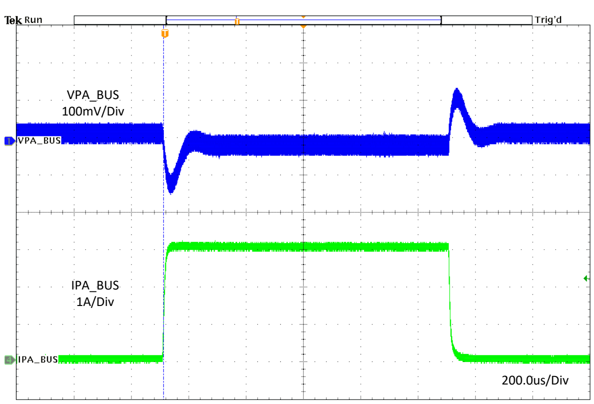
VSET = GND f_{SW} = 400 kHz

Figure 11-5. Load Regulation



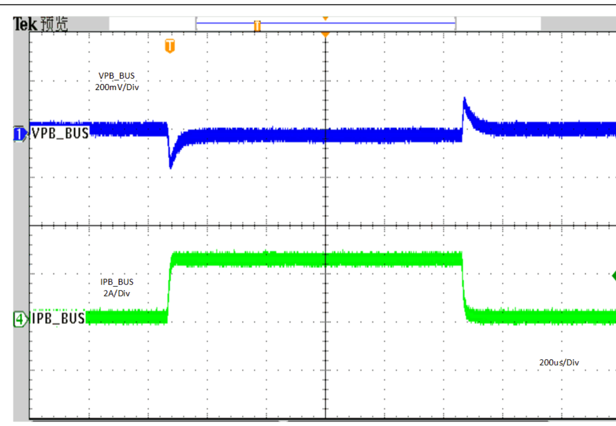
VSET = GND f_{SW} = 400 kHz

Figure 11-6. Line Regulation



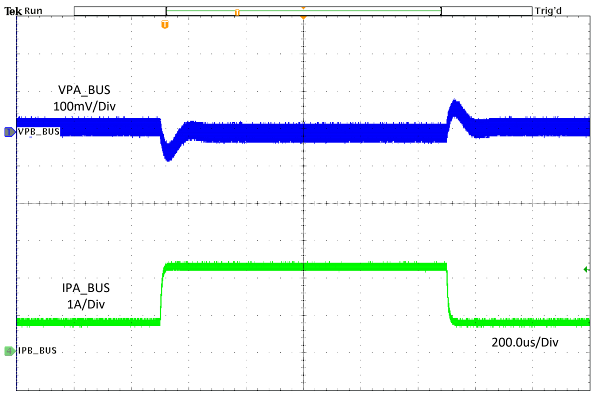
VSET = V_{SENSE} I_{PA_BUS} = 0 A to 3 A I_{PB_BUS} = 2.4 A f_{SW} = 400 kHZ

Figure 11-7. Load Transient Without Cable Compensation



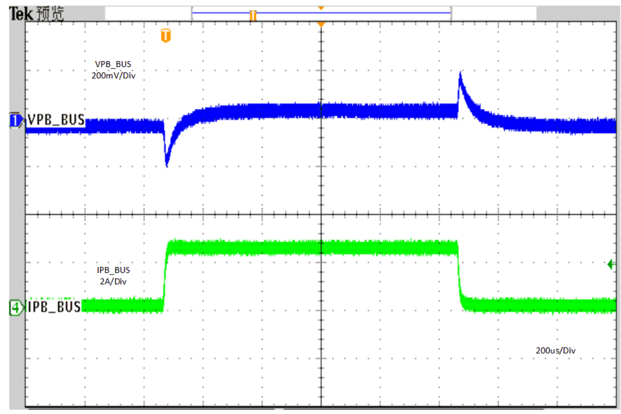
VSET = V_{SENSE} I_{PB_BUS} = 0 A to 2.4 A I_{PA_BUS} = 3 A f_{SW} = 400 kHz

Figure 11-8. Load Transient Without Cable Compensation



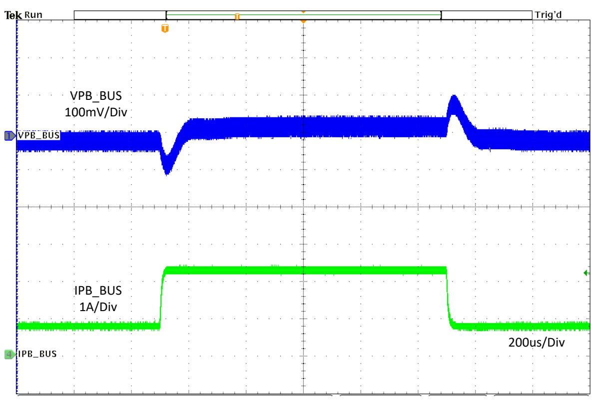
VSET = V_{SENSE} I_{PA_BUS} = 0.75 A to 2.25 A I_{PB_BUS} = 0 A f_{SW} = 400 kHZ

Figure 11-9. Load Transient Without Cable Compensation



VSET = GND I_{PB_BUS} = 0 A to 2.4 A I_{PA_BUS} = 3 A f_{SW} = 400 kHZ

Figure 11-10. Load Transient With Cable Compensation



VSET = GND I_{PB_BUS} = 0.75 A to 2.25 A I_{PA_BUS} = 0 A f_{SW} = 400 kHZ

Figure 11-11. Load Transient With Cable Compensation

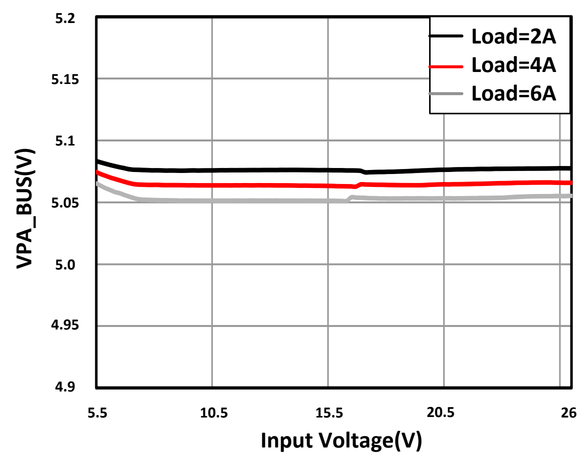
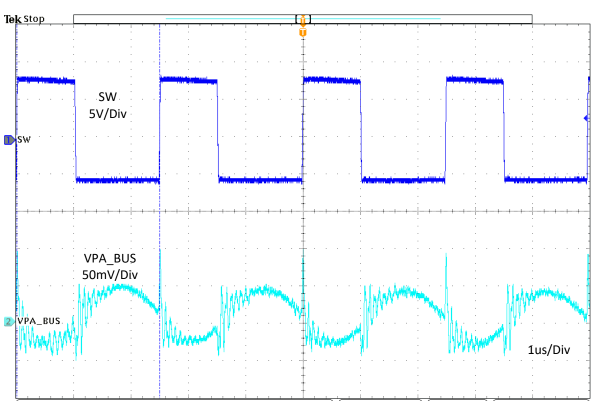
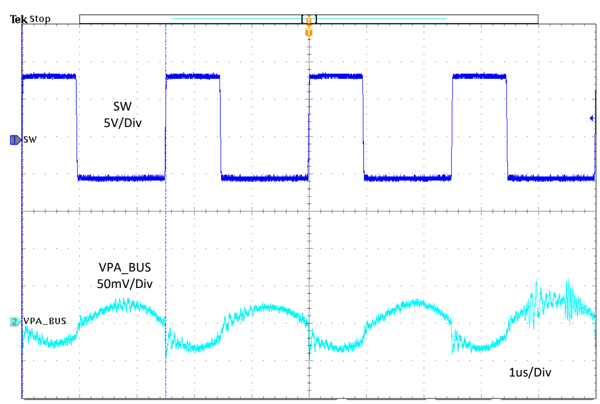


Figure 11-12. Dropout Characteristic



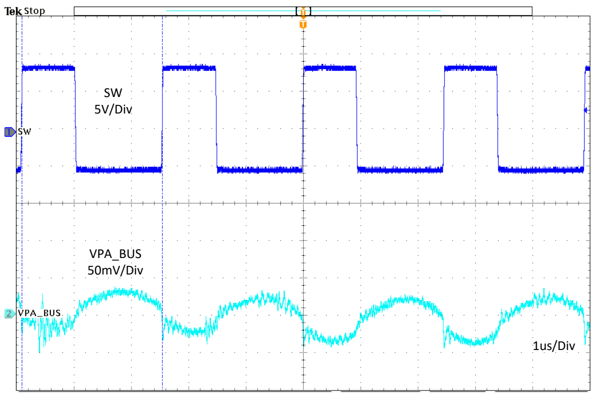
VSET = GND I_{PA_BUS} = 3 A I_{PB_BUS} = 2.4 A f_{SW} = 400 kHZ

Figure 11-13. 6-A Output Ripple



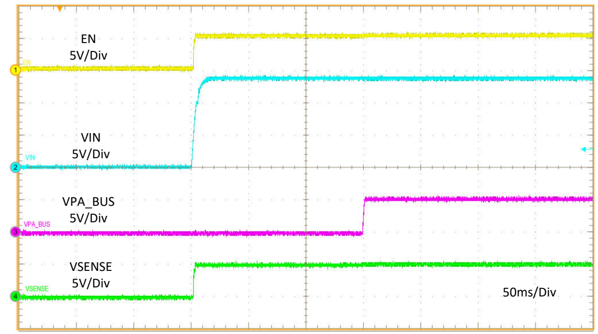
VSET = GND I_{PA_BUS} = 0.1 A I_{PB_BUS} = 0 A f_{SW} = 400 kHZ

Figure 11-14. 100-mA Output Ripple



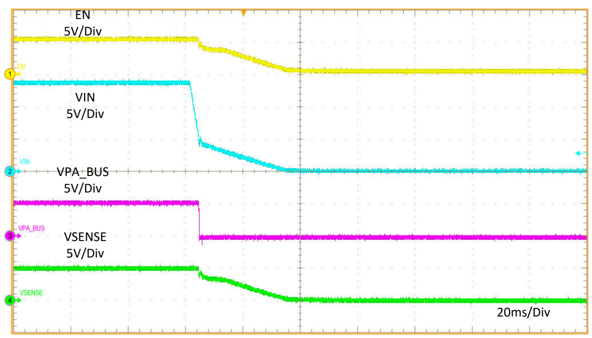
VSET = GND I_{PA_BUS} = 0 A I_{PB_BUS} = 0 A f_{SW} = 400 kHZ

Figure 11-15. No Load Output Ripple



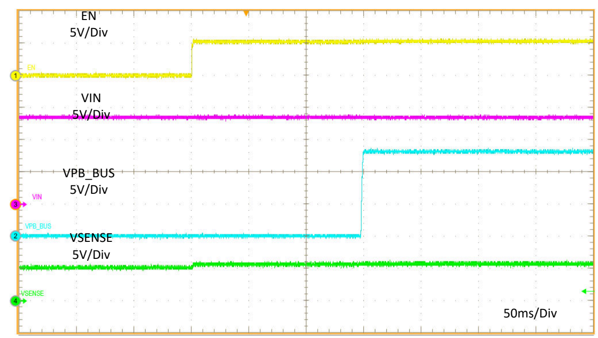
VIN = 0 V to 13.5 V PA_CC1 = R_d I_{PA_BUS} = 3 A

Figure 11-16. Startup Relate to VIN



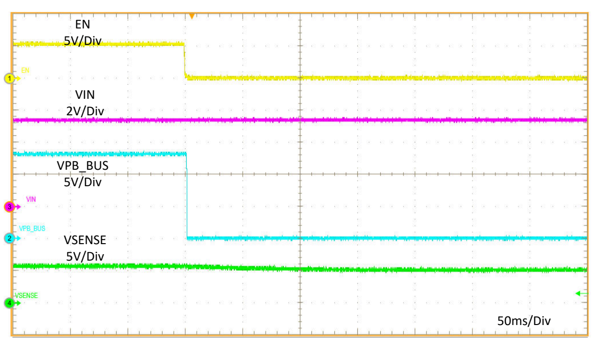
VIN = 13.5 V to 0 V PA_CC1 = R_d I_{PA_BUS} = 3 A

Figure 11-17. Shutdown Relate to VIN



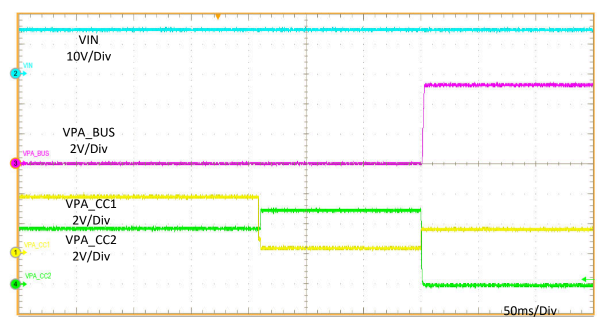
EN = 0 V to 5 V I_{PB_BUS} = 2.4 A

Figure 11-18. Startup Relate to EN



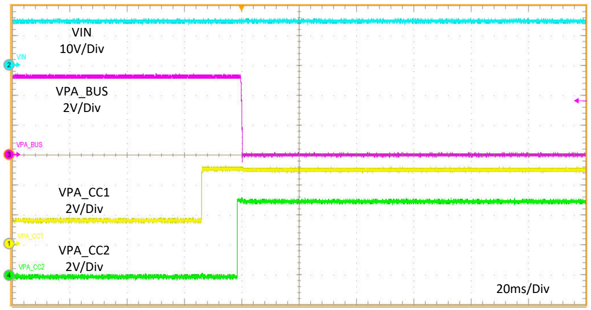
EN = 5 V to 0 V I_{PB_BUS} = 2.4 A

Figure 11-19. Shutdown Relate to EN



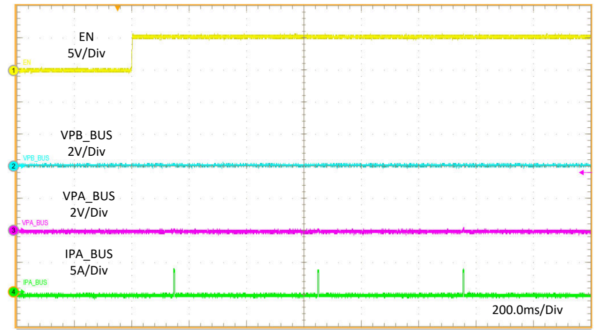
PA_CC1 = Open to R_d PA_CC2 = Open I_{PA_BUS} = 3 A

Figure 11-20. Rd Assert



PA_CC1 = R_d to Open PA_CC2 = Open I_{PA_BUS} = 3 A

Figure 11-21. Rd Desert



EN to High PA_BUS = GND PB_BUS = GND

Figure 11-22. Enable Into Short

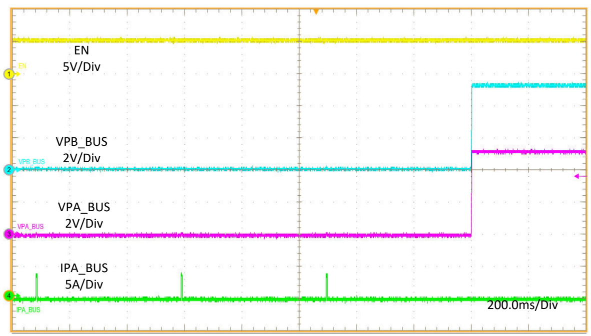
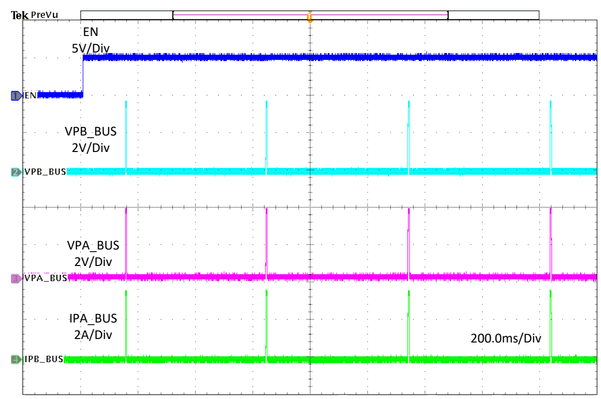


Figure 11-23. Short Circuit Recovery



EN to High PA_BUS = 1 Ω PB_BUS = 1 Ω

Figure 11-24. Enable Into 1-Ω Load

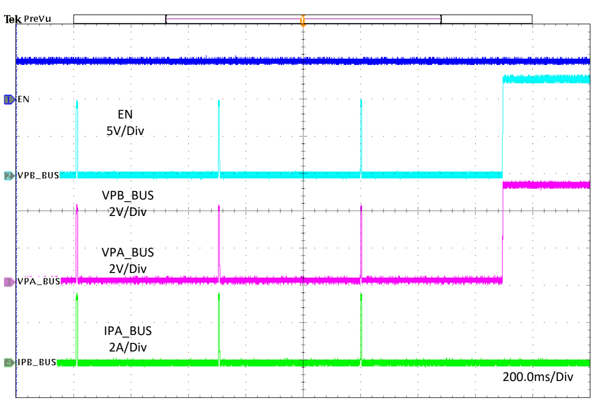


Figure 11-25. 1-Ω Load Recovery

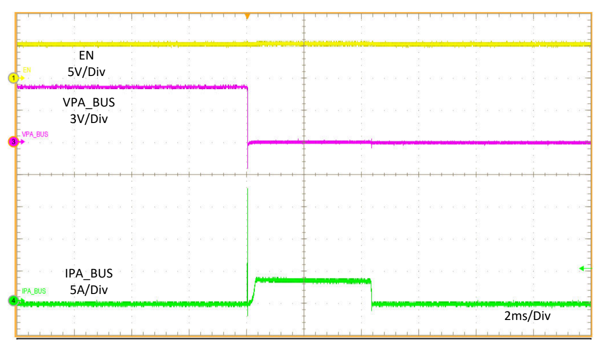
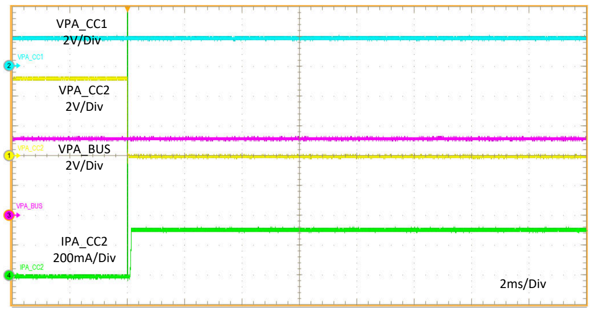
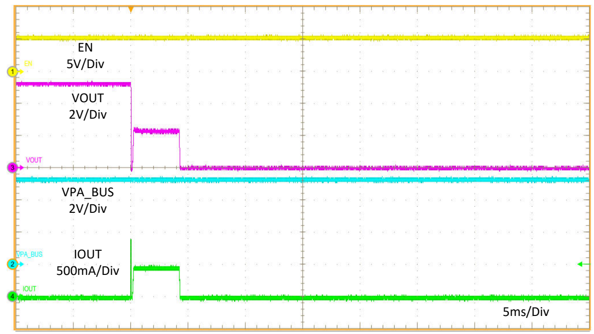


Figure 11-26. VBUS Hot Short to GND



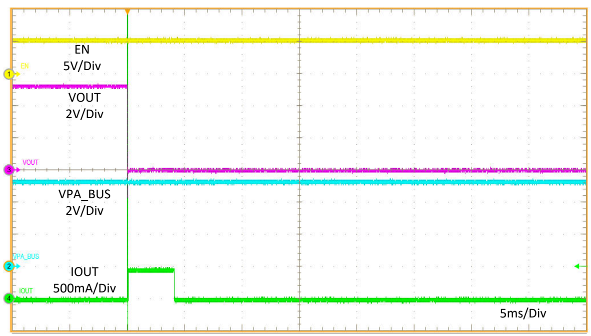
PA_CC1 = R_d PA_CC2 = R_a

Figure 11-27. PA_CC2 Hot Short to GND



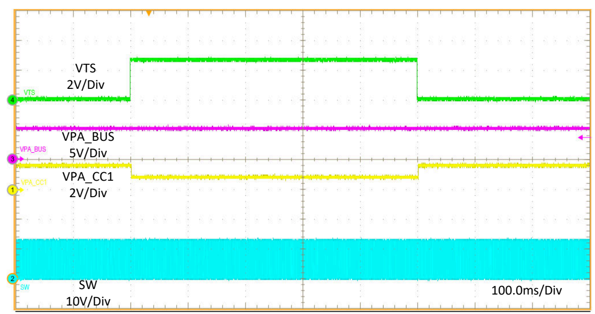
PA_CC1 = R_d OUT = 5.1 Ω PA/B_BUS NO LOAD

Figure 11-28. OUT short to 5.1-Ω Load



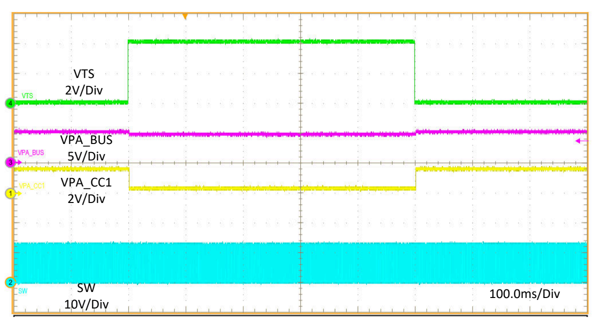
PA_CC1 = R_d OUT = GND PA/B_BUS NO LOAD

Figure 11-29. OUT Hot Short to GND



V_{TS} = 0 V to 2.6 V PA_CC1 = R_d PA_CC2 = OPEN

Figure 11-30. Thermal Sensing - NTC Temperature WARM Behavior



V_{TS} = 0 V to 4 V PA_CC1 = R_d PA_CC2 = OPEN

Figure 11-31. Thermal Sensing - NTC Temperature HOT Behavior

12 Power Supply Recommendations

The input supply must be able to withstand the maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the TPS2586x-Q1 supply voltage that it causes a false UVLO fault triggering and system reset. If the TPS2586x-Q1 is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. An additional bulk capacitance can be required in addition to the ceramic input capacitors. The amount of bulk capacitance is not critical, but a 100-μF electrolytic capacitor is a typical choice.

The input voltage must not be allowed to fall below the output voltage. In this scenario, such as a shorted input test, the output capacitors discharge through the internal parasitic diode found between the VIN and SW pins of the device. During this condition, the current can become uncontrolled, possibly causing damage to the device. If this scenario is considered likely, then a Schottky diode between the input supply and the output must be used.

13 Layout

13.1 Layout Guidelines

The PCB layout of any bulk converter is critical to the optimal performance of the design. Bad PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, the EMI performance of the converter is dependent on the PCB layout to a great extent. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. The input bypass capacitor, C_{IN}, must be placed as close as possible to the VIN and PGND pins. The high frequency ceramic bypass capacitors at the input side provide a primary path for the high di/dt components of the pulsing current. Use a wide VIN plane on a lower layer to connect both of the VIN pairs together to the input supply. Grounding for both the input and output capacitors must consist of localized top-side planes that connect to the PGND pin and PAD.
2. Use ground plane in one of the middle layers as noise shielding and heat dissipation path.
3. Have a single point ground connection to the plane. The ground connections for the feedback and enable components must be routed to the ground plane. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior.
4. The SW pin connecting to the inductor must be as short as possible, and just wide enough to carry the load current without excessive heating. Short, thick traces or copper pours (shapes) must be used for a high current conduction path to minimize parasitic resistance. The output capacitors must be placed close to the V_{SENSE} end of the inductor and closely grounded to PGND pin and exposed PAD.
5. Make V_{IN}, V_{SENSE}, and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
6. Provide enough PCB area for proper heat sinking. Enough copper area must be used to ensure a low $R_{\theta JA}$, commensurate with the maximum load current and ambient temperature. Make the top and bottom PCB layers with two-ounce copper; and no less than one ounce. If the PCB design uses multiple copper layers (recommended), thermal vias can also be connected to the inner layer heat-spreading ground planes. Note that the package of this device dissipates heat through all pins. Wide traces must be used for all pins except where noise considerations dictate minimization of area.
7. Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has multiple copper layers, these thermal vias can also be connected to inner layer heat-spreading ground planes. Ensure enough copper area is used for heat-sinking to keep the junction temperature below 150°C.
8. R_{ILIM} and R_{IMON} resistors must be placed as close as possible to the ILIM and IMON pins and connected to AGND. If needed, these components can be placed on the bottom side of the PCB with signals routed through small vias.
9. Keep the CC lines close to the same length. Do not create stubs or test points on the CC lines.

13.2 Layout Example

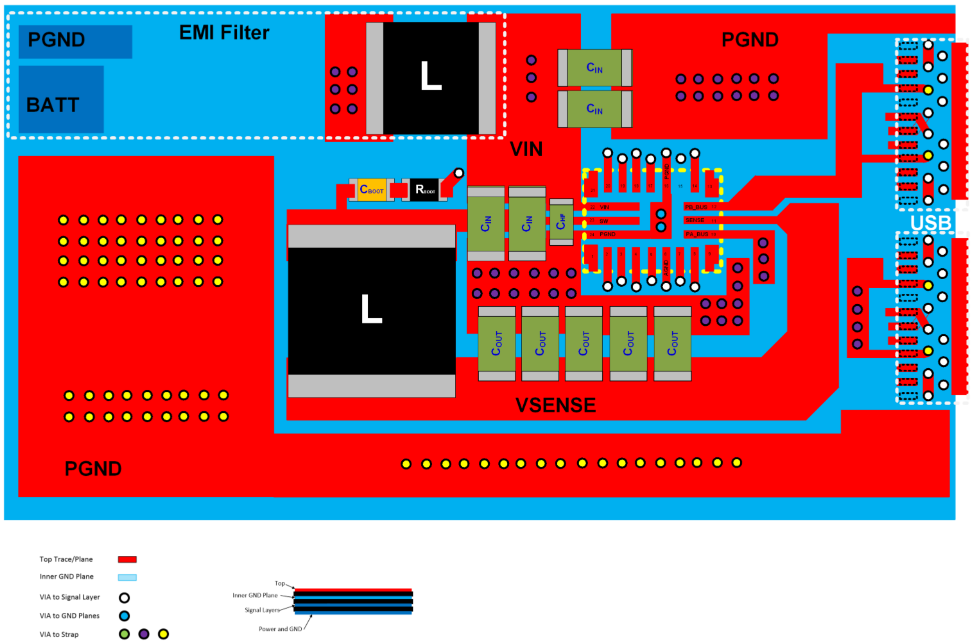


Figure 13-1. Layout Example

13.3 Ground Plane and Thermal Considerations

It is recommended to use one of the middle layers as a solid ground plane. Ground plane provides shielding for sensitive circuits and traces. It also provides a quiet reference potential for the control circuitry. The AGND and PGND pins must be connected to the ground plane using vias right next to the bypass capacitors. The PGND pin is connected to the source of the internal low-side MOSFET switch, and also connected directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and can bounce due to load variations. The PGND trace, as well as VIN and SW traces, must be constrained to one side of the ground plane. The other side of the ground plane contains much less noise and should be used for sensitive routes.

It is recommended to provide adequate device heat sinking by using the PAD of the IC as the primary thermal path. Use a minimum 4 x 2 array of 12-mil thermal vias to connect the PAD to the system ground plane heat sink. The vias must be evenly distributed under the PAD. Use as much copper as possible, for system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top of 2 oz / 1 oz / 1 oz / 2 oz. Four layer boards with enough copper thickness provide low current conduction impedance, proper shielding, and lower thermal resistance.

The thermal characteristics of the TPS2586x-Q1 are specified using the parameter θ_{JA}, which characterizes the junction temperature of silicon to the ambient temperature in a specific system. Although the value of θ_{JA} is dependent on many variables, it still can be used to approximate the operating junction temperature of the device. To obtain an estimate of the device junction temperature, one can use the following relationship:

$$T_J = P_D \times \theta_{JA} + T_A \quad (16)$$

where

- T_J = Junction temperature in °C
- P_D = V_{IN} × I_{IN} × (1 – Efficiency) – 1.1 × $I_{OUT}{}^2$ × DCR in Watt
- DCR = Inductor DC parasitic resistance in Ω
- θ_{JA} = Junction-to-ambient thermal resistance of the device in °C/W
- T_A = Ambient temperature in °C

The maximum operating junction temperature of the TPS2586x-Q1 is 150°C. θ_{JA} is highly related to PCB size and layout, as well as environmental factors such as heat sinking and air flow.

14 Device and Documentation Support

14.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

14.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

14.3 Trademarks

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TI E2E™ is a trademark of Texas Instruments.
USB Type-C® is a registered trademark of USB Implementers Forum.
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14.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

14.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS25868QRPQRQ1	Active	Production	VQFN-HR (RPQ) | 25	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-45 to 125	T25868
TPS25868QRPQRQ1.A	Active	Production	VQFN-HR (RPQ) | 25	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-45 to 125	T25868
TPS25869QRPQRQ1	Active	Production	VQFN-HR (RPQ) | 25	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-45 to 125	T25869
TPS25869QRPQRQ1.A	Active	Production	VQFN-HR (RPQ) | 25	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-45 to 125	T25869

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

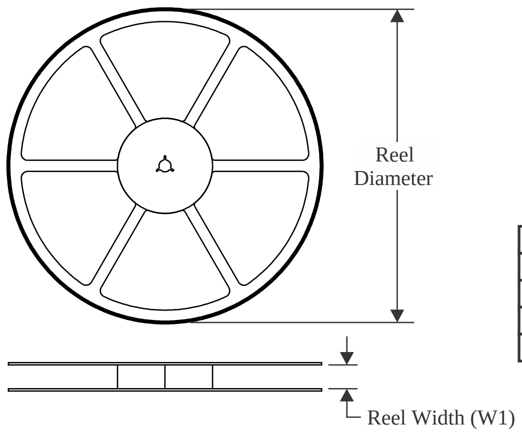
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

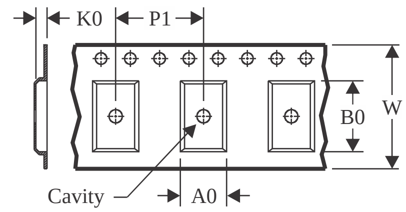
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

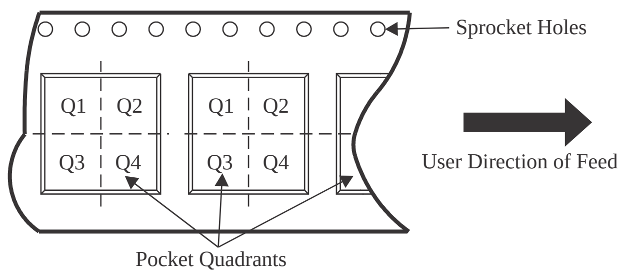


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

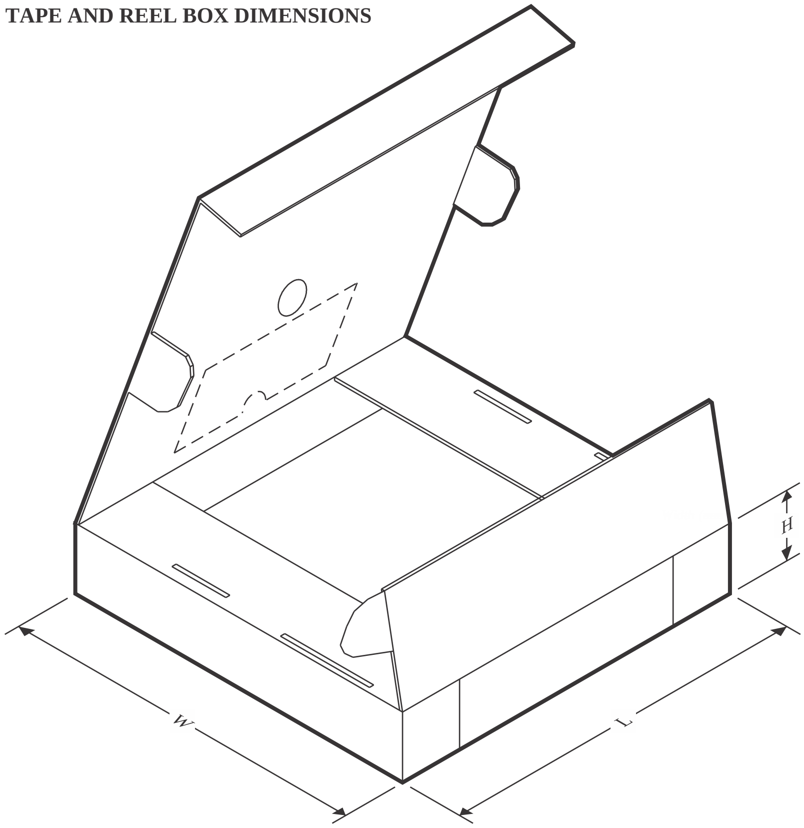
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS25868QRPQRQ1	VQFN-HR	RPQ	25	3000	330.0	12.4	3.8	4.8	1.18	8.0	12.0	Q1
TPS25868QRPQRQ1	VQFN-HR	RPQ	25	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
TPS25869QRPQRQ1	VQFN-HR	RPQ	25	3000	330.0	12.4	3.8	4.8	1.18	8.0	12.0	Q1
TPS25869QRPQRQ1	VQFN-HR	RPQ	25	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



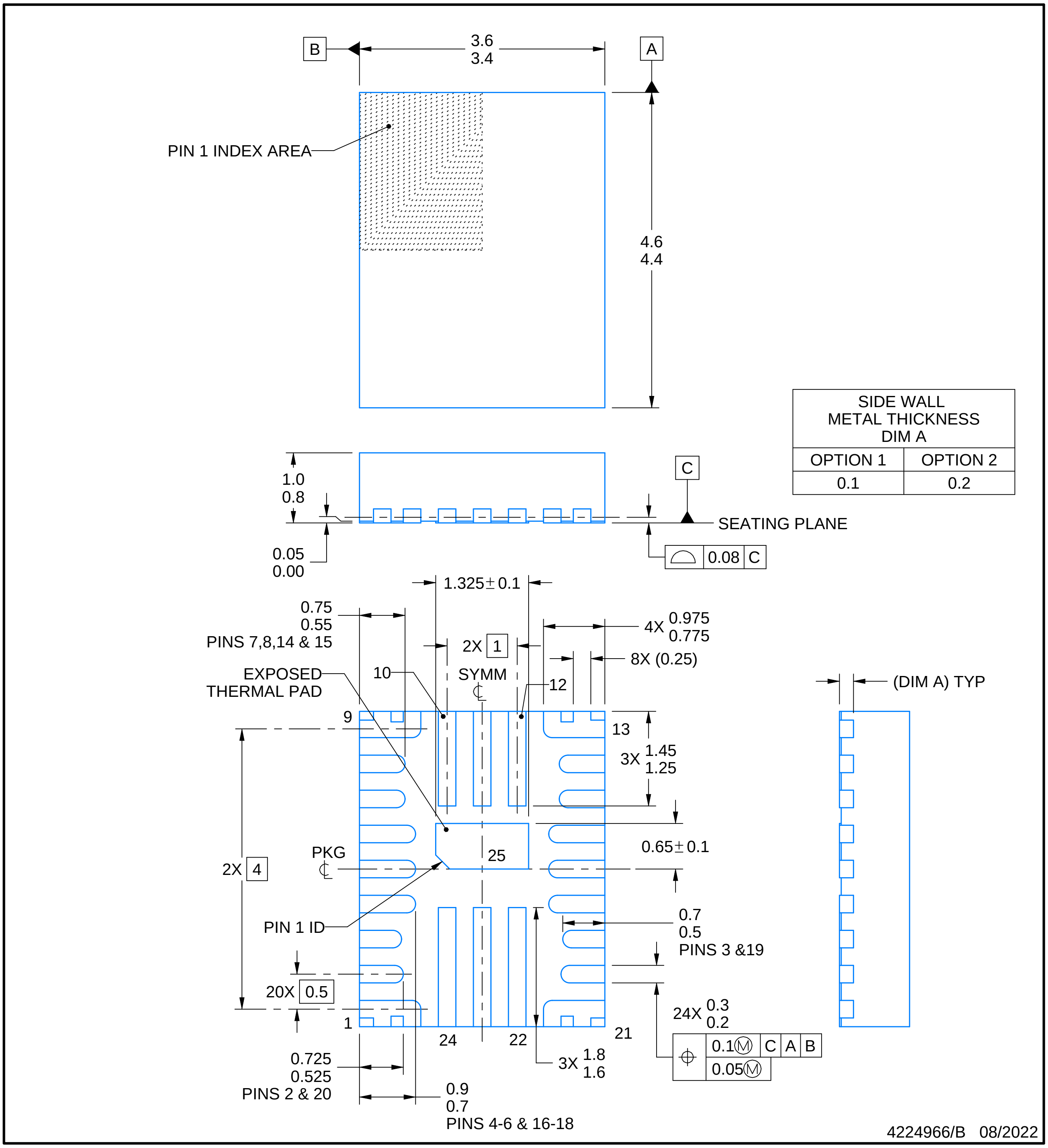
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS25868QRPQRQ1	VQFN-HR	RPQ	25	3000	367.0	367.0	38.0
TPS25868QRPQRQ1	VQFN-HR	RPQ	25	3000	367.0	367.0	35.0
TPS25869QRPQRQ1	VQFN-HR	RPQ	25	3000	367.0	367.0	38.0
TPS25869QRPQRQ1	VQFN-HR	RPQ	25	3000	367.0	367.0	35.0

PACKAGE OUTLINE

VQFN - 1 mm max height

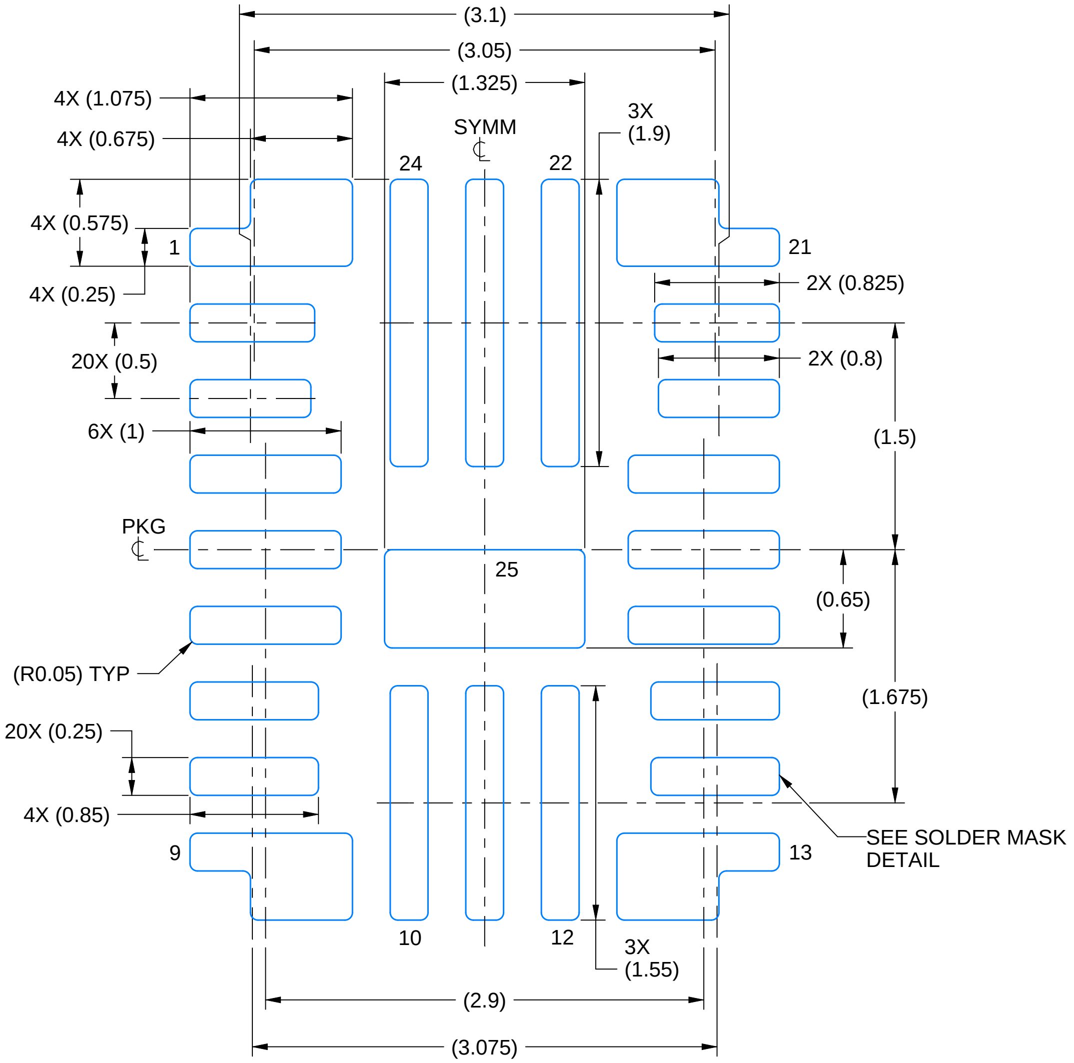
PLASTIC QUAD FLATPACK - NO LEAD



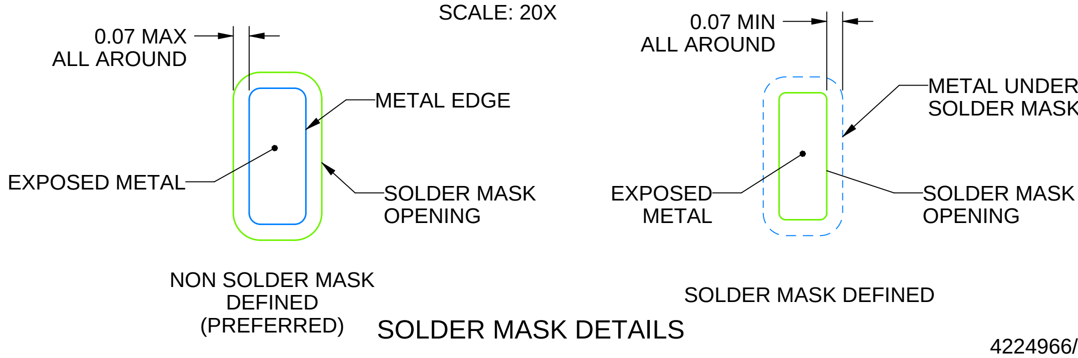
SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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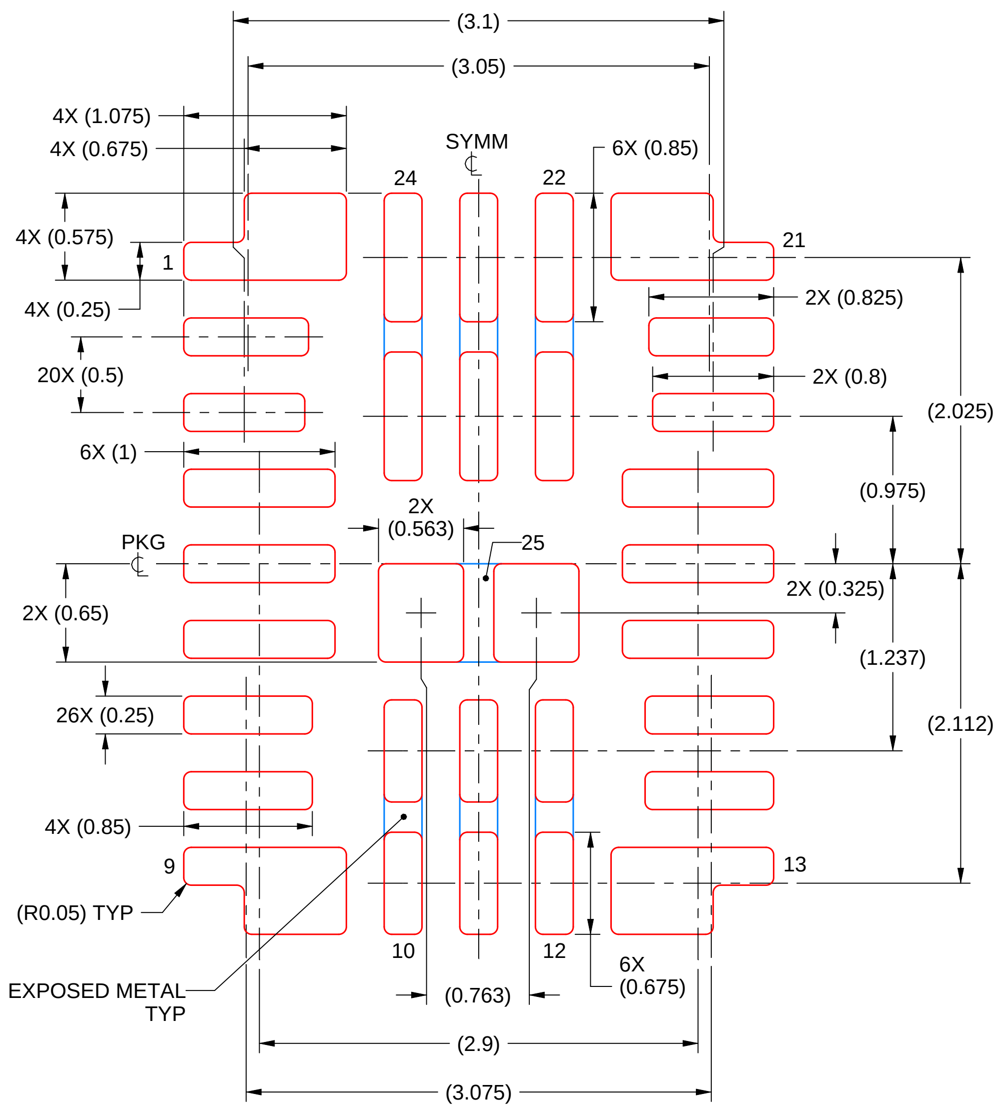
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 25
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.