TPS25948xx 3.5V–23V, 12.2mΩ, 8A eFuse With Bi-directional Power Delivery

1 Features

- Wide operating input voltage range: 3.5V to 23V
  - 28V absolute maximum
  - Can be powered from either IN or OUT
- Integrated back-to-back FETs with low ON-resistance: R_{ON} = 12.2mΩ (typ)
- Ideal diode operation with true reverse current blocking (RCB)
  - External pin control (RCBCTRL) to disable RCB and allow bi-directional power delivery in steady-state to support USB OTG or DRP operation
- Fast overvoltage protection
  - Adjustable overvoltage lockout (OVLO) with 1µs (typ) response time
- Overcurrent protection with load current monitor output (ILM)
  - Active current limit response
  - Adjustable threshold (I_{LIM}) 1A–9A
    - ±10% accuracy (max) for I_{LIM} > 3A
  - Adjustable transient blanking timer (ITIMER) to allow peak currents > I_{LIM}
  - Output load current monitor accuracy: ±6% (typ) (I_{OUT} ≥ 3A)
- Fast-trip response for short-circuit protection
  - < 1µs (typ) response time
  - Adjustable and fixed thresholds
- Active high enable input with adjustable undervoltage lockout threshold (UVLO)
- Adjustable output slew rate control (dVdt)
- Overtemperature protection
- Digital outputs: Supply Good (SPLYGD/$\overline{\text{SPLYGD}}$) and Fault Indication ($\overline{\text{FLT}}$)
- UL 2367 recognition (planned)
- IEC 62368-1 CB certification (planned)
- IEC 61000-4-5: 28V on IN
- Small footprint: PowerWCSP 2.4mm × 1.7mm, 0.5mm pitch

2 Applications

- Adapter and charger input protection
- USB PD protection: smartphone, tablet, PC, notebook, monitor, dock
- Server motherboard, add-on cards
- Enterprise storage: HBA, SAN, and eSSD
- Power MUXing and ORing

3 Description

The TPS25948xx family of eFuses is a highly integrated, circuit-protection and power-management solution in a small package. The devices provide multiple protection modes that use few external components and are a robust defense against overloads, short-circuits, voltage surges and excessive inrush current. With integrated back-to-back FETs, reverse current flow from output to input is blocked at all times, making the devices well suited for power MUX and ORing applications, as well as systems that need load side energy hold up storage if input power supply fails. The devices use a linear ORing based scheme to ensure almost zero DC reverse current and emulate ideal diode behavior with minimum forward voltage drop and power dissipation. The devices also provide an external pin control option to disable the reverse current blocking and allow bi-directional power delivery in steady-state.

Output slew rate and inrush current can be adjusted using a single external capacitor. Loads are protected from input overvoltage conditions by cutting off the output if input exceeds an adjustable overvoltage threshold. The devices respond to output overload by actively limiting the current. The output current limit threshold as well as the transient overcurrent blanking timer are user adjustable. The current limit control pin also functions as an analog load current monitor.

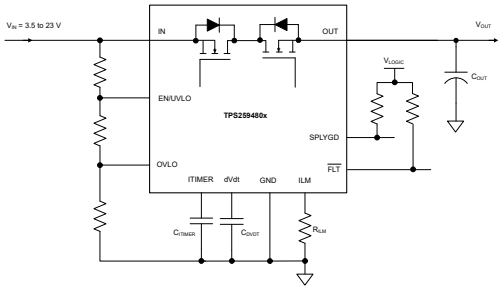
The devices are available in a 2.4mm × 1.7mm, 12-ball power wafer chip scale package (PowerWCSP) for improved thermal performance and reduced system footprint.

The devices are characterized for operation over a junction temperature range of –40°C to +125°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS25948xxYWP	YWP (PWCSP, 12)	2.43mm × 1.71mm

(1) For all available variants, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Device Comparison Table

PART NUMBER	STEADY-STATE FAST-TRIP THRESHOLD	SPLYGD POLARITY	$\overline{FLT}$ OR RCBCTRL	RESPONSE TO FAULT
TPS259480AYWP	Adjustable (2 × I_{LIM})	Active High	$\overline{FLT}$	Auto-Retry
TPS259480LYWP				Latch-Off
TPS259482AYWP			RCBCTRL	Auto-Retry
TPS259482LYWP				Latch-Off
TPS259481AYWP	Fixed	Active Low		Auto-Retry
TPS259481LYWP				Latch-Off
TPS259483AYWP		Active High		Auto-Retry

5 Pin Configuration and Functions

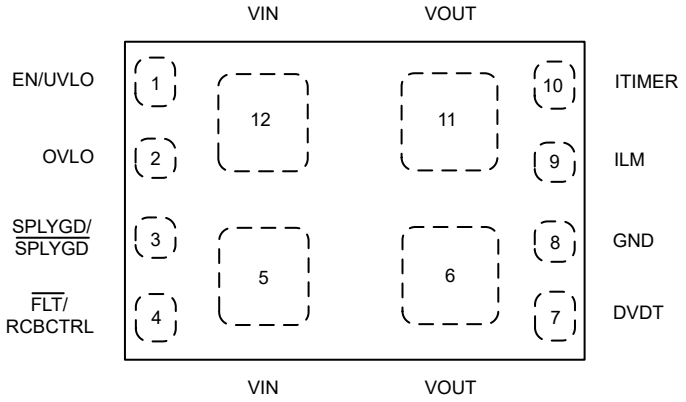


Figure 5-1. YWP Package, 12-Ball PWCSP (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN/UVLO	1	Analog input	Active high enable for the device. A resistor divider on this pin from input supply to GND can be used to adjust the undervoltage lockout threshold. *Do not leave floating.* Refer to Section 7.3.1 for details.
OVLO	2	Analog input	A resistor divider on this pin from supply to GND can be used to adjust the overvoltage lockout threshold. This pin can also be used as an Active low enable for the device. *Do not leave floating.* Refer to Section 7.3.2 for details.
SPLYGD	3	Digital output	*TPS259480x/2x/3x:* Active high Supply Good indication. This is an open drain signal which is asserted high when the input supply is valid and channel has completed inrush sequence. This can be used to enable/disable the auxiliary supply eFuse to facilitate smooth switchover in a priority power MUXing configuration. Refer to Section 7.3.8 for more details.
$\overline{\text{SPLYGD}}$		Digital output	*TPS259481x:* Active low Supply Good indication. This is an open drain signal which is asserted Low when the input supply is valid and channel has completed inrush sequence. This can be used to enable/disable the auxiliary supply eFuse to facilitate smooth switchover in a priority power MUXing configuration. Refer to Section 7.3.8 for more details.
$\overline{\text{FLT}}$	4	Digital output	*TPS259480x:* Active low fault event indicator. This is an open drain signal which is pulled low when a fault is detected. Refer to Section 7.3.7 for more details.
RCBCTRL		Digital input	*TPS259481x/2x/3x:* Active high reverse current blocking enable input. Leave the pin floating or pull it high to enable reverse current blocking at all times. Pull the pin low to disable reverse current blocking in steady-state to enable bi-directional current flow.
IN	5, 12	Power	Power input.
OUT	6, 11	Power	Power output.
DVDT	7	Analog output	A capacitor from this pin to GND sets the output turn on slew rate. Leave this pin floating for the fastest turn on slew rate. Refer to Section 7.3.3.1 for details.
GND	8	Ground	This is the ground reference for all internal circuits and must be connected to system GND.
ILM	9	Analog output	This is a dual function pin used to limit and monitor the output current. An external resistor from this pin to GND sets the output current limit threshold during start-up as well as steady state. The pin voltage can also be used as analog output load current monitor signal. *Do not leave floating.* Refer to Section 7.3.3.2 for more details.
ITIMER	10	Analog output	A capacitor from this pin to GND sets the overcurrent blanking interval during which the output current can temporarily exceed set current limit (but lower than fast-trip threshold) before the device overcurrent response takes action. Leave this pin open for fastest response to overcurrent events. Refer to Section 7.3.3.2 for more details.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter		Pin	MIN	MAX	UNIT
$V_{IN,MAX}$	Maximum input voltage range, –40°C ≤ T_J ≤ 125°C	IN	–0.3	28	V
$V_{OUT,MAX}$	Maximum output voltage range, –40°C ≤ T_J ≤ 125°C	OUT	–0.3	min (28, V_{IN} + 21)	
$V_{OUT,MAX}$	Maximum output voltage range, -10°C ≤ T_J ≤ 125 °C	OUT	–0.3	min (28, V_{IN} + 22)	
$V_{OUT,MAX,PLS}$	Minimum output voltage pulse (< 1 µs)	OUT	–0.8		
$V_{EN/UVLO,MAX}$	Maximum enable pin voltage range	EN/UVLO	–0.3	6.5	V
$V_{OVLO,MAX}$	Maximum OVLO pin voltage range	OVLO	–0.3	6.5	V
$V_{dVdt,MAX}$	Maximum dVdT pin voltage range	dVdt	Internally limited		V
$V_{ITIMER,MAX}$	Maximum ITIMER pin voltage range	ITIMER	Internally limited		V
$V_{RCBCTRL,MAX}$	Maximum RCBCTRL pin voltage range	RCBCTRL	–0.3	6.5	V
$V_{SPLYGD,MAX}$	Maximum SPLYGD/$\overline{\text{SPLYGD}}$ pin voltage range	SPLYGD/$\overline{\text{SPLYGD}}$	–0.3	6.5	V
$V_{FLTB,MAX}$	Maximum $\overline{\text{FLT}}$ pin voltage range	$\overline{\text{FLT}}$	–0.3	6.5	V
$V_{ILM,MAX}$	Maximum ILM pin voltage range	ILM	Internally limited		V
I_{MAX}	Maximum continuous switch current	IN to OUT or OUT to IN	Internally limited		A
$T_{J,MAX}$	Maximum operating junction temperature		Internally limited		°C
$T_{LEAD,MAX}$	Maximum lead temperature			300	°C
$T_{STG,MAX}$	Maximum storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Input voltage range	IN	3.5	23	V
V_{OUT}	Output voltage range	OUT		min (23, V_{IN} + 20)	V
$V_{EN/UVLO}$	Enable pin voltage range	EN/UVLO		5(1)	V
V_{OVLO}	OVLO pin voltage range	OVLO	0.5	1.5	V
V_{dVdt}	dVdT capacitor voltage rating	dVdt	V_{IN} + 5 V(2)		V
$V_{RCBCTRL}$	RCBCTRL pin voltage range	RCBCTRL		5	V
V_{FLTB}	FLTB pin voltage range	FLTB		5	V
V_{SPLYGD}	SPLYGD/$\overline{\text{SPLYGD}}$ pin voltage range	SPLYGD/$\overline{\text{SPLYGD}}$		5	V

6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

Parameter		Pin	MIN	MAX	UNIT
V_{ITIMER}	ITIMER pin capacitor voltage rating	ITIMER	4		V
R_{ILM}	ILM pin resistance	ILM	536	4834	Ω
I_{LOAD}	Continuous switch current, $T_J \leq 125℃$	IN to OUT or OUT to IN		8	A
T_J	Junction temperature		–40	125	°C

(1) For supply voltages below 5 V, it is okay to pull up the EN pin to IN directly. For supply voltages greater than 5 V, it is recommended to use a resistor divider to step down the voltage.
(2) In a PowerMUX scenario with unequal supplies, the dVdt capacitor rating for each device should be chosen based on the highest of the 2 rails.

6.4 Thermal Information

THERMAL METRIC (1)		TPS25948xx YWP (PWCSP) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.4(2)	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3(2)	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	11.2(2)	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Custom PCB layout 2s2p

6.5 Electrical Characteristics

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, V_{OVLO} = 0 V, R_{ILM} = 536 Ω , dVdT = Open, ITIMER = Open, SPLYGD/$\overline{\text{SPLYGD}}$ = Open, $\overline{\text{FLT}}$ = Open for TPS259480x, RCBCTRL = Open for TPS259481x/2x/3x. All voltages referenced to GND.

Test Parameter	Description	MIN	TYP	MAX	UNITS
INPUT SUPPLY (IN)					
$V_{UVP(R),IN}$	IN supply undervoltage protection rising threshold	2.7	3.0	3.3	V
$V_{UVP(F),IN}$	IN supply undervoltage protection falling threshold	2.2	2.4	2.65	V
$I_{Q(ON,IN)}$	IN supply ON state quiescent current when powered from IN, $V_{EN} > V_{UVLO(R)}$		439	640	µA
$I_{Q(OFF,UVLO,IN)}$	IN supply OFF state current when powered from IN, $V_{SD(F)} < V_{EN} < V_{UVLO(R)}$		73	193	µA
$I_{OUTLKG(ON)}$	OUT supply leakage current when powered from IN		432	640	µA
$I_{OUTLKG(OFF)}$	OUT supply leakage current when powered from IN, UVLO condition ($V_{SD(F)} < V_{EN} < V_{UVLO(R)}$)		7	29	µA
$I_{SD(IN)}$	IN supply shutdown current when powered from IN, $V_{EN} < V_{SD(F)}$		7	12	µA
$V_{UVP(R),OUT}$	OUT supply undervoltage protection rising threshold	2.7	3.0	3.3	V
$V_{UVP(F),OUT}$	OUT supply undervoltage protection falling threshold	2.2	2.4	2.65	V
OUTPUT SUPPLY (OUT)					
$I_{Q(ON,OUT)}$	OUT supply ON state quiescent current when powered from OUT, $V_{EN} > V_{UVLO(R)}$		422	640	µA
$I_{Q(OFF,UVLO,OUT)}$	OUT supply OFF state current when powered from OUT, $V_{SD(F)} < V_{EN} < V_{UVLO(R)}$		71	110	µA

6.5 Electrical Characteristics (continued)

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, V_{OVLO} = 0 V, R_{ILM} = 536 Ω , dVdT = Open, ITIMER = Open, SPLYGD/$\overline{\text{SPLYGD}}$ = Open, $\overline{\text{FLT}}$ = Open for TPS259480x, RCBCTRL = Open for TPS259481x/2x/3x. All voltages referenced to GND.

Test Parameter	Description	MIN	TYP	MAX	UNITS
$I_{SD(OUT)}$	OUT supply shutdown current when powered from OUT, V_{EN} < $V_{SD(F)}$		7	29	µA
ON RESISTANCE (IN - OUT)					
R_{ON}	V_{IN} = 12 V, I_{OUT} = 3 A, T_J = 25℃		12.2	15	mΩ
	3.5 ≤ V_{IN} ≤ 23 V, I_{OUT} = 3 A, –40℃ ≤ T_J ≤ 125℃			20	mΩ
ENABLE/UNDERVOLTAGE LOCKOUT (EN/UVLO)					
$V_{UVLO(R)}$	EN/UVLO pin rising threshold to turn FET ON	1.17	1.2	1.23	V
$V_{UVLO(F)}$	UVLO pin falling threshold to turn FET OFF	1.07	1.1	1.12	V
$V_{SD(F)}$	EN/UVLO falling threshold for lowest shutdown current	0.54	0.75		V
I_{ENLKG}	EN/UVLO pin leakage current	–0.1		0.1	µA
OVERVOLTAGE LOCKOUT (OVLO)					
$V_{OV(R)}$	OVLO pin rising threshold	1.18	1.2	1.23	V
$V_{OV(F)}$	OVLO pin falling threshold	1.07	1.1	1.12	V
I_{OVLKG}	OVLO pin leakage current, 0.5 V < V_{OVLO} < 1.5 V	–0.1		0.1	µA
OUTPUT LOAD CURRENT MONITOR (IMON)					
G_{IMON}	Analog load current monitor gain (IMON : IOUT), I_{OUT} = 1 A, I_{OUT} < I_{LIM}	114	133	154	µA/A
G_{IMON}	Analog load current monitor gain (IMON : IOUT), I_{OUT} = 3 A to 8 A, I_{OUT} < I_{LIM}	116	133	149	µA/A
OVERCURRENT PROTECTION (OUT)					
I_{LIM}	Overcurrent threshold, R_{ILM} = 2.43 kΩ	1.75	1.99	2.25	A
	Overcurrent threshold, R_{ILM} = 1.62 kΩ	2.7	2.98	3.3	A
	Overcurrent threshold, R_{ILM} = 604 Ω	7.2	8	8.7	A
I_{FLT}	Circuit-breaker threshold, ILM pin open (Single point failure)			0.1	A
	Circuit-breaker threshold, ILM pin shorted to GND (Single point failure)		1.4	2.5	A
I_{SCGain}	Scalable Fast-trip current threshold (I_{SC}) : I_{LIM} Ratio (Steady-state/Start-up for TPS259480x/2x variants and Start-up for TPS259481x/3x variants)	170%	184%	240%	
I_{FFT}	Fixed Fast-trip current threshold, TPS259480x/2x variants only	16.9	25.1	31.0	A
	Fixed Fast-trip current threshold, TPS259481x/3x variants only	15	22.8	29	A
V_{FB}	V_{OUT} threshold to exit current limit foldback	1.5	1.9	2.3	V
OVERCURRENT FAULT TIMER (ITIMER)					
V_{INT}	ITIMER pin internal pull-up voltage	2.3	2.6	2.7	V
R_{ITIMER}	ITIMER pin internal pull-up resistance		15.7		kΩ
I_{ITIMER}	ITIMER pin discharge current, I_{OUT} > I_{LIM}	1.5	1.9	2.45	µA
ΔV_{ITIMER}	ITIMER discharge differential voltage threshold	1.28	1.51	1.75	V
REVERSE CURRENT BLOCKING (IN - OUT)					
V_{FWD}	V_{IN} – V_{OUT} forward regulation voltage, I_{OUT} = 10 mA	0.1	10.6	24.5	mV
V_{REVTH}	V_{IN} – V_{OUT} threshold for fast BFET turn off (enter reverse current blocking)	–44.8	–29.5	–14.8	mV

6.5 Electrical Characteristics (continued)

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, V_{OVLO} = 0 V, R_{ILM} = 536 Ω , dVdT = Open, ITIMER = Open, SPLYGD/$\overline{\text{SPLYGD}}$ = Open, $\overline{\text{FLT}}$ = Open for TPS259480x, RCBCTRL = Open for TPS259481x/2x/3x. All voltages referenced to GND.

Test Parameter	Description	MIN	TYP	MAX	UNITS
V_{FWDTH}	V_{IN} – V_{OUT} threshold for fast BFET turn on (exit reverse current blocking)	70	105.9	140	mV
I_{REVLKG}	Reverse leakage current during reverse current blocking condition	–2	–1.1		µA
SUPPLY GOOD INDICATION (SPLYGD/$\overline{\text{SPLYGD}}$)					
V_{SPLYGD}	SPLYGD pin low voltage V_{IN} > 3.3V, Strong pull-up			600	mV
V_{SPLYGD}	SPLYGD pin low voltage V_{IN} < 3.3V, EN < $V_{SD(F)}$, weak pull-up		650	930	mV
V_{SPLYGD}	SPLYGD pin low voltage V_{IN} < 3.3V, EN < $V_{SD(F)}$, strong pull-up		785	990	mV
$I_{SPLYGDLKG}$	SPLYGD High leakage current	–3		3	µA
$I_{SPLYGDBLKG}$	$\overline{\text{SPLYGD}}$ High leakage current	–3		3	µA
FAULT INDICATION ($\overline{\text{FLT}}$) or REVERSE BLOCKING CONTROL (RCBCTRL)					
$I_{FLTBLKG}$	$\overline{\text{FLT}}$ leakage current	–1		1	µA
R_{FLTB}	$\overline{\text{FLT}}$ pin internal pull-down resistance, TPS259480x variants only		11.8		Ω
$I_{RCBCTRL}$	RCBCTRL pin internal pull-up current, TPS259481x/2x/3x variants only		5		µA
$V_{IH,RCBCTRL}$	RCBCTRL pin logic high detection threshold, TPS259481x/2x/3x variants only	1.09	1.15	1.2	V
$V_{IL,RCBCTRL}$	RCBCTRL pin logic low detection threshold, TPS259481x/2x/3x variants only	1.0	1.0	1.11	V
OVERTEMPERATURE PROTECTION (OTP)					
TSD	Thermal shutdown rising threshold, T_J rising		154		°C
TSD_{HYS}	Thermal shutdown hysteresis, T_J falling		10		°C
SLEW RATE CONTROL (DVDT)					
I_{dvdt}	dVdt pin charging current	2.6	5.3	9	µA

6.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OVLO}	Overvoltage lock-out response time	V_{OVLO} > $V_{OV(R)}$ to V_{OUT}↓		1		µs
t_{LIM}	Current limit response time	I_{OUT} > 1.2 × I_{LIM} and ITIMER expired to I_{OUT} settling to within 5% of I_{LIM}		250		µs
t_{SC}	Scalable fast-trip response time (TPS259480x/2x only)	I_{OUT} > 3 × I_{LIM} to I_{OUT}↓		900		ns
t_{FT}	Fixed fast-trip response time	I_{OUT} > I_{FFT} to I_{OUT}↓		750		ns
t_{RST}	Auto-Retry interval after fault (TPS25948xA only)			103		ms
t_{SWOV}	OVLO fast recovery response time	V_{OVLO} < $V_{OV(F)}$ to V_{OUT}↑		85.3		µs
t_{SWRCB}	Reverse Current Blocking recovery time	(V_{IN} – V_{OUT}) > V_{FWDTH} to V_{OUT}↑		46.5		µs
t_{RCB}	Reverse Current Blocking comparator response time	(V_{OUT} – V_{IN}) > 1.3 × V_{REVTH} to BFET OFF		1.1		µs
$t_{SPLYGDA}$	Supply Good assertion de-glitch			14.7		µs
$t_{SPLYGDD}$	Supply Good de-assertion de-glitch			14.3		µs

6.7 Switching Characteristics

The output rising slew rate is internally controlled and constant across the entire operating voltage range to ensure the turn on timing is not affected by the load conditions. The rising slew rate can be adjusted by adding capacitance from the dVdt pin to ground. As C_{dVdt} is increased it will slow the rising slew rate (SR). See Slew Rate and Inrush Current Control (dVdt) section for more details. The Turn-Off Delay and Fall Time, however, are dependent on the RC time constant of the load capacitance (C_{OUT}) and Load Resistance (R_L). The Switching Characteristics are only valid for the power-up sequence where the supply is available in steady state condition and the load voltage is completely discharged before the device is enabled. Typical values are taken at T_J = 25°C unless specifically noted otherwise. R_{OUT} = 100 Ω, C_{OUT} = 1 µF

PARAMETER		VIN	C_{dVdt} = Open	C_{dVdt} = 3.3 nF	C_{dVdt} = 6.8 nF	UNITS
$t_{D,ON}$	Turn on delay	3.5	0.15	0.78	1.31	ms
		12	0.17	1.04	2.04	ms
		23	0.18	1.60	3.44	ms
SR_{ON}	Output rising slew rate	3.5	14.40	1.25	0.58	V/ms
		12	25.30	1.36	0.60	V/ms
		23	38.30	1.44	0.65	V/ms
t_R	Rise time	3.5	0.20	2.12	4.59	ms
		12	0.36	7.04	17.08	ms
		23	0.47	12.83	27.70	ms
t_{ON}	Turn on time	3.5	0.41	2.88	5.89	ms
		12	0.55	8.09	19.14	ms
		23	0.65	14.66	31.20	ms
$t_{D,OFF}$	Turn off delay	3.5	17.30	17.30	17.30	µs
		12	15.80	15.80	15.80	µs
		23	13.50	13.50	13.50	µs
t_F	Fall time	3.5	Depends on R_{OUT} and C_{OUT}			µs
		12				
		23				

6.8 Typical Characteristics

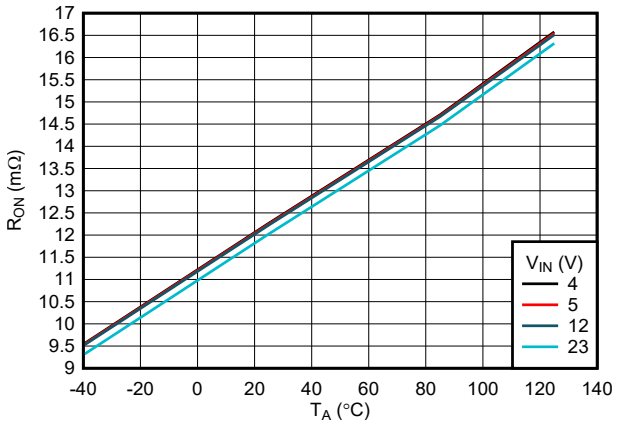


Figure 6-1. ON-Resistance vs Temperature

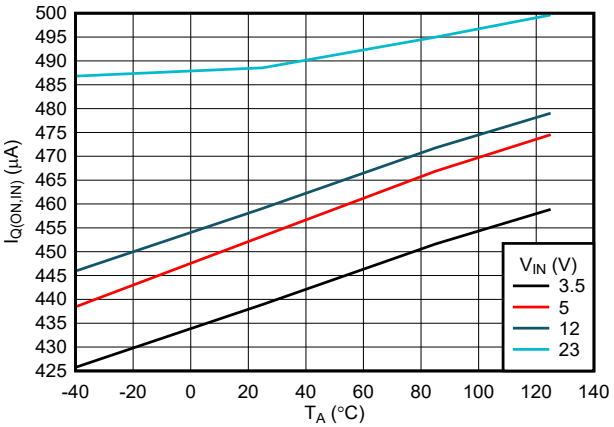


Figure 6-2. IN Quiescent Current vs Temperature

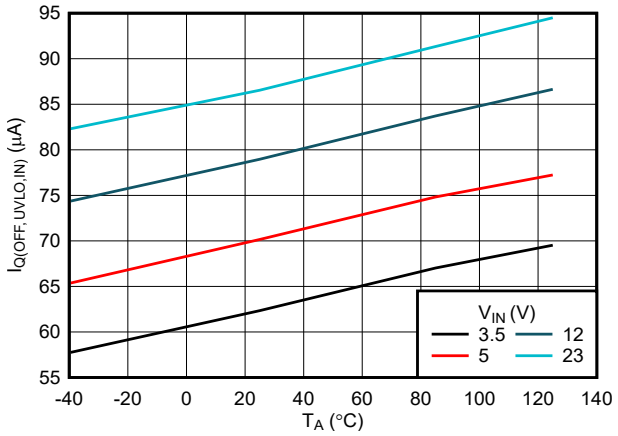


Figure 6-3. IN OFF state (UVLO) current vs Temperature

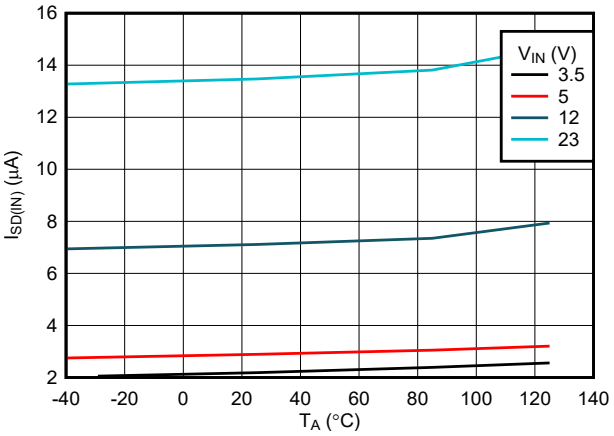


Figure 6-4. IN Shutdown Current vs Temperature

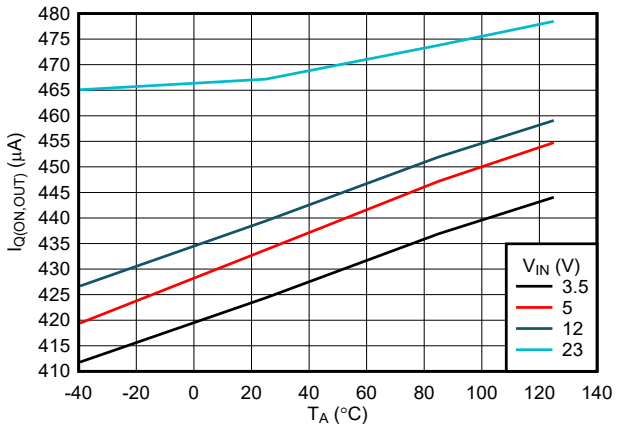


Figure 6-5. OUT Quiescent Current vs Temperature

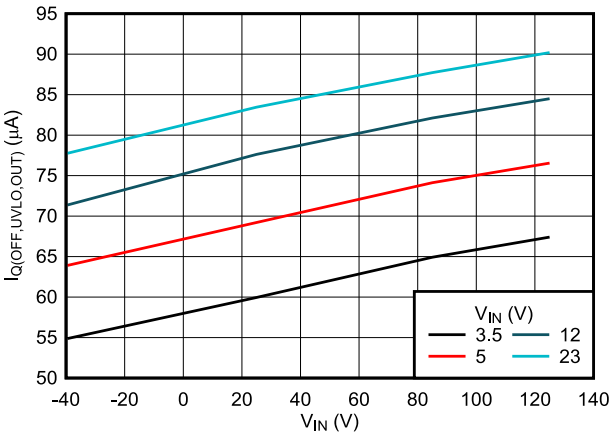


Figure 6-6. OUT OFF State (UVLO) Current vs Temperature

6.8 Typical Characteristics (continued)

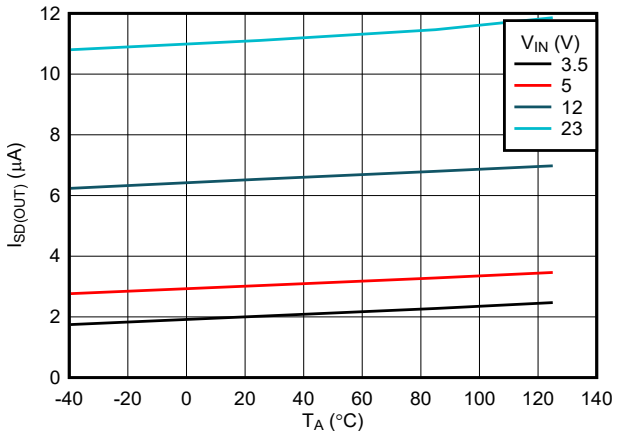


Figure 6-7. OUT Shutdown Current vs Temperature

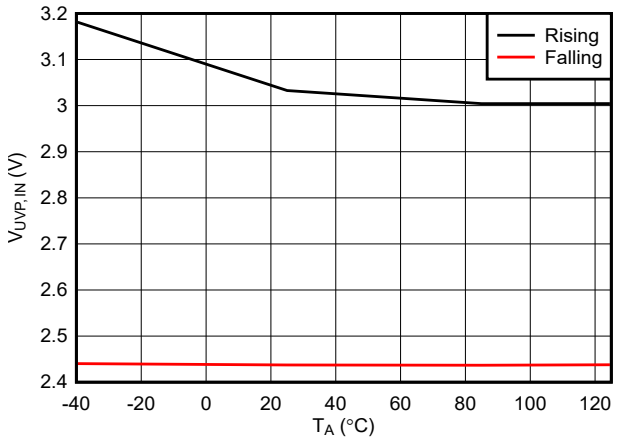


Figure 6-8. IN Undervoltage Threshold vs Temperature

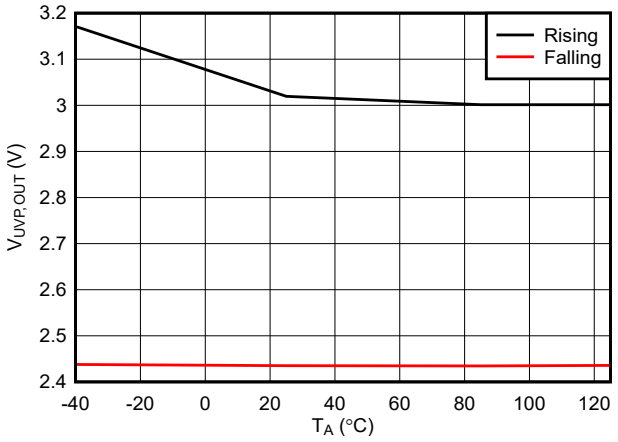


Figure 6-9. OUT Undervoltage Threshold vs Temperature

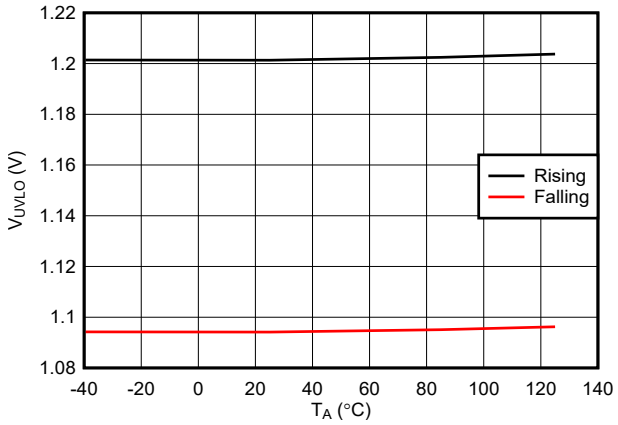


Figure 6-10. EN/UVLO FET Turn OFF Threshold vs Temperature

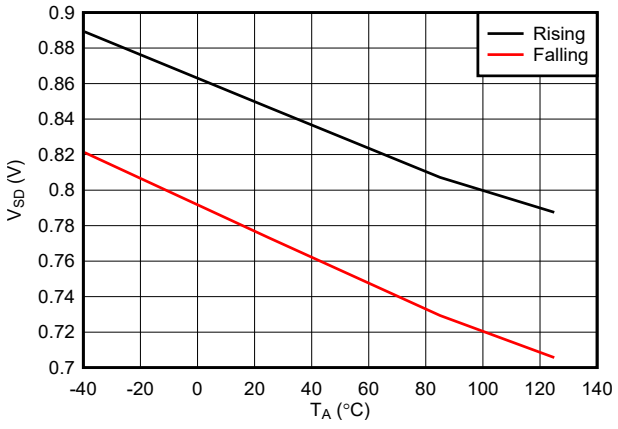


Figure 6-11. EN/UVLO Shutdown Threshold vs Temperature

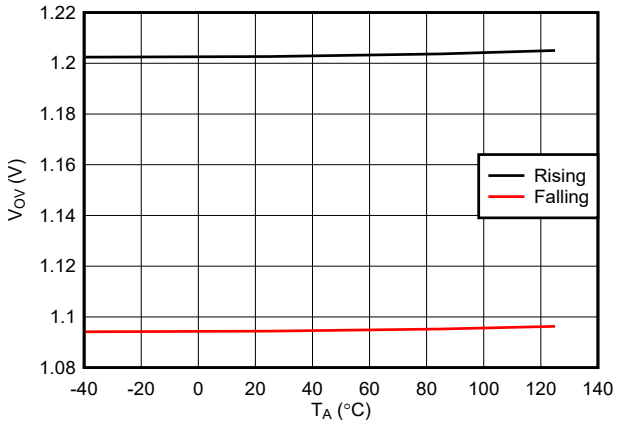


Figure 6-12. OVLO Threshold vs Temperature

6.8 Typical Characteristics (continued)

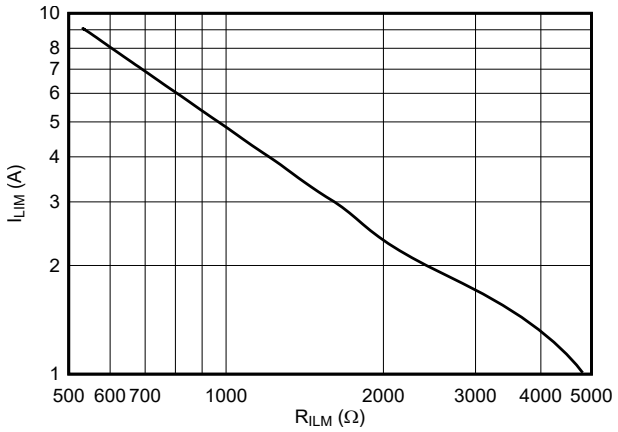


Figure 6-13. Overcurrent Threshold vs ILM Resistor

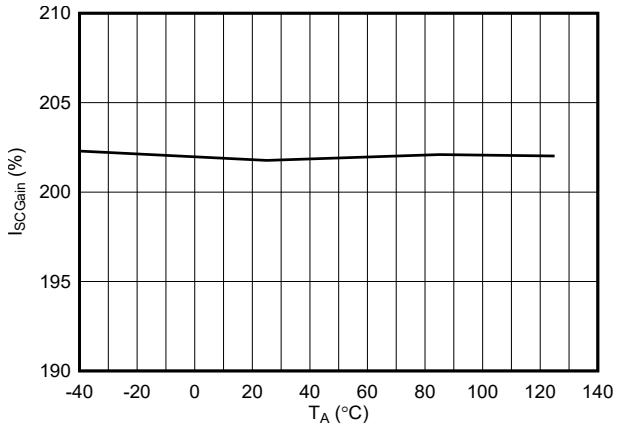


Figure 6-14. Steady State Scalable Fast-trip Threshold: Current Limit Threshold (I_{LIM}) Ratio vs Temperature (TPS259480x/2x)

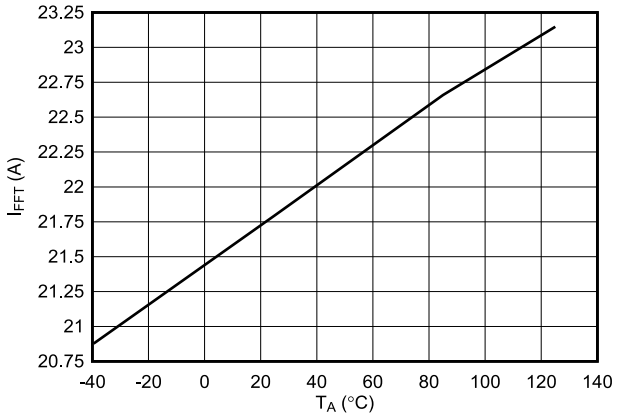


Figure 6-15. Steady State Fixed Fast-Trip Current Threshold vs Temperature (TPS259481x/3x)

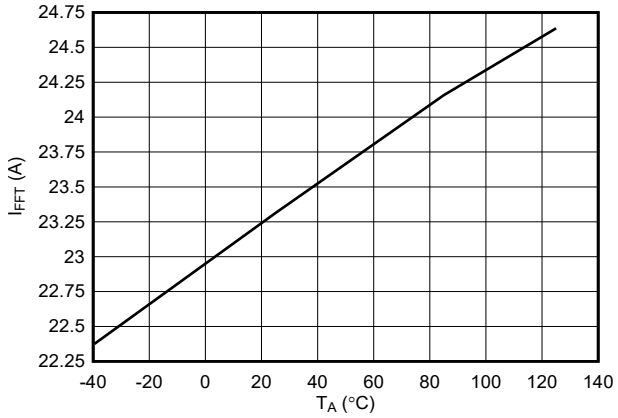


Figure 6-16. Steady State Fixed Fast-Trip Current Threshold vs Temperature (TPS259480x/2x)

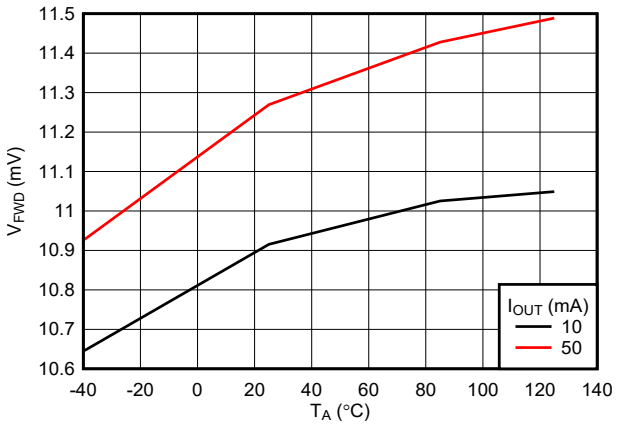


Figure 6-17. RCB - Forward Regulation Voltage vs Temperature

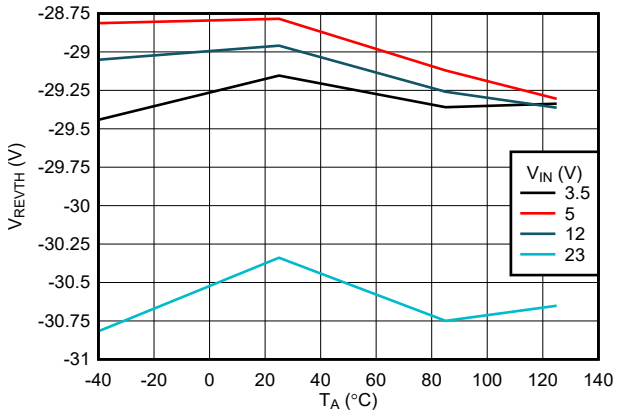


Figure 6-18. RCB - Reverse Comparator Threshold vs Temperature

6.8 Typical Characteristics (continued)

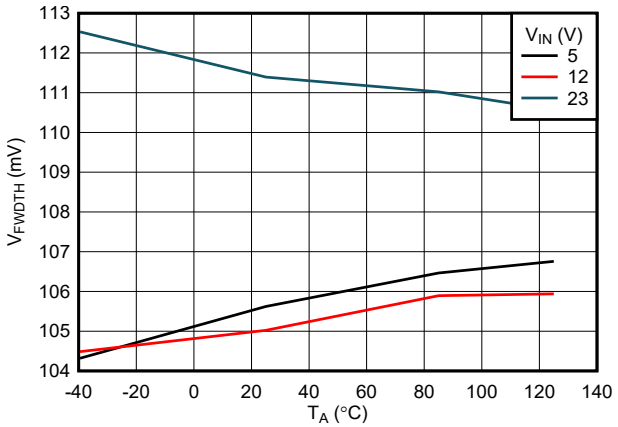


Figure 6-19. RCB - Forward Comparator Threshold vs Temperature

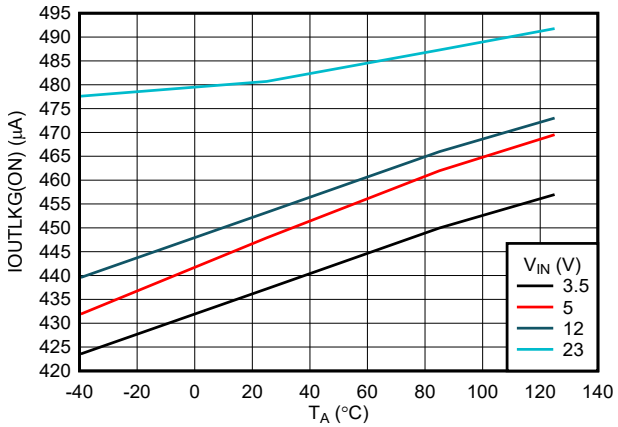


Figure 6-20. OUT Leakage Current During ON-State Reverse Current Blocking

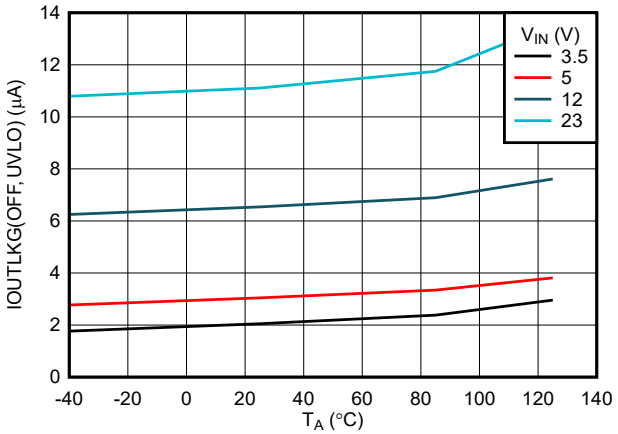


Figure 6-21. Reverse Leakage Current During OFF-State

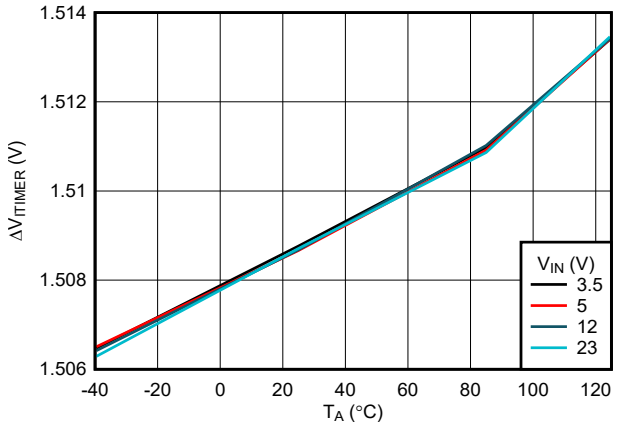


Figure 6-22. ITIMER Discharge Differential Voltage Threshold vs Temperature

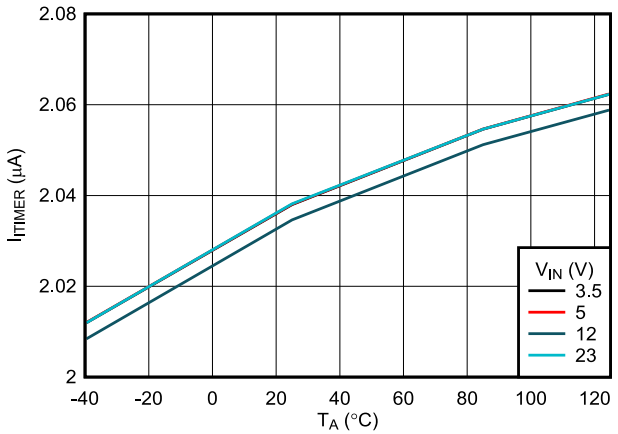


Figure 6-23. ITIMER Discharge Current vs Temperature

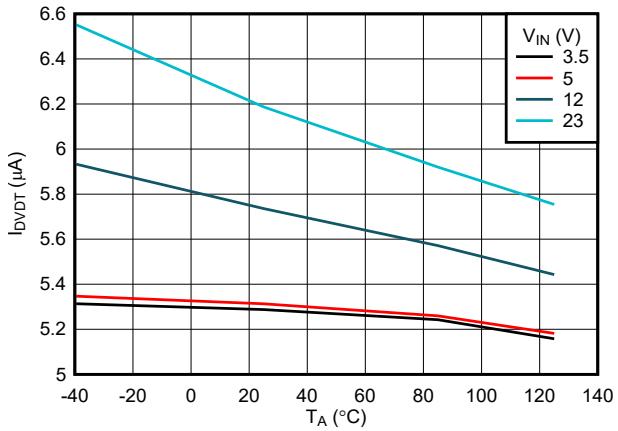


Figure 6-24. DVDT Charging Current vs Temperature

6.8 Typical Characteristics (continued)

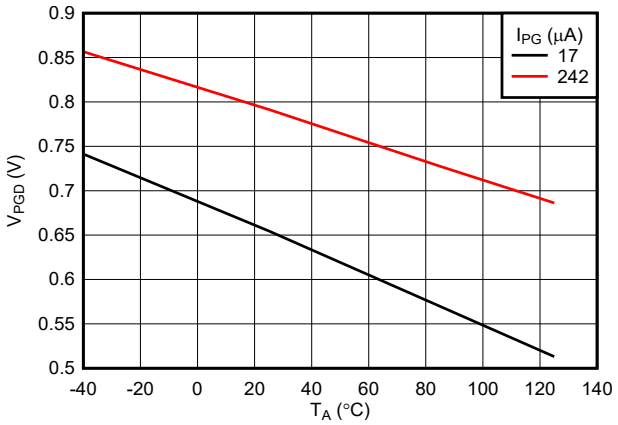


Figure 6-25. PG Low Voltage Without Input Supply vs Temperature

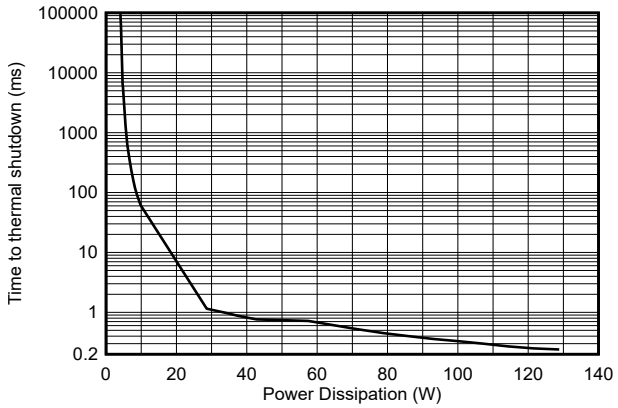
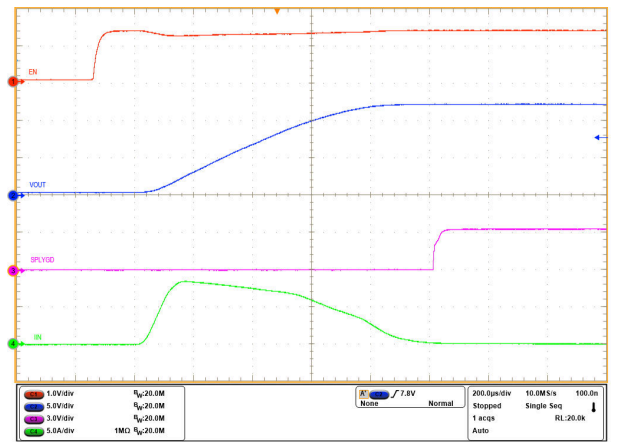
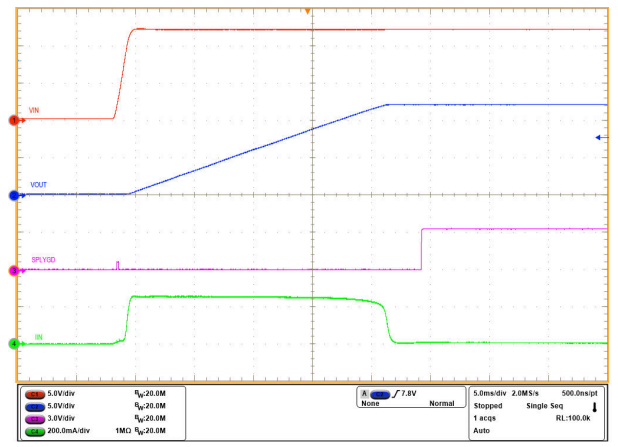


Figure 6-26. Time to Thermal Shut-Down During Inrush State



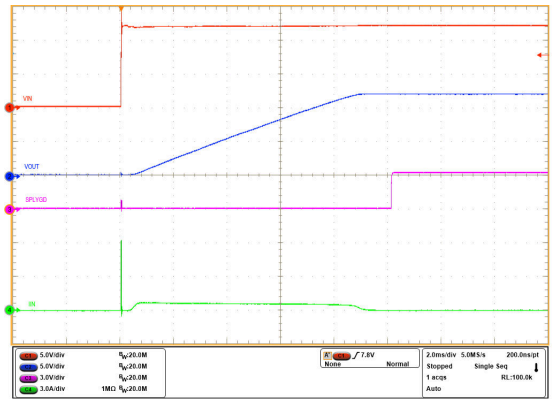
V_{IN} = 12 V, C_{OUT} = 220 µF, C_{dVdt} = Open, $V_{EN/UVLO}$ stepped up to 2 V

Figure 6-27. Start Up With Enable



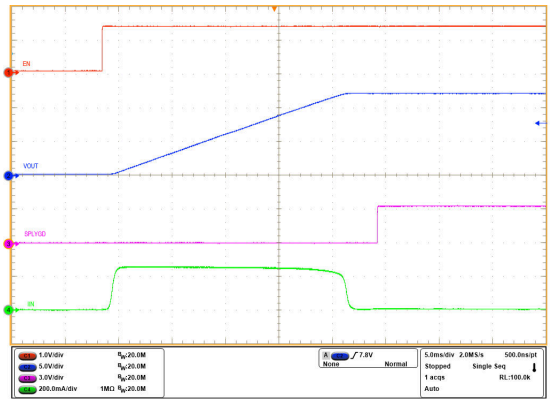
$V_{EN/UVLO}$ = 2 V, C_{OUT} = 220 µF, C_{dVdt} = 10 nF, V_{IN} ramped up to 12 V

Figure 6-28. Start Up With Supply



C_{IN} = 0.1 µF, C_{OUT} = 220 µF, C_{dVdt} = 10 nF, EN/UVLO connected to IN through resistor ladder, 12 V hot-plugged to IN

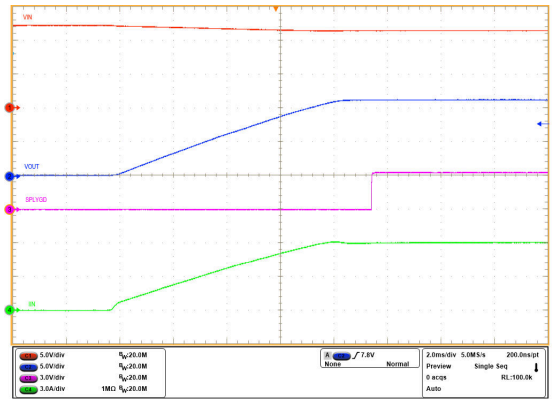
Figure 6-29. Input Hot-Plug



V_{IN} = 12 V, C_{OUT} = 220 µF, C_{dVdt} = 10 nF, $V_{EN/UVLO}$ stepped up to 2 V

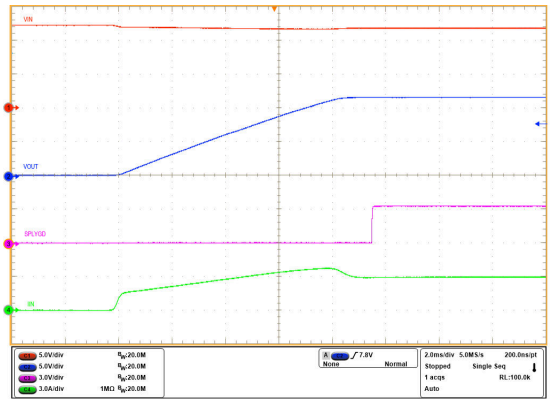
Figure 6-30. Inrush Current With Capacitive Load

6.8 Typical Characteristics (continued)



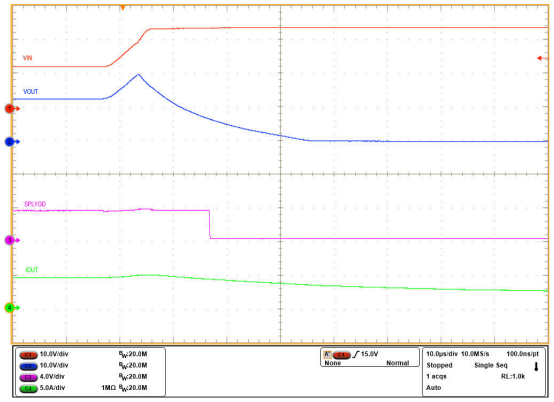
V_{IN} = 12 V, C_{OUT} = 220 µF, R_{OUT} = 2 Ω, C_{dVdt} = 3300 pF, $V_{EN/UVLO}$ stepped up to 2 V

Figure 6-31. Inrush Current With Resistive and Capacitive Load



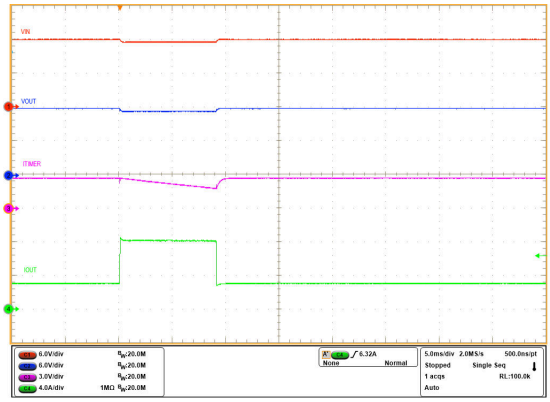
V_{IN} = 12 V, C_{OUT} = 690 µF, R_{OUT} = 4 Ω, C_{dVdt} = 3300 pF, $V_{EN/UVLO}$ stepped up to 2 V

Figure 6-32. Inrush Current With Resistive and Capacitive Load



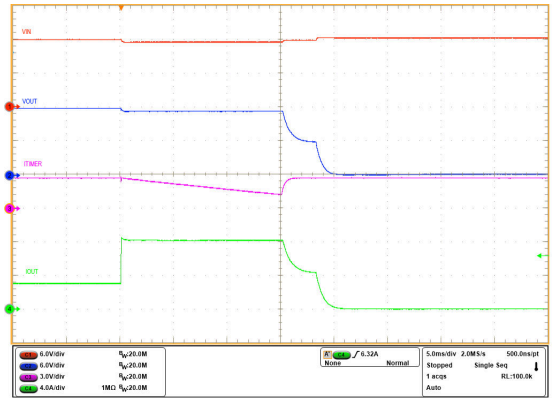
V_{IN} Overvoltage threshold set to 20 V, V_{IN} ramped up from 12 V to 23 V

Figure 6-33. Overvoltage Lockout Response



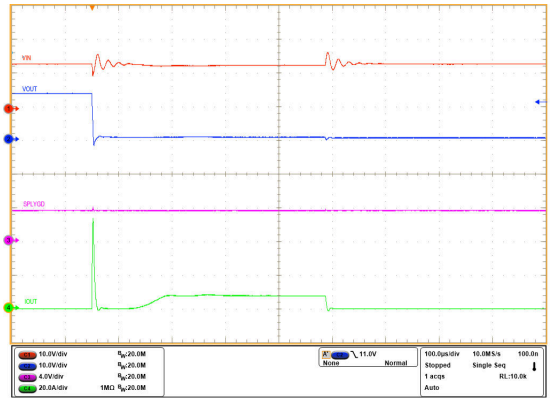
V_{IN} = 12 V, C_{ITIMER} = 22 nF, C_{OUT} = 220 µF, I_{LIM} set to 4.5 A, I_{OUT} ramped from 3 A → 8 A→ 3 A within 9 ms

Figure 6-34. Transient Overcurrent Blanking Timer Response



V_{IN} = 12 V, C_{ITIMER} = 22 nF, C_{OUT} = 220 µF, I_{LIM} set to 4.5 A, I_{OUT} stepped from 3 A → 9 A

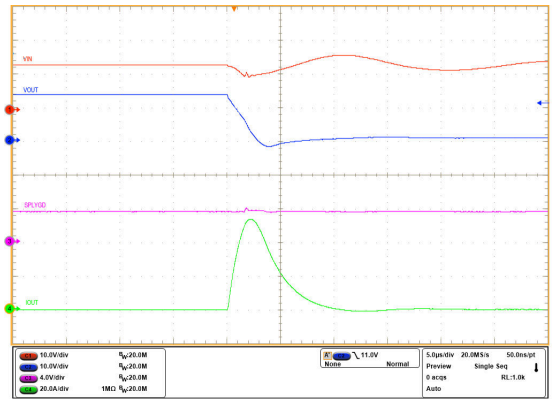
Figure 6-35. Active Current Limit Response Followed by TSD



V_{IN} = 12 V, I_{LIM} set to 9 A, $V_{EN/UVLO}$ = 2 V, OUT stepped from Open → Short-circuit to GND

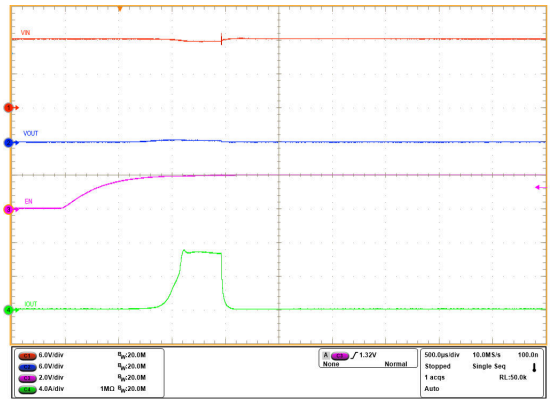
Figure 6-36. Output Short-Circuit During Steady State

6.8 Typical Characteristics (continued)



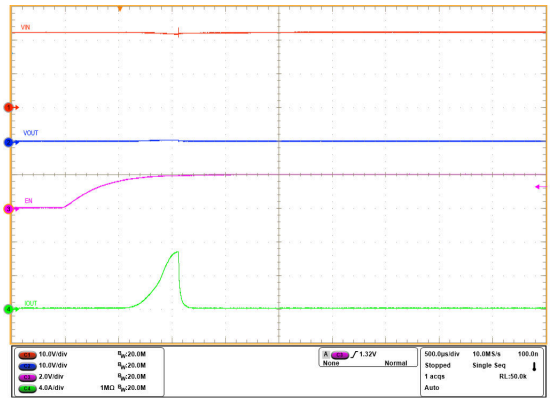
V_{IN} = 12 V, I_{LIM} set to 9 A, $V_{EN/UVLO}$ = 2 V, OUT stepped from Open → Short-circuit to GND

Figure 6-37. Output Short-Circuit During Steady State (Zoomed In)



V_{IN} = 12 V, OUT short-circuit to GND, I_{LIM} set to 4.5 A, $V_{EN/UVLO}$ stepped from 0 V to 2 V

Figure 6-38. Power Up Into Short-Circuit



V_{IN} = 22 V, OUT short-circuit to GND, I_{LIM} set to 9 A, $V_{EN/UVLO}$ stepped from 0 V to 2 V

Figure 6-39. Power Up Into Short-Circuit

7 Detailed Description

7.1 Overview

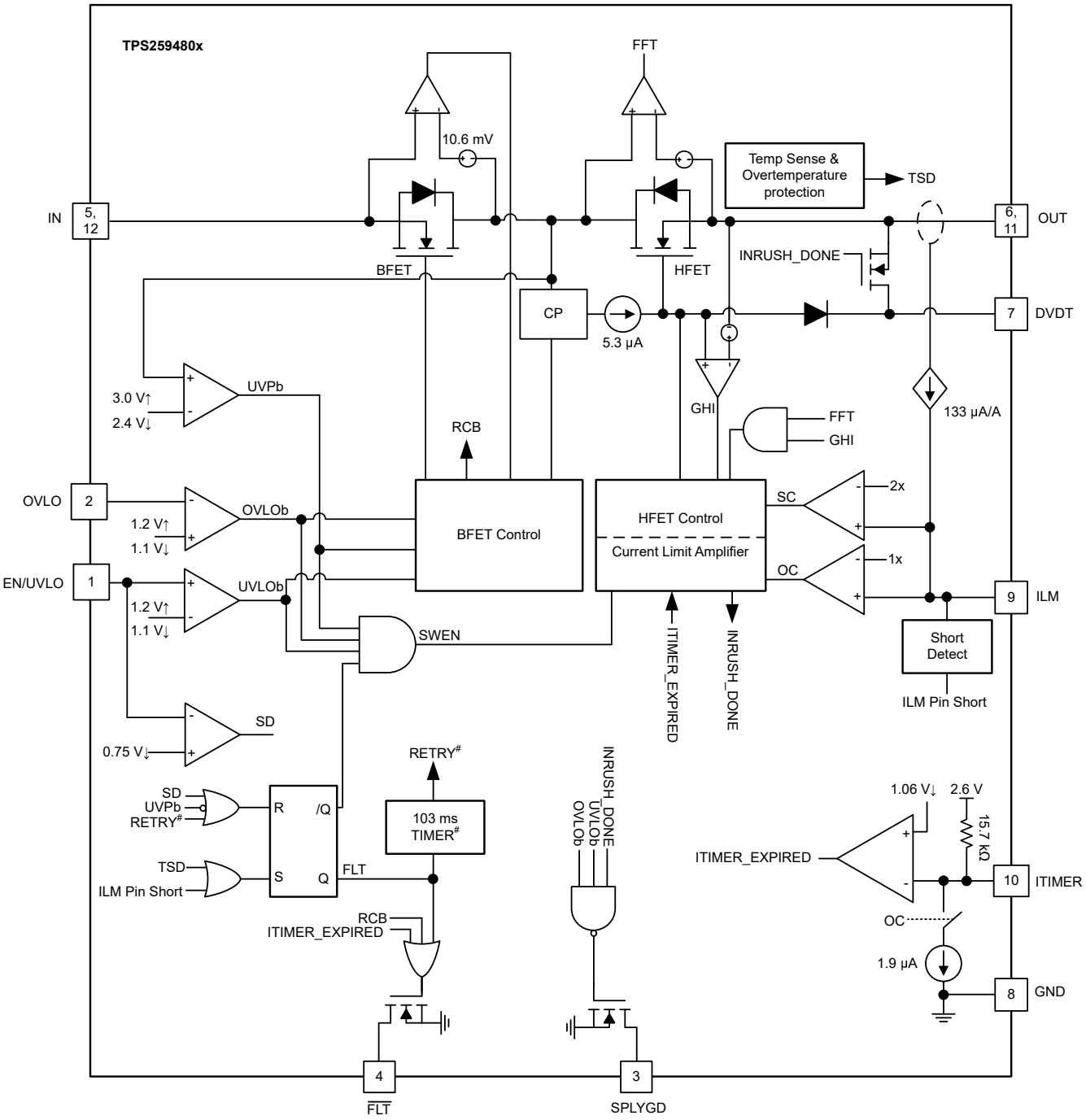
The TPS25948xx is an eFuse with integrated power path that is used to ensure safe power delivery in a system. The device starts its operation by monitoring the IN and OUT bus voltage. When the supply voltage (V_{IN} or V_{OUT}) exceeds the Undervoltage Protection threshold (V_{UVP}), the device samples the EN/UVLO pin. A high level (> V_{UVLO}) on this pin enables the internal power path (BFET+HFET) to start conducting and allow current to flow between IN and OUT. When EN/UVLO is held low (< V_{UVLO}), the internal power path is turned off to block current flow between IN and OUT.

After a successful start-up sequence, the device now actively monitors its load current and bus voltage and controls the internal HFET to ensure that the user adjustable overcurrent limit threshold (I_{LIM}) is not exceeded and overvoltage spikes are cut-off once they cross the user adjustable overvoltage lockout threshold (V_{OVLO}). The device also provides fast protection against severe overcurrent during short-circuit events. This keeps the system safe from harmful levels of voltage and current. At the same time, a user adjustable overcurrent blanking timer allows the system to pass moderate transient peaks in the load current profile without tripping the eFuse. This ensures a robust protection solution against real faults which is also immune to transients, thereby ensuring maximum system uptime.

The device has integrated reverse current blocking FET (BFET) which operates like an ideal diode. The BFET is linearly regulated to maintain a small constant forward drop (V_{FWD}) in forward conduction mode and turned off completely to block reverse current if output voltage exceeds the input voltage. In some device variants, the reverse current blocking can be disabled using an external pin control (RCBCTRL) to allow bi-directional current flow to support applications such as USB On-the-go or DRP (Dual Role Port).

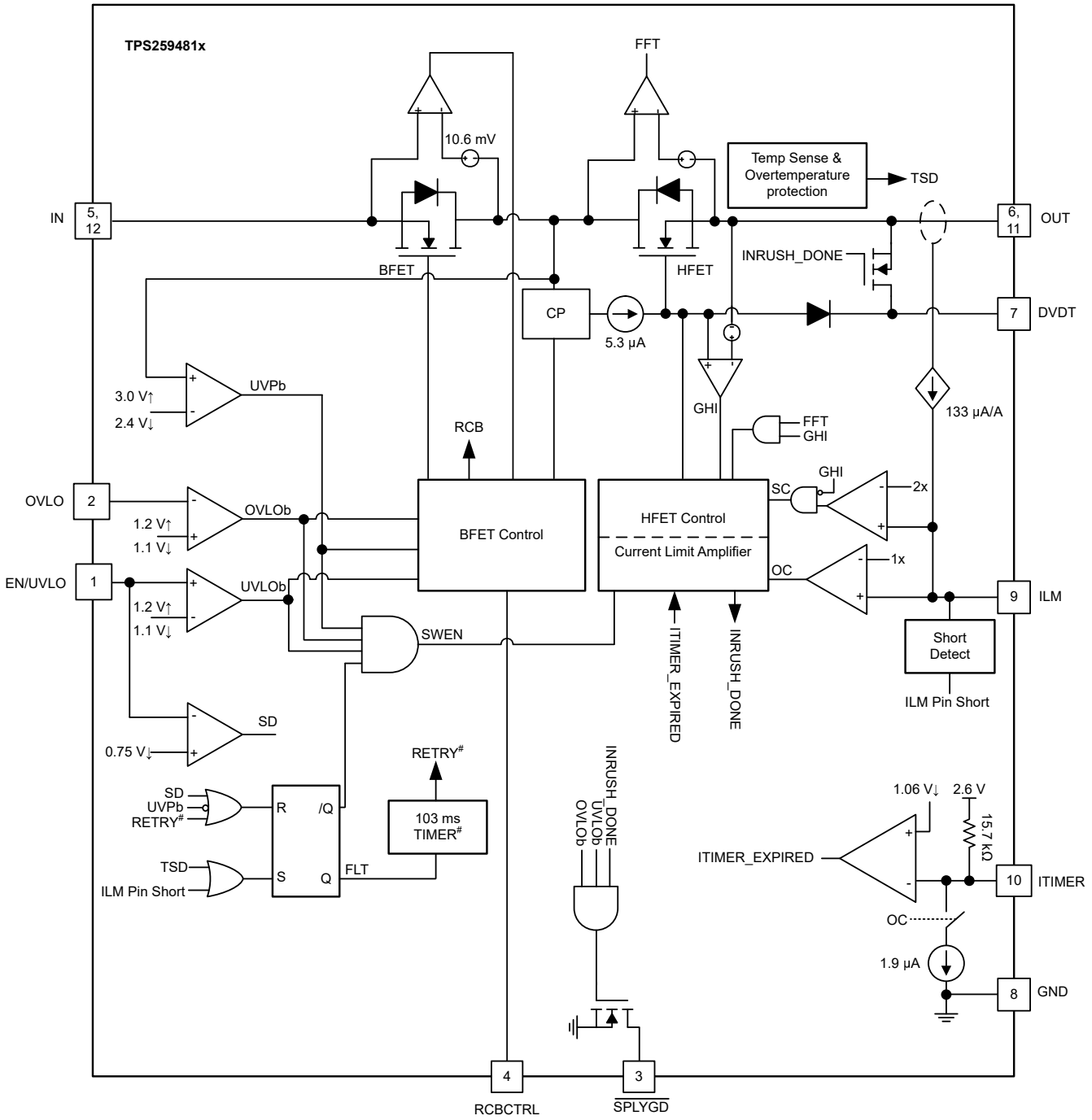
The device also has a built-in thermal sensor based shutdown mechanism to protect itself in case the device temperature (T_J) exceeds the recommended operating conditions.

7.2 Functional Block Diagram



Not applicable to Latch-off variant (TPS259480L)

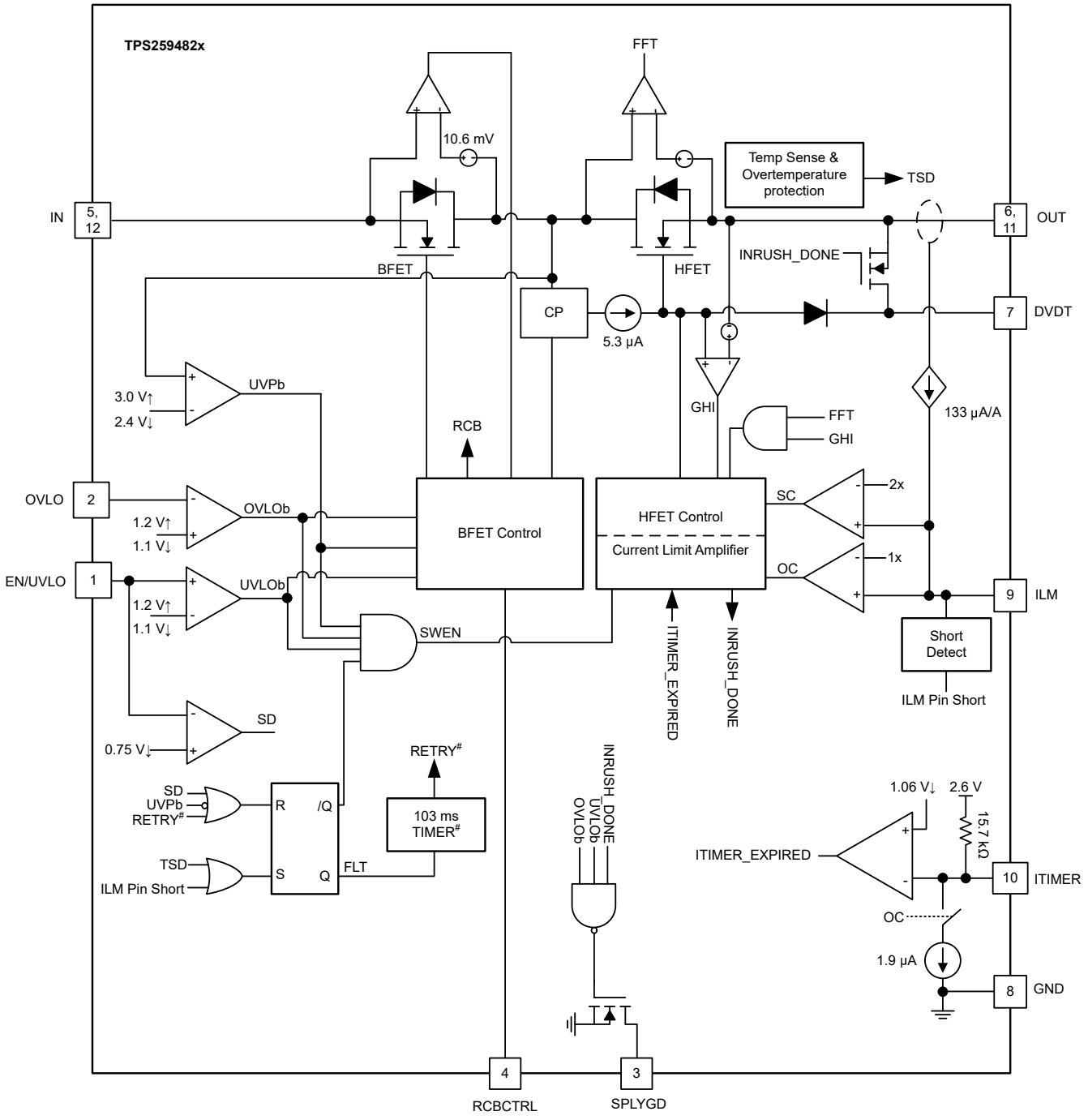
Figure 7-1. TPS259480x Block Diagram



Not applicable to Latch-off variant (TPS259481L)

TPS259483 will have same block diagram except the SPLYGD polarity is flipped from TPS259481

Figure 7-2. TPS259481x Block Diagram



Not applicable to Latch-off variant (TPS259482L)

Figure 7-3. TPS259482x Block Diagram

7.3 Feature Description

The TPS25948xx eFuse is a compact, feature rich power management device that provides detection, protection ,and indication in the event of system faults.

7.3.1 Undervoltage Lockout (UVLO and UVP)

The TPS25948xx implements undervoltage protection on IN and OUT in case the applied voltage becomes too low for the system or device to properly operate. The undervoltage protection has a default lockout threshold of V_{UVP} which is fixed internally. Also, the UVLO comparator on the EN/UVLO pin allows the undervoltage protection threshold to be externally adjusted to a user defined value. Figure 7-4 and Equation 1 show how a resistor divider can be used to set the UVLO set point for a given voltage supply.

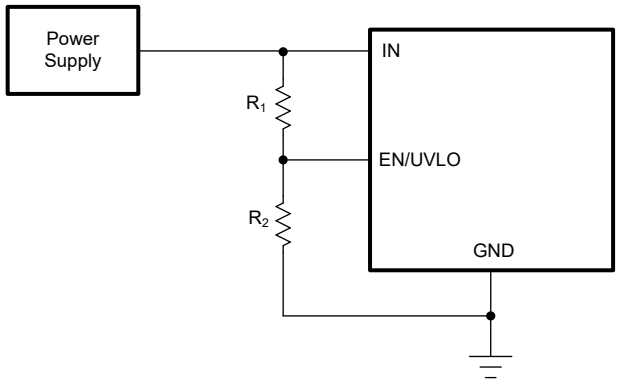


Figure 7-4. Adjustable Undervoltage Protection

$$\mathrm{VIN(UV)} = \mathrm{VUVLO(F)} \times \frac{\mathrm{R1} + \mathrm{R2}}{\mathrm{R2}} \quad (1)$$

7.3.2 Overvoltage Lockout (OVLO)

The TPS25948xx allows the user to implement Overvoltage protection on the bus to shield the system against supply overvoltage conditions. The internal fast comparator on the OVLO pin allows the Overvoltage Lockout threshold to be adjusted to a user defined value. Once the voltage at the OVLO pin crosses the OVLO rising threshold $V_{OV(R)}$, the device turns off both the FETs to cut off the power path. Thereafter, the devices wait for the voltage at the OVLO pin to fall below the OVLO falling threshold $V_{OV(F)}$ before the FETs are turned ON again. The rising and falling thresholds are slightly different to provide hysterisis. Figure 7-5 and Equation 2 show how a resistor divider can be used to set the OVLO set point for a given voltage supply.

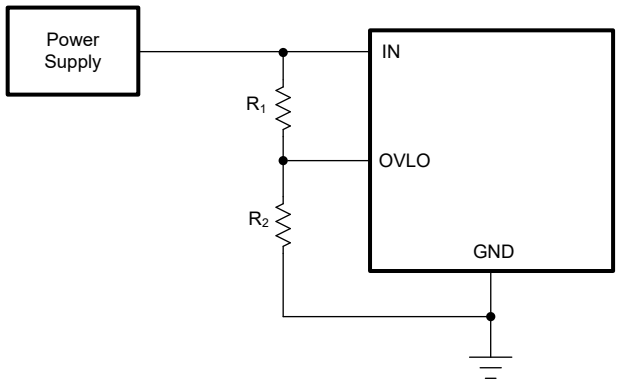


Figure 7-5. Adjustable Overvoltage Protection

$$\mathrm{VIN(OV)} = \mathrm{VOV(F)} \times \frac{\mathrm{R1} + \mathrm{R2}}{\mathrm{R2}} \quad (2)$$

While recovering from a OVLO event, the TPS25948xx bypasses the inrush control (dVdt) and starts up in a current limited manner to provide faster turn ON and minimize power supply droop during supply transient conditions.

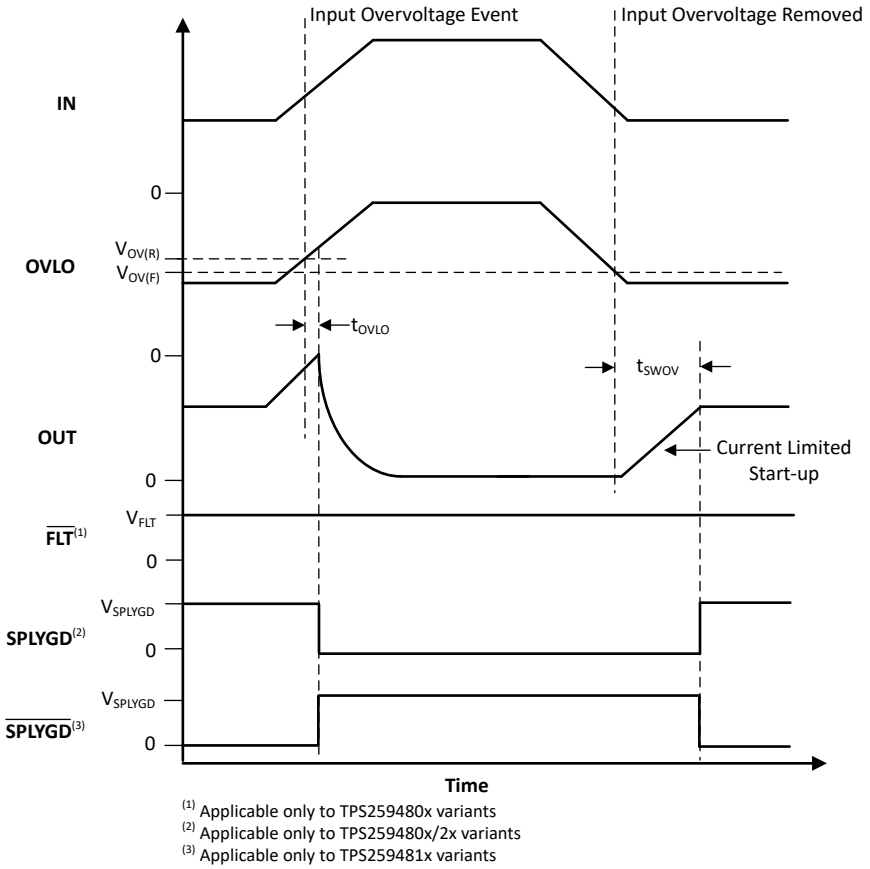


Figure 7-6. TPS25948xx Overvoltage Lockout and Recovery

7.3.3 Inrush Current, Overcurrent, and Short Circuit Protection

TPS25948xx incorporates four levels of protection against overcurrent:

1. Adjustable slew rate (dVdt) for inrush current control
2. Adjustable threshold (I_{LIM}) for overcurrent protection during start-up or steady-state
3. Adjustable threshold (I_{SC}) for fast-trip response to severe overcurrent during start-up or steady-state
4. Fixed threshold (I_{FFT}) for fast-trip response to quickly protect against hard output short-circuits during steady-state

7.3.3.1 Slew Rate (dVdt) and Inrush Current Control

During hot-plug events or while trying to charge a large output capacitance at start-up, there can be a large inrush current. If the inrush current is not managed properly, it can damage the input connectors and/or cause the system power supply to droop leading to unexpected restarts elsewhere in the system. The inrush current during turn on is directly proportional to the load capacitance and rising slew rate.

Equation 3 can be used to find the slew rate (SR) required to limit the inrush current (I_{INRUSH}) for a given load capacitance (C_{OUT}):

$$\mathrm{IINRUSH\ (mA)} = \mathrm{COUT\ (\mu F)} \times \mathrm{SRON\ (V/ms)} \quad (3)$$

A capacitor can be connected to the dVdt pin to control the rising slew rate and lower the inrush current during turn on. The required C_{dVdt} capacitance to produce a given slew rate can be calculated using the equation:

$$\text{CDVDT (pF)} = \frac{5000}{\text{SRON (V/ms)}} \quad (4)$$

The fastest output slew rate is achieved by leaving the dVdt pin open.

Note

1. The slew rate calculation above holds good for C_{dVdt} > 1nF. For lower C_{dVdt} values, the internal gate capacitance may dominate and cause the actual slew rate to deviate from the calculation.
2. Slew rate control during start-up is provided only on the HFET which enables inrush current control from IN to OUT.
3. For C_{dVdt} > 10nF, it is recommended to add a 100Ω resistor in series with the capacitor on the dVdt pin.

7.3.3.2 Active Current Limiting

The TPS25948xx responds to output overcurrent conditions by actively limiting the current after a user adjustable transient fault blanking interval. When the load current exceeds the set overcurrent threshold (I_{LIM}) set by the ILM pin resistor (R_{ILM}), but stays lower than the short-circuit threshold (2 × I_{LIM} or I_{FFT} depending on the variant), the device starts discharging the ITIMER pin capacitor using an internal 1.9µA pulldown current. If the load current drops below the overcurrent threshold before the ITIMER capacitor (C_{ITIMER}) discharges by ΔV_{ITIMER}, the ITIMER is reset by pulling it up to V_{INT} internally and the current limit action is not engaged. This allows short load transient pulses to pass through the device without getting current limited. If the overcurrent condition persists, the C_{ITIMER} continues to discharge and once it discharges by ΔV_{ITIMER}, the current limit starts regulating the HFET to actively limit the current to the set overcurrent threshold (I_{LIM}). At the same time, the C_{ITIMER} is charged up to V_{INT} again so that it is at its default state before the next overcurrent event. This ensures the full blanking timer interval is provided for every overcurrent event. Equation 5 can be used to calculate the R_{ILM} value for a desired overcurrent threshold.

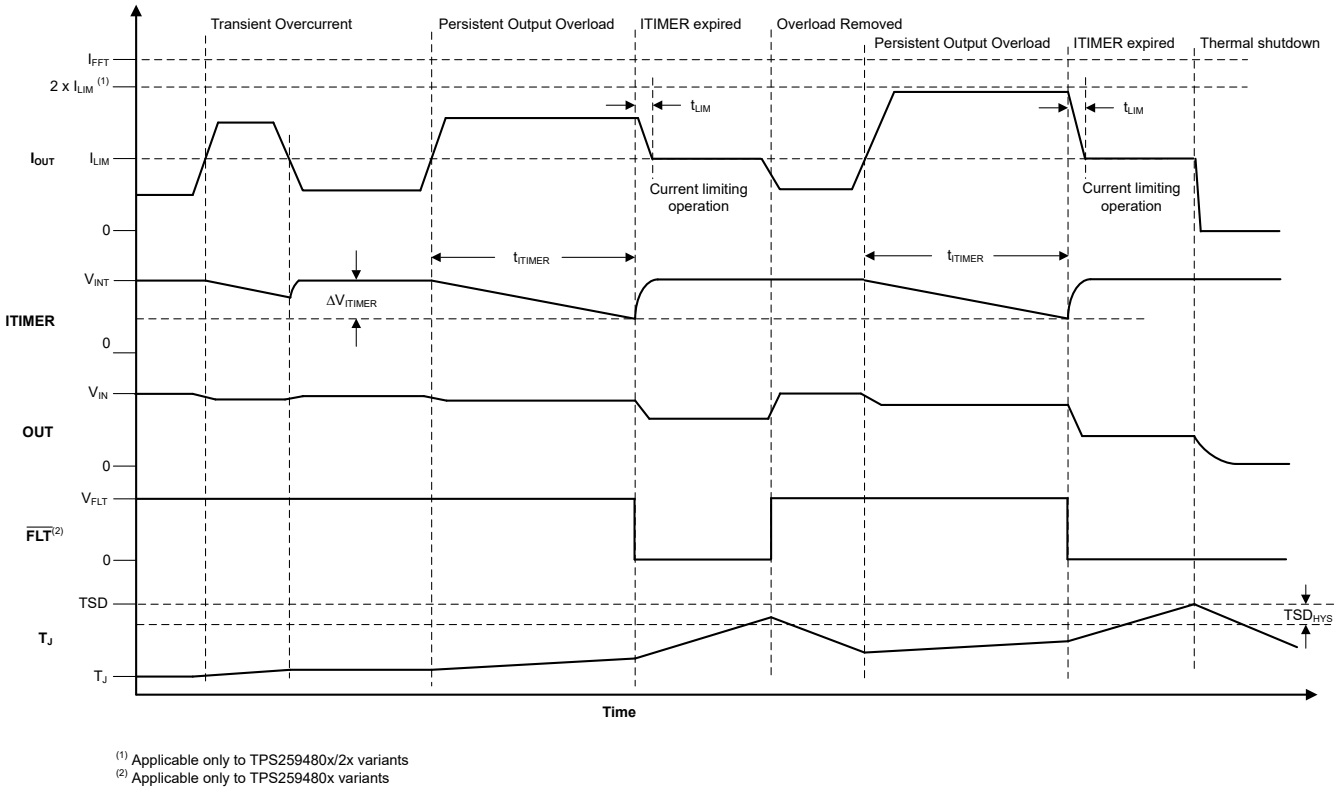
$$\text{RILM } (\Omega) = \frac{4834}{\text{ILIM (A)}} \quad (5)$$

Note

1. The TPS259480x/2x variants allow a maximum transient load current up to 2 × I_{LIM} for the ITIMER duration. The TPS259481x/3x variants allow a maximum transient load current up to I_{FFT} for the ITIMER duration.
2. Leaving the ILM pin Open sets the current limit to zero and results in the part entering current limit or performing a fast-trip with the slightest amount of loading at the output.
3. The current limit circuit employs a foldback mechanism. The current limit threshold in the foldback region (0V < V_{OUT} < V_{FB}) is lower than the steady state current limit threshold (I_{LIM}).
4. Shorting the ILM pin to ground at any point during normal operation is detected as a fault and the part shuts down. There's a minimum current (I_{FLT}) which the part allows in this condition before the pin short condition is detected.

The duration for which transients are allowed can be adjusted using an appropriate capacitor value from ITIMER pin to ground. The C_{ITIMER} value needed to set the desired transient overcurrent blanking interval can be calculated using Equation 6.

$$\text{CITIMER (nF)} = \frac{\text{tITIMER (ms)} \times \text{IITIMER (µA)}}{\Delta\text{VITIMER (V)}} \quad (6)$$



(1) Applicable only to TPS259480x/2x variants
(2) Applicable only to TPS259480x variants

Figure 7-7. TPS25948xx Active Current Limit Response

Note

1. Leave the ITIMER pin open to allow the part to limit the current with the minimum possible delay.
2. Shorting the ITIMER pin to ground results in minimum overcurrent response delay (similar to ITIMER pin open condition), but increases the device current consumption. This is not a recommended mode of operation.
3. Active current limiting based on R_{ILM} is active during startup. In case the startup current exceeds I_{LIM}, the device regulates the current to the set limit. However, during startup the current limit is engaged without waiting for the ITIMER delay.
4. Increasing the C_{ITIMER} value extends the overcurrent blanking interval, but it also extends the time needed for the C_{ITIMER} to recharge up to V_{INT}. If the next overcurrent event occurs before the C_{ITIMER} is recharged fully, it will take lesser time to discharge to the ITIMER expiry threshold, thereby providing a shorter blanking interval than intended.

During active current limit, the output voltage will drop resulting in increased device power dissipation across the HFET. If the device internal temperature (T_J) exceeds the thermal shutdown threshold (TSD), the HFET is turned off. Once the part shuts down due to TSD fault, it would either stay latched off (TPS25948xL variants) or restart automatically after a fixed delay (TPS25948xA variants). See *Overtemperature Protection (OTP)* for more details on device response to overtemperature.

7.3.3.3 Short-Circuit Protection

During an output short-circuit event, the current through the device increases very rapidly. When a severe overcurrent condition is detected, the device triggers a fast-trip response to limit the current to a safe level. For the TPS259480x/2x variants, the internal fast-trip comparator employs a scalable threshold (I_{SC} = 2 × I_{LIM}). This enables the user to adjust the fast-trip threshold rather than using a fixed threshold which can be too high for some low current systems. The device also employs a fixed fast-trip threshold (I_{FFT}) to protect fast protection against hard short-circuits during steady state. The fixed fast-trip threshold is higher than the

maximum recommended user adjustable scalable fast-trip threshold. The TPS259481x/3x variants employ only the fixed fast-trip threshold. Once the current exceeds I_{SC} or I_{FFT}, the HFET is turned off completely within t_{SC} or t_{FT}. Thereafter, the devices tries to turn the HFET back on after a short de-glitch interval (30 µs) in a current limited manner instead of a dVdt limited manner. This ensures that the HFET has a faster recovery after a transient overcurrent event and minimizes the output voltage droop. However, if the fault is persistent, the device will stay in current limit causing the junction temperature to rise and eventually enter thermal shutdown. See *Overtemperature Protection (OTP)* section for details on the device response to overtemperature.

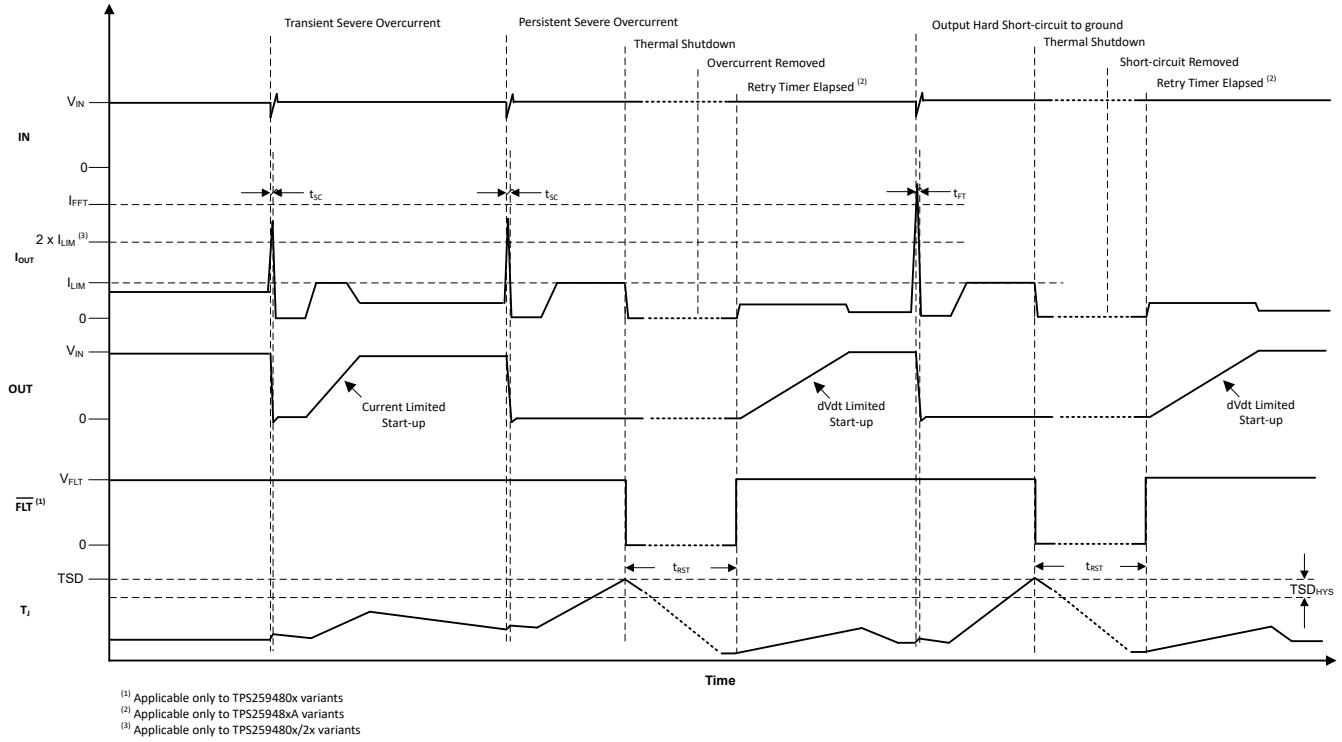


Figure 7-8. TPS259480x/2x Short-Circuit Response

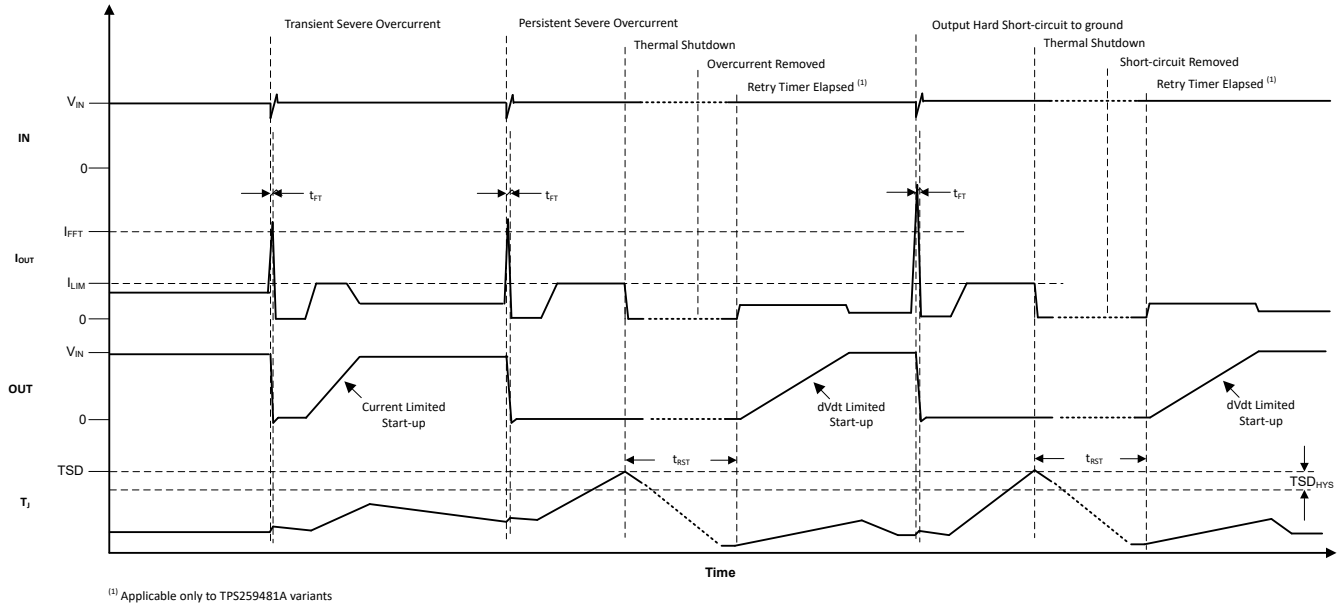
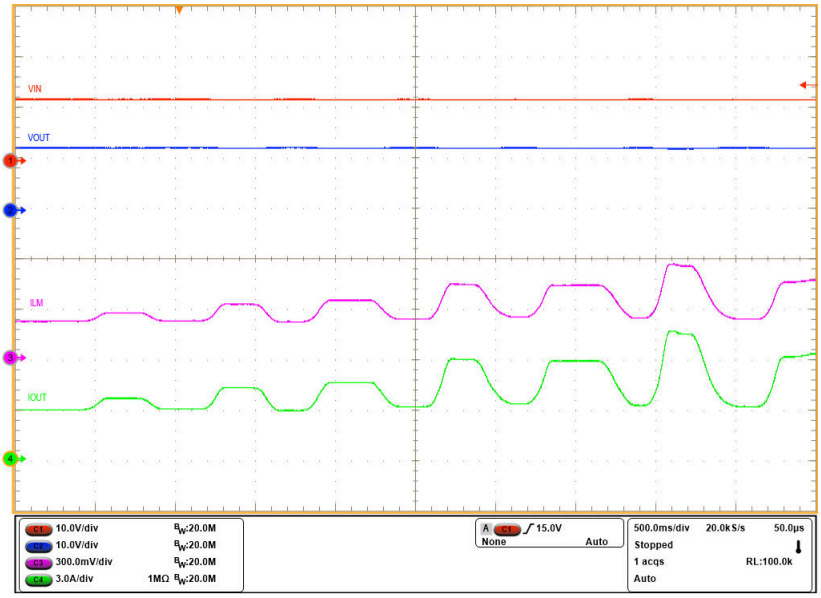


Figure 7-9. TPS259481x/3x Short-Circuit Response

7.3.4 Analog Load Current Monitor

The TPS25948xx allows the system to accurately monitor the output load current by providing an analog current sense output on the ILM pin which is proportional to the current through the FET. The user can sense the voltage (V_{ILM}) across the R_{ILM} to get a measure of the output load current.

$$\text{ILOAD (A)} = \frac{\text{VIMON (µV)}}{\text{RILM (Ω)} \times \text{GIMON (µA/A)}} \quad (7)$$



V_{IN} = 12V, C_{OUT} = 220µF, R_{ILM} = 536Ω, I_{OUT} varied dynamically between 3A and 8A

Figure 7-10. Analog Load Current Monitor Response

Note

The ILM pin is sensitive to capacitive loading. Careful design and layout is needed to ensure the parasitic capacitive loading on the ILM pin is < 50pF for stable operation.

7.3.5 Reverse Current Protection

The TPS25948xx functions like an ideal diode and blocks reverse current flow from OUT to IN under all conditions. The device has integrated back-to-back MOSFETs connected in a common drain configuration. The voltage drop between the IN and OUT pins is constantly monitored and the gate drive of the blocking FET (BFET) is adjusted as needed to regulate the forward voltage drop at V_{FWD}. This closed loop regulation scheme (linear ORing control) enables graceful turn off of the MOSFET during a reverse current event and ensures there is almost no DC reverse current flow.

The device also uses a conventional comparator (V_{REVTH}) based reverse blocking mechanism to provide fast response (t_{RCB}) to transient reverse currents. Once the device enters reverse current blocking condition, it waits for the (V_{IN} – V_{OUT}) forward drop to exceed the V_{FWDTH} before it performs a fast recovery to reach full forward conduction state. This provides sufficient hysteresis to prevent supply noise or ripple from affecting the reverse current blocking response. The recovery from reverse current blocking is very fast (t_{SWRCB}). This ensures minimum supply droop which is helpful in applications such as supply MUXing/ORing and USB Fast Role Swap (FRS).

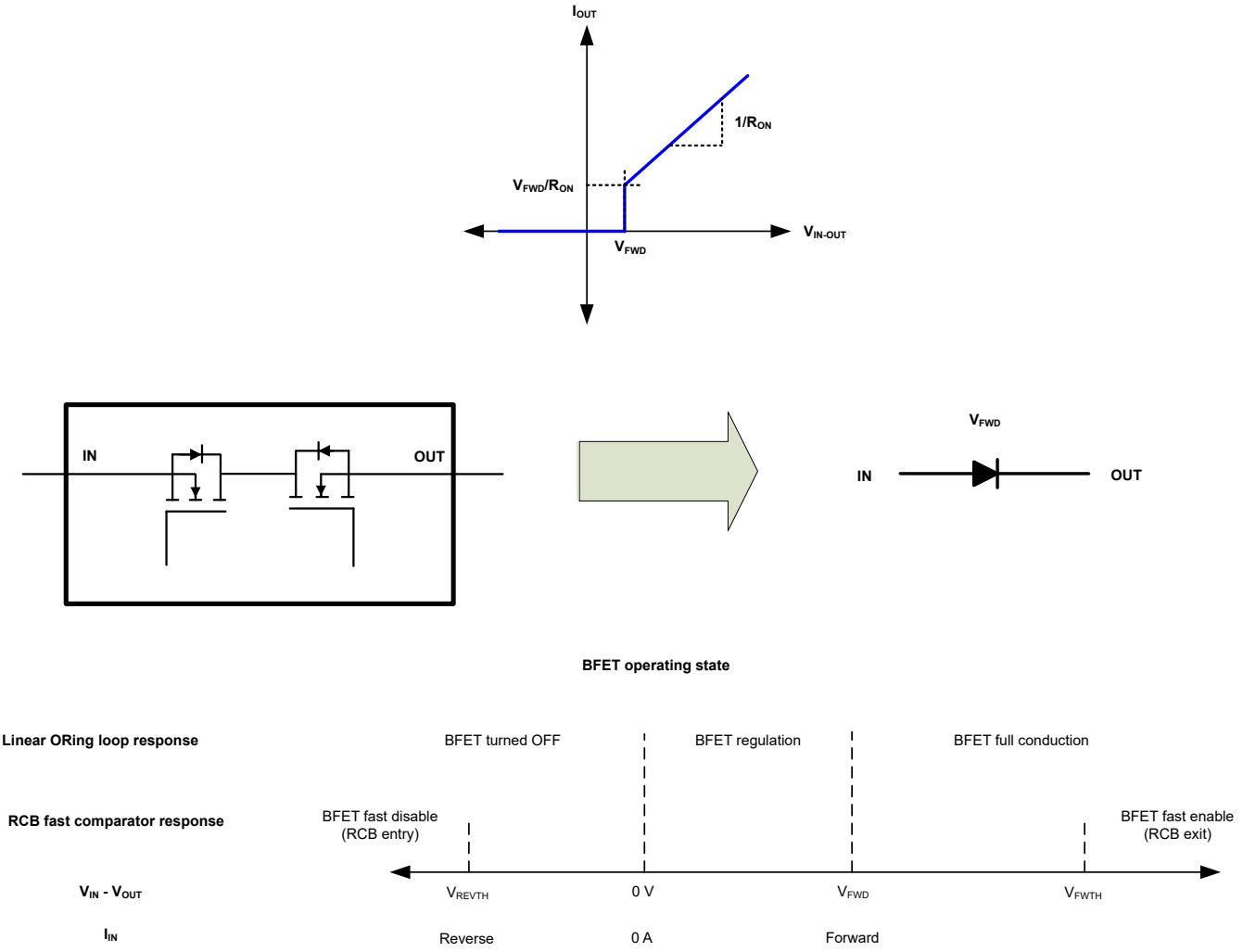


Figure 7-11. Reverse Current Blocking Response

The following waveforms illustrate the reverse current blocking performance in various scenarios.

During fast voltage step at output (for example, hot-plug), the fast comparator based reverse blocking mechanism ensures minimum jump or glitch on the input rail.

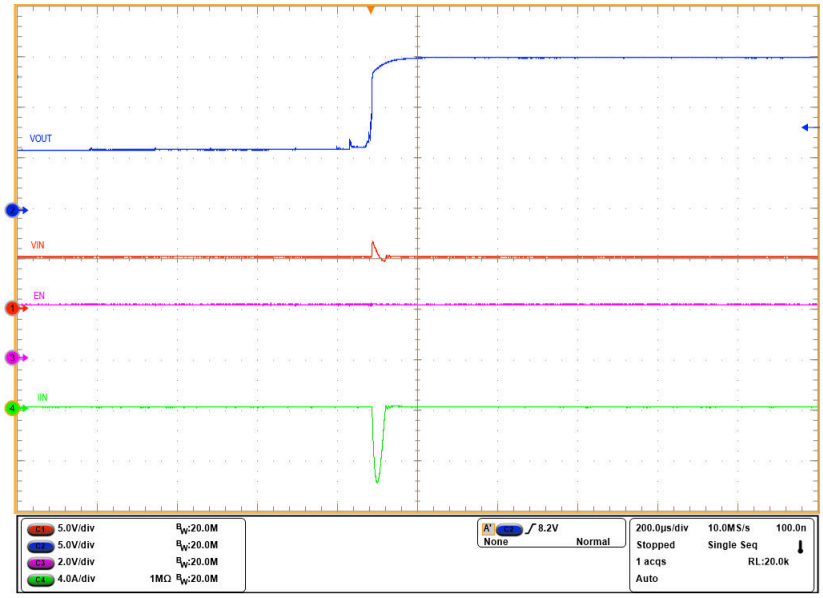


Figure 7-12. Reverse Current Blocking Performance During Fast Voltage Step at Output

During slow voltage ramp at output, the linear ORing based reverse blocking mechanism ensures there is almost no DC current flow from OUT to IN, thereby avoiding input rail from getting slowly charged up to output voltage.

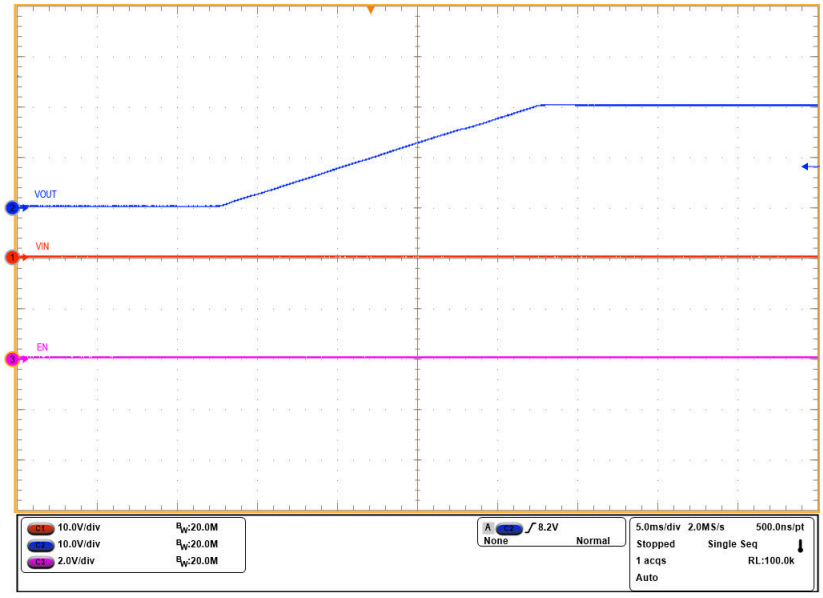


Figure 7-13. Reverse Current Blocking Performance During Slow Voltage Ramp at Output

When the input supply droops or gets disconnected while the output storage element (bulk capacitor or super capacitor) is charged to the full voltage, the linear ORing scheme minimizes the self-discharge from OUT to IN. This ensures maximum holdup time for the output storage element in critical power back-up applications.

It also prevents incorrect supply presence indication in applications which sense the input voltage to detect if the supply is connected.

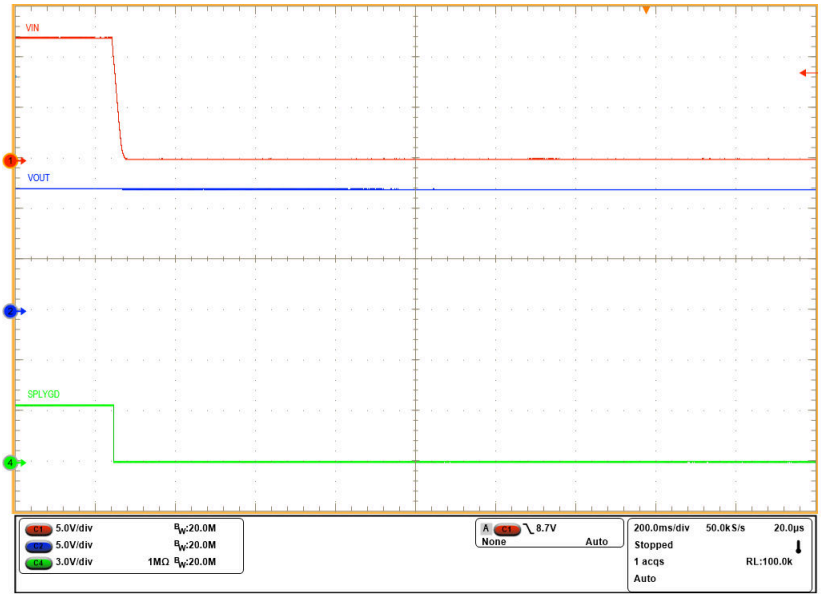


Figure 7-14. Reverse Current Blocking Performance During Input Supply Failure

The TPS259481x/2x/3x variants provide the option of disabling the reverse current blocking scheme using the RCBCTRL pin. Leaving the RCBCTRL pin floating or pulling it high enables the reverse current blocking during steady-state, while pulling the pin low disables it.

Note

RCBCTRL pin controls the reverse current blocking mechanism only during steady-state. It has no effect during disabled or fault state where the reverse current blocking is always active.

7.3.6 Overtemperature Protection (OTP)

The TPS25948xx monitors the internal die temperature (T_J) at all times and shuts down the part as soon as the temperature exceeds a safe operating level (TSD) thereby protecting the device from damage. The device will not turn back on until the junction cools down sufficiently, that is the die temperature falls below (TSD – TSD_{HYS}).

When the TPS25948xL (latch-off variant) detects thermal overload, it will be shut down and remain latched-off until the device is power cycled or re-enabled. When the TPS25948xA (auto-retry variant) detects thermal overload, it will remain off until it has cooled down by TSD_{HYS}. Thereafter, it will remain off for an additional delay of t_{RST} after which it will automatically retry to turn on if it is still enabled.

Table 7-1. Thermal Shutdown

DEVICE	ENTER TSD	EXIT TSD
TPS25948xL (Latch-Off)	$T_J \geq$ TSD	$T_J <$ TSD – TSD_{HYS} V_{IN} cycled to 0V and then above $V_{UVP(R)}$ OR EN/UVLO toggled below $V_{SD(F)}$
TPS25948xA (Auto-Retry)	$T_J \geq$ TSD	$T_J <$ TSD – TSD_{HYS} V_{IN} cycled to 0V and then above $V_{UVP(R)}$ OR EN/UVLO toggled below $V_{SD(F)}$ OR t_{RST} timer expired

7.3.7 Fault Response and Indication ($\overline{FLT}$)

The following table summarizes the device response to various fault conditions. Additionally, an active low external fault indication ($\overline{FLT}$) pin is available on the TPS259480x variants.

Table 7-2. Fault Summary

EVENT	PROTECTION RESPONSE	FAULT LATCHED INTERNALLY	$\overline{FLT}$ PIN STATUS (1)	$\overline{FLT}$ ASSERTION DELAY(1)
Overtemperature	Shutdown	Y	L	
Undervoltage (UVP or UVLO)	Shutdown	N	H	
Input Overvoltage	Shutdown	N	H	
Transient Overcurrent (I_{LIM} < I_{OUT} < 2 × I_{LIM} or I_{FFT} for duration less than t_{ITIMER})	None	N	H	
Persistent Overcurrent	Current Limit	N	L	t_{ITIMER}
Output Short-Circuit to GND	Circuit Breaker followed by Current Limit	N	H	
ILM Pin Open (During Steady State)	Shutdown	N	H	
ILM Pin Shorted to GND	Shutdown	Y	L	
Reverse Current ((V_{OUT} - V_{IN}) > V_{REVTH})	Reverse Current Blocking	N	H	

(1) Applicable to TPS259480x variants only.

Faults which are latched internally can be cleared either by power cycling the part (pulling V_{IN} to 0V) or by pulling the EN/UVLO pin voltage below $V_{SD(F)}$. This also releases the $\overline{FLT}$ pin pull-down for the TPS259480x variants and resets the t_{RST} timer for the TPS25948xA (auto-retry) variants.

During a latched fault, pulling the EN/UVLO just below the UVLO threshold has no impact on the device. This is true for both TPS25948xL (latch-off) and TPS25948xA (auto-retry) variants.

For TPS25948xA (auto-retry) variants, on expiry of the t_{RST} timer after a fault, the device restarts automatically and the $\overline{FLT}$ pin is de-asserted (TPS259480A variant).

7.3.8 Supply Good Indication (SPLYGD/$\overline{SPLYGD}$)

The TPS25948xx provides a digital output (SPLYGD/$\overline{SPLYGD}$) which is asserted to indicate when the priority input supply is in a valid range (above UVP/UVLO and below OVLO thresholds) and the device has successfully completed its inrush sequence. The SPLYGD/$\overline{SPLYGD}$ pin is an open-drain signal which needs to be pulled up to an external supply. For the TPS259480x/2x/3x variants, SPLYGD is an active high output. For the TPS259481x variant, $\overline{SPLYGD}$ is an active low output.

After power up, SPLYGD/$\overline{SPLYGD}$ pin is de-asserted initially. The device initiates a inrush sequence in which the HFET is turned on in a controlled manner. When the FET gate voltage has reached the full overdrive indicating that the inrush sequence is complete and device is capable of delivering full power, the SPLYGD/$\overline{SPLYGD}$ pin is asserted. Thereafter, the SPLYGD/$\overline{SPLYGD}$ pin is de-asserted only if the input supply becomes invalid (below UVP/UVLO or above OVLO thresholds). No load side events/faults have any control over the SPLYGD/$\overline{SPLYGD}$ de-assertion.

This pin is used to control the auxiliary channel when two TPS25948xx devices are connected in a priority power MUX configuration. It can also be used as a supply valid status indication to the downstream load or system supervisor.

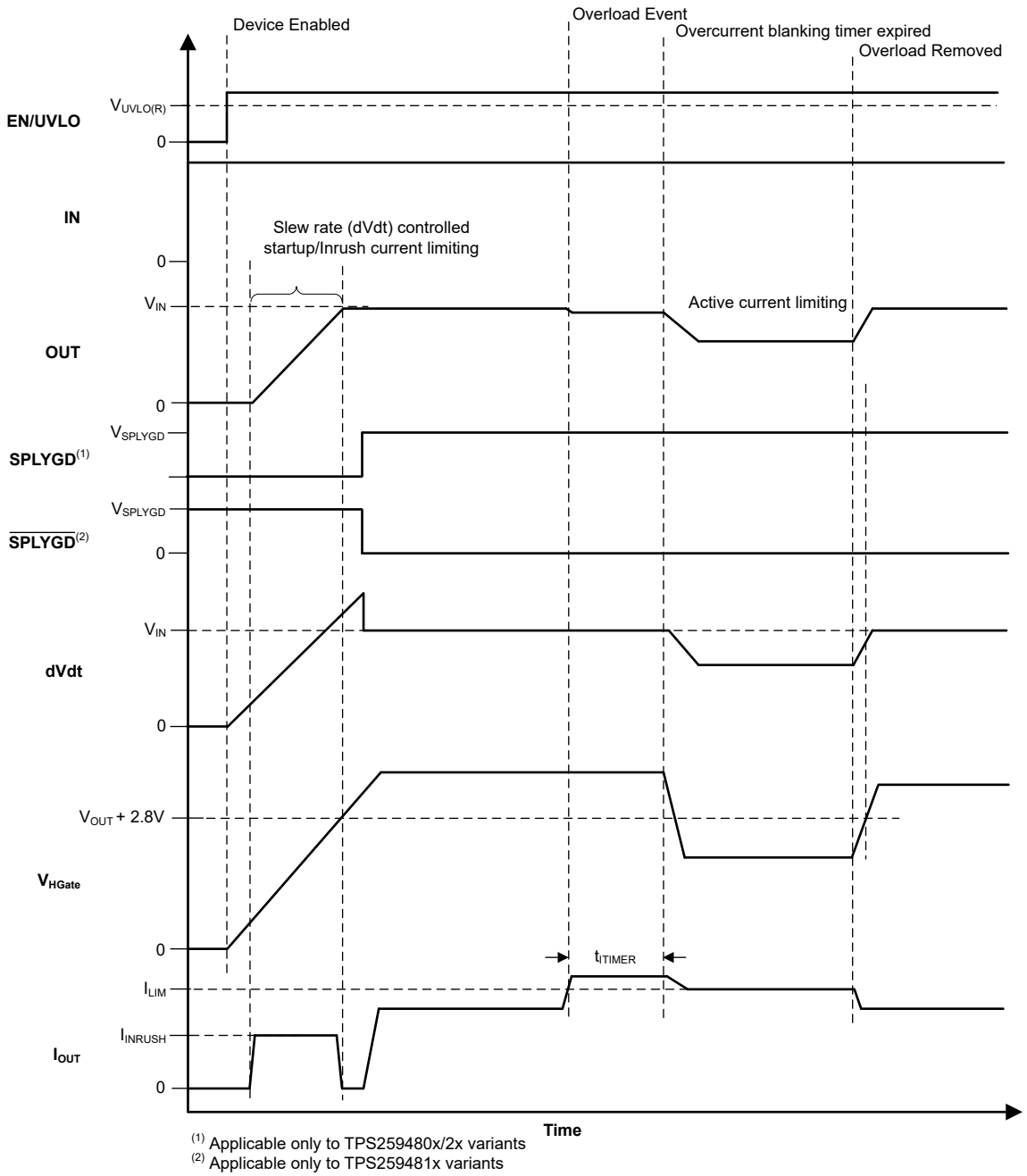


Figure 7-15. TPS25948xx SPLYGD Behavior

Table 7-3. TPS25948xx SPLYGD/$\overline{\text{SPLYGD}}$ Indication Summary

EVENT/CONDITION	SPLYGD PIN(1)	$\overline{\text{SPLYGD}}$ PIN(2)
Supply Brownout (UVP)	L	L
Shutdown (EN < V_{SD})	L	L
Undervoltage (UVLO)	L	H
Overvoltage (OVLO)	L	H
Inrush	L	H
Steady State	H	L
Overcurrent	H	L
Short-Circuit	H	L
ILM Pin Open	H	L
ILM Pin Shorted to GND	H	L
Reverse current ((V_{OUT} – V_{IN}) > V_{REVTH})	H	L
Overtemperature	H	L

(1) Applicable only to TPS259480x/2x/3x variants.
(2) Applicable only to TPS259481x variants.

When there is no supply to the device, the SPLYGD pin is expected to stay low. However, there is no active pull-down in this condition to drive this pin all the way down to 0V. If the SPLYGD pin is pulled up to an independent supply which is present even if the device is unpowered, there can be a small voltage seen on this pin depending on the pin sink current, which is a function of the pull-up supply voltage and resistor. Minimize the sink current to keep this pin voltage low enough not to be detected as a logic HIGH by associated external circuits in this condition. This also ensures that the auxiliary channel is not turned off inadvertently in a priority power MUX configuration.

7.4 Device Functional Modes

Table 7-4. TPS259481x/2x/3x Reverse Current Blocking Operation

RCBCTRL PIN CONNECTION	REVERSE CURRENT BLOCKING IN STEADY-STATE
Low	Disabled
Open or High	Enabled

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS25948x is a 3.5V to 23V, 8A eFuse that is typically used for power rail protection applications. It operates from 3.5V to 23V with adjustable overvoltage and undervoltage protection. It provides ability to control inrush current and protection against reverse current conditions. It can be used in a variety of systems such as adapter or charger input protection, USB PD protection in smartphone, tablet, PC, notebook, monitor, dock, server and PC motherboard, add-on cards, enterprise storage – RAID/HBA/SAN/eSSD, power MUXing/ ORing. The design procedure explained in the subsequent sections can be used to select the supporting component values based on the application requirement. Additionally, a spreadsheet design tool TPS25948x Design Calculator is available in the web product folder.

8.2 Single Device, Self-Controlled

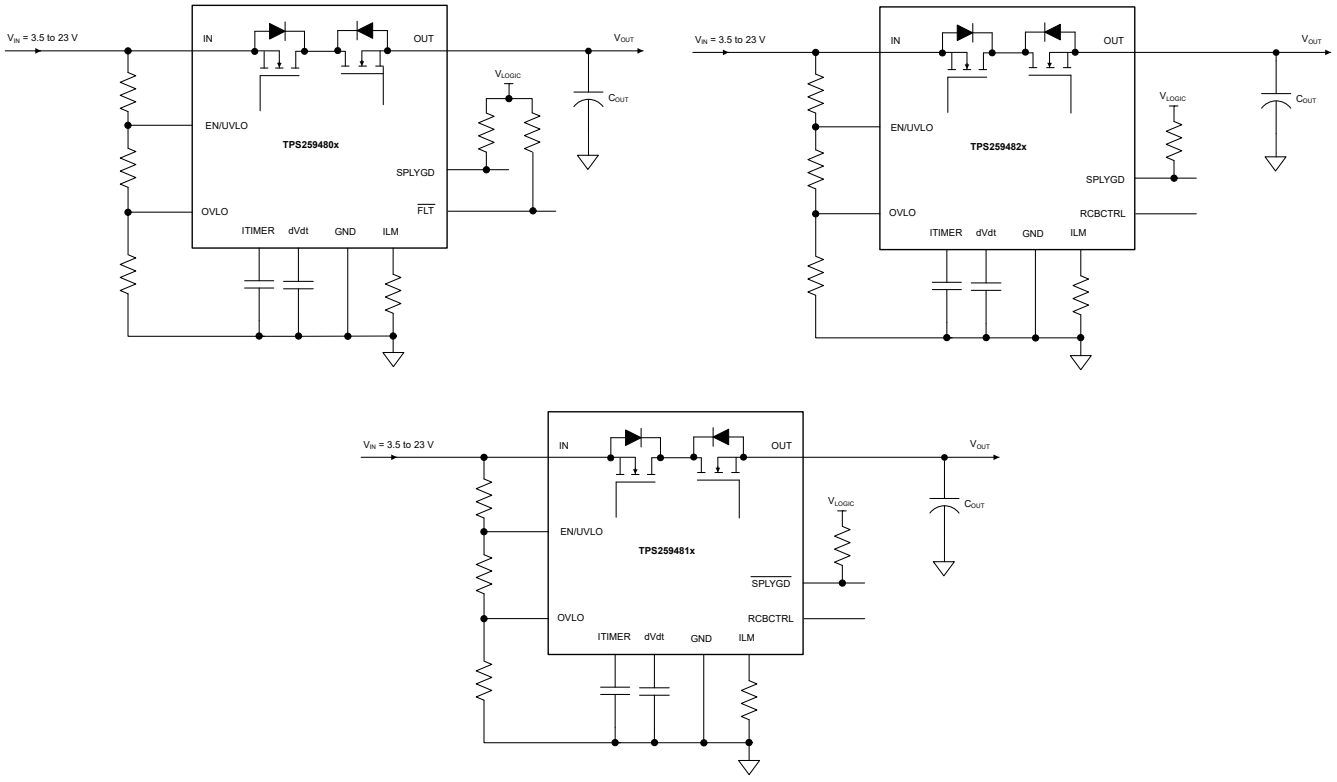


Figure 8-1. Single Device, Self-Controlled

Other variations:

In a Host MCU controlled system, EN/UVLO or OVLO can also be driven from the host GPIO to control the device.

ILM pin can be connected to the MCU ADC input for current monitoring purpose.

Note

It is recommended to keep parasitic capacitance on ILM pin below 50pF to ensure stable operation.

8.3 Typical Application

Smartphones come equipped with USB OTG functionality that allows their USB port to be used not only for charging the phone battery but also allow the smartphone to act as a USB host and deliver power to external accessories such as headphones, pen drives, and so forth. Some smartphones also support a wireless charging path which can also be used to wirelessly share power to other devices. TPS259482x can be used as a bi-directional power switch in such applications as shown in Figure 8-3. For the USB power path, when an external charger is connected at the port, TPS259482x provides a conduction path from IN pin to OUT pin and the battery charger IC is configured to charge the battery and also power the internal circuits. TPS259482x also provides overvoltage and overcurrent protection in this case. In another use case scenario where an accessory such as headphone is connected to the USB port, the phone MCU detects this and the battery charger is configured in OTG boost mode to provide power from battery to the USB port. MCU will also pull down RCBCTRL pin to allow current flow from OUT pin to IN pin of TPS259482x and enables the TPS259482x and establishes a low impedance power path capable of delivering high power to the accessory. Similarly, the TPS259482x also provides controlled bi-directional power flow in the wireless charging and power share sub-system.

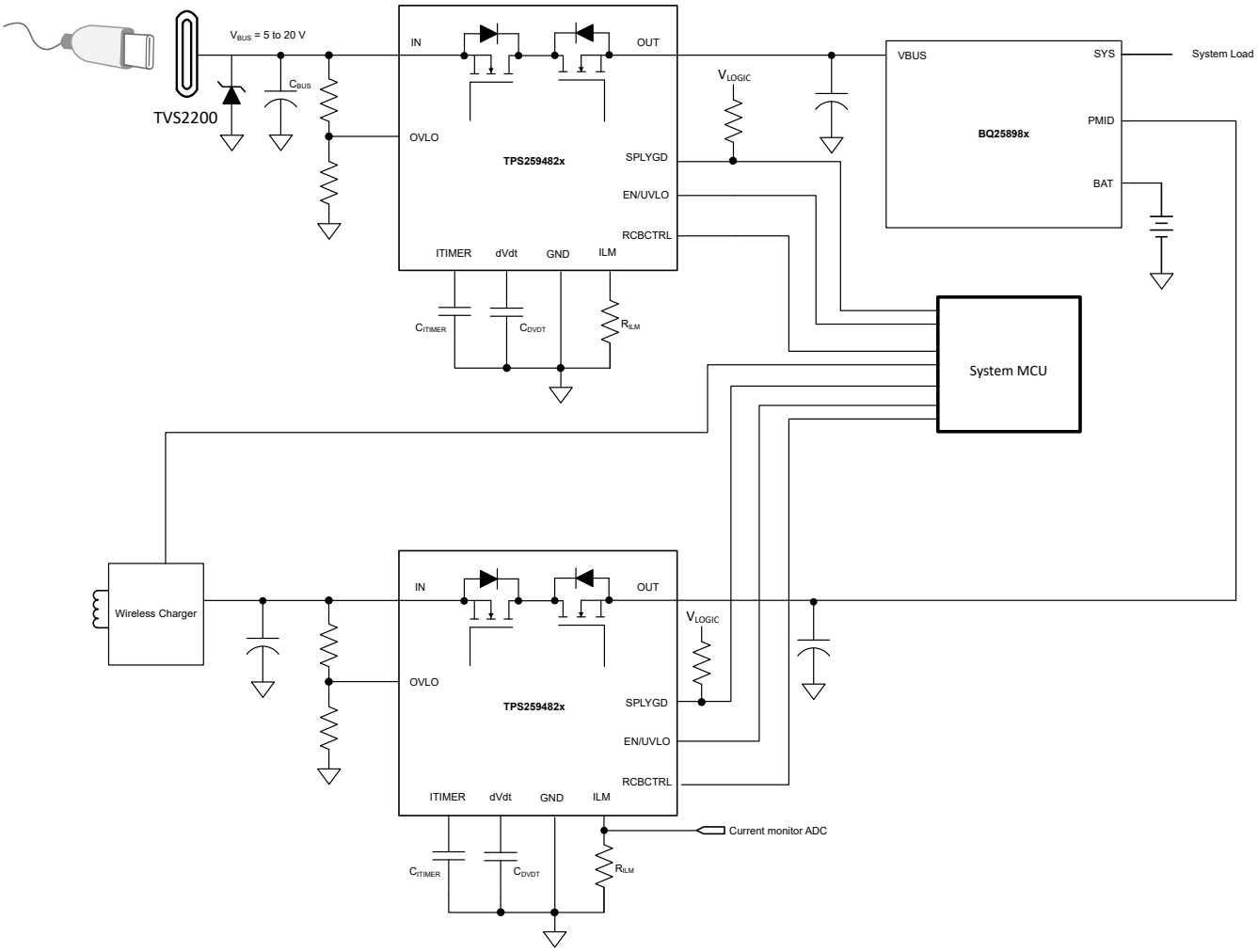
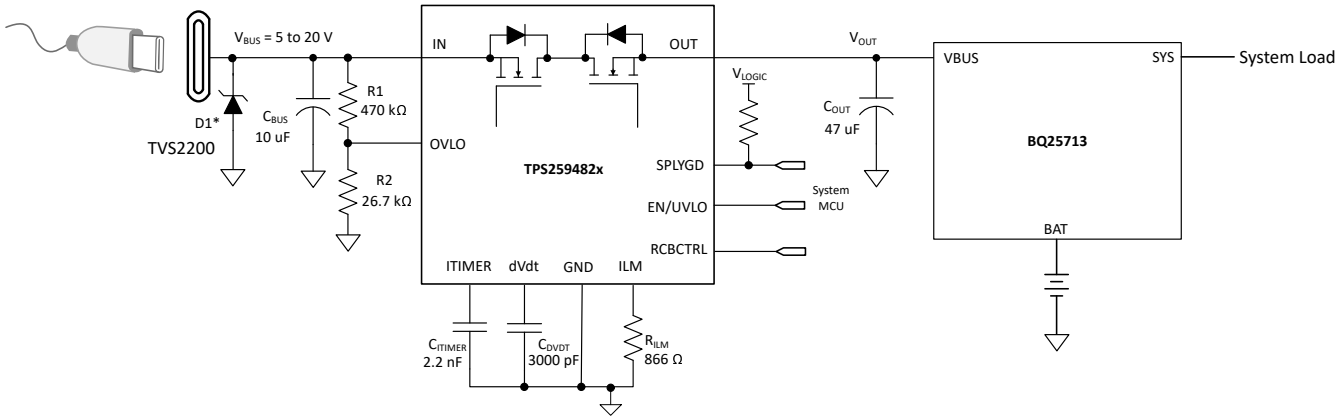


Figure 8-2. Smartphone Power Path Example



* Optional circuit components needed for transient protection depending on input and output inductance. Please refer to *Transient Protection* section for details.

Figure 8-3. USB On-The-Go Port Protection Design Example

8.3.1 Design Requirements

Table 8-1. Design Parameters

PARAMETER	VALUE
Bus voltage during charging (V_{IN})	20V
Overvoltage protection threshold during charging ($V_{IN(OV)}$)	22V
Max continuous charging current	5A
Load transient blanking interval during charging (t_{ITIMER})	2ms
Output capacitance (C_{OUT})	47µF
Output rise time (t_R)	12ms
Overcurrent threshold (I_{LIM}) during charging	5.5A

8.3.2 Detailed Design Procedure

8.3.2.1 Setting Overvoltage Threshold

The supply overvoltage threshold is set using the resistors, R1 and R2, whose values can be calculated as:

$$VIN(OV) = \frac{VOV(R) \times (R1 + R2)}{R2} \quad (8)$$

Where $V_{OV(R)}$ is the OVLO rising threshold. Because R1, R2 leak the current from input supply V_{IN}, these resistors must be selected based on the acceptable leakage current from input power supply V_{IN}. The current drawn by R1, R2 from the power supply is IR12 = V_{IN} / (R1 + R2). However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, IR12, must be chosen to be 20 times greater than the leakage current expected on the OVLO pin.

From the device electrical specifications, OVLO leakage current is 0.1µA (maximum), $V_{OV(R)}$ = 1.2V. From design requirements, $V_{IN(OV)}$ = 22V. To solve the equation, first choose the value of R1 = 470kΩ and use the above equation to solve for R2 = 27.11kΩ.

Using the closest standard 1% resistor values, we get R1 = 470kΩ, R2 = 26.7kΩ.

8.3.2.2 Setting Output Voltage Rise Time (t_R)

For a successful design, the junction temperature of device must be kept below the absolute maximum rating during both dynamic (start-up) and steady-state conditions. Dynamic power stresses often are an order of

magnitude greater than the static stresses, so it is important to determine the right start-up time and inrush current limit required with system capacitance to avoid thermal shutdown during start-up.

The slew rate (SR) needed to achieve the desired output rise time can be calculated as:

$$\text{SR (V/ms)} = \frac{\text{VIN (V)}}{\text{tR (ms)}} = \frac{20\text{ V}}{12\text{ ms}} = 1.67\text{ V/ms} \quad (9)$$

The C_{dVdt} needed to achieve this slew rate can be calculated as:

$$\text{CdVdt (pF)} = \frac{5000}{\text{SR (V/ms)}} = \frac{5000}{1.67} = 2994\text{ pF} \quad (10)$$

Choose the nearest standard capacitor value as 3000pF.

For this slew rate, the inrush current can be calculated as:

$$\text{IINRUSH (mA)} = \text{SR (V/ms)} \times \text{COUT (µF)} = 1.67 \times 47 = 79\text{ mA} \quad (11)$$

The average power dissipation inside the part during inrush can be calculated as:

$$\text{PDINRUSH (W)} = \frac{\text{IINRUSH (A)} \times \text{VIN (V)}}{2} = \frac{0.079 \times 20}{2} = 0.8\text{ W} \quad (12)$$

For the given power dissipation, the thermal shutdown time of the device must be greater than the ramp-up time t_R to avoid start-up failure. Figure 8-4 shows the thermal shutdown limit, for 0.8W of power, the shutdown time is more than 10s which is very large as compared to t_R = 12ms. Therefore, it is safe to use 12ms as the startup time for this application.

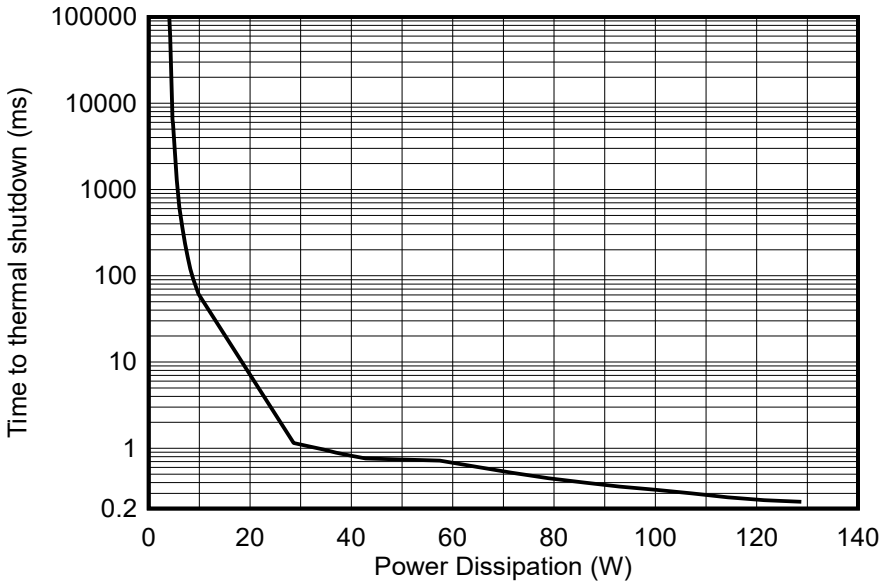


Figure 8-4. Thermal Shut-Down Plot During Inrush

8.3.2.3 Setting Overcurrent Threshold (I_{LIM})

The overcurrent protection threshold can be set using the R_{ILM} resistor whose value can be calculated as:

$$\text{RILM (Ω)} = \frac{4834}{\text{ILIM (A)}} = \frac{4834}{5.5\text{ A}} = 879\text{ Ω} \quad (13)$$

Choose nearest 1% standard resistor value as 866Ω.

8.3.2.4 Setting Overcurrent Blanking Interval (t_{ITIMER})

The overcurrent blanking timer interval can be set using the C_{ITIMER} capacitor whose value can be calculated as:

$$\text{CITIMER (nF)} = \frac{\text{tITIMER (ms) x IITIMER (µA)}}{\Delta\,\text{VITIMER (V)}} = \frac{2 \text{ x } 1.9}{1.51} = 2.51 \text{ nF} \quad (14)$$

Choose nearest standard capacitor value as 2.2nF.

8.3.3 Application Curves

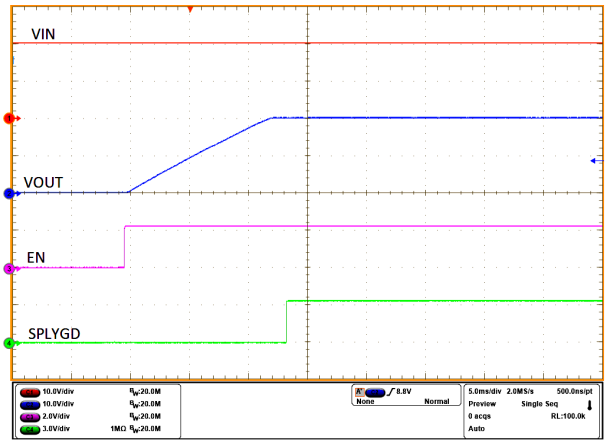


Figure 8-5. Power Up

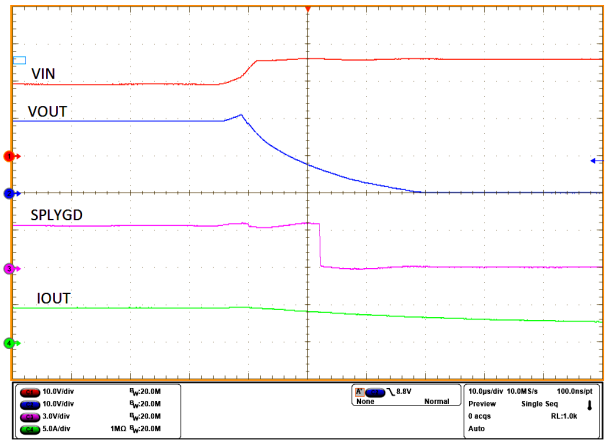


Figure 8-6. Overvoltage Protection

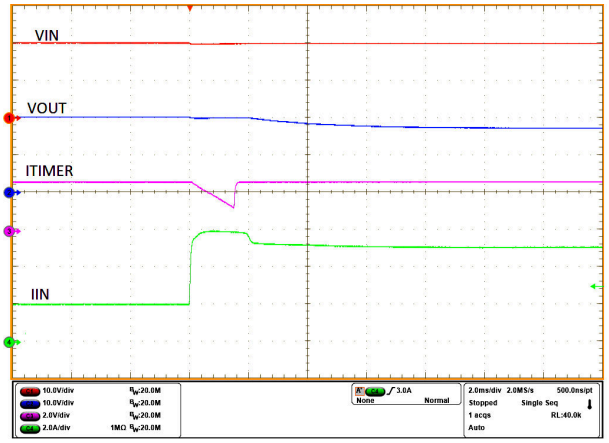


Figure 8-7. Overcurrent Protection

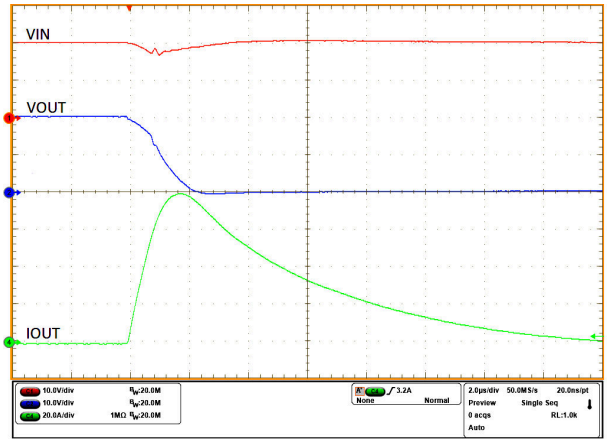


Figure 8-8. Short at Output Protection

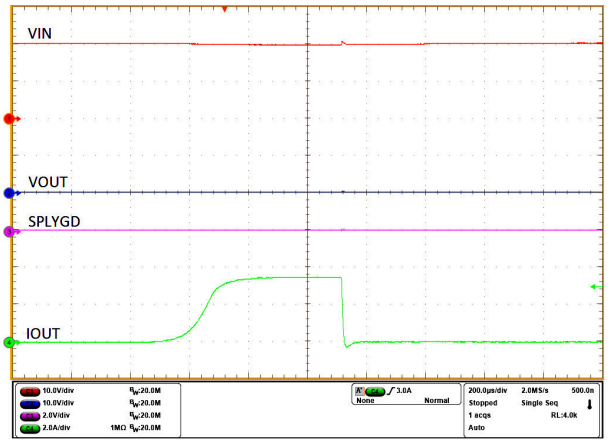


Figure 8-9. Wake up into Short Protection

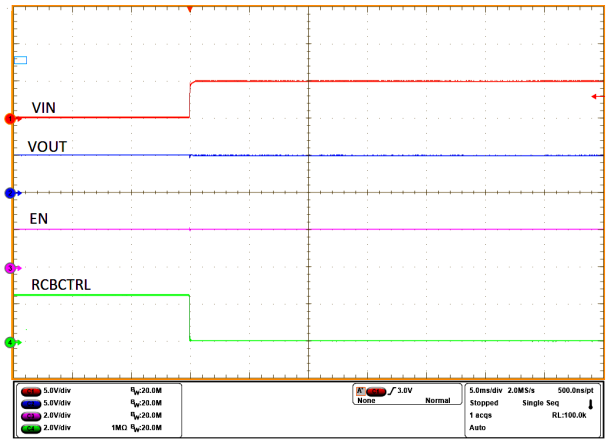


Figure 8-10. Power Up in OTG Mode

8.4 Active ORing

A typical redundant power supply configuration is shown in Figure 8-11 below. Schottky ORing diodes have been popular for connecting parallel power supplies, such as parallel operation of wall adapter with a battery or a hold-up storage capacitor. The disadvantage of using ORing diodes is high voltage drop and associated power loss. The TPS25948xx with integrated, low-ohmic, back-to-back FETs provide a simple and efficient solution. Figure 8-11 below shows the Active ORing implementation using TPS259480x devices.

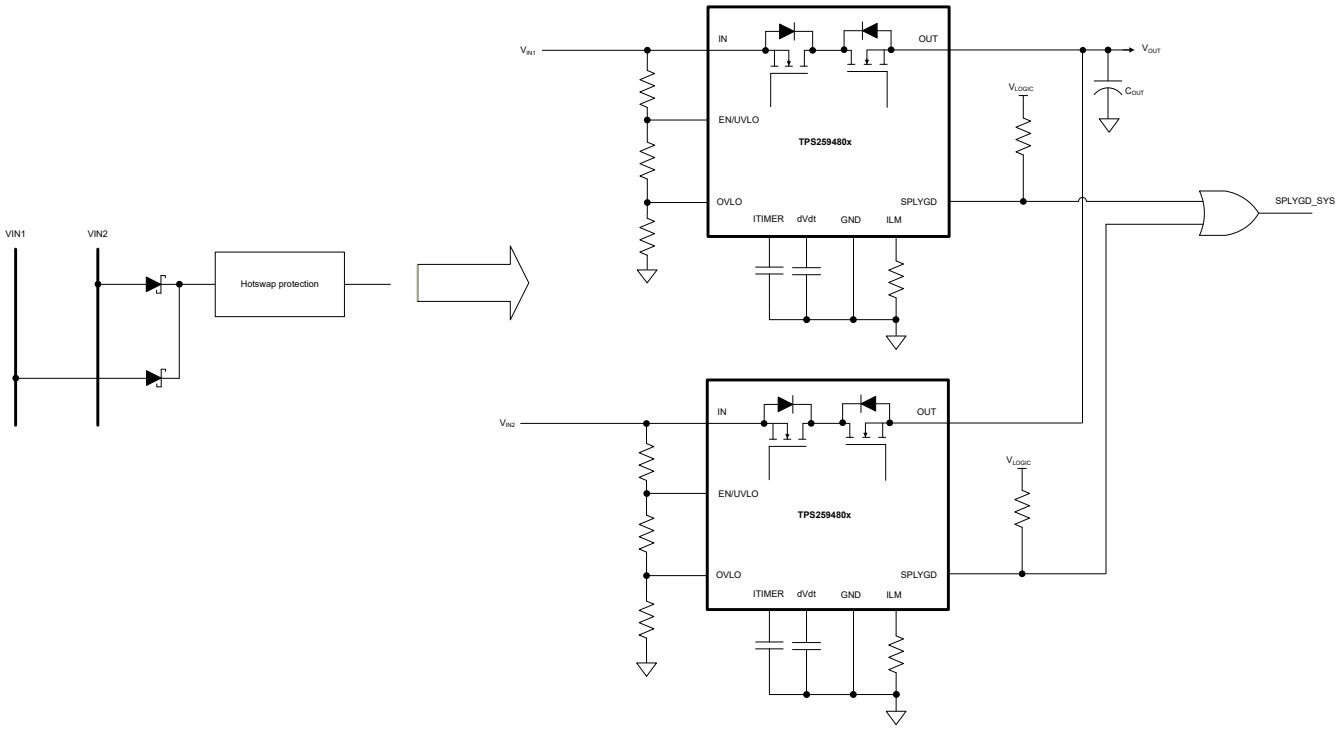


Figure 8-11. Two Devices, Active ORing Configuration

The linear ORing mechanism in TPS25948xx ensures that there's no reverse current flowing from one power source to the other during fast or slow ramp of either supply.

The following waveform illustrates the active ORing behavior when the supply rails are being ramped up sequentially.

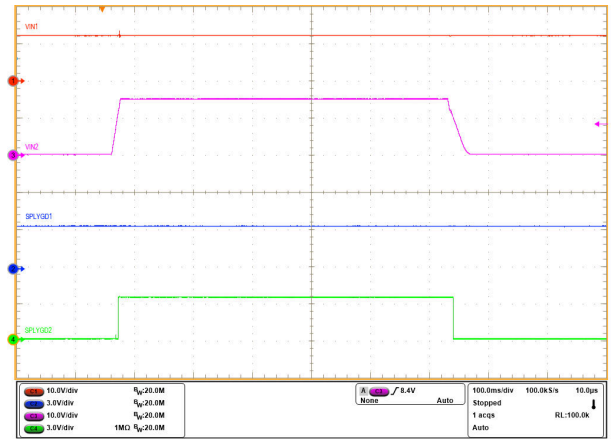


Figure 8-12. Active ORing Response

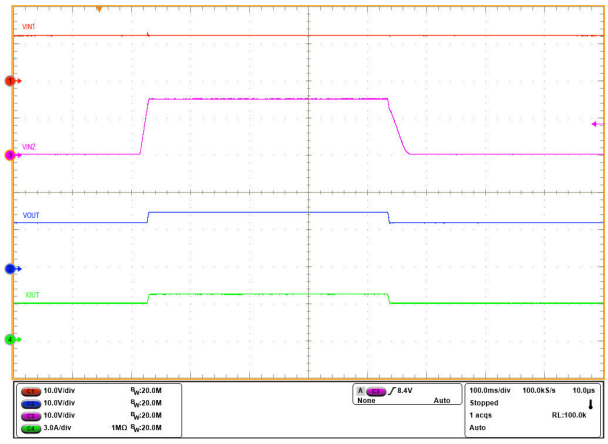


Figure 8-13. Active ORing Response

When the bus voltages (IN1 and IN2) are matched, device in each path sees a forward voltage drop and is ON delivering the load current. During this period, current is shared between the rails in the ratio of differential voltage drop across each device.

In addition to supply ORing, the devices protect the system from overvoltage, excessive inrush current, overload and short-circuit faults at all times.

Note

ORing can be done either between two similar rails or between dissimilar rails. For ORing cases with skewed voltage combinations, the dVdt pin capacitor rating should be chosen based on the highest of the 2 supplies. Refer to Recommended Operating Conditions table for more details.

8.5 Priority Power MUXing

Applications having two energy sources such as PCIe cards, Tablets and Portable battery powered equipment require preference of one source to another. For example, mains power (wall-adapter) has the priority over the internal battery back-up power. These applications demand for switchover from mains power to backup power only when main input voltage falls below a user defined threshold. The TPS25948xx devices provide a simple solution for priority power multiplexing needs.

Figure 8-14 shows a typical priority power multiplexing implementation using TPS259480x devices. When primary (priority) power source (IN1) is present and within the valid range (not in UV/OV condition), the primary path device path powers the OUT bus irrespective of whether auxiliary supply voltage (V_{IN2}) is greater than, equal to or less than primary supply voltage (V_{IN1}). The device in auxiliary path is held in off condition by forcing its OVLO pin to high using the SPLYGD signal from the primary path device.

Once the primary supply voltage falls outside the user-defined valid operating range (UV/OV condition), the primary path device de-asserts the SPLYGD which signals the auxiliary path device to turn on and the system starts operating from the auxiliary supply. During this transition, the auxiliary path device bypasses its dVdt limited startup and performs a fast recovery to start delivering power within t_{SWOV}.

When the primary supply is restored, the primary path device turns on fully at a defined slew rate and then asserts its SPLYGD pin high to turn the auxiliary path device off, allowing a seamless transition from auxiliary to the primary supply with minimal output voltage droop and with no shoot-through current.

A key consideration in power MUXing applications is the minimum voltage the output bus droops to during the switchover from one supply to another. This in turn depends on multiple factors including the output load current (I_{LOAD}), output bus hold-up capacitance (C_{OUT}) and switchover time (t_{SW}).

While switching from primary supply (V_{IN1}) to auxiliary supply (V_{IN2}), the minimum bus voltage can be calculated using Equation 15. Here, the switchover time (t_{SW}) is equal to the fast OVLO recovery time (t_{SWOV}) taken by the TPS259480x variants to turn on fully and start delivering current to the load.

$$\text{VOUT,min (V)} = \min(\text{VIN1, VIN2}) - \frac{\text{tSW (µs)} \times \text{ILOAD (A)}}{\text{COUT (µF)}} \quad (15)$$

While switching from auxiliary supply (V_{IN2}) to primary supply (V_{IN1}), the minimum bus voltage can be calculated using Equation 16. Here the maximum switchover time is equal to the RCB recovery time (t_{SWRCB}), depending on whether V_{IN1} is equal to or lower than V_{IN2} to start with.

$$\text{VOUT,min (V)} = \min(\text{VIN1, VIN2}) - \text{VFWDTH (V)} - \frac{\text{tSWRCB (µs)} \times \text{ILOAD (A)}}{\text{COUT (µF)}} \quad (16)$$

The SPLYGD pins of the devices can be used as a digital indication to identify which of the two supplies is active and delivering power to the load.

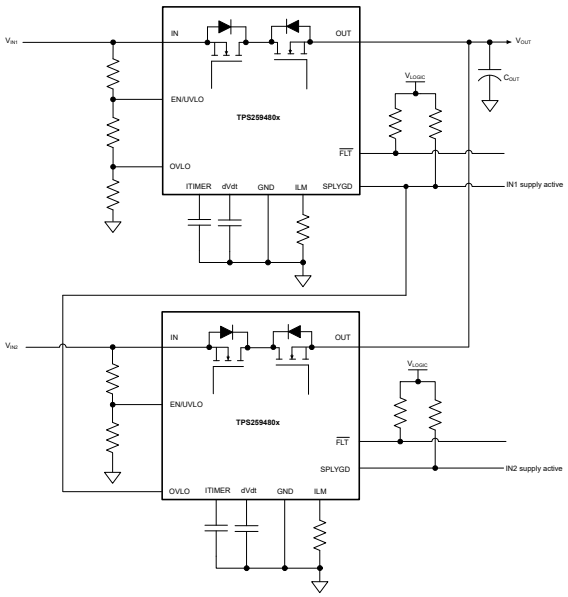


Figure 8-14. Priority Power MUXing With 2 × TPS259480x - Option 1

This configuration provides the most compact priority power MUXing solution with multiple benefits, including active current limit protection on both channels as well as overvoltage protection on primary channel. It also provides the fastest switchover time from primary to auxiliary, but at the cost of a slightly increased quiescent current on the auxiliary path while primary path is active. Also, it uses the fewest external components, but at the cost of bypassing overvoltage protection on auxiliary channel.

The following waveforms illustrate the TPS259480x performance in a priority power MUXing configuration.

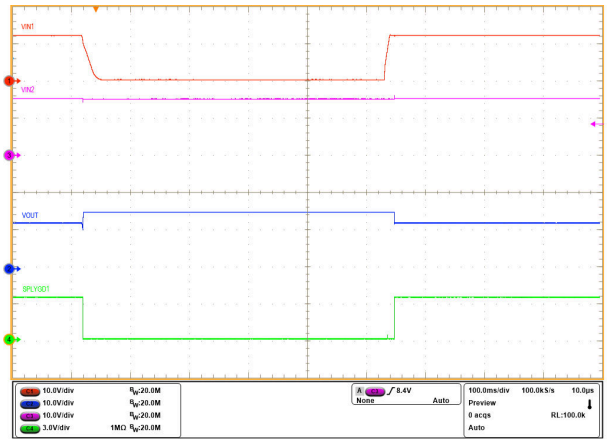


Figure 8-15. TPS259480x Power MUX - Switchover Between Primary and Auxiliary Supplies

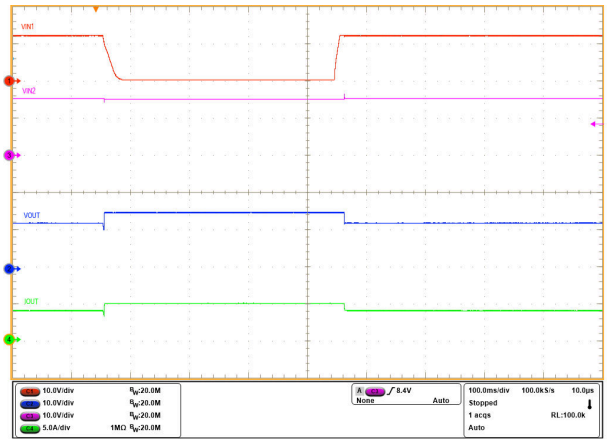


Figure 8-16. TPS259480x Power MUX - Switchover Between Primary and Auxiliary Supplies

There is a possible variation to the above configuration in case overvoltage protection is needed on both channels. This needs an additional signal N-FET to drive the OVLO pin of the auxiliary path device as shown in Figure 8-17. The switchover times are similar to the previous configuration.

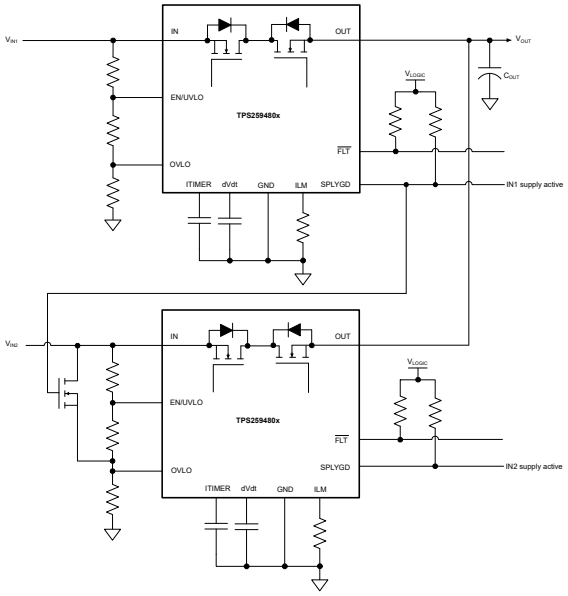


Figure 8-17. Priority Power MUXing With 2 × TPS259480x - Option 2

Another variation of the previous configuration ensures minimum quiescent current on the auxiliary channel while primary channel is active, but at the cost of additional N-FET to drive the EN/UVLO pin of auxiliary path device as shown in Figure 8-18. At the same time, it has a higher switchover delay from primary to auxiliary supply as compared to the previous configuration.

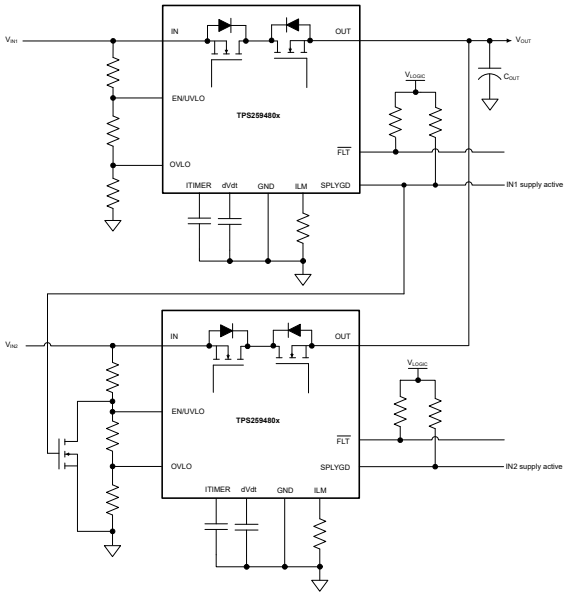


Figure 8-18. Priority Power MUXing With 2 × TPS259480x - Option 3

While switching from a higher supply rail to lower supply rail, the minimum bus voltage can be calculated using Equation 17. Here, the switchover time is equal to the time taken by the device to come out of reverse current blocking state (t_{SWRCB}).

$$\text{VOUT,min (V)} = \min(\text{VIN1, VIN2}) - \text{VFWDTH (V)} - \frac{\text{tSWRCB (µs)} \times \text{ILOAD (A)}}{\text{COUT (µF)}} \quad (17)$$

While switching from a lower supply rail to higher supply rail, the minimum bus voltage can be calculated using Equation 18. Here, the switchover time (t_{SW}) is the time taken by the device to turn on fully and start delivering current to the load, which is equal to the device turn-on time (t_{ON}), which in turn includes the turn-on delay ($t_{D,ON}$) and rise time (t_R) determined by the dVdt capacitor (C_{dVdt}) and bus voltage.

$$\text{VOUT,min (V)} = \min(\text{VIN1, VIN2}) - \frac{\text{tSW (µs)} \times \text{ILOAD (A)}}{\text{COUT (µF)}} \quad (18)$$

Note

1. Power MUXing can be done either between two similar rails (such as 12V Primary and 12V Aux, 3.3V Primary and 3.3V Aux) or between dissimilar rails (such as 12V Primary and 5V Aux or vice versa).
2. For power MUXing cases with skewed voltage combinations, care must be taken to design circuit components on EN/OVLO pins for the lower voltage channel devices such that the absolute maximum ratings on those pins are not exceeded when higher voltage is present on the other channel. Also, the dVdt pin capacitor rating should be chosen based on the highest of the two supplies. Refer to Recommended Operating Conditions table for more details.

8.6 Parallel Operation

Applications which need higher steady current can use two or more TPS25948x devices connected in parallel as shown in Figure 8-19. In this configuration, the first device turns on initially to provide the inrush current limiting. The second device is held in an OFF state by driving its EN/UVLO pin low using the SPLYGD signal of the first device. Once the inrush sequence is complete, the first device asserts its SPLYGD pin high and turns on the second device. The second device asserts its SPLYGD signal to indicate when it has turned on fully, thereby indicating to the system that the parallel combination is ready to deliver the full steady state current.

Once in steady state, both devices share current nearly equally. There could be a slight skew in the currents depending on the part-to-part variation in the R_{ON} as well as the PCB trace resistance mismatch.

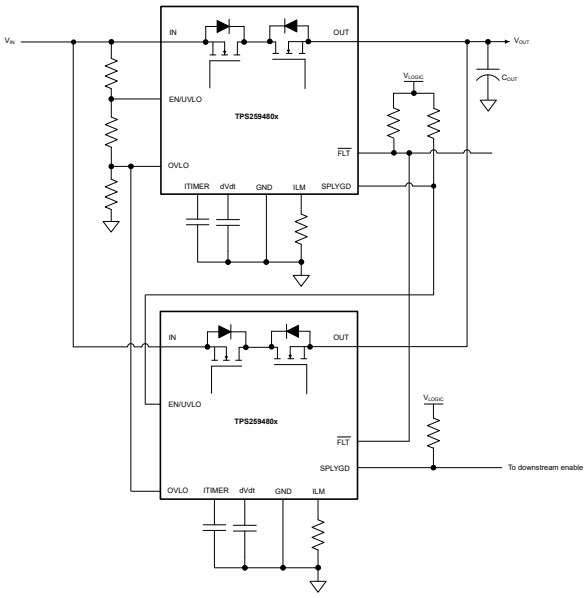


Figure 8-19. Two Devices Connected in Parallel for Higher Steady State Current Capability

The following waveforms illustrate the behavior of parallel configuration during start-up as well as during steady state.

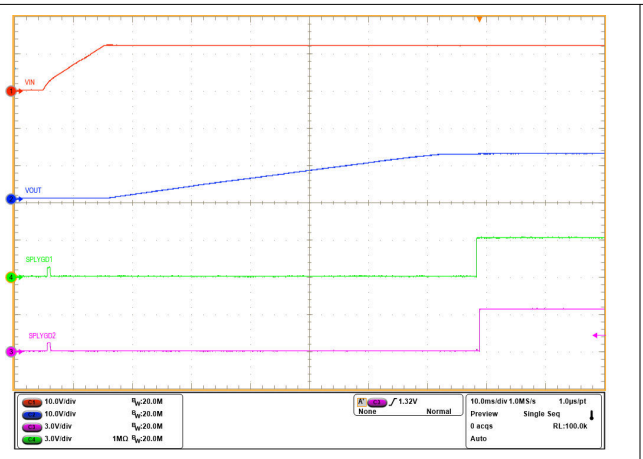


Figure 8-20. Parallel Devices Sequencing During Start-Up

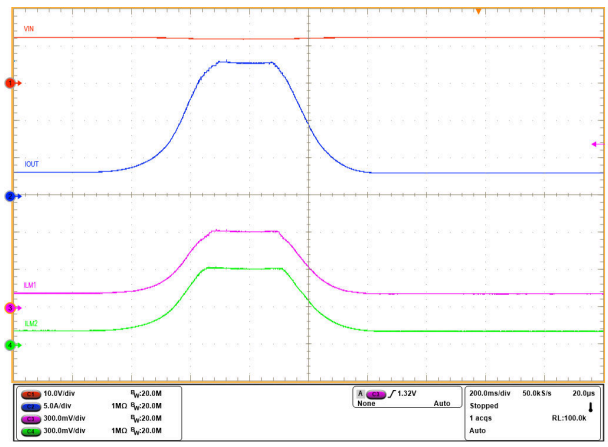


Figure 8-21. Parallel Devices Load Current During Steady State

8.7 USB PD Port Protection

End equipments like PC, notebooks, docking stations, monitors, and so on, have USB PD ports which can be configured as DFP (Source), UFP (Sink) or DRP (Source+Sink). TPS25948xx can be used to as a fully integrated power path solution for USB PD ports as shown in Figure 8-22 below.

TPS25948xx provides all the basic protection functions needed on the USB power path, for example: overvoltage, overcurrent, and short-circuit protection along with monitoring and control. The linear ORing mechanism in TPS25948xx ensures that there's no reverse current flowing from one power source to the other during fast or slow ramp of either supply.

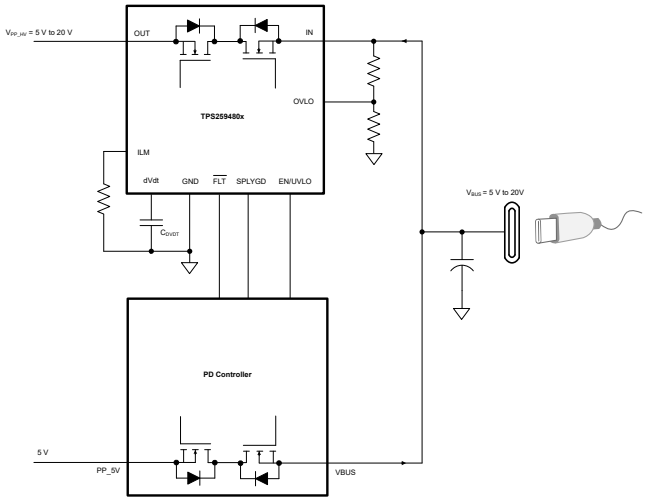


Figure 8-22. USB PD Port Protection

8.8 Power Supply Recommendations

The TPS25948x devices are designed for a supply voltage range of 3.5V ≤ V_{IN} or V_{OUT} ≤ 23V. An input ceramic bypass capacitor higher than 0.1µF is recommended if the input supply is located more than a few inches from the device. The power supply must be rated higher than the set current limit to avoid voltage droops during overcurrent and short-circuit conditions.

8.8.1 Transient Protection

In the case of a short-circuit and overload current limit when the device interrupts current flow, the input inductance generates a positive voltage spike on the input, and the output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on the value of inductance in series to the input or output of the device. Such transients can exceed the absolute maximum ratings of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Minimize lead length and inductance into and out of the device.
- Use a large PCB GND plane.
- Connect a Schottky diode from the OUT pin ground to absorb negative spikes.
- Connect a low ESR capacitor larger than 1µF at the OUT pin very close to the device.
- Use a low-value ceramic capacitor C_{IN} = 1 µF to absorb the energy and dampen the transients. The capacitor voltage rating should be at least twice the input supply voltage to be able to withstand the positive voltage excursion during inductive ringing.

  The approximate value of input capacitance can be estimated with the equation:

$$\text{VSPIKE(ABSOLUTE)} = \text{VIN} + \text{ILOAD} \times \sqrt{\frac{\text{LIN}}{\text{CIN}}} \tag{19}$$

  where

  – V_{IN} is the nominal supply voltage.
  – • I_{LOAD} is the load current.
  – L_{IN} equals the effective inductance seen looking into the source.
  – C_{IN} is the capacitance present at the input.
- Some applications may require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the absolute maximum ratings of the device. In some cases, even if the maximum amplitude of the transients is below the absolute maximum rating of the device, a TVS can help to absorb the excessive energy dump and prevent it from creating very fast transient voltages on the input supply pin of the IC, which can couple to the internal control circuits and cause unexpected behavior.
- For applications such as USB-C ports where a powered cable can be plugged to the output of the device, there could be excess voltage stress from OUT to IN which exceeds the absolute maximum rating of the device. It's recommended to add a TVS diode from OUT to IN to clamp the voltage to a safe level.

The circuit implementation with optional protection components is shown in Figure 8-23.

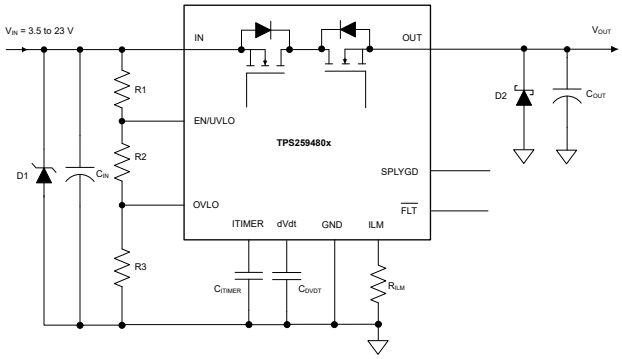


Figure 8-23. Circuit Implementation with Optional Protection Components

8.8.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. The following contribute to variation in results:

- Source bypassing
- Input leads
- Circuit layout
- Component selection
- Output shorting method
- Relative location of the short
- Instrumentation

The actual short exhibits a certain degree of randomness because it microscopically bounces and arcs. Ensure that configuration and methods are used to obtain realistic results. Do not expect to see waveforms exactly like those in this data sheet because every setup is different.

8.9 Layout

8.9.1 Layout Guidelines

- For all applications, a ceramic decoupling capacitor of 0.1µF or greater is recommended between the IN terminal and GND terminal.
- The optimal placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC.
- High current-carrying power-path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC with the shortest possible trace. The PCB ground must be a copper plane or island on the board. It is recommended to have a separate ground plane island for the eFuse. This plane does not carry any high currents and serves as a quiet ground reference for all the critical analog signals of the eFuse. The device ground plane should be connected to the system power ground plane using a star connection.
- The IN and OUT pads are used for heat dissipation. Connect to as much copper area on top and bottom PCB layers using as possible with thermal vias. The vias under the device also help to minimize the voltage gradient across the IN and OUT pads and distribute current uniformly through the device, which is essential to achieve the best on-resistance and current sense accuracy.
- Locate the following support components close to their connection pins:
  - R_{ILM}
  - C_{dVdT}
  - C_{ITIMER}
  - Resistors for the EN/UVLO and OVLO pins
- Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for the R_{ILM}, C_{ITIMER} and C_{dVdt} components to the device must be as short as possible to reduce parasitic effects on the current limit , overcurrent blanking interval and soft start timing. It is recommended to keep parasitic capacitance on ILM pin below 50pF to ensure stable operation. These traces must not have any coupling to switching signals on the board.
- Since the bias current on ILM pin directly controls the overcurrent protection behavior of the device, the PCB routing of this node must be kept away from any noisy (switching) signals.

- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect. These protection devices must be routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads. It's also recommended to add a ceramic decoupling capacitor of 1µF or greater between OUT and GND. These components must be physically close to the OUT pins. Care must be taken to minimize the loop area formed by the Schottky diode/bypass-capacitor connection, the OUT pin and the GND terminal of the IC.

8.9.2 Layout Example

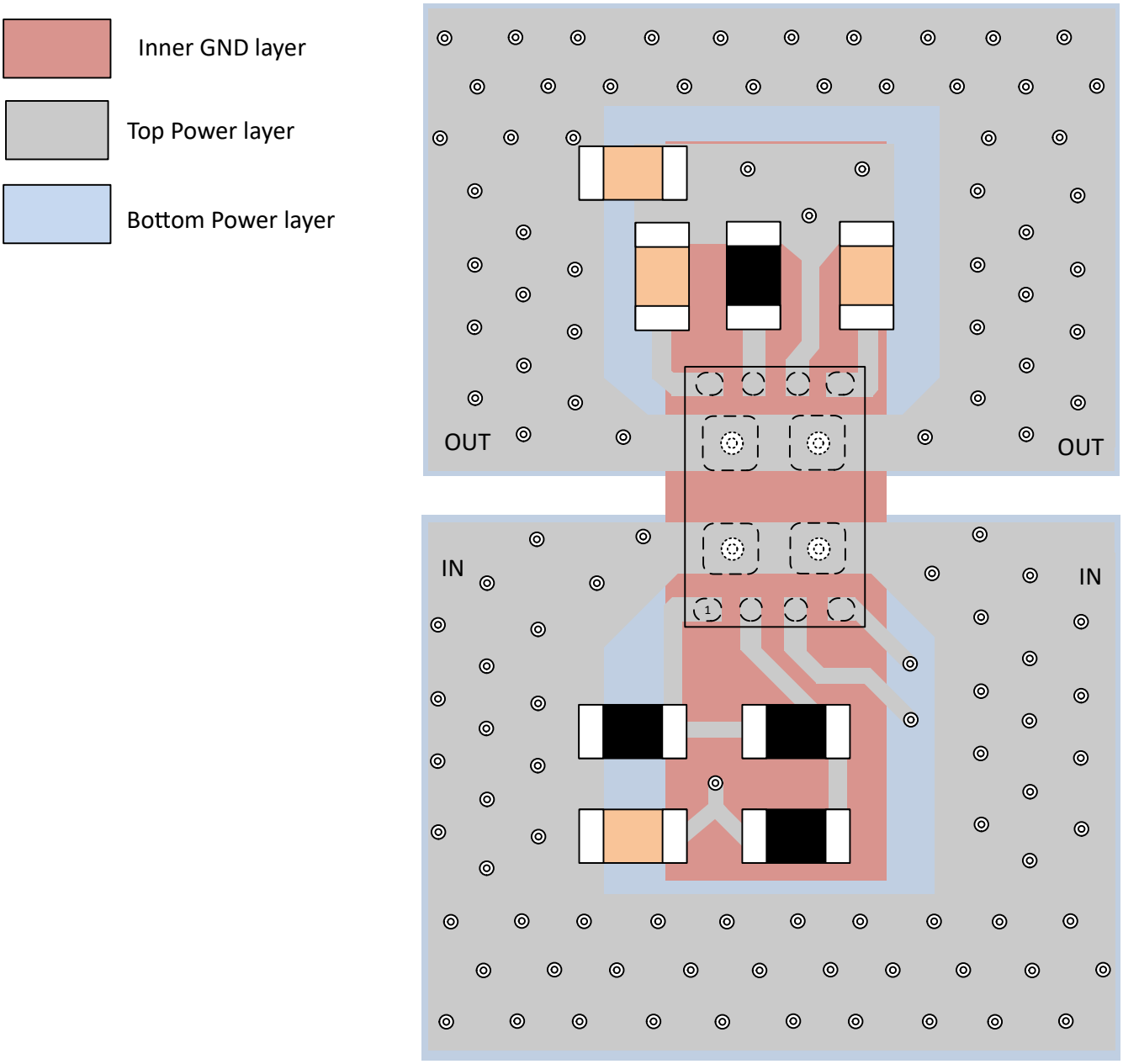


Figure 8-24. Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- *TPS25948EVM eFuse Evaluation Board*
- *TPS25948x Design Calculator*
- *Application brief - eFuses for USB Type-C protection*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2024) to Revision C (August 2025)	Page
• Added TPS259483 OPN	3
• Added TPS259483 to Pin Functions Table	4
• Added TPS259483 also in the Description column of Electrical Characteristics Table where applicable	6
• Added TPS259483 where applicable	10

Changes from Revision A (September 2023) to Revision B (June 2024)	Page
• Added IEC 61000-4-5 to the *Features* section	1
• Deleted reference to reverse polarity in the *Description* section	1
• Changed $V_{IN,MAX}$, –40°C ≤ T_J ≤ 125°C from: V_{OUT} – 21V to: –0.3V in the *Absolute Maximum Ratings* section	5
• Deleted $V_{IN,MAX}$, –10°C ≤ T_J ≤ 125°C from the *Absolute Maximum Ratings* section	5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS259480AYWPR	Active	Production	DSBGA (YWP) | 12	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	259480A
TPS259480AYWPR.A	Active	Production	DSBGA (YWP) | 12	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	259480A
TPS259480LYWPR	Active	Production	DSBGA (YWP) | 12	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	259480L
TPS259480LYWPR.A	Active	Production	DSBGA (YWP) | 12	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	259480L
TPS259481AYWPR	Active	Production	DSBGA (YWP) | 12	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	259481A
TPS259481AYWPR.A	Active	Production	DSBGA (YWP) | 12	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	259481A
TPS259481LYWPR	Active	Production	DSBGA (YWP) | 12	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	259481L
TPS259481LYWPR.A	Active	Production	DSBGA (YWP) | 12	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	259481L
TPS259482AYWPR	Active	Production	DSBGA (YWP) | 12	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	259482A
TPS259482AYWPR.A	Active	Production	DSBGA (YWP) | 12	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	259482A
TPS259482LYWPR	Active	Production	DSBGA (YWP) | 12	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	259482L
TPS259482LYWPR.A	Active	Production	DSBGA (YWP) | 12	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	259482L
TPS259483AYWPR	Active	Production	DSBGA (YWP) | 12	3000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	259483A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

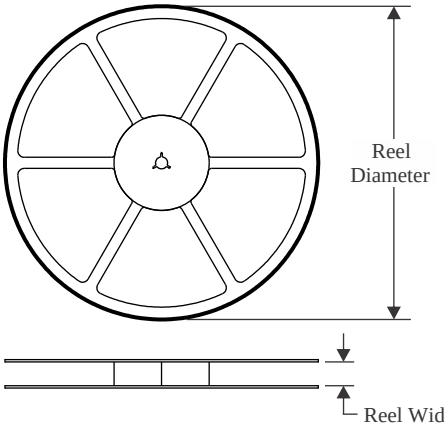
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

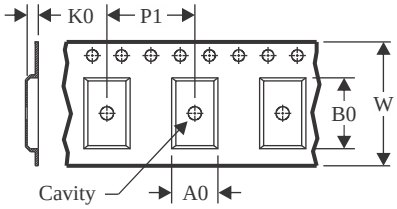
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

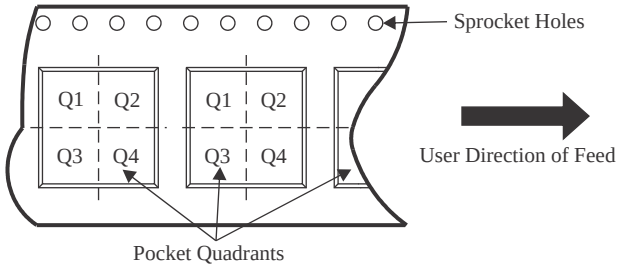


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

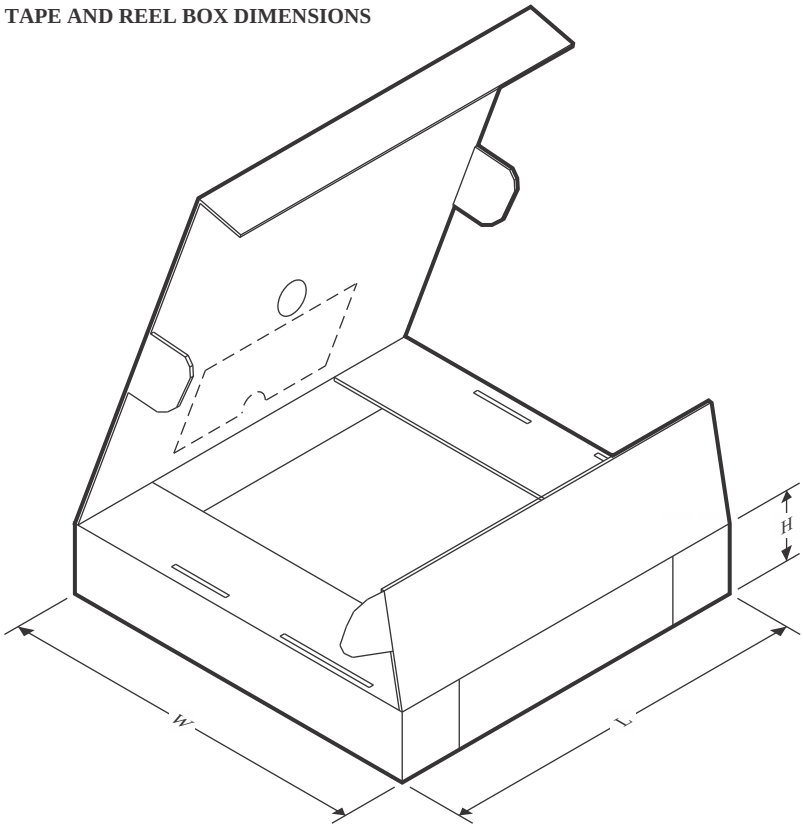
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS259480AYWPR	DSBGA	YWP	12	3000	180.0	8.4	1.88	2.59	0.53	4.0	8.0	Q2
TPS259480LYWPR	DSBGA	YWP	12	3000	180.0	8.4	1.88	2.59	0.53	4.0	8.0	Q2
TPS259481AYWPR	DSBGA	YWP	12	3000	180.0	8.4	1.88	2.59	0.53	4.0	8.0	Q2
TPS259481LYWPR	DSBGA	YWP	12	3000	180.0	8.4	1.88	2.63	0.53	4.0	8.0	Q2
TPS259481LYWPR	DSBGA	YWP	12	3000	180.0	8.4	1.88	2.59	0.53	4.0	8.0	Q2
TPS259482AYWPR	DSBGA	YWP	12	3000	180.0	8.4	1.88	2.63	0.53	4.0	8.0	Q2
TPS259482AYWPR	DSBGA	YWP	12	3000	180.0	8.4	1.88	2.59	0.53	4.0	8.0	Q2
TPS259482LYWPR	DSBGA	YWP	12	3000	180.0	8.4	1.88	2.59	0.53	4.0	8.0	Q2
TPS259483AYWPR	DSBGA	YWP	12	3000	180.0	8.4	1.88	2.63	0.53	4.0	8.0	Q2
TPS259483AYWPR	DSBGA	YWP	12	3000	180.0	8.4	1.88	2.59	0.53	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

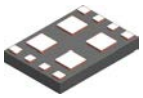


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS259480AYWPR	DSBGA	YWP	12	3000	182.0	182.0	20.0
TPS259480LYWPR	DSBGA	YWP	12	3000	182.0	182.0	20.0
TPS259481AYWPR	DSBGA	YWP	12	3000	182.0	182.0	20.0
TPS259481LYWPR	DSBGA	YWP	12	3000	182.0	182.0	20.0
TPS259481LYWPR	DSBGA	YWP	12	3000	182.0	182.0	20.0
TPS259482AYWPR	DSBGA	YWP	12	3000	182.0	182.0	20.0
TPS259482AYWPR	DSBGA	YWP	12	3000	182.0	182.0	20.0
TPS259482LYWPR	DSBGA	YWP	12	3000	182.0	182.0	20.0
TPS259483AYWPR	DSBGA	YWP	12	3000	182.0	182.0	20.0
TPS259483AYWPR	DSBGA	YWP	12	3000	182.0	182.0	20.0

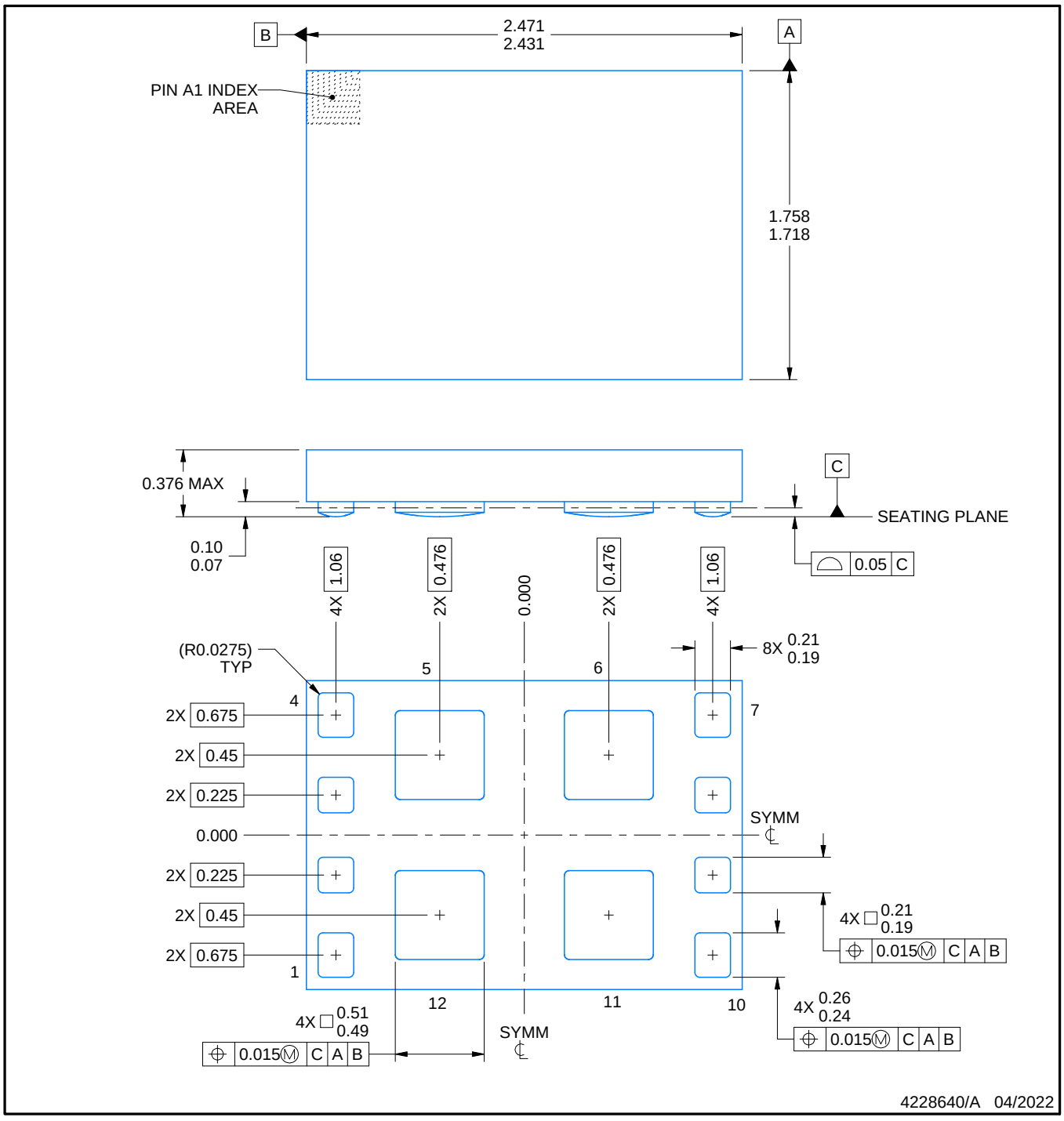
PACKAGE OUTLINE

YWP0012A



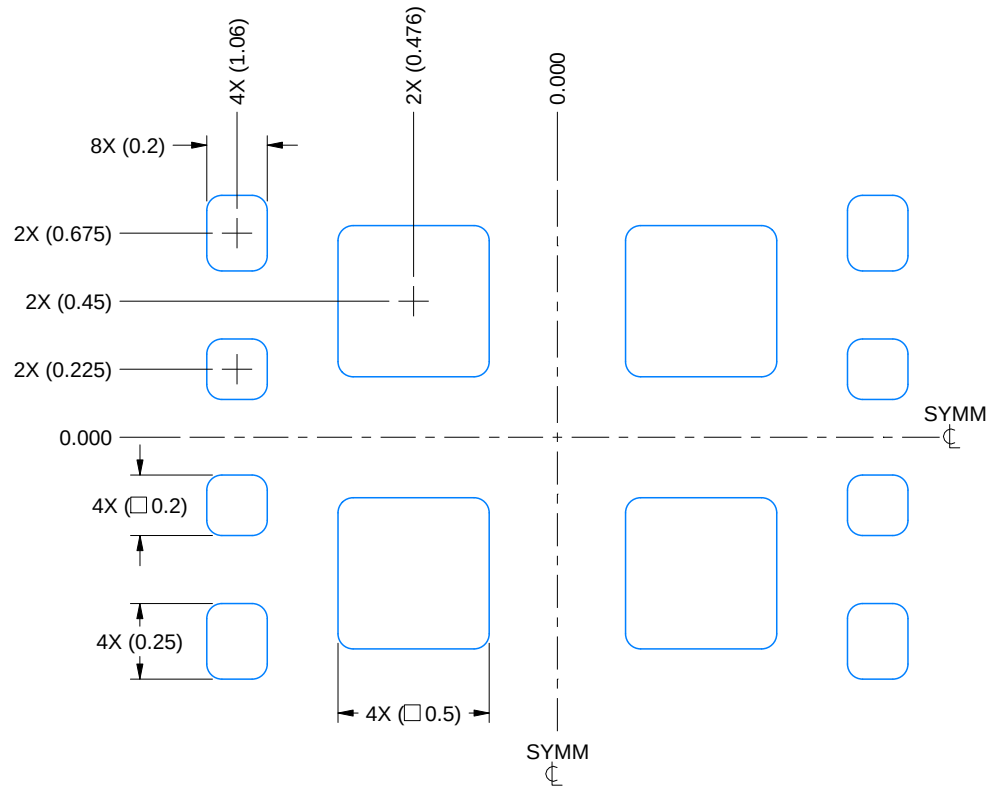
PowerWCSP - 0.376 mm max height

POWER CHIP SCALE PACKAGE

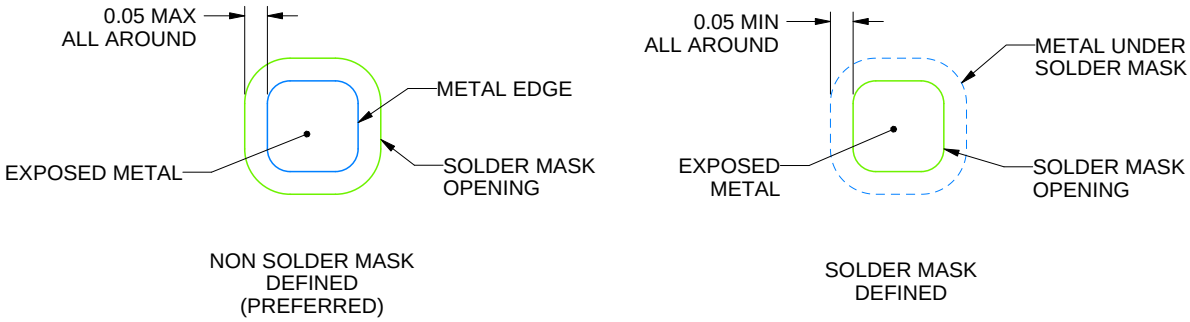


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

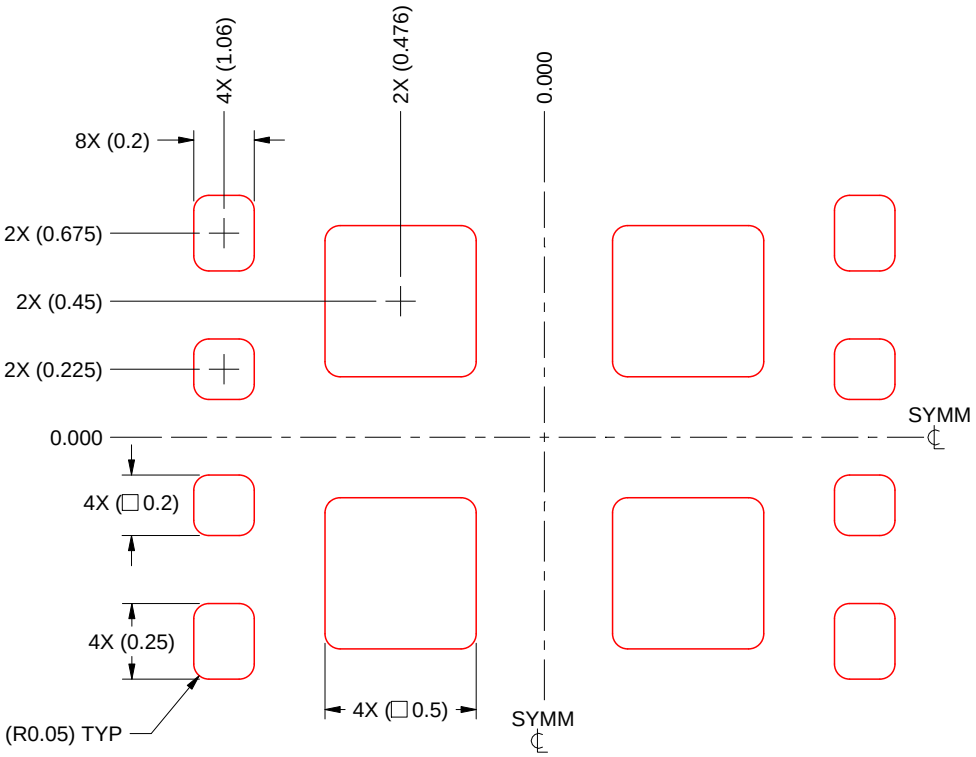
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

YWP0012A

PowerWCSP - 0.376 mm max height

POWER CHIP SCALE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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Last updated 10/2025