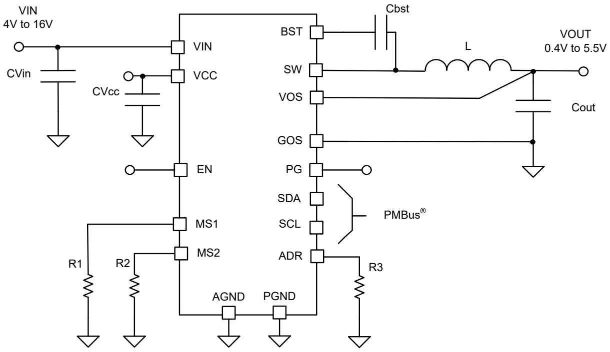
TPS544B28 4V to 16V Input, 20A, Remote Sense Synchronous Buck Converter With PMBus®

1 Features

- 4V to 16V input voltage range without external bias
- 2.7V to 16V input voltage range with external bias
- 3.1V to 4.3V external VCC bias support
- 8.4mΩ and 3.3mΩ MOSFETs (V_{VCC} = 3.3V)
- 20A continuous output current
- Optimized 19-pin WQFN-HR package for efficiency and thermal performance
- ±1.25% output voltage accuracy with internal feedback, T_J = –40°C to +150°C
- 0.4V to 5.5V output voltage range
- Differential remote sense
- D-CAP4 with ultra-fast load-step response
- User programmable NVM
- Supports all ceramic output capacitors
- Selectable auto-skip Eco-mode for high light-load efficiency
- Programmable valley current limit
- 500kHz, 600kHz, 800kHz, 1.0MHz, 1.2MHz, 1.4MHz selectable switching frequency
- Programmable soft-start time
- Prebiased start-up capability
- Open-drain power-good output
- Overvoltage and undervoltage fault protection
- 3mm × 3mm (0.4mm pin pitch) and 3mm × 3.5mm (0.5 pin pitch) 19-pin QFN packages
- Pin-to-pin compatible with 12A TPS544A28 and 6A TPS544628

2 Applications

- Rack server and blade server
- Data center switches
- Wireless infrastructure
- Hardware accelerator and add-in cards
- Industrial PC
- Baseband unit (BBU)



Simplified Schematic

3 Description

The TPS544B28 device is a small, high-efficiency, synchronous buck converter with an adaptive on-time D-CAP4 control mode. The control method provides low minimum on-time and fast load-transient response across the entire output voltage range without requiring an external compensation network.

The TPS544B28 device has differential remote sense, high-performance integrated MOSFETs, and supports ±1.25% output voltage accuracy with internal reference. The device features accurate load and line regulation and Eco-mode or Forced Continuous Conduction Mode (FCCM) operation.

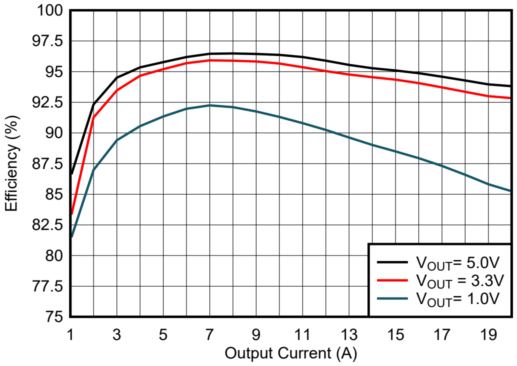
The PMBus® interface with 1MHz clock support gives a convenient, standardized digital interface for device configuration as well as output voltage, output current, and die temperature telemetry. Pin strap options allow for the configuration of the overcurrent limit, fault response, internal or external feedback, output voltage selection, switching frequency, and compensation. Internal NVM is also available to store a variety of the PMBus parameters.

The TPS544B28 device is a lead-free device. The device is RoHS compliant without exemption.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
TPS544B28	VAN (WQFN-HR, 19)	3.00mm × 3.00mm
	RBH (WQFN-HR, 19)	3.00mm × 3.50mm

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



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4 Device Options

DEVICE NUMBER	MAXIMUM OUTPUT CURRENT	V_O ADJUST	PIN STRAP CONFIGURABILITY	DIGITAL INTERFACE	TELEMETRY
TPS548B23	20A	0.5V – 5.5V	Internal, external FB, F_{SW}, FCCM/PFM, OCP, hiccup/ latch-off, SS time	N/A	No
TPS548A23	12A				
TPS544B28	20A	0.4V – 5.5V		PMBus®	Yes
TPS544A28	12A				

5 Pin Configuration and Functions

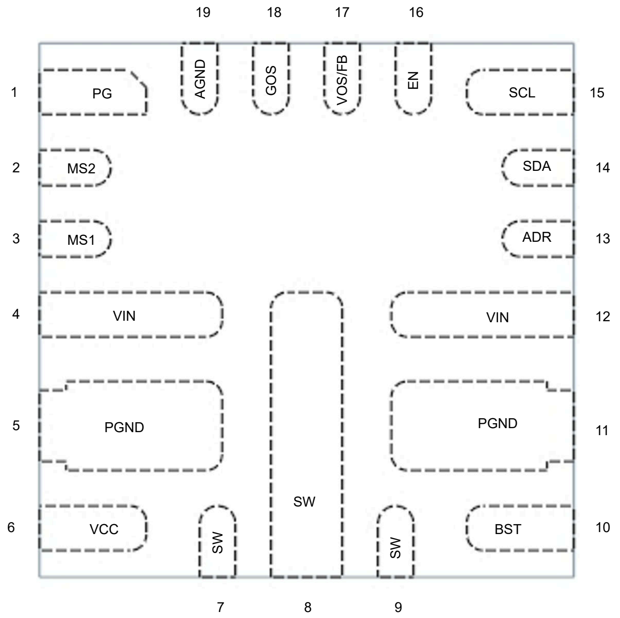


Figure 5-1. VAN Package, 19-Pin, 3mm × 3mm (0.4mm Pin Pitch) WQFN-HR (Top View)

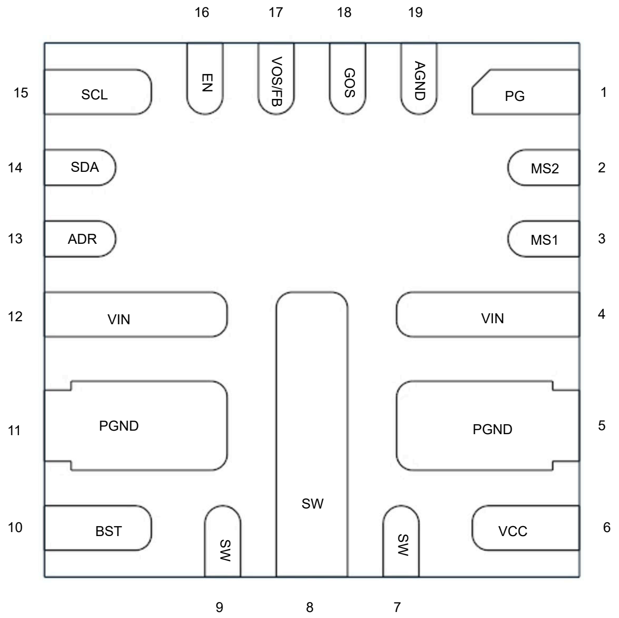


Figure 5-2. VAN Package, 19-Pin, 3mm × 3mm (0.4mm Pin Pitch) WQFN-HR (Bottom View)

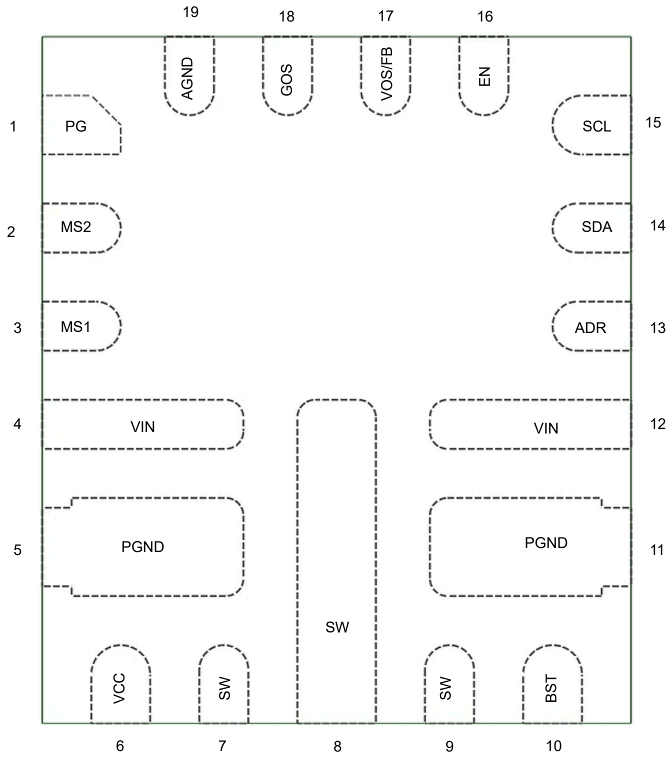


Figure 5-3. RBH Package 19-Pin 3mm × 3.5mm (0.5mm Pin Pitch) WQFN-HR (Top View)

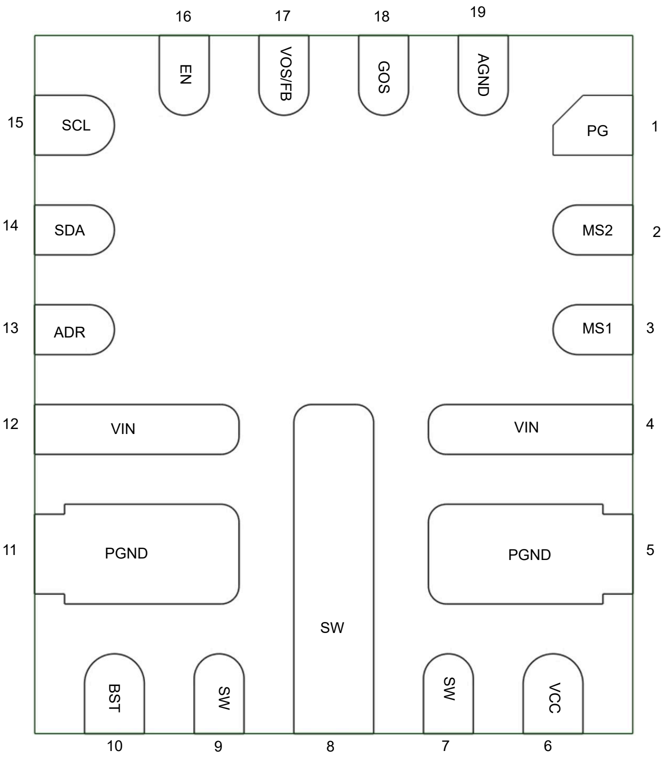


Figure 5-4. RBH Package 19-Pin 3mm × 3.5mm (0.5mm Pin Pitch) WQFN-HR (Bottom View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO		
PG	1	O	Open-drain power-good status signal. Connect an external pullup resistor to a voltage source. When the FB voltage moves outside the specified limits, PG goes low after the specified delay.
MS2	2	I	Multifunction select pin. A resistor from the MS2 pin to AGND selects the output voltage setting, configuration (internal or external FB).
MS1	3	I	Multifunction select pin. A resistor from the MS1 pin to AGND selects the switching frequency, valley current limit threshold, and soft start time.
VIN	4, 12	P	Power-supply input pins for both the power stage MOSFETs and the internal LDO. Place the decoupling input capacitors from VIN pins to PGND pins as close as possible. A capacitor from each VIN to PGND close to IC is required.
PGND	5, 11	G	Ground return for the power stage. This pin is internally connected to the source of the low-side MOSFET. Place as many vias as possible beneath the PGND pins and as close as possible to the PGND pins. This action minimizes parasitic impedance and also lowers thermal resistance.
VCC	6	P	Internal 3V LDO output. A 3.1V to 5.3V external bias can be connected to this pin to save the power losses on the internal LDO. The voltage source on this pin powers both the internal circuitry and gate driver. Bypass with a 1µF, > 6.3V rating, ceramic capacitor from VCC pin to PGND. Place this capacitor as close to the VCC and PGND pins as possible.
SW	7, 8, 9	O	Output switching terminal of the power converter. Connect this pin to the output inductor.
BST	10	I/O	Supply for the internal high-side MOSFET gate driver (boost terminal). Connect the bootstrap capacitor from this pin to SW node.
ADR	13	I	PMBus Address select pin. A resistor from the ADR pin to AGND selects the PMBus device address and the fault recovery (hiccup or latch-off) mode.
SDA	14	I	PMBus bi-directional serial data pin
SCL	15	I	PMBus serial clock pin
EN	16	I	Enable pin. The enable pin turns the DC/DC switching converter on or off. Floating EN pin before start-up disables the converter. The recommended maximum voltage applied to the EN pin is 5.5V. TI *does not* recommend connecting the EN pin to VIN pin directly.
VOS/FB	17	I	Output voltage feedback input. Positive input of the differential remote sense circuit, connect to the Vout sense point on the load side. When configured for external feedback, a resistor divider from the VOUT to GOS (tapped to FB pin) sets the output voltage.
GOS	18	I	Negative input of the differential remote sense circuit. Connect to a ground sense point near the load.
AGND	19	G	Analog ground return and reference for the internal control circuits

(1) I = Input, O = Output, P = Supply, G = Ground

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage	VIN	–0.3	19	V
Pin voltage	SW - PGND, DC	–0.3	19	V
Pin voltage	SW - PGND, transient < 10ns	–3	20	V
Pin voltage	VIN – SW, DC	–0.3	19	V
Pin voltage	VIN – SW, transient < 10ns	–3	25	V
Pin voltage	BOOT - PGND	–0.3	24.5	V
Pin voltage	BOOT – SW	–0.3	5.5	V
Pin voltage	MS1, MS2, SDA, SCL, VCC	–0.3	5	V
Pin voltage	VOS/FB, PG, EN	–0.3	6	V
Pin voltage	GOS, PGND	–0.3	0.3	V
Sink current	PG		15	mA
Operating junction temperature	T_J	–40	150	°C
Storage Temperature	Tstg	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	Internal LDO	4		16	V
V_{IN}	Input voltage range	3.1V ≤ V_{VCC} External Bias ≤ 4.3V	2.7		16	V
Pin voltage		V_{GOS} versus V_{AGND}	–0.1		0.1	V
		EN, PG	–0.1		5.5	V
V_{VCC}	External bias range	V_{VIN} ≤ 16V	3.1		4.3	V
V_{OUT}	Output voltage range	VOUT	0.4		5.5	V
I_{PG}	Power-good sinking current	PG			10	mA
I_{OUT}	Output current	SW			20	A
IL_{PEAK}	Maximum peak inductor current	SW			31	A
T_J	Operating junction temperature		–40		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS544B28				UNIT
		VAN (WQFN-HR, JEDEC LAYOUT)	VAN (WQFN-HR, APPLICATION LAYOUT, 6-LAYER PCB)	RBH (WQFN-HR, JEDEC LAYOUT)	RBH (WQFN-HR, APPLICATION LAYOUT, 6-LAYER PCB)	
		19 PINS	19 PINS	19 PINS	19 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	59	19.0(2)	54.4	TBD(2)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.6	Not applicable (3)	30.9	Not applicable (3)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.4	Not applicable (3)	21.5	Not applicable (3)	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.77	Not applicable (3)	1.0	Not applicable (3)	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18.4	Not applicable (3)	21.5	Not applicable (3)	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) Measured on TPS544B28EVM with 1.0W dissipated in the device.
(3) The thermal test or simulation setup is not applicable to an application layout.

6.5 Electrical Characteristics

T_J = –40°C to +150°C, V_{VCC} = 3.3 V (external), V_{VIN} = 4 V to 16 V. Typical values are at T_J = 25°C and V_{VIN} = 12 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$I_{Q(VIN)}$	VIN quiescent current	Non-switching, V_{EN} = 2V, V_{FB} = V_{FB_REG} + 50mV, no external bias on VCC pin		2800		µA
$I_{Q(VIN)}$	VIN quiescent current with external VCC bias	T_J = 25°C, V_{IN} = 12V, V_{EN} = 2V, V_{FB} = V_{FB_REG} + 10mV (non-switching), 3.3V external bias on VCC pin		300	500	µA
$I_{SD(VIN)}$	VIN shutdown supply current	V_{IN} = 12V, V_{EN} = 0V, no external bias on VCC pin		2000		µA
		V_{IN} = 12V, V_{EN} = 0V, external bias on VCC pin		250	500	µA
$I_{Q(VCC)}$	VCC quiescent current	T_J = 25°C, V_{IN} = 12V, V_{EN} = 2V, V_{FB} = V_{FB_REG} + 10mV (non-switching), 3.3V external bias on VCC pin		2500	5000	µA
I_{VCC}	VCC external bias current	T_J = 25°C, V_{IN} = 12V, V_{EN} = 2V, regular switching, V_{OUT} = 1.0V, f_{SW} = 600kHz, 3.3V external bias on VCC pin		10		mA
I_{VCC}	VCC external bias current	T_J = 25°C, V_{IN} = 12V, V_{EN} = 2V, regular switching, V_{OUT} = 1.0V, f_{SW} = 1200kHz, 3.3V external bias on VCC pin		16		mA
INTERNAL LDO (VCC)						
V_{VCC}	Internal LDO output voltage		2.85	3.0	3.1	V
I_{VCC}	Internal LDO short-circuit current limit	V_{VIN} = 12V	50	180		mA
UVLO						
$VIN_{UVLO(R)}$	VIN UVLO rising threshold	V_{IN} rising, 3.3V external bias on VCC pin		2.4	2.5	V
$VIN_{UVLO(F)}$	VIN UVLO falling threshold	V_{IN} falling, 3.3V external bias on VCC pin		2.25	2.35	V
$VIN_{UVLO(H)}$	VIN UVLO hysteresis			0.15		V
ENABLE						
$V_{EN(R)}$	EN voltage rising threshold	EN rising, enable switching	1.15	1.2	1.25	V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching	0.95	1.0	1.05	V
$V_{EN(H)}$	EN voltage hysteresis			200		mV
$I_{EN(Hys)}$	EN pin hysteresis current	EN > $V_{EN(R)}$		5		µA
	EN internal pull-down resistance	EN pin to AGND	0.74	1	1.27	MΩ
PINSTRAP						
R_{MSx_TRIP}	MSx resistor step range accuracy		- 2%		+ 2%	

6.5 Electrical Characteristics (continued)

T_J = –40°C to +150°C, V_{VCC} = 3.3 V (external), V_{VIN} = 4 V to 16 V. Typical values are at T_J = 25°C and V_{VIN} = 12 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SERIAL INTERFACE						
$V_{IH(SDx)}$	High-level input voltage on SDA, SCL		1.35			V
$V_{IL(SDx)}$	Low-level input voltage on SCL, SDA				0.8	
$V_{th\_rise(SDx)}$	Rising Threshold SCL, SDA		1.03	1.1	1.17	V
$V_{th\_fall(SDx)}$	Falling Threshold on SCL, SDA		0.84	0.9	0.96	V
$V_{th\_hys(SDx)}$	Hysteresis on SCL, SDA		0.188	0.2	0.212	V
$I_{IH(SDx)}$	Input high level current into SCL, SDA		–10		10	µA
$I_{IL(SDx)}$	Input low level current into SCL, SDA		–10		10	µA
$V_{OL(SDx)}$	Output low level voltage on SDA	VCC ≥ 4.5V, I_{pin} = 20mA			0.4	V
$I_{OH(SDx)}$	Output high level open drain leakage current into SDA	V_{pin} = 5.5V			10	µA
$I_{OL(SDx)}$	Output low level open drain sinking current on PMB_DATA	V_{pin} = 0.4V	20			mA
C_{PIN_SDx}	SCL and SDA pin input capacitance	V_{pin} = 0.1V to 1.35V			5	pF
f_{SDxmin}	Minimum PMBus operating Frequency				10	kHz
f_{SDxmax}	Maximum PMBus operating Frequency		1000			kHz
f_{SDx_CLK}	PMBus operating frequency range		10		1000	kHz
t_{BUF}	Bus free time between a STOP and START condition		0.5			µs
t_{HD_STA}	Hold time for a (repeated) START condition		0.26			µs
t_{SU_STA}	Setup time for a repeated START condition		0.26			µs
t_{SU_STO}	Setup time for a STOP condition		0.26			µs
t_{HD_SDA}	SDA hold time		0			µs
t_{SU_SDA}	SDA setup time		50			ns
$t_{TIMEOUT}$	Detect clock low timeout		25	30	35	ms
t_{LOW}	Low period of SCL		0.5			µs
t_{HIGH}	High period of SCL		0.26			µs
t_{R_SDx}	SCL and SDA rise time	1000kHz class; $V_{IL(MAX)}$ - 150mV to $V_{IH(MIN)}$ + 150mV			120	ns
t_{F_SDx}	SCL and SDA fall time	1000kHz class; $V_{IH(MIN)}$ + 150mV to $V_{IL(MAX)}$ - 150mV			120	ns
N_{WR_NVM}	Number of NVM writeable cycles	–40°C ≤ T_J ≤ 125°C	1000			cycle
START-UP						
$R_{PIN\text{-}STRAP}$	Pin-strap resistor step range accuracy	0.82kΩ ≤ R_{ADDR} ≤ 82kΩ	- 4%		+ 4%	
t_{SS}	Soft-start time	From start of switching to V_{FB} = 0.5V, t_{SS} = 0.5ms setting	0.4	0.5	0.6	ms
t_{SS}	Soft-start time	From start of switching to V_{FB} = 0.5V, t_{SS} = 1ms setting	0.8	1	1.2	ms
t_{SS}	Soft-start time	From start of switching to V_{FB} = 0.5V, t_{SS} = 2ms setting	1.6	2	2.4	ms
t_{SS}	Soft-start time	From start of switching to V_{FB} = 0.5V, t_{SS} = 4ms setting	3.2	4	4.8	ms
t_{EN_DLY}	EN HIGH to start of switching delay	TON_Delay = 0		50		µs
REFERENCE VOLTAGE (FB)						
V_{VOS_REG}	Output voltage regulation accuracy	Internal Feedback Configuration, T_J = 0°C to +85°C	–0.75 %		+ 0.75 %	
V_{VOS_REG}	Output volatge regulation accuracy	Internal Feedback Configuration	–1.25 %		+1.25 %	
V_{FB_REG}	Feedback regulation voltage	External Feedback Configuration, T_J = 0°C to +85°C	796	800	804	mV
V_{FB_REG}	Feedback regulation voltage	External Feedback Configuration	792	800	808	mV
$I_{FB(LKG)}$	FB input leakage current	V_{FB} = V_{FB_REG}			160	nA

6.5 Electrical Characteristics (continued)

T_J = –40°C to +150°C, V_{VCC} = 3.3 V (external), V_{VIN} = 4 V to 16 V. Typical values are at T_J = 25°C and V_{VIN} = 12 V (unless otherwise noted).

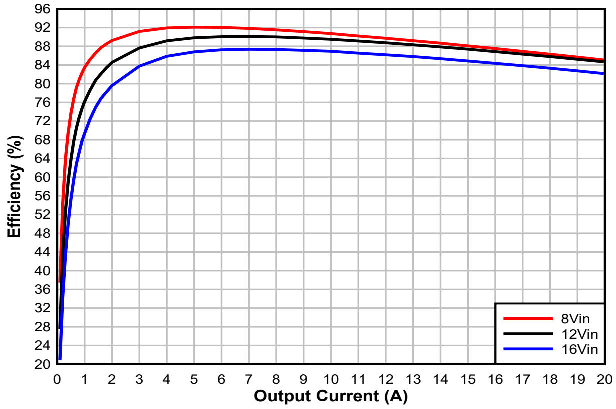
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIFFERENTIAL REMOTE SENSE AMPLIFIER						
I_{GOSNS}	Leakage current out of GOS pin	V_{GOS} - V_{AGND} = 100mV			80	µA
V_{ICM}	GOS common mode voltage for regulation	V_{GOS} versus V_{AGND}	–0.1		0.1	V
TELEMETRY						
$M_{IOUT(rng)}$	Output current measurement range		0		24	A
$M_{IOUT(acc)}$	Output current measurement accuracy	6A ≤ I_{OUT} ≤ 10A	-15%		15%	
		10A < I_{OUT} ≤ 20A	-10%		10%	
$M_{IOUT(off)}$	Output current measurement offset	I_{OUT} ≤ 6A	-1		1	A
$M_{VOUT(rng)}$	Output voltage measurement range		0		6	V
$M_{VOUT(acc)}$	Output voltage measurement accuracy	400mV ≤ V_{OUT} ≤ 5.5V	-2%		2%	
$M_{VOUT(lsb)}$	Output voltage measurement bit resolution			1		mV
$M_{TSNS(rng)}$	Internal temperature sense range		–40		150	°C
$M_{TSNS(lsb)}$	Internal temperature sense bit resolution, (8Dh) READ_TEMP1			1		°C
$M_{TSNS(acc)}$	Internal temperature sense accuracy	–40°C ≤ T_J ≤ 150°C	-1.5	+2.5	6.5	°C
SWITCHING FREQUENCY						
$f_{SW(FCCM)}$	Switching frequency, FCCM operation	V_{VIN} = 12V, V_{OUT} = 3.3V, F_{SW} = 500kHz, No load	425	500	575	kHz
$f_{SW(FCCM)}$	Switching frequency, FCCM operation	V_{VIN} = 12V, V_{OUT} = 3.3V, F_{SW} = 600kHz, No load	510	600	690	kHz
$f_{SW(FCCM)}$	Switching frequency, FCCM operation	V_{VIN} = 12V, V_{OUT} = 3.3V, F_{SW} = 800kHz, No load	680	800	920	kHz
$f_{SW(FCCM)}$	Switching frequency, FCCM operation	V_{VIN} = 12V, V_{OUT} = 3.3V, F_{SW} = 1.0MHz, No load	850	1000	1150	kHz
$f_{SW(FCCM)}$	Switching frequency, FCCM operation	V_{VIN} = 12V, V_{OUT} = 3.3V, F_{SW} = 1.2MHz, No load	1020	1200	1380	kHz
$f_{SW(FCCM)}$	Switching frequency, FCCM operation	V_{VIN} = 12V, V_{OUT} = 3.3V, F_{SW} = 1.4MHz, No load	1190	1400	1610	kHz
POWER STAGE						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	$V_{BOOT-SW}$ = 3.3V		8.7		mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	V_{VCC} = 3.3V		3		mΩ
$t_{ON(min)}$	Minimum ON pulse width			25		ns
$t_{OFF(min)}$	Minimum OFF pulse width				150	ns
	Output discharge resistor on SW pin	V_{IN} = 12V, V_{SW} = 1V, power conversion disabled		100		Ω
$I_{BOOT(LKG)}$	Leakage current into BOOT pin	$V_{BOOT-SW}$ = 3V, Enabled, Not switching.		30		µA
POWER GOOD						
$V_{PGTH(RISE\_OV)}$	Power-Good threshold	FB rising, PG high to low	107%	110%	113%	
$V_{PGTH(RISE\_UV)}$	Power-Good threshold	FB rising, PG low to high	87.5%	90%	92.5%	
$V_{PGTH(FALL\_UV)}$	Power-Good threshold	FB falling, PG high to low	82%	85%	87%	
t_{PG_DLY}	PG delay going from low to high during startup			1.1	1.5	ms
	PG delay going from high to low			4	6.2	µs
$I_{PG(LKG)}$	PG pin leakage current when open drain output is high	V_{PG} = 4.5V			5	µA
	PG pin output low-level voltage	I_{PG} = 7mA			500	mV
	PG pin output low-level when VIN and VCC are low	V_{VIN} = 0V, V_{VCC} = 0V, V_{EN} = 0V, PG pulled up to 3.3V through a 100kΩ resistor			850	mV
	PG pin output low-level when VIN and VCC are low	V_{VIN} = 0V, V_{VCC} = 0V, V_{EN} = 0V, PG pulled up to 3.3V through a 10kΩ resistor			1000	mV

6.5 Electrical Characteristics (continued)

T_J = –40°C to +150°C, V_{VCC} = 3.3 V (external), V_{VIN} = 4 V to 16 V. Typical values are at T_J = 25°C and V_{VIN} = 12 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVERCURRENT PROTECTION						
	Low-side valley current limit	Valley current on LS FET, R_{MS1} = GND	19	21	23	A
		Valley current on LS FET, R_{MS1} = 4.7kΩ	16	18	20	A
		Valley current on LS FET, R_{MS1} = 22kΩ	13	15	17	A
		Valley current on LS FET, R_{MS1} = 56kΩ	11.5	13	14.5	A
$I_{LS(NOC)}$	Low-side negative current limit	Sinking current limit on LS FET		–10	–8	A
I_{ZC}	Zero-cross detection current threshold to enter DCM, open loop	V_{IN} = 12V		–750		mA
$I_{ZC(HYS)}$	Zero-cross detection current threshold hysteresis after entering DCM, open loop	V_{IN} = 12V		1000		mA
OUTPUT OVP AND UVP						
V_{OVP}	Overvoltage-protection (OVP) threshold voltage	V_{FB} rising	113%	116%	119%	
t_{OVPDLY}	OVP delay	With 100mV overdrive		400		ns
V_{UVP}	Undervoltage-protection (UVP) threshold voltage	V_{FB} falling	77%	80%	83%	
t_{UVPDLY}	UVP filter delay			70		µs
	Hiccup wait time	Hiccup mode enabled		56		ms
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold	Temperature rising	150	165		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis			15		°C

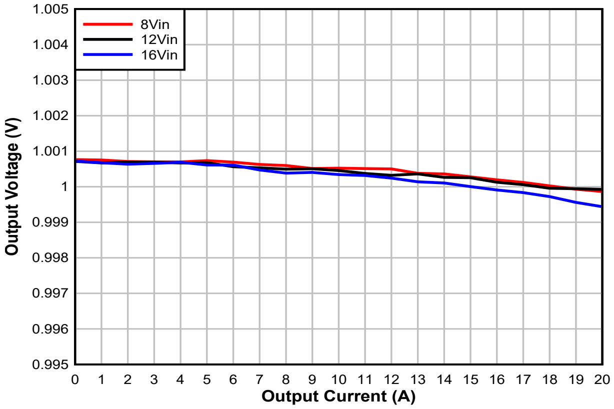
6.6 Typical Characteristics



L = 550nH Vout = 1V Int Vcc

DCR = 1.56mΩ 800Khz

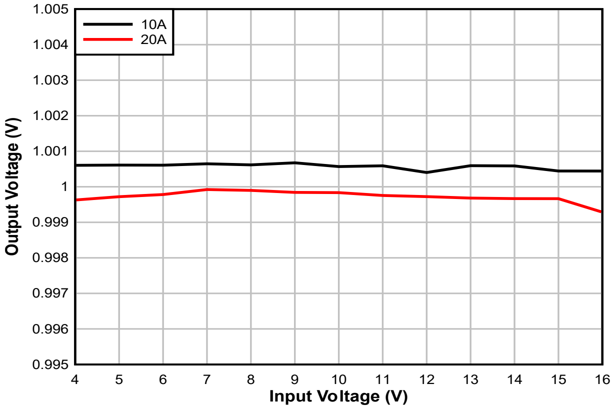
Figure 6-1. Efficiency vs Output Current



L = 550nH Vout = 1V Int Vcc

DCR = 1.56mΩ 800Khz

Figure 6-2. Load Regulation



L = 550nH Vout = 1V Int Vcc

DCR = 1.56mΩ 800Khz

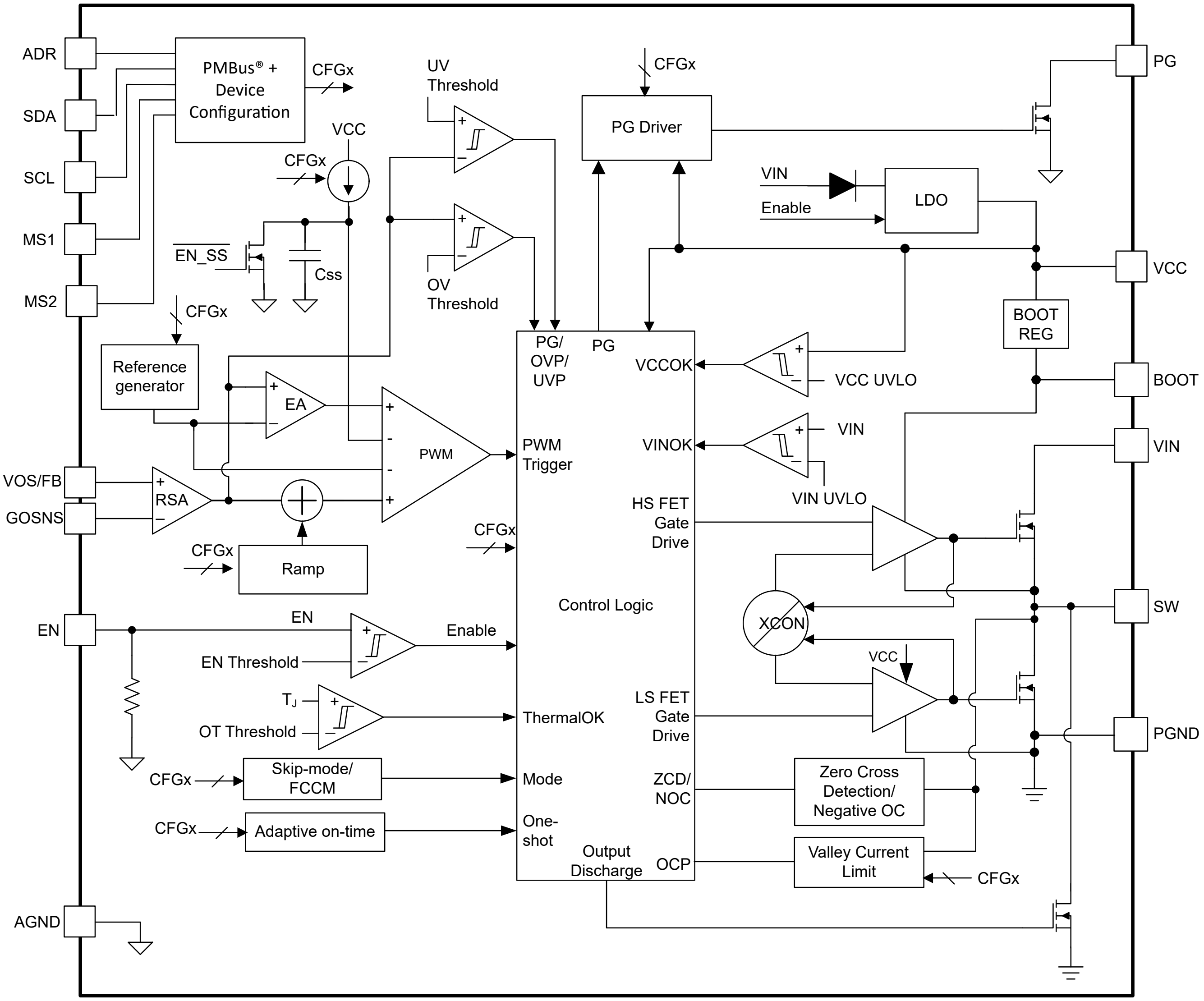
Figure 6-3. Line Regulation

7 Detailed Description

7.1 Overview

The TPS544B28 device is a high-efficiency, single-channel, small-sized synchronous buck converter. The device is designed for low output voltage point-of-load applications with 20A or lower output current in server, storage, and similar computing applications. The TPS544B28 features proprietary D-CAP4 mode control combined with adaptive on-time architecture. This combination builds modern low-duty-ratio and ultra-fast load-step-response DC/DC converters in an excellent fashion. The output voltage set by the feedback voltage divider ranges from 0.4V to 5.5V. The conversion input voltage ranges from 2.7V to 16V, and the VCC input voltage ranges from 3.1V to 5.3V. The D-CAP4 modulator uses emulated current information to control the modulation. The D-CAP4 modulator reduces loop gain variation with different output voltages providing better transient response in higher output voltage applications. An advantage of this control scheme is that this control scheme does not require a phase-compensation network outside which makes the device easy-to-use and also allows low external component count. Another advantage of this control scheme is that this control scheme supports stable operation with all low ESR output capacitors (such as ceramic capacitors and low ESR polymer capacitors). Lastly, adaptive on-time control tracks the preset switching frequency over a wide range of input and output voltages while increasing switching frequency as needed during load-step transients.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 D-CAP4 Control

The device uses D-CAP4 control to achieve a fast load transient response while maintaining ease-of-use. The D-CAP4 control architecture includes an internal ripple generation network enabling the use of very low-ESR output capacitors such as multi-layered ceramic capacitors (MLCC) and low ESR polymer capacitors. No external current sensing network or voltage compensators are required with D-CAP4 control architecture. The role of the internal ripple generation network is to emulate the ripple component of the inductor current information and then combine with the voltage feedback signal to regulate the loop operation.

D-CAP4 control architecture reduces loop gain variation across V_{OUT}, enabling a fast load transient response across the entire output voltage range with one ramp setting. The R-C time-constant of the internal ramp circuit sets the zero frequency of the ramp, similar to other R-C based internal ramp generation architectures. The reduced variation in loop gain also mitigates the need for a feedforward capacitor to optimize the transient response. The ramp amplitude varies with V_{IN} to minimize variation in loop gain across input voltage, commonly referred to as input voltage feedforward. Lastly, the device uses internal circuitry to correct for the dc offset caused by the injected ramp, and significantly reduces the dc offset caused by the output ripple voltage, especially with light load current.

For any control topologies supporting no external compensation, there is a minimum range, maximum range, or both, for the output filter the control topologies can support. The output filter used for a typical buck converter is a low-pass L-C circuit. This L-C filter has double pole that Equation 1 describes.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (1)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency L-C double pole has a 180-degree drop in phase. At the output filter frequency, the gain rolls off at a –40dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40dB to –20dB per decade and increases the phase by 90 degrees per decade above the zero frequency.

The inductor and capacitor selected for the output filter must be such that the f_P double pole of Equation 1 is located no higher than the value given in Table 7-1, then adjusted based on the nominal duty cycle in the application using Equation 2. Equation 2 scales up the $f_{P(TABLE)}$ because, as the duty cycle increases the gain of the D-CAP4 ramp decreases, so the maximum L-C double pole also increases.

$$f_{P(MAX)} = f_{P(TABLE)} \times \left(1 + \left(\frac{V_{OUT}}{V_{IN(typ)}}\right)^2\right) \quad (2)$$

Table 7-1. Maximum L-C Double Pole

SWITCHING FREQUENCY (kHz)	MAXIMUM L-C DOUBLE POLE FREQUENCY (kHz)
600	14.9
800	19.9
1000	24.9
1200	29.9

An L-C double pole frequency that violates these guidelines for each setting can be possible, but must be validated in the application with measurements.

After identifying the application requirements, the output inductance is typically designed so the inductor peak-to-peak ripple current is approximately between 15% and 40% of the maximum output current in the application. Choosing very small output capacitance leads to a high frequency L-C double pole which causes the overall loop gain to stay high until the L-C double pole frequency. Given the zero from the internal ripple generation network is a relatively high frequency as well, the loop with very small output capacitance can have too high of a crossover frequency which can cause instability. In general, where reasonable (or smaller) output capacitance is desired, output ripple requirement and load transient requirement can be used to determine the necessary output capacitance for stable operation.

If MLCCs are used, consider the derating characteristics to determine the final output capacitance for the design. For example, when using an MLCC with specifications of 10µF, X5R and 6.3V, the derating by DC bias and AC bias are 80% and 50%, respectively. The effective derating is the product of these two factors, which in this case is 40% and 4µF. Consult with capacitor manufacturers for specific characteristics of the capacitors to be used in the application.

As a simplified rule, if an output capacitor with an ESR zero that is less than 10 × the L-C double pole frequency, TI recommends to ignore when calculating the L-C double pole frequency for stability purposes. The L-C double pole frequency must be recalculated using only the low ESR MLCCs. For more accurate analysis when using mixed type output capacitors, TI recommends simulations or measurements.

For the maximum output capacitance recommendation, select the inductor and capacitor values so that the L-C double pole frequency is no less than 1/100th of the operating frequency. With this starting point, verify the small signal response on the board using the following criteria: The phase margin at the loop crossover is greater than 45 degrees. The actual maximum output capacitance can go higher as long as phase margin is greater than 45 degrees. However, a small signal measurement (Bode plot) must be done to confirm the design.

For large output filters with an L-C double pole near 1/100th of the operating frequency, additional phase boost can be required. A feedforward capacitor placed in parallel with R_{FB_HS} can boost the phase. See also the *Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor application note*.

Besides boosting the phase, a feedforward capacitor feeds more V_{OUT} node information into the FB node through AC coupling. This feedforward during load transient event enables faster response of the control loop to a V_{OUT} deviation. However, this feedforward during steady state operation also feeds more V_{OUT} ripple and noise into FB. High ripple and noise on FB usually leads to more jitter, or even double-pulse behavior. To determine the final feedforward capacitor value impacts to phase margin, consider load transient performance, ripple, and noise on FB. TI recommends using frequency analysis equipment to measure the crossover frequency and the phase margin.

7.3.2 Internal VCC LDO and Using External Bias On the VCC Pin

The TPS544B28 has an internal 3.0V LDO featuring input from VIN and output to VCC. When the VIN voltage rises above the UVLO threshold ($VIN_{UVLO(R)}$), the internal LDO is enabled and starts regulating output voltage on the VCC pin. The VCC voltage provides the bias voltage for the internal analog and digital circuitry and also provides the supply voltage for the gate drivers.

Bypass the VCC pin with a 1µF, at least 6.3V rating ceramic capacitor. An external bias that is above the output voltage of the internal LDO can override the internal LDO. This override enhances the efficiency of the converter because the VCC current now runs off this external bias instead of the internal linear regulator. An external bias between 3.1V and 4.3V can be used to provide additional efficiency enhancement by reducing the R_{DSON} of the integrated power MOSFETs.

The VCC UVLO circuit monitors the VCC pin voltage and disables the whole converter when VCC falls below the VCC UVLO falling threshold. Maintaining a stable and clean VCC voltage is required for a smooth operation of the device.

Considerations when using an external bias on the VCC pin are as follows:

- When the external bias is applied on the VCC pin early enough (for example, before EN signal comes in), the internal LDO pass device is always off and the internal analog circuits have a stable power supply rail at the power enable.
- This consideration is not recommended. When the external bias is applied on the VCC pin late (for example, after EN signal comes in), any power-up and power-down sequencing can be applied as long as there is no excess current pulled out of the VCC pin. With this sequence, be cautious of external discharge paths on the

VCC pin which can pull a current higher than the current limit of the internal VCC LDO. A load exceeding the current limit of the internal VCC LDO can potentially pull the VCC voltage low and turn off the VCC LDO through the UVLO, thereby shutting down the converter output.

- A good power-up sequence is when at least one of VIN UVLO rising threshold or EN rising threshold is satisfied later than VCC UVLO rising threshold. For example, a practical power-up sequence is: VIN applied first, then the external bias applied, and then EN signal goes high.

7.3.2.1 Powering the Device From a Single Bus

The device works well when powered by a single V_{IN} configuration. In a single V_{IN} configuration, the internal LDO is typically powered by a 5V or 12V bus and generates a 3V output to bias the internal analog circuitry and power MOSFET gate drivers. The V_{IN} input range under this configuration is 2.7V to 16V for up to 20A load current. Figure 7-1 shows an example for this single V_{IN} configuration.

V_{IN} and EN are the two signals to enable the device. For start-up sequence, any sequence between the V_{IN} and EN signals can power the device up correctly.

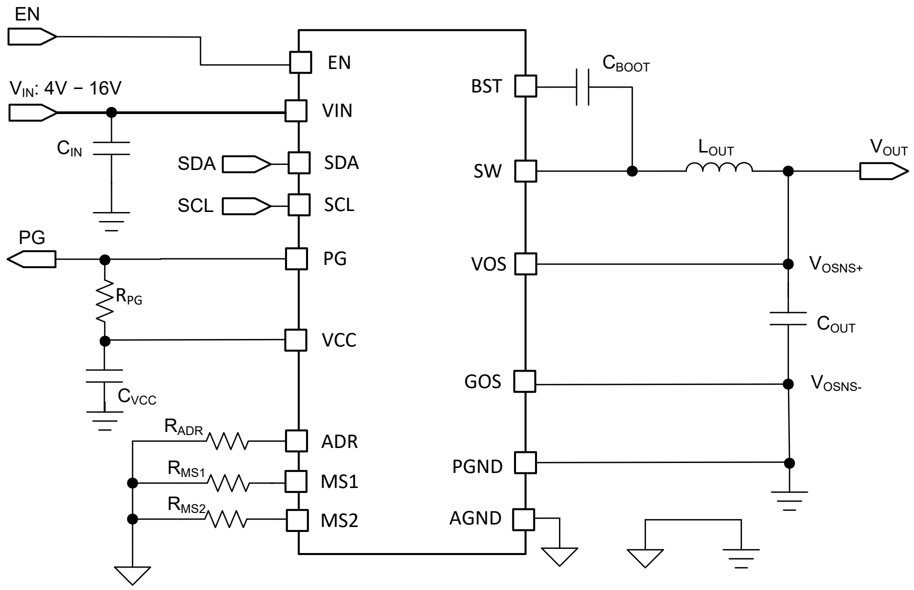


Figure 7-1. Single V_{IN} Configuration for a 12V Bus

7.3.2.2 Powering the Device From a Split-Rail Configuration

When an external bias, which is at a different level from main V_{IN} bus, is applied onto the VCC pin the device can be configured to split-rail by using both the main V_{IN} bus and VCC bias. Connecting a valid VCC bias to VCC pin overrides the internal LDO, thus saves power loss on the internal LDO. This configuration helps to improve overall system level efficiency but requires a valid VCC bias. A 3.3V rail is the common choice as VCC bias. With a stable VCC bias, the recommended V_{IN} input range under this configuration is extended, from 2.7V to 16V.

The noise of the external bias affects the internal analog circuitry. To make sure of a proper operation, a clean, low-noise external bias and good local decoupling capacitor from VCC pin to PGND pin are required. Figure 7-2 shows an example for this split rail configuration.

The VCC external bias current during nominal operation varies with the bias voltage level and also the operating frequency. For example, by setting the device to skip-mode, the VCC pin draws less current from the external bias when the frequency decreases under a light load condition. The typical VCC external bias current under FCCM operation is listed in *Electrical Characteristics.* The external bias must be capable of supplying this current or the external bias voltage can drop and the internal LDO can no longer be overridden.

Under split rail configuration, V_{IN}, VCC bias, and EN are the signals to enable the part. For start-up sequence, TI recommends that at least one of VIN UVLO rising threshold or EN rising threshold is satisfied later than VCC UVLO rising threshold. A practical start-up sequence example is:

1. V_{IN} applied
2. External VCC bias applied
3. EN signal goes high

Similarly, for power-down sequence, TI recommends that at least one of the VIN UVLO falling threshold or the EN falling threshold is satisfied before the external VCC bias supply turns off. If the external VCC bias supply turns off first, the internal LDO of the device prevents the VCC voltage from dropping below 3.0V and be loaded by other circuits powered by the external VCC bias supply.

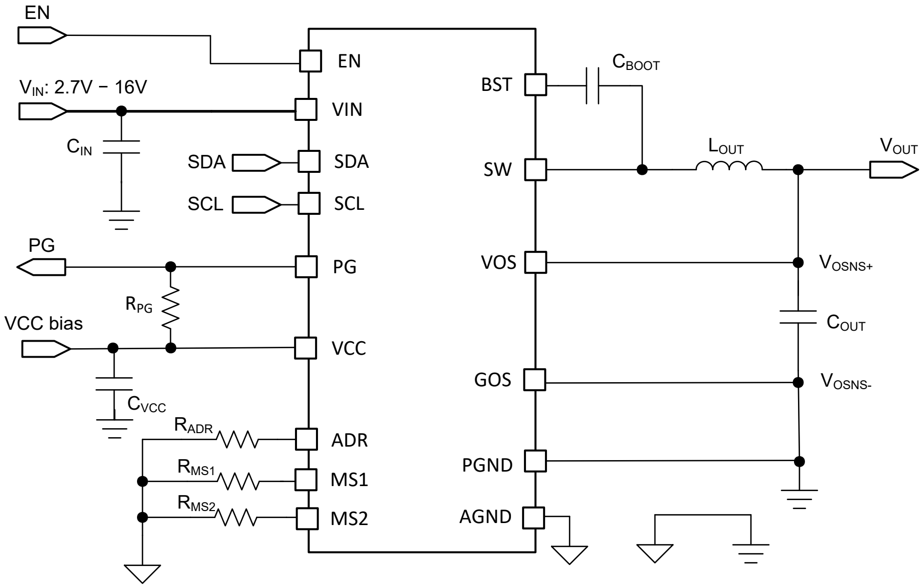


Figure 7-2. Split-Rail Configuration With External VCC Bias

7.3.3 Multifunction Select (MS1) Pin

The device allows users to select the switching frequency, current limit, and soft start time by connecting a resistor from the MS1 pin to AGND pin. Table 7-2 lists the resistor values for the switching frequency, operation mode, and soft start selections. A ±1% tolerance resistor with a typical temperature coefficient of ±100ppm/°C is required for accurate detection across the device operating range.

The MS1 state is set and latched during the internal power-on delay period. Changing the MS1 pin resistance after the power-on delay does not change the status of the device.

To make sure the internal circuit detects the resistor value correctly, *do not* place any capacitor on the MS1 pin.

Table 7-2. MS1 Pin Selection

MS1 PIN RESISTANCE TO AGND (kΩ)	SWITCHING FREQUENCY (f_{SW}) (kHz) (1)	VALLEY CURRENT LIMIT (A)	SS TIME (ms)
0 / GND	600 (2)	21 (2)	1 (2)
0.82	1200	21	1
1.2	600	21	4
1.8	800	21	4
2.2	1200	21	4
2.7	600	18	1
3.3	800	18	1
3.9	1200	18	1
4.7	600	18	4
5.6	800	18	4
6.8	1200	18	4
8.2	600	15	1
10	800	15	1
12	1200	15	1
15	600	15	4
18	800	15	4
22	1200	15	4
27	600	13	1
39	800	13	1
47	1200	13	1
56	600	13	4
68	800	13	4
82	1200	13	4
≥ 118 (FLOAT/VCC)	800	21	1

(1) Switching frequency is based on 3.3V output voltage. Frequency varies with output voltage.
(2) Default value from factory. If NVM is programmed to a different value, the device uses a value that is programmed in the NVM.

7.3.4 Multifunction Select (MS2) Pin

The device allows users to select the output voltage by connecting a resistor from the MS2 pin to AGND pin. Table 7-3 lists the resistor values for output voltage selection. A ±1% tolerance resistor with a typical temperature coefficient of ±100ppm/°C is required for accurate detection across the device operating range.

In addition to expanded output voltage programmability through PMBus, the output voltage can also be set with an external feedback resistor divider using any of the 0.4V to 0.8V VOS/FB pin regulation settings.

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The MS2 state is set and latched during the internal power-on delay period. Changing the MS2 pin resistance after the power-on delay does not change the status of the device.

To make sure the internal circuit detects the resistor value correctly, *do not* place any capacitor on the MS2 pin.

Table 7-3. MS2 Pin Selection

MS2 PIN RESISTANCE TO AGND (kΩ)	VOS/FB PIN REGULATION (V)	SUPPORTS EXTERNAL FEEDBACK
0 / GND	1.0 (1)	No
0.82	0.4	Yes
1.2	0.45	Yes
1.8	0.5	Yes
2.2	0.55	Yes
2.7	0.6	Yes
3.3	0.65	Yes
3.9	0.7	Yes
4.7	0.75	Yes
5.6	0.8	Yes
6.8	0.85	No
8.2	0.9	No
10	0.95	No
12	1.05	No
15	1.10	No
18	1.15	No
22	1.20	No
27	1.25	No
39	1.3	No
47	1.5	No
56	1.8	No
68	2.5	No
82	5.0	No
≥118 (FLOAT/VCC)	3.3	No

(1) Defualt value from factory. If NVM is programmed to a different value, the device uses a value that is programmed in the NVM.

7.3.5 Address (ADR) Pin

The device allows users to select the PMBus device address and Fault Recovery Mode by connecting a resistor from the ADR pin to AGND pin. Table 7-3 lists the resistor values for address and fault recovery mode selection. A ±1% tolerance resistor with a typical temperature coefficient of ±100ppm/°C is required for accurate detection across the device operating range.

The ADR state is set and latched during the internal power-on delay period. Changing the ADR pin resistance after the power-on delay does not change the status of the device.

To make sure the internal circuit detects the resistor value correctly, *do not* place any capacitor on the ADFR pin.

Table 7-4. ADR Pin Selection

ADR PIN RESISTANCE TO AGND (kΩ)	PMBus® ADDRESS	FAULT RECOVERY MODE
0	0x21h	Hiccup
0.82	0x22h	Hiccup
1.2	0x23h	Hiccup
1.8	0x24h	Hiccup
2.2	0x25h	Hiccup
2.7	0x26h	Hiccup
3.3	0x29h	Hiccup
3.9	0x2Ah	Hiccup
4.7	0x2Bh	Hiccup
5.6	0x2Ch	Hiccup
6.8	0x2Dh	Hiccup
8.2	0x2Eh	Hiccup
10	0x21h	Latch Off
12	0x22h	Latch Off
15	0x23h	Latch Off
18	0x24h	Latch Off
22	0x25h	Latch Off
27	0x26h	Latch Off
39	0x29h	Latch Off
47	0x2Ah	Latch Off
56	0x2Bh	Latch Off
68	0x2Ch	Latch Off
82	0x2Dh	Latch Off
≥118 (FLOAT/VCC)	0x2Eh	Latch Off

7.3.6 Enable

When the EN pin voltage rises above the enable threshold voltage ($V_{EN(R)}$) and VIN rises above the VIN UVLO rising threshold, the device enters the internal power-up sequence.

The EN pin has an internal filter to avoid unexpected ON or OFF due to small glitches. The time constant of this RC filter is 2μs. For example, when applying 3.3V voltage source on the EN pin that jumps from 0V to 3.3V with an ideal rising edge, the internal EN signal reaches 2.1V after 2μs, which is 63.2% of applied 3.3V voltage level.

An internal pulldown resistor is implemented between the EN pin and AGND pin. With this pulldown resistor, floating the EN pin before start-up keeps the device in the disabled state. A resistor divider to the EN pin can be used to increase the input voltage the device begins the start-up sequence. The internal pulldown resistor must be accounted for when using an external resistor divider. To reduce impact to the EN rising and falling threshold, this internal pulldown resistor is 1MΩ. During nominal operation when the power stage switches, this large internal pulldown resistor can not have enough noise immunity to hold EN pin low for the device to enter the disabled state.

If an external resistor divider is connected to the EN pin, an additional 5μA current source is activated when the EN voltage exceeds the rising threshold to provide a programmable hysteresis based on the enable falling threshold voltage ($V_{EN(F)}$) and external resistors.

The recommended operating condition for the EN pin is a maximum of 5.5V. *Do not* connect the EN pin to the VIN pin directly if VIN can exceed 5.5V.

7.3.7 Soft Start

The device implements a selectable (0.5ms, 1ms, 2ms, or 4ms) soft-start time which can be configured via pinstrap or digitally.

7.3.8 Power Good

The device has a power-good (PG or PGOOD) output that goes high to indicate when the converter output is in regulation. The power-good output is an open-drain output and must be pulled up to the VCC pin or an external voltage source (< 5.5V) through a pullup resistor (typically 30.1kΩ) to go high. The recommended power-good pullup resistor value is 1kΩ to 100kΩ.

Note

For systems using an external voltage source to pull up the PG pin, TI recommends that this same external voltage source also be used to bias the VCC pin.

After the soft-start ramp finishes, the power-good signal becomes high after a internal delay t_{PG_DLY}. An internal soft-start done signal goes high when the SS voltage reaches $V_{SS(DONE)}$ to indicate the soft-start ramp has finished. If the FB voltage drops to 85% of the V_{REF} voltage or exceeds 110% of the V_{REF} voltage, the power-good signal latches low after a 4µs internal delay. The power-good signal can only be pulled high again after re-toggling EN or a reset of VIN.

If an OV event causes the FB voltage to exceed the OV threshold during soft start, but the FB voltage drops below the OV threshold before soft-start is completed, the power-good signal does not latch low until FB exceeds the OV threshold or drops below UV threshold. The OV or UV event must occur after the soft-start ramp finishes for the power-good signal to latch low. FB exceeding the OV threshold during soft start does, however, trigger the OV fault, and the devices response to OV (described in *Overvoltage and Undervoltage Protection*) typically pulls the output voltage below the UV threshold.

If the input supply fails to power up the device (for example, VIN and VCC both stay at zero volts) and this pin is pulled up through an external resistor, the power-good pin clamps low to the low-level specified in the POWER GOOD section in the *Electrical Characteristics*

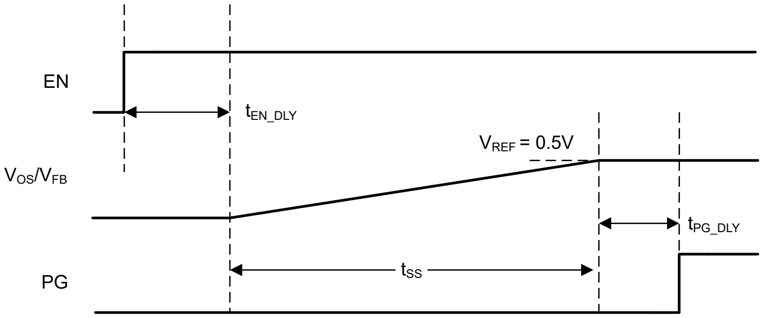

Figure 7-3. EN, SS, & PG Timing Diagram

7.3.9 Overvoltage and Undervoltage Protection

The device monitors a resistor-divided feedback voltage to detect overvoltage and undervoltage events. The OVP function enables when the output is enabled. The UVP function enables after the soft-start period is complete.

After soft-start is complete, if the FB voltage becomes lower than 85% of the V_{REF} voltage, the UVP comparator trips and an internal UVP delay counter begins counting. After the 70µs UVP delay time, depending on the selected fault recovery mode, the device either hiccups and re-starts after a sleep time of 56ms or latches off both high-side and low-side MOSFETs. The latch-off fault can be cleared with a reset of VIN or by toggling the EN pin.

When the output is enabled, the FB voltage must rise above the 90% PG low-to-high threshold to clear the UVP comparator. If the FB voltage does not exceed the 90% threshold by the end of the soft-start period, the device responds to the undervoltage event.

During the UVP delay time, if the FB voltage becomes higher than the 90% PG low-to-high threshold, the undervoltage event is cleared and the timer is reset to zero. When the output voltage falls below the 85% UVP threshold again, the 70-µs timer re-starts.

When the FB voltage becomes higher than 110% of the V_{REF} voltage, the OVP comparator trips and the circuit latches the fault condition and drives the PG pin low. The high-side MOSFET turns off and the low-side MOSFET turns on until reaching a negative current limit I_{NOCL}. Upon reaching the negative current limit, the low-side MOSFET is turned off, and the high-side MOSFET is turned on again, for a proper on-time (determined by $V_O/V_{IN}/f_{SW}$). The device operates in this mode until the output voltage is pulled down under the UVP threshold. The device then responds to the undervoltage event as described above.

If there is an overvoltage condition prior to the output being enabled (such as a high prebiased output), the device responds to the overvoltage event as described above at the beginning of the soft-start period. The device waits until the completion of the soft-start period for UVP to be enabled, and depending on the selected fault recovery mode, the device either hiccups and re-starts after a sleep time of 14 × the soft-start period or latches off .

7.3.10 Output Voltage Setting (External Feedback Configuration)

When pinstrapped for external feedback support, the output voltage is programmed by voltage-divider resistors, R_{FB_T} and R_{FB_B}. Connect R_{FB_T} between the FB pin and the positive node of the load, and connect R_{FB_B} between the FB pin and GOS pin. The FB pin is regulated to the internal reference (V_{REF}). The recommended R_{FB_B} value is 10kΩ, ranging from 1kΩ to 20kΩ. Use Equation 3 to determine R_{FB_T}.

$$R_{FB\_T} = \frac{V_O - V_{FB\_REG}}{V_{FB\_REG}} \times R_{FB\_B} \quad (3)$$

To improve the overall V_{OUT} accuracy, using ±1% accuracy or better resistors for the FB voltage divider is highly recommended. The FB voltage divider resistors must be kept near the device to minimize the trace length connected to the FB pin. The connections from the top of R_{FB_T} & GOS to the remote location must be a pair of PCB traces with Kelvin sensing across a high-frequency bypass capacitor of 0.1µF or higher. To maintain stable output voltage and minimize the ripple, the pair of remote sensing lines must stay away from any noise sources such as inductor and SW nodes, or high frequency clock lines.

Single-ended V_{OUT} sensing is often used for local sensing. For this configuration, connect the higher FB resistor, R_{FB_T}, to a high-frequency local bypass capacitor of 0.1µF or higher, and short GOS to AGND. Regardless of remote sensing or single-ended sensing, the FB voltage divider, RFB_T and RFB_B, must always be placed as close as possible to the device.

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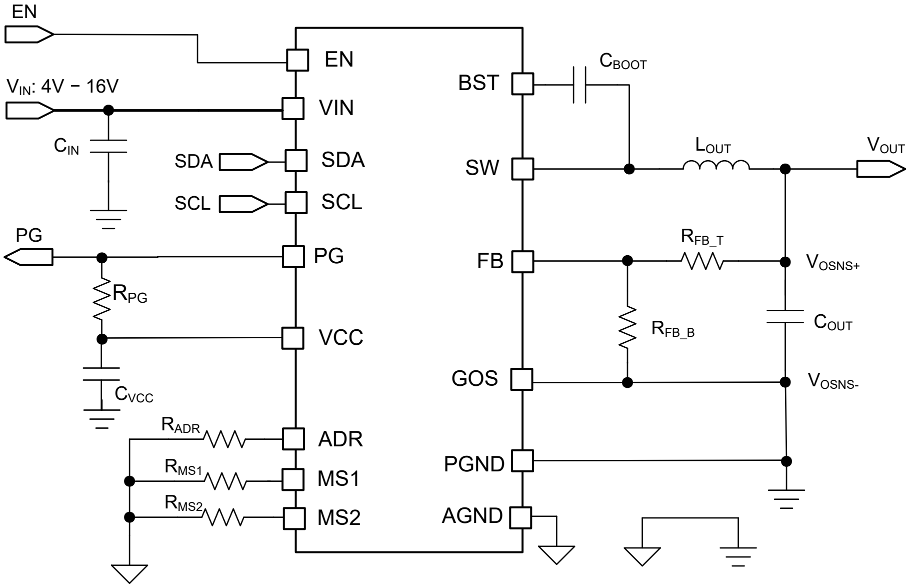

Figure 7-4. Output Voltage Setting through External Feedback With Remote Sense

7.3.11 Remote Sense

The device integrates a remote sense amplifier across the VOS/FB and GOS pins. The remote sense function compensates for voltage drop on the PCB traces helping to maintain V_{OUT} accuracy under steady state operation and load transient events.

The connections from the VOS & GOS pins to the remote location must be a pair of PCB traces with Kelvin sensing across a high-frequency local bypass capacitor of 0.1µF or higher. To maintain stable output voltage and minimize the ripple, the pair of remote sensing lines must stay away from any noise sources such as inductor and SW nodes, or high frequency clock lines. TI recommends to shield the pair of remote sensing lines with ground planes above and below.

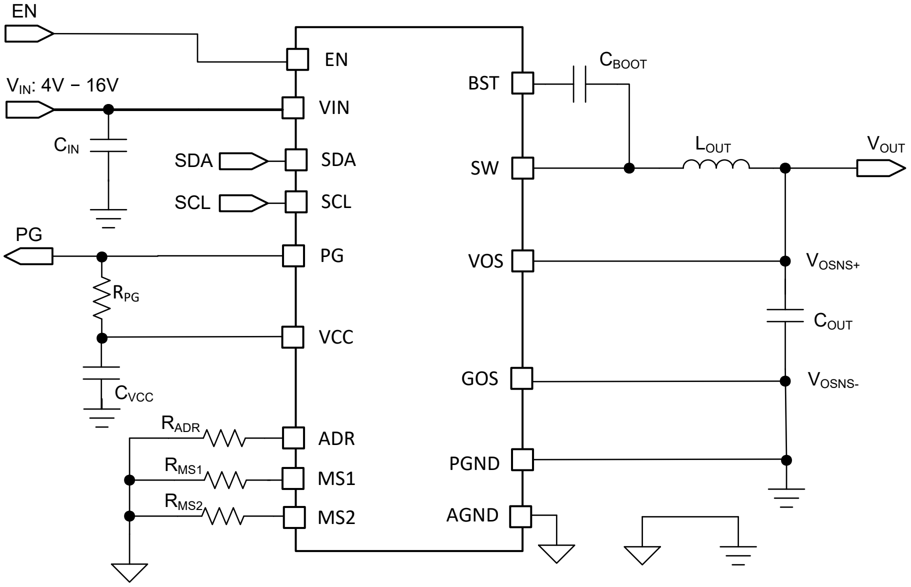

Figure 7-5. Output Voltage Setting through Internal Feedback and Remote Sense

The recommended GOS operating range (relative to the AGND pin) is –100mV to +100mV.

7.3.12 Low-side MOSFET Zero-Crossing

The device uses a zero-crossing (ZC) circuit to perform the zero inductor current detection during skip-mode operation. The ZC threshold is set to a small negative value before the low-side MOSFET is turned off, entering discontinuous conduction mode (DCM) operation. After entering DCM, the ZC threshold hysteresis increases the threshold to a small positive value after entering DCM. As a result, the device delivers better light-load efficiency.

When the load current increases enough such that the device exits DCM, the ZC circuit must detect 16 consecutive cycles of negative inductor current below the ZC threshold before returning to DCM. Only one cycle without ZC detection is required to exit DCM.

When the output is enabled, the ZC circuit is also enabled during the first 32 switching cycles while the device is in soft start. If the device is configured for FCCM, ZC is disabled and the device transitions to FCCM when soft start is complete. See *Soft Start* for a description on soft-start completion. If there are not at least 32 switching cycles before soft-start is done, such as during start-up with a high output prebias, the ZC is not disabled until the first high-side MOSFET on-time after soft-start done is complete.

7.3.13 Current Sense and Positive Overcurrent Protection

For a buck converter, during the on-time of the high-side MOSFET, the switch current increases at a linear rate determined by the input voltage, output voltage, on-time, and output inductor value. During the on-time of the low-side MOSFET, the current decreases linearly. The average value of the switch current equals the load current.

The output overcurrent limit (OCL) in the device is implemented using a cycle-by-cycle valley current detect control circuit. The inductor current is monitored during the on-time of the low-side MOSFET by measuring the low-side MOSFET drain-to-source current. If the measured drain-to-source current of the low-side MOSFET is above the current limit threshold, the low-side MOSFET stays ON until the current level becomes lower than the current limit threshold. This type of behavior reduces the average output current sourced by the device.

During an overcurrent condition, the current to the load exceeds the current to the output capacitors. Thus, the output voltage tends to decrease. Eventually, when the output voltage falls below the undervoltage-protection threshold (85%), the UVP comparator detects the fall and shuts down the device after a wait time of 70 µs. Depending on the fault recovery configuration, the device either hiccups or latches off, as described in *Overvoltage and Undervoltage Protection*

Note

If an OCL condition happens during start-up, the device still has cycle-by-cycle current limit based on low-side valley current, but the UVP comparator does not shut down the device until after soft start has completed.

7.3.14 Low-side MOSFET Negative Current Limit

The device has a fixed, cycle-by-cycle negative overcurrent limit ($I_{LS(NOC)}$). Similar with the positive overcurrent limit, the inductor current is monitored during the on-time of the low-side MOSFET. To prevent too large negative current flowing through the low-side MOSFET, when the device detects a –9A current (typical threshold) through the low-side MOSFET, the device turns off the low-side MOSFET and then turns on the high-side MOSFET for the on-time set by the one-shot timer (determined by $V_{IN}/V_{OUT}/f_{SW}$). After the high-side MOSFET on-time expires, the low-side MOSFET turns on again.

The device must not trigger the –9A negative current limit threshold during nominal operation, unless a small inductor value that is too small is chosen or the inductor becomes saturated. This negative current limit is used to discharge output capacitors after an output OVP event. See also *Overvoltage and Undervoltage*.

7.3.15 Output Voltage Discharge

When the device is disabled through EN, the device enables the output voltage discharge mode. This mode forces both high-side and low-side MOSFETs to latch off, but turns on the internal discharge MOSFET, which is connected from SW to PGND, to discharge the output voltage. After the FB voltage drops below 50mV, the discharge MOSFET and the internal VCC LDO is turned off.

When the EN pin goes low to disable the converter and while the VCC voltage is sufficient to turn on the discharge switch, the output voltage discharge mode is activated.

7.3.16 UVLO Protection

The device monitors the voltage on both the VIN and the VCC pins. If the VCC pin voltage is lower than the VCC_{UVLO} falling threshold voltage, the device shuts off. If the VCC voltage increases beyond the VCC_{UVLO} rising threshold voltage, the device turns back on. VCC UVLO is a non-latch protection.

When the VIN pin voltage is lower than the VIN_{UVLO} falling threshold voltage but the VCC pin voltage is still higher than VCC_{UVLO} rising threshold voltage, the device stops switching and discharges the SS pin. After the VIN voltage increases beyond the VIN_{UVLO} rising threshold voltage, the device re-initiates the soft start and switches again. VIN UVLO is a non-latch protection.

7.3.17 Thermal Shutdown

The device monitors internal junction temperature. If the temperature exceeds the threshold value (typically 165°C), the device stops switching and discharges the SS pin. When the temperature falls approximately 15°C below the threshold value, the device turns back on with a re-initiated soft start. Thermal shutdown is a non-latch protection.

7.4 Device Functional Modes

7.4.1 Auto-Skip (PFM) Eco-mode Light Load Operation

If Skip (PFM)-mode is selected through the PMBus interface, the device automatically reduces the switching frequency at light-load conditions to maintain high efficiency. See the *Programming Registers* section on how to select the PFM mode.

As the output current decreases from heavy load condition, the inductor current also decreases until the valley of the inductor ripple current touches the zero-crossing threshold (*Low-side MOSFET Zero-Crossing*). The zero-crossing threshold sets the boundary between the continuous-conduction and discontinuous-conduction modes. The synchronous MOSFET turns off when this zero-crossing threshold is detected. As the load current decreases further, the converter runs into discontinuous-conduction mode (DCM). The on-time is maintained to a level approximately the same as during continuous-conduction mode operation so that discharging the output capacitor with a smaller load current to the level of the reference voltage requires more time. Use Equation 4 to calculate the transition point to light-load operation $I_{OUT(LL)}$ (for example: the boundary between continuous- and discontinuous-conduction mode).

For low output ripple, TI recommends using only ceramic output capacitors for designs that operate in skip-mode.

$$I_{OUT(LL)} = \frac{1}{2} \times \frac{(V_{IN} - V_O) \times V_O}{V_{IN}} \times \frac{1}{L \times f_{SW}} \tag{4}$$

7.4.2 Forced Continuous-Conduction Mode

If FCCM mode is selected through the PMBus interface, the controller operates in continuous-conduction mode (CCM) during light-load conditions. See the *Programming Registers* section on how to select the FCCM mode.

During FCCM, the switching frequency is maintained to an almost constant level over the entire load range, which is designed for applications requiring tight control of the switching frequency and output ripple at the cost of reduced light-load efficiency. Use Equation 4 to calculate the typical light-load operation boundary. Below this calculated load current, the device operates in FCCM.

8 Programming Registers

The Supported PMBus Registers and Default Values Table lists the implemented registers and also the default for the bit behavior and register values.

Table 8-1. Supported PMBus® Register and Default Values

REGISTER ADDRESS	REGISTER NAME	R/W	NVM	DEFAULT VALUE (HEX)	DEFAULT BEHAVIOR
01h	OPERATION	R/W	NO	00h	Defines the operation of the device.
02h	ON_OFF_CONFIG	R/W	YES	12h	Turn ON/OFF by CNTL pin.
03h	CLEAR_FAULTS	W	NO	N/A	Clear all faults.
10h	WRITE_PROTECT	R/W	YES	00h	All commands are writable.
15h	STORE_USER_ALL	W	NO	N/A	Stores all current storable register settings into NVM.
16h	RESTORE_USER_ALL	W	NO	N/A	Restores all storable register settings from NVM.
19h	CAPABILITY	R	NO	C0h	PEC and 1MHz support.
20h	VOUT_MODE	R	NO	96h	Indicates the device is relative format with an exponent value of -10 for an equivalent LSB of 0.976mV.
21h	VOUT_COMMAND	R/W	NO	VBOOT	Set the output voltage through PMBus.
25h	VOUT_MARGIN_HIGH	R/W	YES	210h	Sets the margin high percentage when selected in OPERATION register.
26h	VOUT_MARGIN_LOW	R/W	YES	1F0h	Sets the margin low percentage when selected in OPERATION register.
27h	VOUT_TRANSITION_RATE	R/W	YES	E81Ah	Sets the rate in mV/µs the output changes voltage.
29h	VOUT_SCALE_LOOP	R	NO	VBOOT	Sets the feedback resistor ratio.
33h	FREQUENCY_SWITCH	R/W	YES	R_{MS2}	Sets the switching frequency with default set to 800kHz
41h	VOUT_OV_FAULT_RESPONSE	R/W	YES	R_{MS2}	Latch-off after a fault.
45h	VOUT_UV_FAULT_RESPONSE	R/W	YES	R_{MS2}	Latch-off after a fault, and the response delay before disabling the power conversion is 2µs.
46h	IOUT_OC_FAULT_RESPONSE	R/W	YES	R_{MS2}	Low-side valley current limiting threshold = 100%, changed by pin strap.
60h	TON_DELAY	R/W	YES	0000h	50µs delay when a start condition is received (as programmed by the ON_OFF_CONFIG register) until the output voltage starts to rise.
61h	TON_RISE	R/W	YES	F800h	0.5ms from when the output starts to rise until the output voltage has entered the regulation band.
64h	TOFF_DELAY	R/W	YES	0000h	0ms from when a stop condition is received (as programmed by the ON_OFF_CONFIG register) until the unit starts the soft-stop operation.
65h	TOFF_FALL	R	NO	F800h	Same as TON_RISE setting.
78h	STATUS_BYTE	R	NO	40h	Status is device is OFF.
79h	STATUS_WORD	R	NO	2800h	VIN is off and PGOOD_Z is 1b.
7Eh	STATUS_CML	R/W	NO	0h	Current status
80h	STATUS_MFR_SPECIFIC	R/W	YES	0h	Manufacture specific status.
8Bh	READ_VOUT	R	NO	N/A	Measured output voltage.
8Ch	READ_IOUT	R	NO	N/A	Measured output current.
8Dh	READ_TEMP1	R	NO	N/A	Measured Controller die temperature.
98h	PMBUS_REVISION	R	NO	55h	PMBus Revision
99h	MFR_ID	R	NO	4954h	ASCII for "TI"
9Ah	MFR_MODEL	R	NO	00234C54h	Device model
9Bh	MFR_REVISION	R/W	YES	00h	Device revision
ADh	IC_DEVICE_ID	R	NO	00234C544954h	IC part number
AEh	IC_DEVICE_REV	R	NO	00h	IC revision
D1h	SYS_CFG_USER1	R/W	YES	00h	Miscellaneous system configuration settings.
D2h	PASSKEY	R/W	YES	00h	Customer programmable lock access code.
D4h	COMP	R/W	YES	00h	Feedback compensation settings.

Table 8-1. Supported PMBus® Register and Default Values (continued)

REGISTER ADDRESS	REGISTER NAME	R/W	NVM	DEFAULT VALUE (HEX)	DEFAULT BEHAVIOR
D5h	VBOOT	R/W	YES	R_{MS1}	Set by pin strap, can be written through PMBus. When external divider is selected, VBOOT is the reference voltage at the FB pin.
D9h	NVM_CHECKSUM	R	NO	0000h	CRC value from reading contents of the non-volatile memory.
FCh	FUSION_ID0	R	NO	02C0h	Device Identification used by FUSION.
FDh	FUSION_ID1	R	NO	4B434F4C4945h	Device Identification used by FUSION.

8.1 OPERATION (Address = 1h) [Reset = 00h]

OPERATION (Address = 1h) [Reset = 00h]

OPERATION is shown in Section 8.1 and described in Section 8.1.

Write Transaction: Write Byte
Read Transaction: Read Byte
Data Format: Unsigned Binary (1 byte)
NVM Back-up: No
Updates: On-the-fly

The OPERATION command is used to turn the device output on or off, in conjunction with the input from the EN pin, according to the configuration of the ON_OFF_CONFIG command. It is also used to set the output voltage to the upper or lower MARGIN levels, and select soft-stop when turned off through OPERATION.

Figure 8-1. OPERATION

7	6	5	4	3	2	1	0
ON	OFF	MARGIN				RESERVED	
R/W-0h	R/W-0h	R/W-0h				R-0h	

Table 8-2. OPERATION Field Descriptions

Bit	Field	Type	Reset	Description
7	ON	R/W	0h	Turn the device output on or off when the ON_OFF_CONFIG command is configured with its CMD bit high. There can be several other requirements that must be satisfied before the power conversion can begin. The input voltages must be above their UVLO thresholds and, if the CPR bit in ON_OFF_CONFIG is high, the enable pin must be high. 0h = The device output is off 1h = The device output is on
6	OFF	R/W	0h	Sets the turn-off behavior when commanding the device output off via OPERATION[7] (the ON bit transitions from 1 to 0) and when the ON_OFF_CONFIG command is configured with its CMD bit high. If the ON bit is 1, then the OFF bit is ignored. 0h = Immediately turn the device output off forcing the power stage to a high-Z state, not honoring the programmed TOFF_DELAY and programmed TOFF_FALL, when commanded off via OPERATION[7]. 1h = Soft off. Use the programmed turn-off delay in TOFF_DELAY and ramp down in TOFF_FALL when commanded off via OPERATION[7].
5:2	MARGIN	R/W	0h	Sets the margin state, independent of the OPERATION[7] bit value. Values other than those listed below are invalid/unsupported data. If margin is off, the output voltage source is VOUT_COMMAND and OV/UV faults behave normally as programmed in their respective fault response registers. 0h = Margin off and faults behave as programmed. 1h = Margin off and faults behave as programmed. 2h = Margin off and faults behave as programmed. 3h = Margin off and faults behave as programmed. 5h = Margin low (Ignore fault). Output voltage target uses VOUT_MARGIN_LOW. UV faults are ignored and do not trigger shut-down, but will trigger STATUS updates. 6h = Margin low (Act on fault). Output voltage target uses VOUT_MARGIN_LOW. OV/UV faults trigger per their respective fault response settings. 9h = Margin high (Ignore fault). Output voltage target uses VOUT_MARGIN_HIGH. OV faults are ignored and do not trigger shut-down, but will trigger STATUS updates. Ah = Margin high (Act on fault). Output voltage target uses VOUT_MARGIN_HIGH. OV/UV faults trigger per their respective fault response settings.

Table 8-2. OPERATION Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	RESERVED	R	0h	Reserved

8.2 ON_OFF_CONFIG (Address = 2h) [Reset = XXh]

ON_OFF_CONFIG is shown in Figure 8-2 and described in Table 8-3.

Write Transaction: Write Byte
Read Transaction: Read Byte
Data Format: Unsigned Binary (1 byte)
NVM Back-up: EEPROM
Updates: On-the-fly

The ON_OFF_CONFIG command configures the combination of enable pin input and serial bus commands needed to turn the device output on and off. This includes how the unit responds when power is applied to VIN. For the purposes of ON_OFF_CONFIG, the device EN pin is the CONTROL pin.

Figure 8-2. ON_OFF_CONFIG

7	6	5	4	3	2	1	0
RESERVED			PU	CMD	CPR	POL	CPA
R-0h			R/W-Xh	R/W-Xh	R/W-Xh	R-1h	R/W-Xh

Table 8-3. ON_OFF_CONFIG Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0h	Reserved
4	PU	R/W	0h	Sets the default to either turn on the device output any time power is present, or for the device output on and off to be controlled by the CONTROL pin and/or the OPERATION command. On reset the value will be determined by NVM. 0h = Device output turns on any time sufficient input power is present regardless of state of the CONTROL pin or OPERATION command.
3	CMD	R/W	0h	The CMD bit sets how the device responds to the OPERATION command. On reset the value will be determined by NVM. 0h = Device ignores the ON bit in the OPERATION command. 1h = Device responds to the ON bit being set high in the OPERATION command (and the CONTROL pin if configured by CPR) to enable the device output.
2	CPR	R/W	0h	The CPR bit sets the CONTROL pin response. On reset the value will be determined by NVM. 0h = Device ignores the CONTROL pin to enable its output. 1h = The device output responds to the CONTROL pin.
1	POL	R	1h	The POL bit sets the polarity of the CONTROL pin. 1h = The CONTROL pin has active high polarity.
0	CPA	R/W	0h	The CPA bit sets the CONTROL pin action when the device output is turned off with the CONTROL pin. The device must be configured to respond to the CONTROL pin through the CPR bit. On reset the value will be determined by NVM. 0h = When the output is turned off by the CONTROL pin, continue regulating for the time programmed into TOFF_DELAY and ramp down in the time programmed into TOFF_FALL. 1h = When the output is turned off by the CONTROL pin, immediately turn off the output.

8.3 CLEAR_FAULTS (Address = 3h) [Reset = 00h]

CLEAR_FAULTS is shown in Figure 8-3 and described in Table 8-4.

Write Transaction: Send Byte
Read Transaction:N/A
Data Format: Data-less
NVM Back-up: No
Updates: On-the-fly

CLEAR_FAULTS is a command used to clear any fault bits that have been set. This command clears all bits in all status registers. At the same time, the device releases its SMB_ALERT# signal output if SMB_ALERT# is asserted. CLEAR_FAULTS is a write-only command with no data.

The CLEAR_FAULTS command does not cause a unit that has latched off for a fault condition to restart. If the fault is still present when the bit is cleared, the fault bit is immediately set again and the host is notified by the usual means

If the device responds to an Alert Response Address (ARA) from the host, it will clear SMB_ALERT# but not the offending status bit or bits (as it has successfully notified the host and then expects the host to handle the interrupt appropriately). The original fault (and any faults that occur between the initial assertion of SMB_ALERT# and the successful response of the device to the ARA) must be cleared (through CLEAR_FAULTS, turning on the output through the mechanism programmed into ON_OFF_CONFIG, writing 1b to the status bits set, or power reset) before any of these sources are allowed to re-trigger SMB_ALERT#. However, fault sources which become active after the device response to the ARA trigger SMB_ALERT#.

Figure 8-3. CLEAR_FAULTS

<table>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="8">CLEAR_FAULTS</td></tr>
<tr><td colspan="8">W-0h</td></tr>
</table>

Table 8-4. CLEAR_FAULTS Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CLEAR_FAULTS	W	0h	N/A

8.4 WRITE_PROTECT (Address = 10h) [Reset = 00h]

WRITE_PROTECT is shown in Figure 8-4 and described in Table 8-5.

Write Transaction: Write Byte
Read Transaction: Read Byte
Data Format: Unsigned Binary (1 byte)
NVM Back-up: EEPROM
Updates: On-the-fly

The WRITE_PROTECT command is used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. This command is not intended to provide protection against deliberate or malicious changes to a devices configuration or operation. All supported commands may have their parameters read, regardless of the WRITE_PROTECT settings.

Note

Send Byte commands such as CLEAR_FAULTS, STORE_USER_ALL and RESTORE_USER_ALL shall be blocked by write protection unless listed as an allowed command. When RESTORE_USER_ALL is blocked, restore after power-up must still be allowed.

Figure 8-4. WRITE_PROTECT

7	6	5	4	3	2	1	0
PROTECTION			RESERVED				
R/W-0h			R-0h				

Table 8-5. WRITE_PROTECT Field Descriptions

Bit	Field	Type	Reset	Description
7:5	PROTECTION	R/W	0h	On reset the value will be determined by NVM. 0h = Enable writes to all commands. 1h = Disables all WRITES except to the WRITE_PROTECT, STORE_USER_ALL, OPERATION, ON_OFF_CONFIG, VOUT_COMMAND and PASSKEY commands. 2h = Disables all WRITES except to the WRITE_PROTECT, STORE_USER_ALL, OPERATION and PASSKEY commands. 4h = Disables all WRITES except to the WRITE_PROTECT, STORE_USER_ALL and PASSKEY commands.
4:0	RESERVED	R	0h	Reserved

8.5 STORE_USER_ALL (Address = 15h) [Reset = 00h]

STORE_USER_ALL is shown in Figure 8-5 and described in Table 8-6.

Write Transaction: Send Byte
Read Transaction: N/A
Data Format: Data-less
NVM Back-up: No
Updates: On-the-fly

The STORE_USER_ALL command stores all of the current storable register settings in the EEPROM memory as the new defaults on power up.

Due to the EEPROM programming time, the duration of this command is approximately 125ms. For any incoming PMBus traffic while the device is busy programming EEPROM, the device will ACK its device address; but, NACK any other bytes (as well as returns all 1s for data) per PMBus Part II section 10.8.7. The device will not set any status for NACKd transactions during EEPROM programming.

EEPROM programming faults will set the cml bit in the (78h) STATUS_BYTE and the oth bit in the STATUS_CML registers.

TI recommends disabling regulation and waiting a minimum of 125 ms before continuing with programming.

Figure 8-5. STORE_USER_ALL

7	6	5	4	3	2	1	0
STORE_USER_ALL							
W-0h							

Table 8-6. STORE_USER_ALL Field Descriptions

Bit	Field	Type	Reset	Description
7:0	STORE_USER_ALL	W	0h	N/A

8.6 RESTORE_USER_ALL (Address = 16h) [Reset = 00h]

RESTORE_USER_ALL is shown in Figure 8-6 and described in Table 8-7.

Write Transaction: Send Byte
Read Transaction: N/A
Data Format: Data-less
NVM Back-up: No
Updates: On-the-fly

The RESTORE_USER_ALL command instructs the PMBus device to copy the entire contents of the non-volatile User Store Memory to the matching locations in the Operating Memory. Additionally, any values set through a Pin Detection during the last power-cycle will overwrite the values in Operating Memory, also overwriting the value retrieved from the User Store. However if a correspinding Pin Detection override bit is set, the value from User Store is not overwritten with the value from Pin Detection

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Note

It is permitted to use the RESTORE_USER_ALL command while the output is enabled. However, PMBus commands will be ignored during the copy operation and there can be unpredictable, undesirable or even catastrophic results if done while the output is enabled. TI recommendeds to turn the device output off before issuing this command through the method programmed into ON_OFF_CONFIG.

Figure 8-6. RESTORE_USER_ALL

7	6	5	4	3	2	1	0
RESTORE_USER_ALL							
W-0h							

Table 8-7. RESTORE_USER_ALL Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RESTORE_USER_ALL	W	0h	N/A

8.7 CAPABILITY (Address = 19h) [Reset = C0h]

CAPABILITY is shown in Figure 8-7 and described in Table 8-8.

Write Transaction: N/A
Read Transaction: Read Byte
Data Format: Unsigned Binary (1 byte)
NVM Back-up: No
Updates: N/A

This command provides a way for a host system to determine some key capabilities of this PMBus device.

Figure 8-7. CAPABILITY

7	6	5	4	3	2	1	0
PEC	SPD		ALRT	FORMAT	AVS	RESERVED	
R-1h	R-2h		R-0h	R-0h	R-0h	R-0h	

Table 8-8. CAPABILITY Field Descriptions

Bit	Field	Type	Reset	Description
7	PEC	R	1h	1h = Packet Error Checking is supported.
6:5	SPD	R	2h	2h = The maximum supported bus speed is 1MHz.
4	ALRT	R	0h	0h = This device does not have a SMB_ALERT# pin and does not support the SMBus Alert Response Protocol.
3	FORMAT	R	0h	0h = This device supports LINEAR11, ULINEAR16, SLINEAR16, or DIRECT format (as against the IEEE Half Precision Floating Point Format).
2	AVS	R	0h	0h = Indicates that AVSBus is not supported.
1:0	RESERVED	R	0h	Reserved

8.8 VOUT_MODE (Address = 20h) [Reset = 96h]

VOUT_MODE is shown in Figure 8-8 and described in Table 8-9.

Write Transaction: N/A
Read Transaction: Read Byte
Data Format: Unsigned Binary (1 byte)
NVM Back-up: No
Updates: N/A

The PMBus spec dictates that the data word for the VOUT_MODE command is one byte that consists of a 3-bit Mode and 5-bit parameter. VOUT_MODE is a standard PMBus configuration in the linear format (that has approximately 0.976mV steps). Bit 7 is hardwired to 1 to indicate voltage related commands are to use a relative percentage of vout_command as opposed to absolute values. Reference PMBus Part II, rev 1.5 section 8.5 for additional information.

Data Validity: Attempts to write the VOUT_MODE command shall be considered as invalid data or unsupported data (ivd) and the device shall respond as described in ivd.

Figure 8-8. VOUT_MODE

7	6	5	4	3	2	1	0
VOUT_MODE			VOUT_EXPONENT				
R-4h			R-16h				

Table 8-9. VOUT_MODE Field Descriptions

Bit	Field	Type	Reset	Description
7:5	VOUT_MODE	R	4h	4h = Relative Mode, Linear Format (ULINEAR16, SLINEAR16).
4:0	VOUT_EXPONENT	R	16h	16h = Exponent value is -10 (equivalent to 0.976mV/count).

8.9 VOUT_COMMAND (Address = 21h) [Reset = 0000h]

VOUT_COMMAND is shown in Figure 8-9 and described in Table 8-10.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: ULINEAR16
NVM Back-up: No
Updates: On-the-fly

The regulated output can be set by PMBus. When PMBus is used to set the regulated voltage, the commanded output voltage in volts is determined by a combination of VOUT_COMMAND, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW, and OPERATION commands, as below. As stated in the description of the (20h) VOUT_MODE command, the VOUT step size is 0.976 mV.

The range of recommended VOUT_COMMAND values is dependent upon the configured (29h) VOUT_SCALE_LOOP. The design does not limit the VOUT_COMMAND value to be within this recommended range. However there will be a max clamp on VOUT_COMMAND to 5.5V. This max clamp is not affected when doing MARGIN_HIGH. There is no min clamp for low voltages.

At power up, the reset value of VOUT_COMMAND is derived from VBOOT/VOUT_SCALE_LOOP . When the rail is disabled by the mechanism programmed to ON_OFF_CONFIG or due to a fault, the value in VOUT_COMMAND is updated to VBOOT.

Note

This register can be changed during soft-start. However, the rail will continue to ramp up/down to the original target (VBOOT) at the rate programmed into TON_RISE. After soft-start completes (and if VOUT_COMMAND is different from the VBOOT value), the device will immediately transition from the VBOOT value to the latest written VOUT_COMMAND at the programmed VOUT_TRANSITION_RATE.

During regulation, preemptive writes to VOUT_COMMAND are allowed even if the DAC is still slewing to a previously programmed VOUT_COMMAND. The device will immediately start slewing to the new target at the rate programmed into VOUT_TRANSITION_RATE.

Figure 8-9. VOUT_COMMAND

15	14	13	12	11	10	9	8
RESERVED			VOUT_COMMAND				
R-0h			R/W-0h				

7	6	5	4	3	2	1	0
VOUT_COMMAND							
R/W-0h							

Table 8-10. VOUT_COMMAND Field Descriptions

Bit	Field	Type	Reset	Description
15:13	RESERVED	R	0h	Reserved
12:0	VOUT_COMMAND	R/W	0h	Sets the output voltage target via the PMBus interface.

8.10 VOUT_MARGIN_HIGH (Address = 25h) [Reset = 0000h]

VOUT_MARGIN_HIGH is shown in Figure 8-10 and described in Table 8-11.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: ULINEAR16, Relative
NVM Back-up: No
Updates: On-the-fly

This command is used to increase the value of the regulated voltage by shifting the VREF reference voltage higher when the OPERATION command is set to Margin High. Since the Vout format is set to relative in the (20h) VOUT_MODE register bit [7], the commanded Vout will increase by the multiplicative factor indicated in this command. This command also uses the LSB specified by (20h) VOUT_MODE.#br

Figure 8-10. VOUT_MARGIN_HIGH

15	14	13	12	11	10	9	8
RESERVED					VOUT_MARGIN_HIGH		
R-0h					R/W-0h		

7	6	5	4	3	2	1	0
VOUT_MARGIN_HIGH							
R/W-0h							

Table 8-11. VOUT_MARGIN_HIGH Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED	R	0h	Reserved
10:0	VOUT_MARGIN_HIGH	R/W	0h	Margin High output voltage. 420h = 3.125% 440h = 6.25%

8.11 VOUT_MARGIN_LOW (Address = 26h) [Reset = 0000h]

VOUT_MARGIN_LOW is shown in Figure 8-11 and described in Table 8-12.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: ULINEAR16, Relative
NVM Back-up: No
Updates: On-the-fly

This command is used to decrease the value of the regulated voltage by shifting the VREF reference voltage lower when the OPERATION command is set to Margin Low. Since the Vout format is set to relative in the (20h) VOUT_MODE register bit [7], the commanded Vout will decrease by the multiplicative factor indicated in this command. This command also uses the LSB specified by (20h) VOUT_MODE.#br

Figure 8-11. VOUT_MARGIN_LOW

15	14	13	12	11	10	9	8
RESERVED						VOUT_MARGIN_LOW	
R-0h						R/W-0h	
7	6	5	4	3	2	1	0
VOUT_MARGIN_LOW							
R/W-0h							

Table 8-12. VOUT_MARGIN_LOW Field Descriptions

Bit	Field	Type	Reset	Description
15:10	RESERVED	R	0h	Reserved
9:0	VOUT_MARGIN_LOW	R/W	0h	Margin Low output voltage. 3C0h = -6.25% 3E0h = -3.125%

8.12 VOUT_TRANSITION_RATE (Address = 27h) [Reset = E81Ah]

VOUT_TRANSITION_RATE is shown in Figure 8-12 and described in Table 8-13.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format:LINEAR11
NVM Back-up: No
Updates: On-the-fly

When a PMBus device receives either a VOUT_COMMAND, or OPERATION (Margin High, Margin Low, Margin Off), that causes the output voltage to change, this command sets the rate in mV/us at which the output should change voltage. This commanded rate of change does not apply when the unit is commanded to turn on or to turn off.

Data Validity:
Writes to the read-only bits in the exponent and mantissa will be ignored and their value will not be updated. Every binary combination in the read/write mantissa bits is writeable and readable. However, the actual output voltage slew rate is set to the nearest supported setting. Additionally, the mantissa value restored from EEPROM is fixed for each supported setting. Refer to Table xxxx.

Figure 8-12. VOUT_TRANSITION_RATE

15	14	13	12	11	10	9	8
EXPONENT					RESERVED		
R-1Dh					R-0h		

7	6	5	4	3	2	1	0
RESERVED	VOUT_TRANSITION_RATE						
R-0h	R/W-1Ah						

Table 8-13. VOUT_TRANSITION_RATE Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT	R	1Dh	Linear format twos complement exponent. Fixed exponent of -3 resulting in 0.125mV/us LSB.
10:7	RESERVED	R	0h	Reserved
6:0	VOUT_TRANSITION_RATE	R/W	1Ah	Linear format twos complement mantissa.

8.13 VOUT_SCALE_LOOP (Address = 29h) [Reset = E804h]

VOUT_SCALE_LOOP is shown in Figure 8-13 and described in Table 8-14.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: SLINEAR11
NVM Back-up: EEPROM
Updates: Output disabled: see below. Output enabled: read-only.

VOUT_SCALE_LOOP allows PMBus devices to map between the commanded voltage and the voltage at the control circuit input. The VOUT_SCALE_LOOP also programs an internal precision resistor divider so no external divider is required.

Figure 8-13. VOUT_SCALE_LOOP

15	14	13	12	11	10	9	8
EXPONENT					RESERVED		
R-1Dh					R-0h		

7	6	5	4	3	2	1	0
RESERVED				VOUT_SCALE_LOOP			
R-0h				R-4h			

Table 8-14. VOUT_SCALE_LOOP Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT	R	1Dh	Linear format twos complement exponent. Fixed exponent of -3 resulting in 0.125 LSB.
10:4	RESERVED	R	0h	Reserved
3:0	VOUT_SCALE_LOOP	R	4h	Linear format twos complement mantissa.

8.14 FREQUENCY_SWITCH (Address = 33h) [Reset = 380Xh]

FREQUENCY_SWITCH is shown in Figure 8-14 and described in Table 8-15.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: SLINEAR11
NVM Back-up: EEPROM
Updates: On-the-fly

FREQUENCY_SWITCH sets the switching frequency of the active device.

Figure 8-14. FREQUENCY_SWITCH

15	14	13	12	11	10	9	8
EXPONENT					RESERVED		
R-7h					R-0h		
7	6	5	4	3	2	1	0
RESERVED				FREQUENCY_SWITCH			
R-0h				R/W-Xh			

Table 8-15. FREQUENCY_SWITCH Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT	R	7h	Linear format twos complement exponent. Fixed exponent of 7 resulting in 128kHz LSB.
10:4	RESERVED	R	0h	Reserved
3:0	FREQUENCY_SWITCH	R/W	0h	Linear format twos complement mantissa. On reset the value will be determined by NVM.

8.15 VOUT_OV_FAULT_RESPONSE (Address = 41h) [Reset = XXh]

VOUT_OV_FAULT_RESPONSE is shown in Figure 8-15 and described in Table 8-16.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: Unsigned Binary (1 byte)
NVM Back-up: EEPROM
Updates: On-the-fly

The VOUT_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an output over-voltage fault.

Figure 8-15. VOUT_OV_FAULT_RESPONSE

7	6	5	4	3	2	1	0
RESERVED		RS_OV			TD_OV		
R-0h		R/W-Xh			R-0h		

Table 8-16. VOUT_OV_FAULT_RESPONSE Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:3	RS_OV	R/W	0h	Output voltage over voltage retry setting. On reset the value will be determined by NVM. 0h = The device does not attempt to restart. The output remains disabled until the fault is cleared (See section 10.7 of the PMBus spec.) 7h = The device goes through a normal startup (Soft start) continuously, without limitation, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown. **Data Validity:** Any value other than 000 or 111 will not be accepted and such an attempt shall be considered as invalid data or unsupported data (ivd) and the device shall respond as described in ivd. Note, that since all 3 bits must be the same, only one (bit 5) is stored in EEPROM.
2:0	TD_OV	R	0h	Output over voltage retry time delay setting. 0h = A zero value for the Retry time delay setting means that the unit does not delay a restart. This is only supported when Restart is disabled by RS_OV[2:0] = 000. The output remains disabled until the fault is cleared (See section 10.7 of the PMBus spec.)

8.16 VOUT_UV_FAULT_RESPONSE (Address = 45h) [Reset = XXh]

VOUT_UV_FAULT_RESPONSE is shown in Figure 8-16 and described in Table 8-17.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: Unsigned Binary (1 byte)
NVM Back-up: EEPROM
Updates: On-the-fly

he VOUT_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an output under-voltage fault.

Figure 8-16. VOUT_UV_FAULT_RESPONSE

7	6	5	4	3	2	1	0
RESERVED		RS_UV			TD_UV		
R-0h		R/W-Xh			R-2h		

Table 8-17. VOUT_UV_FAULT_RESPONSE Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0h	Reserved
5:3	RS_UV	R/W	0h	Output voltage under voltage retry setting. On reset the value will be determined by NVM. 0h = The device does not attempt to restart. The output remains disabled until the fault is cleared (See section 10.7 of the PMBus spec.) 7h = The device goes through a normal startup (Soft start) continuously, without limitation, until it is commanded off or bias power is removed or another fault condition causes the unit to shutdown. **Data Validity:** Any value other than 000 or 111 will not be accepted and such an attempt shall be considered as invalid data or unsupported data (ivd) and the device shall respond as described in ivd. Note, that since all 3 bits must be the same, only one (bit 5) is stored in EEPROM.
2:0	TD_UV	R	2h	These bits select the delay from the detection of the the fault condition signal to the rail shutting down. In other words, this sets the fault de-glitch duration such that if the fault condition goes away before the delay counter expires, then the delay counter is reset to zero. The error in the deglitch counter is +/- 1 us so this will be more visible with lower settings. The hiccup duration or the time between consecutive restart attempts is also configured with a Response delay of 64us and a Hiccup delay of 52ms. 2h = Output under voltage retry/hiccup time delay setting

8.17 IOUT_OC_FAULT_LIMIT (Address = 46h) [Reset = 00XXh]

IOUT_OC_FAULT_LIMIT is shown in Figure 8-17 and described in Table 8-18.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: LINEAR11
NVM Back-up: EEPROM
Updates: On-the-fly

The IOUT_OC_FAULT_LIMIT command sets the value of the output current that causes the overcurrent detector to indicate an overcurrent fault condition. The thresholds selected here are compared to the sensed low-side valley current. See Overcurrent Limit and Low-side Current Sense for more details.

Figure 8-17. IOUT_OC_FAULT_LIMIT

15	14	13	12	11	10	9	8
EXPONENT					RESERVED		
R-0h					R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED			IOUT_OC_FAULT_LIMIT				
R-0h			R/W-Xh				

Table 8-18. IOUT_OC_FAULT_LIMIT Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT	R	0h	Linear format twos complement exponent resulting in a 1A LSB.
10:5	RESERVED	R	0h	Reserved
4:0	IOUT_OC_FAULT_LIMIT	R/W	0h	The IOUT_OC_FAULT_LIMIT command sets the value of the output current that causes the overcurrent detector to indicate an overcurrent fault condition. The thresholds selected here are compared to the sensed low-side valley current. See Overcurrent Limit and Low-side Current Sense for more details. On reset the value will be determined by NVM. **Data Validity:** Only IOUT_OC_FAULT_LIMIT[4:0] will be considered for setting the OCL limit. Any values greater than 31 will be aliased. 4h = 4A OCL B28 and A28 8h = 7A OCL B28 and A28 Bh = 10A OCL B28 and A28 Dh = 13A OCL B28 and A28 10h = 15A OCL B28; 13A OCL A28 13h = 18A OCL B28; 13A OCL A28 1Fh = 21A OCL B28; 13A OCL A28

8.18 TON_DELAY (Address = 60h) [Reset = 000Xh]

TON_DELAY is shown in Figure 8-18 and described in Table 8-19.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: LINEAR11
NVM Back-up: EEPROM
Updates: On-the-fly

The TON_DELAY command sets the time, in milliseconds, from when a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to rise.

Figure 8-18. TON_DELAY

15	14	13	12	11	10	9	8
EXPONENT					RESERVED		
R-0h					R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							TON_DELAY
R-0h							R/W-Xh

Table 8-19. TON_DELAY Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT	R	0h	Linear format twos complement exponent. The exponent is not programmable, with a result of 1ms LSB.
10:1	RESERVED	R	0h	Reserved
0	TON_DELAY	R/W	0h	These bits select the TON_DELAY time. When 000b is selected, a minimum 50us delay is enforced. 0h = 0.05ms TON_DELAY 1h = 1ms TON_DELAY

8.19 TON_RISE (Address = 61h) [Reset = F80Xh]

TON_RISE is shown in Figure 8-19 and described in Table 8-20.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: LINEAR11
NVM Back-up: EEPROM
Updates: On-the-fly

The TON_RISE command sets the time, in milliseconds, from when the output starts to rise until the voltage has entered the regulation band, which effectively sets the slew rate of the reference DAC during the soft-start period. The soft-start time varies from the TON_RISE selection when VOUT_COMMAND is used for boot up. See section Start-Up and Shutdown for more details.

Figure 8-19. TON_RISE

15	14	13	12	11	10	9	8
EXPONENT					RESERVED		
R-1Fh					R-0h		

7	6	5	4	3	2	1	0
RESERVED				TON_RISE			
R-0h				R/W-Xh			

Table 8-20. TON_RISE Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT	R	1Fh	Linear format twos complement exponent. The exponent is not programmable, with a result of 0.5ms LSB.
10:4	RESERVED	R	0h	Reserved
3:0	TON_RISE	R/W	0h	This bit selects the TON_RISE time. On reset the value will be determined by NVM. 0h = 0.5ms TON_RISE. 2h = 1ms TON_RISE. 4h = 2ms TON_RISE. 8h = 4ms TON_RISE

8.20 TOFF_DELAY (Address = 64h) [Reset = 000Xh]

TOFF_DELAY is shown in Figure 8-20 and described in Table 8-21.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: LINEAR11
NVM Back-up: EEPROM
Updates: On-the-fly

The TOFF_DELAY command sets the time, in milliseconds, from when a stop condition is received (as programmed by the ON_OFF_CONFIG command) until the device starts the soft-stop operation.

Figure 8-20. TOFF_DELAY

15	14	13	12	11	10	9	8
EXPONENT					RESERVED		
R-0h					R-0h		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							TOFF_DELAY
R-0h							R/W-Xh

Table 8-21. TOFF_DELAY Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT	R	0h	Linear format twos complement exponent. The exponent is not programmable, with a result of 1ms LSB.
10:1	RESERVED	R	0h	Reserved
0	TOFF_DELAY	R/W	0h	This bit selects the TOFF_DELAY time. On reset the value will be determined by NVM. 0h = 0ms TOFF_DELAY 1h = 1ms TOFF_DELAY

8.21 TOFF_FALL (Address = 65h) [Reset = F80Xh]

TOFF_FALL is shown in Figure 8-21 and described in Table 8-22.

Write Transaction: Write Word
Read Transaction: Read Word
Data Format: LINEAR11
NVM Back-up: EEPROM
Updates: On-the-fly

The TOFF_FALL command sets the time, in milliseconds, from the end of the turn-off delay time until the reference DAC is commanded to 0mV. This command is used to cause the output voltage to decrease at a controlled rate, which effectively sets the slew rate of the reference DAC during the soft-off period. In the implementation of TOFF_FALL, the VREF DAC slew rate is adjusted for each of the supported 32 VBOOT levels to obtain a slew rate to have a soft-stop time close to (but not always exactly equal to) the target value. The selected slew rate for the 0.5ms TOFF_FALL is the same as shown in TON_RISE but with a negative slope. TOFF_FALL is scaled in the same manner as TON_RISE with the different settings.

The VOUT fall time is actually not equal to TOFF_FALL value since the device stops SW switching once the output voltage is discharged to 200mV, and the fall time is more for setting the reference DAC slew rate. See Shutdown for more details.

Figure 8-21. TOFF_FALL

15	14	13	12	11	10	9	8
EXPONENT[4:0]					RESERVED		
R-1Fh					R-0h		

7	6	5	4	3	2	1	0
RESERVED				TOFF_FALL[3:0]			
R-0h				R-Xh			

Table 8-22. TOFF_FALL Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT[4:0]	R	1Fh	Linear format twos complement exponent. The exponent is not programmable, with a result of 0.5ms LSB.
10:4	RESERVED	R	0h	Reserved
3:0	TOFF_FALL[3:0]	R	0h	TOFF_FALL will be Read Only and will have the same values as programmed in TON_RISE.On reset the value will be determined by NVM.

8.22 STATUS_BYTE (Address = 78h) [Reset = 81h]

STATUS_BYTE is shown in Table 8-23.

Write Transaction: N/A
Read Transaction: Read Byte
Data Format: Unsigned Binary (1 byte)
NVM Back-up: No
Updates: On-the-fly

The STATUS_BYTE command returns one byte of information with a summary of the most critical faults, such as overvoltage, overcurrent, overtemperature, and so forth. The supported STATUS_BYTE message content is described in the following table. The STATUS_BYTE is equal the low byte of STATUS_WORD. The conditions in the STATUS_BYTE are summary information only. They are asserted to inform the host as to which other STATUS registers should be checked in the event of a fault. Setting and clearing of these bits must be done in the individual status registers.

Table 8-23. STATUS_BYTE Field Descriptions

Bit	Field	Type	Reset	Description
6	OFF	R/W	1h	LIVE (unlatched) status bit. 0h = The the device is enabled and converting power. 1h = The device is NOT converting power for any reason including simply not being enabled.
5	OVF	R/W	0h	An output overvoltage fault has occured. 0h = An output overvoltage fault has NOT occurred. 1h = An output overvoltage fault has occurred.
4	OCF	R/W	0h	An output overcurrent fault has occurred. 0h = An output overcurrent fault has NOT occurred. 1h = An output overcurrent fault has occurred.
3	Not Supported	R	0h	Not supported and always set to 0.
2	OTF	R/W	0h	An overtemperature fault has occured. 0h = A temperature fault or warning has NOT occurred. 1h = A temperature fault or warning has occurred
1	CML	R/W	0h	A communications, memory, or logic fault has occurred in (7Eh) STATUS_CML 0h = A communication, memory, logic fault has NOT occurred. 1h = A communication, memory, logic fault has occurred.
0	OTH	R/W	1h	This bit is used to flag faults not covered with the other bit faults in STATUS_BYTE - in this case: LOW_VIN, UCF, and UVF. 0h = A fault other than those listed above has NOT occurred. 1h = A fault other than those listed above has occurred.

8.23 STATUS_WORD (Address = 79h) [Reset = 2800h]

STATUS_WORD is shown in Figure 8-22 and described in Table 8-24.

Write Transaction: N/A
Read Transaction: Read Word
Data Format: Unsigned Binary (2 bytes)
NVM Back-up: No
Updates: On-the-fly

The STATUS_WORD command returns two bytes of information with a summary of the most critical faults, such as overvoltage, overcurrent, overtemperature, and so forth. The low byte of the STATUS_WORD is the same register as the STATUS_BYTE. The supported STATUS_WORD message content is described in the following table. The conditions in the STATUS_BYTE are summary information only.

Figure 8-22. STATUS_WORD

15	14	13	12	11	10	9	8
VF	CF	INPUT	MFR	PGOOD_Z	Not Supported		
R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-1h	R-0h		

7	6	5	4	3	2	1	0
STATUS_BYTE							
R-0h							

Table 8-24. STATUS_WORD Field Descriptions

Bit	Field	Type	Reset	Description
15	VF	R/W	0h	A VOUT fault is present (OVF + UVF). 0h = An output voltage fault or warning has not occured. 1h = An output voltage fault or warning has occured.
14	CF	R/W	0h	A fault is present (OCF + NOC/UCF). 0h = An output current fault has not occurred. 1h = An output current fault (OCF + NOC/UCF) has occured.
13	INPUT	R/W	1h	INPUT fault or warning is present. 0h = An input fault or warning has not occurred. 1h = An input fault or warning has occurred.
12	MFR	R/W	0h	A fault in (80h) STATUS_MFR_SPECIFIC is present, with the exception of bit 7 DCM 0h = A STATUS_MFR_SPECIFIC fault has not occurred. 1h = A STATUS_MFR_SPECIFIC fault has occurred.
11	PGOOD_Z	R/W	1h	The Power Not Good is used to flag when the converter output voltage moves outside the defined over-voltage warning (OVW) and under-voltage warning (UVW) limits in analog. The signal is unlatched and always represents the current state of the device, however the faults which assert PGOOD low are latched. 0h = Power is Good. 1h = Power is Not Good.
10:8	Not Supported	R	0h	Not supported and always set to 0.
7:0	STATUS_BYTE	R	0h	Always equal to the STATUS_BYTE value.

8.24 STATUS_CML (Address = 7Eh) [Reset = 00h]

STATUS_CML is shown in Figure 8-23 and described in Table 8-25.

Write Transaction: Write Byte
Read Transaction: Read Byte
Data Format: Unsigned Binary (1 byte)
NVM Back-up: No
Updates: On-the-fly

The STATUS_CML command returns one data byte with contents relating to communications, logic, and memory as follows. All supported bits may be cleared either by (03h) CLEAR_FAULTS, turning on the output through the mechanism programmed into (02h) ON_OFF_CONFIG, or individually by writing 1b to the STATUS_CML register in their position, per the PMBus 1.3.1 Part II specification section 10.2.3.

Figure 8-23. STATUS_CML

7	6	5	4	3	2	1	0
IVC	IVD	PEC_FAIL	MEM	RESERVED		OTH	Not Supported
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h		R/W-0h	R-0h

Table 8-25. STATUS_CML Field Descriptions

Bit	Field	Type	Reset	Description
7	IVC	R/W	0h	0h = Latched flag indicating an invalid or unsupported command was NOT received. 1h = Latched flag indicating an invalid or unsupported command was received.
6	IVD	R/W	0h	0h = Latched flag indicating an invalid or unsupported data was NOT received. 1h = Latched flag indicating an invalid or unsupported data was received.
5	PEC_FAIL	R/W	0h	0h = Latched flag indicating NO packet error check has failed. 1h = Latched flag indicating a packet error check has failed.
4	MEM	R/W	0h	The source of the fault could be one of the following sources internally: Failure parity check during/after STORE_USER_ALL. During reset RESTORE (i.e., EEPROM restore at boot-up), either a mismatch between the EEPROM contents and the register contents; OR a failure to pass parity checks. When the user issues a RESTORE_USER_ALL command, a failure to pass parity checks. Failure during the NVM programming sequence. This bit cannot be cleared by any clearing mechanism until the underlying issue is resolved and the memory is updated. 0h = Latched flag indicating NO memory error was detected. 1h = Latched flag indicating a memory error was detected.
3:2	RESERVED	R	0h	
1	OTH	R/W	0h	0h = Latched flag indicating NO communication error detected. 1h = Latched flag indicating communication error detected.
0	Not Supported	R	0h	Not supported and always set to 0.

ADVANCE INFORMATION

8.25 STATUS_MFR_SPECIFIC (Address = 80h) [Reset = 00h]

STATUS_MFR_SPECIFIC is shown in Figure 8-24 and described in Table 8-26.

Write Transaction: N/A
Read Transaction: Read Byte
Data Format: Unsigned Binary (1 byte)
NVM Back-up: No
Updates: On-the-fly

The STATUS_MFR_SPECIFIC command returns one data byte with contents regarding manufacturer defined status as follows. All supported bits may be cleared either by (03h) CLEAR_FAULTS, turning on the output through the mechanism programmed into (02h) ON_OFF_CONFIG, or individually by writing 1b to the STATUS_MFR_SPECIFIC register in their position, per the PMBus 1.3.1 Part II specification section 10.2.3.

Figure 8-24. STATUS_MFR_SPECIFIC

7	6	5	4	3	2	1	0
DCM	Not Supported						
R/W-0h	R-0h						

Table 8-26. STATUS_MFR_SPECIFIC Field Descriptions

Bit	Field	Type	Reset	Description
7	DCM	R/W	0h	LIVE (unlatched) status bit. This bit is set upon detection of DCM operation. This bit does not trigger SMB_ALERT# and does not assert the MFR bit in STATUS_WORD or the OTH bit in STATUS_BYTE. 0h = The device is NOT operating in DCM. 1h = The device is operating in DCM.
6:0	Not Supported	R	0h	Not supported and always set to 0.

8.26 READ_VOUT (Address = 8Bh) [Reset = 0000h]

READ_VOUT is shown in Figure 8-25 and described in Table 8-27.

Write Transaction: N/A
Read Transaction: Read Word
Data Format: LINEAR16, Absolute
NVM Back-up: No
Updates: On-the-fly

The READ_VOUT command returns the actual, measured output voltage (VOSNS-GOSNS) in Volts. See Telemetry for more details. The format and LSB is set by (20h) VOUT_MODE.

Figure 8-25. READ_VOUT

15	14	13	12	11	10	9	8
Not Supported			READ_VOUT				
R-0h			R-0h				

7	6	5	4	3	2	1	0
READ_VOUT							
R-0h							

Table 8-27. READ_VOUT Field Descriptions

Bit	Field	Type	Reset	Description
15:13	Not Supported	R	0h	Not supported and always set to 0.
12:0	READ_VOUT	R	0h	Output voltage telemetry data. Clamped at 0V minimum.

8.27 READ_IOUT (Address = 8Ch) [Reset = DXXXh]

READ_IOUT is shown in Figure 8-26 and described in Table 8-28.

Write Transaction: N/A
Read Transaction: Read Word
Data Format: LINEAR11
NVM Back-up: No
Updates: On-the-fly

The READ_IOUT command returns the measured SW output current in Amperes. See Telemetry for more details.

Figure 8-26. READ_IOUT

15	14	13	12	11	10	9	8
EXPONENT_IOUT					READ_IOUT		
R-1Ah					R-XXh		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
READ_IOUT							
R-XXh							

Table 8-28. READ_IOUT Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT_IOUT	R	1Ah	Linear format two 's complement exponent. Fixed exponent of -5 resulting in 0.03125A LSB.
10:0	READ_IOUT	R	0h	Output current reading. Bit [10] is tied 0 because we do not support negative values.

8.28 READ_TEMP1 (Address = 8Dh) [Reset = 0XXXh]

READ_TEMP1 is shown in Figure 8-27 and described in Table 8-29.

Write Transaction: N/A
Read Transaction: Read Word
Data Format: LINEAR11
NVM Back-up: No
Updates: On-the-fly

The READ_TEMP1 command returns the Controller die temperature in degrees Celsius. See Telemetry for more details.

Figure 8-27. READ_TEMP1

15	14	13	12	11	10	9	8
EXPONENT					READ_TEMP1		
R-0h					R-XXh		

7	6	5	4	3	2	1	0
READ_TEMP1							
R-XXh							

Table 8-29. READ_TEMP1 Field Descriptions

Bit	Field	Type	Reset	Description
15:11	EXPONENT	R	0h	Linear format two 's complement exponent. Fixed exponent of 0 resulting in 1 deg C.
10:0	READ_TEMP1	R	0h	Temperature of the controller die.

8.29 PMBUS_REVISION (Address = 98h) [Reset = 55h]

PMBUS_REVISION is shown in Figure 8-28 and described in Table 8-30.

Write Transaction: N/A
Read Transaction: Read Byte
Data Format: Unsigned Binary (1 byte)
NVM Back-up: No

The PMBUS_REVISION command returns the revision of the PMBus.

Figure 8-28. PMBUS_REVISION

7	6	5	4	3	2	1	0
PMBUS_REVISION							
R-55h							

Table 8-30. PMBUS_REVISION Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PMBUS_REVISION	R	55h	PMBus revision, compliant to revision 1.5 of the PMBus specification (Part I and II).

8.30 MFR_ID (Address = 99h) [Reset = 4954h]

MFR_ID is shown in Figure 8-29 and described in Table 8-31.

Write Transaction: N/A
Read Transaction: Block Read
Data Format: Unsigned Binary (2 bytes)
NVM Back-up: No

This Read-only Block Read command returns a single word (16 bits) with the manufacturers ID (name, abbreviation or symbol that identifies the units manufacturer). The BYTE_COUNT field in the Block Read command will be 2 (indicating 2 bytes will follow).

Figure 8-29. MFR_ID

15	14	13	12	11	10	9	8
ASCII for I							
R-49h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ASCII for T							
R-54h							

Table 8-31. MFR_ID Field Descriptions

Bit	Field	Type	Reset	Description
15:8	ASCII for I	R	49h	
7:0	ASCII for T	R	54h	

8.31 MFR_MODEL (Address = 9Ah) [Reset = 00284B54h]

MFR_MODEL is shown in Figure 8-30 and described in Table 8-32.

Write Transaction: N/A
Read Transaction: Block Read
Data Format: Unsigned Binary (4 bytes)
NVM Back-up: No

This Read-only Block Read command returns 4 bytes (32 bits) with the manufacturers model number. The BYTE_COUNT field in the Block Read command will be 4 (indicating 4 bytes will follow).

Figure 8-30. MFR_MODEL

31	30	29	28	27	26	25	24
Part Number Extension							
R-0h							

23	22	21	20	19	18	17	16
Part Number Fifth Digit				Part Number Sixth Digit			
R-2h				R-8h			

15	14	13	12	11	10	9	8
Part Number Third Digit				Part Number Fourth Digit			
R-4h				R-Bh			

7	6	5	4	3	2	1	0
Part Number First Digit				Part Number Second Digit			
R-5h				R-4h			

Table 8-32. MFR_MODEL Field Descriptions

Bit	Field	Type	Reset	Description
31:24	Part Number Extension	R	0h	
23:20	Part Number Fifth Digit	R	2h	
19:16	Part Number Sixth Digit	R	8h	
15:12	Part Number Third Digit	R	4h	
11:8	Part Number Fourth Digit	R	Bh	
7:4	Part Number First Digit	R	5h	
3:0	Part Number Second Digit	R	4h	

8.32 MFR_REVISION (Address = 9Bh) [Reset = X0h]

MFR_REVISION is shown in Figure 8-31 and described in Table 8-33.

Write Transaction: Block Write
Read Transaction: Block Read
Data Format: Unsigned Binary (1 byte)
NVM Back-up: EEPROM

This single byte Block command is used to either set or read the manufacturers revision number. It is writeable and includes NVM backup.

Figure 8-31. MFR_REVISION

7	6	5	4	3	2	1	0
MFR_REVISION							
R/W-Xh							

Table 8-33. MFR_REVISION Field Descriptions

Bit	Field	Type	Reset	Description
7:0	MFR_REVISION	R/W	0h	

8.33 IC_DEVICE_ID (Address = ADh) [Reset = 00284B544954h]

IC_DEVICE_ID is shown in Figure 8-32 and described in Table 8-34.

Write Transaction: N/A
Read Transaction: Block Read
Data Format: Unsigned Binary (6 bytes)
NVM Back-up: EEPROM

The block read only IC_DEVICE_ID command is used to read the type or part number of an IC embedded within a PMBus that is used for the PMBus interface. IC_DEVICE_ID uses 6-byte block format. The first two byte shall be 5449h for TI in ASCII text format. The Third through Fifth byte shall be a direct readable Hex Part Number representing the 6 digit part number. The Sixth byte shall be a Part Number Extention code.

Figure 8-32. IC_DEVICE_ID

<table>
<tr><td>47</td><td>46</td><td>45</td><td>44</td><td>43</td><td>42</td><td>41</td><td>40</td></tr>
<tr><td colspan="8">Part Number Extension</td></tr>
<tr><td colspan="8">R-0h</td></tr>
<tr><td>39</td><td>38</td><td>37</td><td>36</td><td>35</td><td>34</td><td>33</td><td>32</td></tr>
<tr><td colspan="4">Part Number Fifth Digit</td><td colspan="4">Part Number Sixth Digit</td></tr>
<tr><td colspan="4">R-2h</td><td colspan="4">R-8h</td></tr>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td></tr>
<tr><td colspan="4">Part Number Third Digit</td><td colspan="4">Part Number Fourth Digit</td></tr>
<tr><td colspan="4">R-4h</td><td colspan="4">R-Bh</td></tr>
<tr><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td></tr>
<tr><td colspan="4">Part Number First Digit</td><td colspan="4">Part Number Second Digit</td></tr>
<tr><td colspan="4">R-5h</td><td colspan="4">R-4h</td></tr>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">ASCII for I</td></tr>
<tr><td colspan="8">R-49h</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">ASCII for T</td></tr>
<tr><td colspan="8">R-54h</td></tr>
</table>

Table 8-34. IC_DEVICE_ID Field Descriptions

Bit	Field	Type	Reset	Description
47:40	Part Number Extension	R	0h	
39:36	Part Number Fifth Digit	R	2h	
35:32	Part Number Sixth Digit	R	8h	
31:28	Part Number Third Digit	R	4h	
27:24	Part Number Fourth Digit	R	Bh	
23:20	Part Number First Digit	R	5h	
19:16	Part Number Second Digit	R	4h	
15:8	ASCII for I	R	49h	
7:0	ASCII for T	R	54h	

8.34 IC_DEVICE_REV (Address = AEh) [Reset = 00h]

IC_DEVICE_REV is shown in Figure 8-33 and described in Table 8-35.

Write Transaction: N/A
Read Transaction: Block Read
Data Format: Unsigned Binary (1 byte)
NVM Back-up: No

The block read-only IC_DEVICE_REV command returns a single byte with the unique Device revision identifier. The DEVICE_REV starts at 0 with the first silicon and is incremented with each subsequent silicon revision. The BYTE_COUNT field in the Block Read command will be 01h (indicating 1 byte will follow).

Figure 8-33. IC_DEVICE_REV

<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="3">PS_IC</td><td colspan="4">DEVICE_REVISION</td></tr>
<tr><td>R-0h</td><td colspan="3">R-0h</td><td colspan="4">R-0h</td></tr>
</table>

Table 8-35. IC_DEVICE_REV Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6:4	PS_IC	R	0h	Power stage verision. These bits are mapped from the powerstage die-id.
3:0	DEVICE_REVISION	R	0h	Device Revision.

8.35 SYS_CFG_USER1 (Address = D1h) [Reset = XXh]

SYS_CFG_USER1 is shown in Figure 8-34 and described in Table 8-36.

Write Transaction: Write Byte
Read Transaction: Read Byte
Data Format: Unsigned Binary (1 byte)
NVM Back-up: EEPROM
Updates: On-the-fly

This command contains miscellaneious bits for system configuration.

Figure 8-34. SYS_CFG_USER1

7	6	5	4	3	2	1	0
RESERVED	FCCM	PMB_LOCK	ADDR_CFG	RESERVED	RESERVED	NRSA_L	EN_FIX_OVF
R-0h	R/W-Xh	R/W-Xh	R/W-Xh	R-0h	R-0h	R/W-Xh	R/W-Xh

Table 8-36. SYS_CFG_USER1 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	FCCM	R/W	0h	Forced CCM operation. On reset the value will be determined by NVM. 0h = DCM operation is enabled and automatically entered/exited based on zerocrossing detection of the LFET sensed current. The bit is updated when disabled. PMBus writes are always accepted and the data is updated; however, in order for this bit to take effect, the rail must be disabled. 1h = Forces continuous conduction in the switching converter.
5	PMB_LOCK	R/W	0h	This bit controls write access to the PASSKEY command. On reset the value will be determined by NVM. 0h = As defined in the PASSKEY command description. 1h = Writes to PASSKEY are NACKed with ivc.
4	ADDR_CFG	R/W	0h	This bit selects the PMBus device address range selected by ADR pins pinstrap, as below: On reset the value will be determined by NVM. 0h = As defined in the pinstrapping table. 1h = Top nibble of ADR becomes 3h. This bit takes effect only after writing it, sending a STORE_USER_ALL command and performing a POWER_ON_RESET, or sending the PMBus command RESTORE_USER_ALL.
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	NRSA_L	R/W	0h	This bit selects lower values of NRSA when set to 1 and higher values of NRSA when set to 0 for some vboot voltages. Refer to table in VOUT_SCALE_LOOP. On reset the value will be determined by NVM.
0	EN_FIX_OVF	R/W	0h	This bit is used to enable the fixed OV fault.On reset the value will be determined by NVM. 0h = Fixed OVF is disabled. 1h = Fixed OVF is enabled.

8.36 PASSKEY (Address = D2h) [Reset = X0h]

PASSKEY is shown in Figure 8-35 and described in Table 8-37.

Write Transaction: Write Block
Read Transaction: Read Block
Data Format: Unsigned Binary (1 byte)
NVM Back-up: EEPROM
Updates: On-the-fly

Passkey provides a customer the ability to lock access to (15h) STORE_USER_ALL and (10h) WRITE_PROTECT with a user programmed 8-bit value.

Figure 8-35. PASSKEY

7	6	5	4	3	2	1	0
PASSKEY							
R/W-Xh							

Table 8-37. PASSKEY Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PASSKEY	R/W	0h	

8.37 COMP (Address = D4h) [Reset = XXh]

COMP is shown in Figure 8-36 and described in Table 8-38.

Write Transaction: Write Byte
Read Transaction: Read Byte
Data Format: Unsigned Binary (1 byte)
NVM Back-up: EEPROM
Updates: On-the-fly

This command contains feedback compensation settings for the regulated rail.

Figure 8-36. COMP

7	6	5	4	3	2	1	0
RESERVED			OVRD_SUMCOMP_HIGH	OVRD_SUMCOMP_LOW	SEL_SUMCOMP	SEL_RAMP	
R-0h			R/W-Xh	R/W-Xh	R-0h	R/W-Xh	

Table 8-38. COMP Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0h	Reserved
4	OVRD_SUMCOMP_HIGH	R/W	0h	Setting this bit overrides SEL_SUMCOMP to be high, regardless of DAC target. On reset the value will be determined by NVM.
3	OVRD_SUMCOMP_LOW	R/W	0h	Setting this bit overrides SEL_SUMCOMP to be low, regardless of DAC target. On reset the value will be determined by NVM.
2	SEL_SUMCOMP	R	0h	Defaults to checking DAC target greater than or equal to 750mV (DAC target is only updated during disable).
1:0	SEL_RAMP	R/W	0h	These bits determine the ramp amplitude/slope. On reset the value will be determined by NVM. SEL_SUMCOMP = 0b, SEL_RAMP = 00b, RAMP on FB (mV) = 15 SEL_SUMCOMP = 0b, SEL_RAMP = 01b, RAMP on FB (mV) = 10 SEL_SUMCOMP = 0b, SEL_RAMP = 10b, RAMP on FB (mV) = 10 SEL_SUMCOMP = 0b, SEL_RAMP = 11b, RAMP on FB (mV) = 5 SEL_SUMCOMP = 1b, SEL_RAMP = 00b, RAMP on FB (mV) = 18 SEL_SUMCOMP = 1b, SEL_RAMP = 01b, RAMP on FB (mV) = 15 SEL_SUMCOMP = 1b, SEL_RAMP = 10b, RAMP on FB (mV) = 15 SEL_SUMCOMP = 1b, SEL_RAMP = 11b, RAMP on FB (mV) = 8

8.38 VBOOT (Address = D5h) [Reset = XXh]

VBOOT is shown in Figure 8-37 and described in Table 8-39.

Write Transaction: Write Byte
Read Transaction: Read Byte
Data Format: Unsigned Binary (1 byte)
NVM Back-up: EEPROM
Updates: On-the-fly

This command contains bits for setting the boot-up voltage VBOOT.

Figure 8-37. VBOOT

7	6	5	4	3	2	1	0
RESERVED			VBOOT				
R-0h			R/W-Xh				

Table 8-39. VBOOT Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0h	Reserved
4:0	VBOOT	R/W	0h	These bits contains VBOOT setting that is used for the the VREF DAC target code for soft-start purposes (as against directly specifying the initial VOUT voltage). The user must choose the appropriate VOUT_SCALE_LOOP to achieve the desired output voltage VOUT. On reset the value will be determined by NVM.

8.39 NVM_CHECKSUM (Address = D9h) [Reset = 0000h]

NVM_CHECKSUM is shown in Figure 8-38 and described in Table 8-40.

Write Transaction: N/A
Read Transaction: Read Word
Data Format: Unsigned Binary (2 bytes)
NVM Back-up: No
Updates: On-the-fly

This command contains CRC value from reading contents of the non-volatile memory (NVM). The value of the checksum will be calculated as CRC-16 (polynomial 8005h). The checksum will be calculated in 8 parallel slices. Any padding needed to make the last word of the input 8 bits will be 0s. The checksum value will be stored in NVM to ensure the integrity of the STORE function. Any corrupted data that happens during a STORE operation will be detected on RESTORE when the user compares the calculated NVM_CHECKSUM with a known good value that is expected.

Figure 8-38. NVM_CHECKSUM

15	14	13	12	11	10	9	8
NVM_CHECKSUM							
R-0h							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NVM_CHECKSUM							
R-0h							

Table 8-40. NVM_CHECKSUM Field Descriptions

Bit	Field	Type	Reset	Description
15:0	NVM_CHECKSUM	R	0h	Responds with the Check Sum results of the last stored NVM. The 32-bit (0Eh) PASSKEY NVM bits are excluded from the NVM_CHECKSUM determination to prevent a malicious actor from reading the device configuration and repeatedly setting PASSKEY values in an attempt to discover the PASSKEY value.

8.40 FUSION_ID0 (Address = FCh) [Reset = 02C0h]

FUSION_ID0 is shown in Figure 8-39 and described in Table 8-41.

Write Transaction: N/A
Read Transaction: Read Word
Data Format: Unsigned Binary (2 bytes)
NVM Back-up: No

FUSION_ID0 provides a platform level Identification code to be used by Texas Instruments Digital Power Designer for identifying a TI device.

Writes to this command will be accepted, but ignored otherwise (the readback value of this command does not change following a write attempt). This command is writeable for some TI devices, so to maintain crosscompatibility, the device accepts write transactions to this command as well. No STATUS_CML bits are set as a result of the receipt of a write attempt to this command.

Figure 8-39. FUSION_ID0

15	14	13	12	11	10	9	8
FUSION_ID0							
R-2C0h							
7	6	5	4	3	2	1	0
FUSION_ID0							
R-2C0h							

Table 8-41. FUSION_ID0 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	FUSION_ID0	R	2C0h	Hard Coded to 02C0h.

8.41 FUSION_ID1 (Address = FDh) [Reset = 4h]

FUSION_ID1 is shown in Table 8-42.

Write Transaction: N/A
Read Transaction: Block Read
Data Format: Unsigned Binary (6 bytes)
NVM Back-up: No

FUSION_ID1 provides a platform level Identification code to be used by Texas Instruments Digital Power Designer for identifying a TI device.

Writes to this command will be accepted, but ignored otherwise (the readback value of this command does not change following a write attempt). This command is writeable for some TI devices, so to maintain crosscompatibility, the device accepts write transactions to this command as well. No STATUS_CML bits are set as a result of the receipt of a write attempt to this command.

Table 8-42. FUSION_ID1 Field Descriptions

Bit	Field	Type	Reset	Description
3:0	FUSION_ID1	R	4h	Hard coded to 5h. Hard coded to Ch. Hard coded to Fh. Hard coded to 3h. Hard coded to Bh. Hard coded to 9h. Hard coded to 4h.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS544B28 device is a high-efficiency, single-channel, small-sized, synchronous buck converter. The device is designed for low output voltage point-of-load applications with 20A or lower output current in server, storage, and similar computing applications. The TPS544B28 features proprietary D-CAP4 mode control combined with adaptive on-time architecture. This combination builds modern low-duty-ratio and ultra-fast load-step-response DC/DC converters in an excellent fashion. The output voltage ranges from to 5.5V. The conversion input voltage ranges from 2.7V to 16V, and the VCC input voltage ranges from 3.1V to 5.3V. The D-CAP4 mode uses emulated current information to control the modulation. An advantage of this control scheme is that this control scheme does not require an external phase-compensation network, which makes the device easy-to-use and also allows for a low external component count. Another advantage of this control scheme is that the control scheme supports stable operation with all low ESR output capacitors (such as ceramic capacitor and low ESR polymer capacitor). Adaptive on-time control tracks the preset switching frequency over a wide range of input and output voltages while increasing switching frequency as needed during a load-step transient.

9.2 Typical Application

The schematic shows a typical application for the TPS544B28. This example describes the design procedure of converting an input voltage range of 8V to 16V down to 3.3V with a maximum output current of 20A.

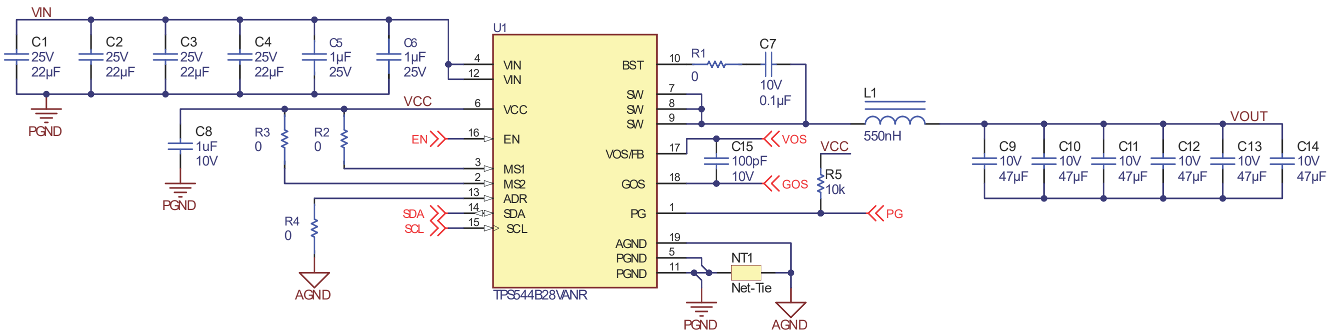

Figure 9-1. Application Circuit Diagram

9.2.1 Design Requirements

This design uses the parameters listed in the following table.

Table 9-1. Design Example Specifications

SPECIFICATION	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} voltage range			8	12	16	V
Input current	V_{IN} = 8V, I_{OUT} = 20A			9		A
V_{IN} start voltage	Set by EN pin resistor divider			3.84		V
Output voltage setpoint	V_{OUT}= 3.3V set by MS2 pin selection.			3.3		V
Output current range	V_{IN} = 8V to 16V		0		20	A
Load transient response	I_{OUT} = 5A to 15A	Voltage change		–99		mV
	I_{OUT} = 15A to 5A	Voltage change		99		mV
Output ripple voltage	I_{OUT} = 20A			16		mVPP
Soft-start time	From start of switching to V_{OUT} = 3.3V, t_{SS} = 1ms setting		0.8	1	1.2	ms
Current limit	OCP = 21A setting by MS1 pin selection		19	21	23	A
Switching frequency (f_{SW})	f_{SW} = 800kHz setting by MS1 pin selection			800		kHz
IC case temperature	I_{OUT} = 20A, 15-minute soak			77.4		°C

9.2.2 Detailed Design Procedure

The external component selection is a simple process using D-CAP4 mode. Select the external components using the following steps.

9.2.2.1 Output Voltage Setting Point

The MS2 pin selects the device output voltage configuration as well as FCCM or PFM operation based on Table 7-3. For this design, use the internal FB configuration option.

If an output voltage other than those is available in Table 7-3 is needed, the external feedback configuration allows the output voltage to be programmed by a voltage-divider resistors, R1 and R2. Connect R1 between the VOS/FB pin and the output, and connect R2 between the VOS/FB pin and GOS. The recommended R2 value is 10kΩ, but the value can also be set to another value between the range of 1kΩ to 20kΩ. Use Equation 5 to determine R1.

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \tag{5}$$

9.2.2.2 Choose the Switching Frequency

For this design, use the internal feedback mode, and the switching frequency is configured by tying the MS1 pin to a pin-strap resistor, GND, or VCC. See also Table 7-2.

Switching frequency selection is a tradeoff between higher efficiency and smaller system design size. Lower switching frequency yields higher overall efficiency but relatively bigger external components. Higher switching frequencies cause additional switching losses which impact efficiency and thermal performance. For this design, connect MS1 pin to VCC to set the switching frequency to 800kHz

When selecting the switching frequency of a buck converter, the minimum on-time and minimum off-time must be considered. Equation 6 calculates the maximum f_{SW} before being limited by the minimum on-time. When hitting the minimum on-time limits of a converter with D-CAP4 control, the effective switching frequency changes to keep the output voltage regulated. This calculation ignores resistive drops in the converter to give a worst case estimation.

$$f_{SW}(\text{max}) = \frac{V_{OUT}}{V_{IN}(\text{max})} \times \frac{1}{t_{ON\_MIN}} = \frac{3.3\text{ V}}{16\text{ V}} \times \frac{1}{40\text{ ns}} = 5156\text{ kHz} \tag{6}$$

Equation 7 calculates the maximum f_{SW} before being limited by the minimum off-time. When hitting the minimum off-time limits of a converter with D-CAP4 control, the operating duty cycle maxes out and the output voltage begins to drop with the input voltage. This equation requires the DC resistance of the inductor, R_{DCR}, selected in the following step so this preliminary calculation assumes a resistance of 1.4mΩ. If operating near the maximum f_{SW} limited by the minimum off-time, the variation in resistance across temperature must be considered when using Equation 8. The selected f_{SW} of 800kHz is below the two calculated maximum values.

$$f_{SW}(\max) = \frac{V_{IN}(\min) - V_{OUT} - I_{OUT}(\max) \times \left(R_{DCR} + R_{DS(ON)\_HS}\right)}{t_{OFF\_MIN}(\max) \times \left(V_{IN}(\min) - I_{OUT}(\max) \times \left(R_{DS(ON)\_HS} - R_{DS(ON)\_LS}\right)\right)} \quad (7)$$

$$f_{SW}(\max) = \frac{8\ \text{V} - 3.3\ \text{V} - 20\ \text{A} \times (1.4\ \text{m}\Omega + 9.5\ \text{m}\Omega)}{150\ \text{ns} \times (8\ \text{V} - 20\ \text{A} \times (9.5\ \text{m}\Omega - 3.3\ \text{m}\Omega))} = 3.8\ \text{MHz} \quad (8)$$

9.2.2.3 Choose the Inductor

To calculate the value of the output inductor (L_{OUT}), use Equation 9. The output capacitor filters the inductor-ripple current ($I_{IND(ripple)}$). Therefore, selecting a high inductor-ripple current impacts the selection of the output capacitor because the output capacitor must have a ripple-current rating equal to or greater than the inductor-ripple current. Larger ripple current increases output ripple voltage, but improves signal-to-noise ratio and helps to stabilize operation. Generally speaking, the inductance value must set the ripple current at approximately 15% to 40% of the maximum output current for a balanced performance.

For this design, the inductor-ripple current is set to 30% of 20 A output current. With a 800kHz switching frequency, 16V as maximum V_{IN}, and 3.3V as the output voltage, Based on these parameters, Equation 9 calculates an inductance of 0.546µH. A nearest standard value of 0.55µH is chosen.

$$L = \frac{\left(V_{IN}(\max) - V_{OUT}\right) \times V_{OUT}}{I_{RIPPLE} \times V_{IN}(\max) \times f_{SW}} = \frac{(16\ \text{V} - 3.3\ \text{V}) \times 3.3\ \text{V}}{0.3 \times 20\text{A} \times 16\ \text{V} \times 800\ \text{kHz}} = 0.546\ \mu\text{H} \quad (9)$$

The inductor requires a low DCR to achieve good efficiency. The inductor also requires enough room above peak inductor current before saturation. Use Equation 10 to estimate the inductor current ripple. For this design, by tying the CFG1 pin to VCC, $I_{OC(valley)}$ is set to 21A, thus peak inductor current under maximum V_{IN} is calculated as 22.98A with Equation 11.

$$I_{RIPPLE} = \frac{\left(V_{IN}(\max) - V_{OUT}\right) \times V_{OUT}}{L \times V_{IN}(\max) \times f_{SW}} = \frac{(16\ \text{V} - 3.3\ \text{V}) \times 3.3\ \text{V}}{0.55\mu\text{H} \times 16\ \text{V} \times 800\ \text{kHz}} = 5.95\ \text{A} \quad (10)$$

$$I_{L(PEAK)} = I_{OUT} + \frac{I_{RIPPLE}}{2} = 20\ \text{A} + \frac{5.95\ \text{A}}{2} = 22.98\ \text{A} \quad (11)$$

$$I_{L(RMS)} = \sqrt{{I_{OUT}}^2 + \frac{{I_{RIPPLE}}^2}{12}} = \sqrt{20\ \text{A}^2 + \frac{5.95\ \text{A}^2}{12}} = 20.07\ \text{A} \quad (12)$$

The selected inductance is a Coilcraft XAL7070-551MEB. This inductance has a saturation current rating of 43A , RMS current rating of 29A and a DCR of 1.6mΩ maximum. This inductor was selected for the low DCR to get high efficiency.

9.2.2.4 Choose the Output Capacitor

There are three considerations for selecting the value of the output capacitor:

1. Stability
2. Steady state output voltage ripple
3. Regulator transient response to a change load current

First, calculate the minimum output capacitance based on these three requirements. Equation 13 calculates the minimum capacitance to keep the LC double pole below the $f_{P(MAX)}$ in Table 7-1 to meet stability requirements. This requirement helps to keep the LC double pole close to the internal zero. Equation 14 calculates the minimum capacitance to meet the steady state output voltage ripple requirement of 16mV. These calculations are for CCM operation and does not include the portion of the output voltage ripple caused by the ESR or ESL of the output capacitors.

$$C_{OUT\_STABLITY} > \left(\frac{1}{2\pi \times f_{P(TABLE)} \times \left(1 + \left(\frac{V_{OUT}}{V_{IN(TYP)}}\right)^2\right)}\right)^2 \times \frac{1}{L_{OUT}} = \left(\frac{1}{2\pi \times 19.9\text{kHz} \times \left(1 + \left(\frac{3.3\text{V}}{12\text{V}}\right)^2\right)}\right)^2 \times \frac{1}{0.55\mu\text{H}} = 101\mu\text{F} \tag{13}$$

$$C_{OUT\_RIPPLE} > \frac{I_{RIPPLE}}{8 \times V_{RIPPLE} \times f_{SW}} = \frac{5.95\text{A}}{8 \times 16\text{mV} \times 800\text{kHz}} = 58.1\mu\text{F} \tag{14}$$

Equation 16 and Equation 17 calculate the minimum capacitance to meet the transient response requirement of 99mV with a 10A step. These equations calculate the necessary output capacitance to hold the output voltage steady while the inductor current ramps up or ramps down after a load step.

$$C_{OUT\_UNDERSHOOT} > \frac{L \times I_{STEP}^2 \times \left(\frac{V_{OUT}}{V_{IN}(\min) \times f_{SW}} + t_{OFF\_MIN}(\max)\right)}{2 \times V_{TRANS} \times V_{OUT} \times \left(\frac{V_{IN}(\min) - V_{OUT}}{V_{IN}(\min) \times f_{SW}} - t_{OFF\_MIN}(\max)\right)} \tag{15}$$

$$C_{OUT\_UNDERSHOOT} > \frac{0.55\mu\text{H} \times 10\text{A}^2 \times \left(\frac{3.3\text{V}}{8\text{V} \times 800\text{kHz}} + 150\text{ns}\right)}{2 \times 99\text{mV} \times 3.3\text{V} \times \left(\frac{8\text{V} - 3.3\text{V}}{8\text{V} \times 800\text{kHz}} - 150\text{ns}\right)} = 95.9\mu\text{F} \tag{16}$$

$$C_{OUT\_OVERSHOOT} > \frac{L \times I_{STEP}^2}{2 \times V_{TRANS} \times V_{OUT}} = \frac{0.55\mu\text{H} \times 10\text{A}^2}{2 \times 99\text{mV} \times 3.3\text{V}} = 84.2\mu\text{F} \tag{17}$$

The output capacitance needed to meet the overshoot requirement is the highest value, so this sets the required minimum output capacitance for this example. Stability requirements can also limit the maximum output capacitance. Equation 18 calculates the recommended maximum output capacitance. This calculation keeps the LC double pole above 1/100th the f_{SW}.

$$C_{OUT\_STABILITY} < \left(\frac{50}{\pi \times f_{SW}}\right)^2 \times \frac{1}{L} = \left(\frac{50}{\pi \times 800\text{kHz}}\right)^2 \times \frac{1}{0.55\mu\text{H}} = 720\mu\text{F} \tag{18}$$

Using more output capacitance is possible, but the stability must be checked through a bode plot or transient response measurement. The selected output capacitance is 6 × 47µF, 10V ceramic capacitors. When using ceramic capacitors, the capacitance must be derated due to DC and AC bias effects. The selected capacitors derate to 48% the nominal value giving an effective total capacitance of 135µF. This effective capacitance meets the minimum and maximum requirements.

This application uses all ceramic capacitors so the effects of ESR on the ripple and transient were ignored. If using non ceramic capacitors, as a starting point, the ESR must be below the values calculated in Equation 19 to meet the ripple requirement and Equation 20 to meet the transient requirement. For more accurate calculations or if using mixed output capacitors, the impedance of the output capacitors must be used to determine if the ripple and transient requirements can be met.

$$R_{ESR\_RIPPLE} < \frac{V_{RIPPLE}}{I_{RIPPLE}} = \frac{26\text{mV}}{5.95\text{A}} = 4.4\text{m}\Omega \tag{19}$$

$$R_{ESR\_TRANS} < \frac{V_{TRANS}}{I_{STEP}} = \frac{99\text{mV}}{10\text{A}} = 9.9\text{m}\Omega \tag{20}$$

9.2.2.5 Choose the Input Capacitors (C_{IN})

The device requires input bypass capacitors between both pairs of VIN and PGND pins to bypass the power-stage. The bypass capacitors must be placed as close as possible to the pins of the IC as the layout allows. At least 20µF nominal of ceramic capacitance and two high frequency ceramic bypass capacitors are required. A 0.1µF to 1µF capacitor must be placed as close as possible to both VIN pins 4 and 12 on the same side of the board of the device to provide the required high frequency bypass, to reduce the high frequency overshoot and undershoot on across the power-stage on the VIN and SW pins. TI recommends at least 1µF of bypass capacitance as close as possible to each VIN pin to minimize the input voltage ripple. The ceramic capacitors must be a high-quality dielectric of X6S or better for the high capacitance-to-volume ratio and stable characteristics across temperature. In addition to this requirement, more bulk capacitance can be needed on the input depending on the application to minimize variations on the input voltage during transient conditions.

Use Equation 21 to calculate the input capacitance required to meet a specific input ripple target. A recommended target input voltage ripple is 5% the minimum input voltage, 780mV in this example. The calculated input capacitance is 5.5µF. This example meets these two requirements with 2 × 10µF ceramic capacitors.

$$C_{IN} > \frac{V_{OUT} \times I_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN}(\mathrm{min})}\right)}{f_{SW} \times V_{IN}(\mathrm{min}) \times V_{IN\_RIPPLE}} = \frac{3.3\mathrm{V} \times 20\mathrm{A} \times \left(1 - \frac{3.3\mathrm{V}}{8\mathrm{V}}\right)}{800\ \mathrm{kHz} \times 8\mathrm{V} \times 780\mathrm{mV}} = 7.8\mu\mathrm{F} \tag{21}$$

The capacitor must also have an RMS current rating greater than the maximum input RMS current in the application. Use Equation 23 to calculate the input RMS current the input capacitors must support. The result is 9.9A in this example. The ceramic input capacitors have a current rating greater than this value.

$$I_{CIN(RMS)} = \sqrt{\frac{V_{OUT}}{V_{IN}(\mathrm{min})} \times \left(\frac{(V_{IN}(\mathrm{min}) - V_{OUT})}{V_{IN}(\mathrm{min})} \times {I_{OUT}}^2 + \frac{{I_{RIPPLE}}^2}{12}\right)} \tag{22}$$

$$I_{CIN(RMS)} = \sqrt{\frac{3.3\mathrm{V}}{8\mathrm{V}} \times \left(\frac{(8\mathrm{V} - 3.3\mathrm{V})}{8\mathrm{V}} \times 20^2 + \frac{5.95^2}{12}\right)} = 9.9\mathrm{A} \tag{23}$$

For applications requiring bulk capacitance on the input, such as ones with low input voltage and high current, TI recommends the selection process in *How to select input capacitors for a buck converter* analog design journal.

9.2.2.6 VCC Bypass Capacitor

At a minimum, a 1.0µF, at least 6.3V rating, X5R ceramic bypass capacitor is needed on VCC pin located as close to the pin as the layout allows. Use the smallest sized capacitor possible, such as an 0402 package, to minimize the loop from the VCC pin to the PGND pin.

9.2.2.7 BOOT Capacitor

At a minimum, a 0.1µF, 10V, X5R ceramic bypass capacitor is needed between the BOOT and SW pins located as close to the pin as the layout allows.

9.2.2.8 PG Pullup Resistor

The PG pin is open-drain, so a pullup resistor is required when using this pin. The recommended value is between 1kΩ and 100kΩ.

9.2.2.9 Choose the PMBus® Address and Fault Recovery Mode

A resistor between the ADR pin and AGND sets the preconfigured PMBus address and Fault Recovery Mode in the memory map. Refer to Table 7-4for the list of PMBus addresses and Fault Recovery Modes selectable by an external resistor. In this application, shorting the pin to AGND using a 0Ω resistor selects a PMBus address of 21h and the Hiccup Fault Recovery Mode.

9.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 4V and 16V. Both input supplies (VIN and VCC bias) must be well regulated. Proper bypassing of input supplies (VIN and VCC bias) is also critical for noise performance, as are PCB layout and grounding scheme. See the recommendations in *Layout*.

9.4 Layout

9.4.1 Layout Guidelines

Before beginning a design using the device, consider the following:

- Make VIN, PGND, and SW traces as wide as possible to reduce trace impedance and improve heat dissipation.
- Place the power components (including input and output capacitors, the inductor, and the IC) on the top side of the PCB. To shield and isolate the small signal traces from noisy power lines, insert at least one solid ground inner plane.
- Placement of the VIN decoupling capacitors are important for the power MOSFET robustness. A 1µF/25V/0402 ceramic high-frequency bypass capacitor on each VIN pin (pins 4 and 12) is required, connected to the adjacent PGND pins (pins 5 and 11 respectively). Place the remaining ceramic input capacitance next to these high frequency bypass capacitors. The remaining input capacitance can be placed on the other side of the board, but use as many vias as possible to minimize impedance between the capacitors and the pins of the IC.
- Place as many vias as possible below and near the PGND pins. This action minimizes parasitic impedance and also lowers thermal resistance.
- Use vias near both VIN pins and provide a low impedance connection between them through an internal layer. A via can also be placed below each of the VIN pins.
- Place the VCC decoupling capacitor as close as possible to the device, with a short return to PGND (pin 5). Make sure the VCC decoupling loop is small and use traces with a width of 12 mil or wider to route the connection.
- Place the BOOT capacitor as close as possible to the BOOT and SW pins. Use traces with a width of 12 mil or wider to route the connection.
- The PCB trace, which connects the SW pin and high-voltage side of the inductor, is defined as switch node. The switch node must be as short and wide as possible.
- If using external feedback, always place the feedback resistors near the device to minimize the FB trace distance, no matter single-end sensing or remote sensing.
  - For remote sensing, the connections from the FB voltage divider resistors to the remote location must be a differential pair of PCB traces, and must implement Kelvin sensing across a bypass capacitor of 0.1µF or higher. The ground connection of the remote sensing signal must be connected to GOS pin. The V_{OUT} connection of the remote sensing signal must be connected to the feedback resistor divider with the bottom feedback resistor terminated to the GOS pin. To maintain stable output voltage and minimize the ripple, the pair of remote sensing lines must stay away from any noise sources such as inductor and SW nodes, or high frequency clock lines. TI recommends to shield the pair of remote sensing lines with ground planes above and below.
  - For single-end sensing, connect the top feedback resistor between the FB pin and the output voltage to a high-frequency local output bypass capacitor of 0.1µF or higher, and short GOS to AGND with a short trace.
- Connect the AGND pin (pin 19) to the PGND pins (pins 5 and 11) beneath the device.
- Avoid routing the PG signal and any other noisy signals in the application near noise sensitive signals, such as VOS/FB and GOS to limit coupling.
- See *Layout Example* for the layout recommendation.

9.4.2 Layout Example

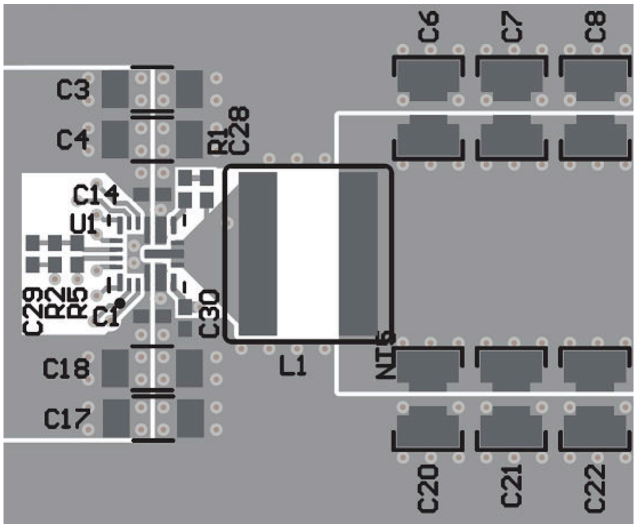

Figure 9-2. Layout Recommendation

For a more detailed layout example, please reference the *TPS548B23 Step-Down Converter Evaluation Module* EVM user's guide.

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

- Texas Instruments, *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feedforward Capacitor* application note
- Texas Instruments, *Non-isolated Point-of-load Solutions for VR13.HC in Rack Server and Datacenter Applications* application note
- Texas Instruments, *TPS548B23 Step-Down Converter Evaluation Module* EVM user's guide
- Texas Instruments, *How to select input capacitors for a buck converter* analog design journal

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

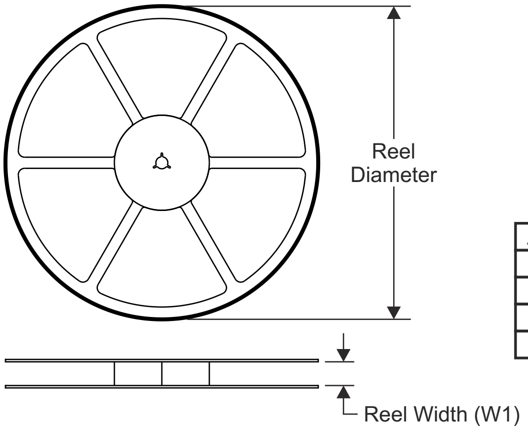
DATE	REVISION	NOTES
January 2026	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

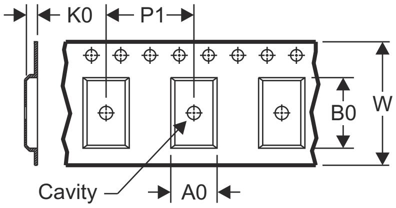
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Tape and Reel Information

REEL DIMENSIONS

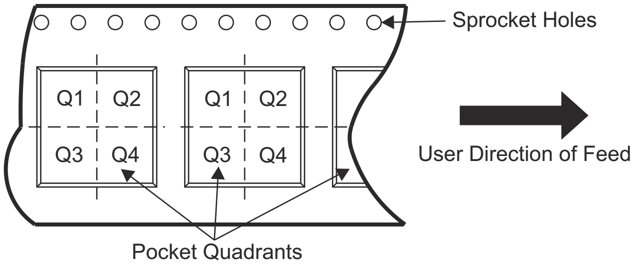


TAPE DIMENSIONS



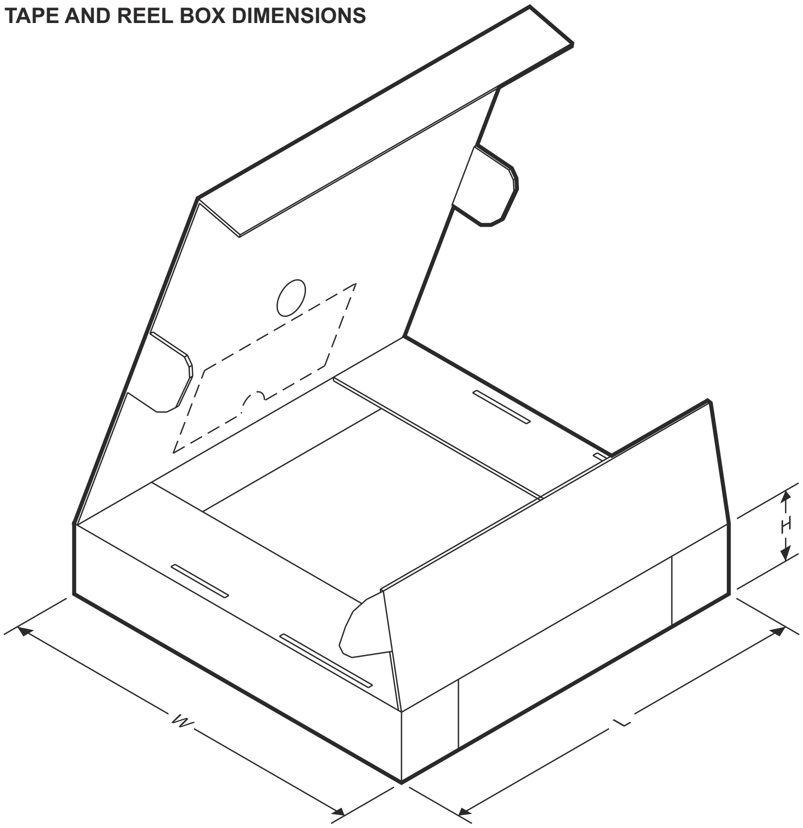
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS544B28	WQFN-HR	VAN	19	5000	330	12.4	3.3	3.3	1.1	8	12	2
		RBH					3.3	3.8	1.2	8	12	2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS544B28	WQFN-HR	VAN	19	5000	367	367	35
		RBH					

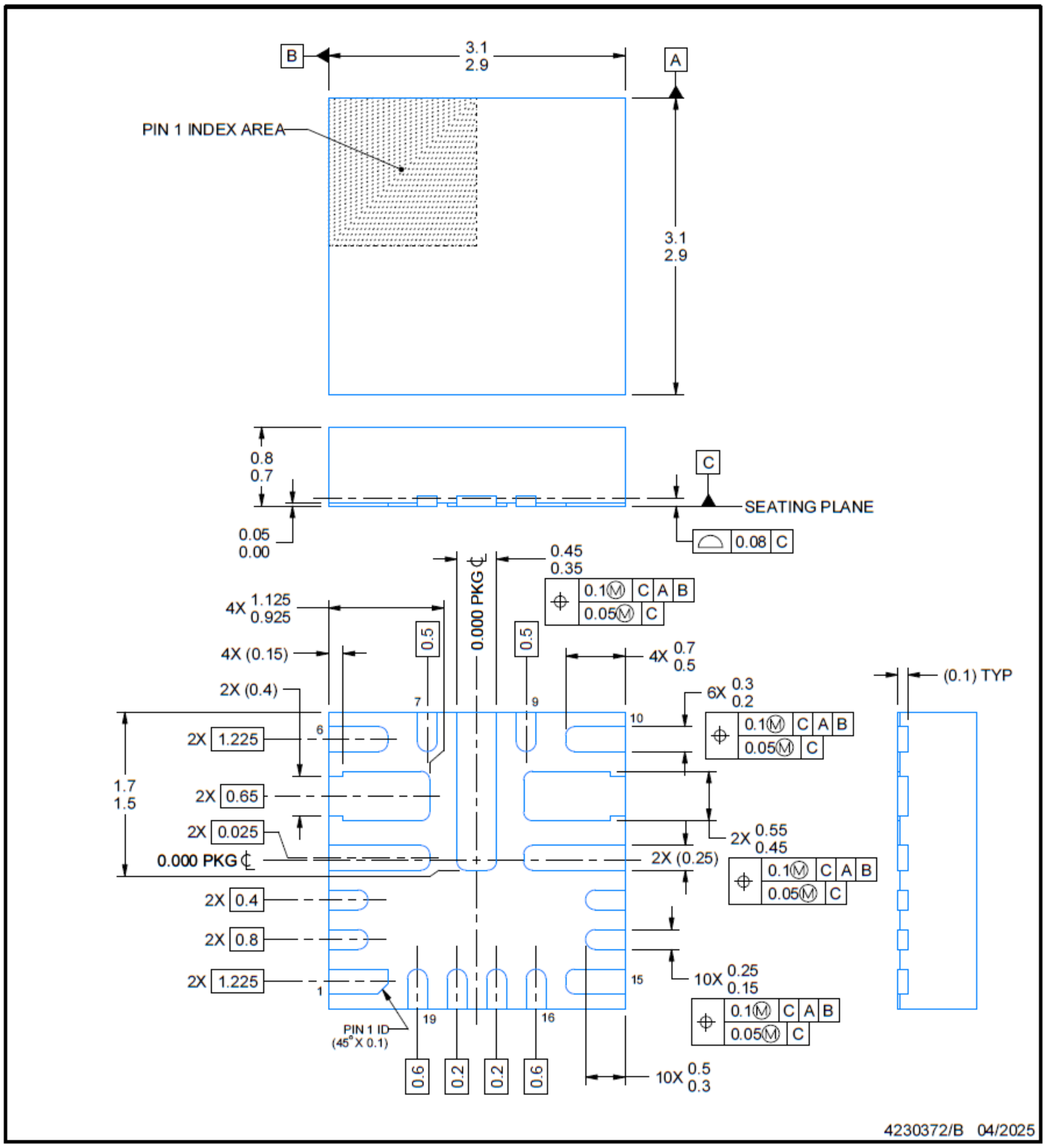
ADVANCE INFORMATION

VAN0019A

PACKAGE OUTLINE

WQFN-HR - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

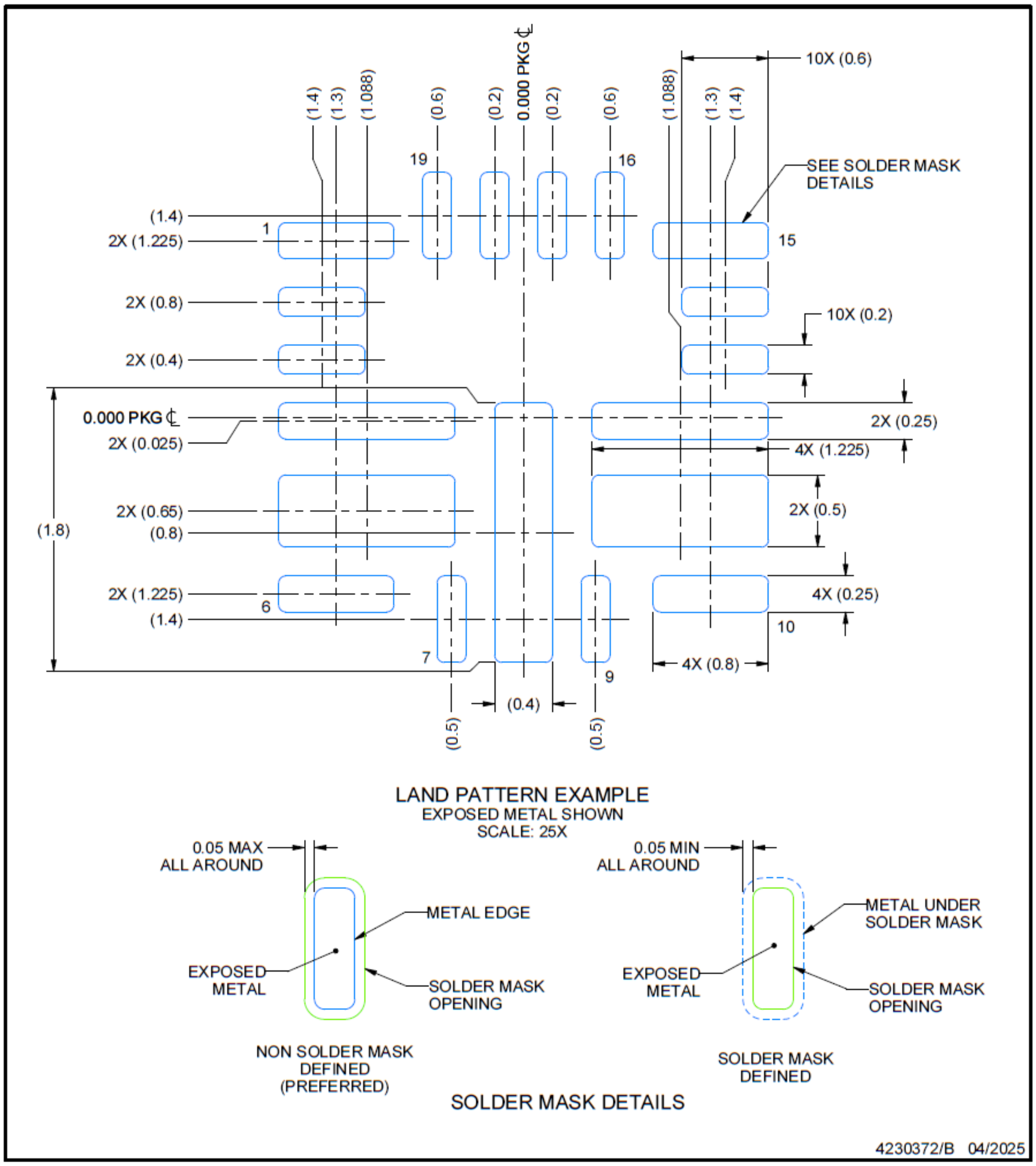
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

TEXAS INSTRUMENTS
www.ti.com

EXAMPLE BOARD LAYOUT

VAN0019A **WQFN-HR - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

SOLDER MASK DETAILS

4230372/B 04/2025

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

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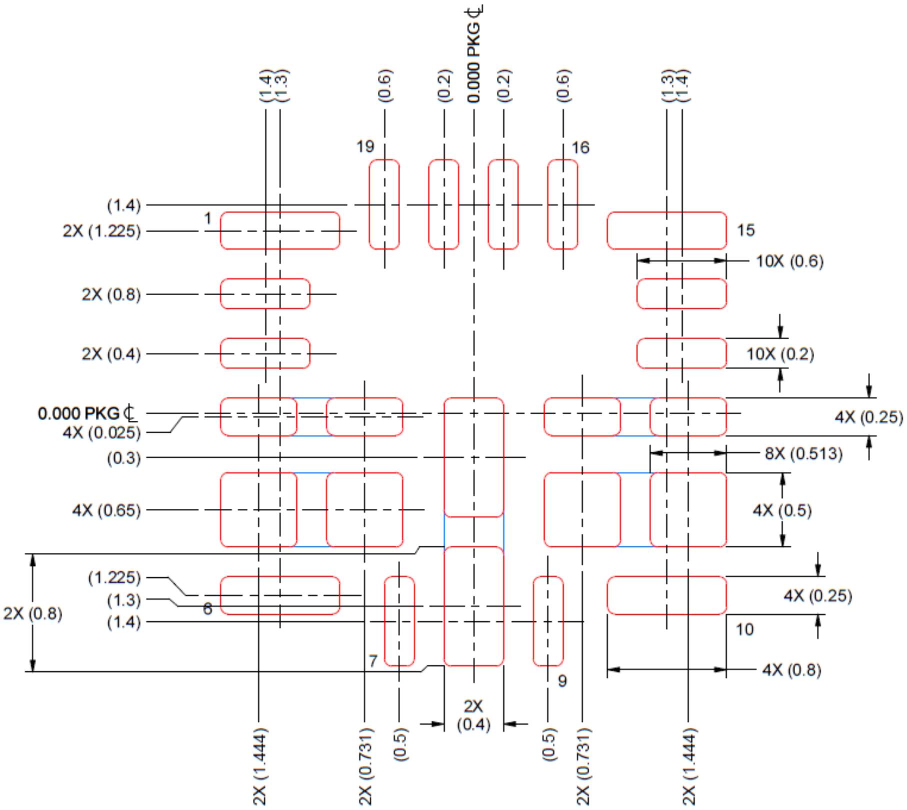
EXAMPLE STENCIL DESIGN

VAN0019A **WQFN-HR - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 4, 5, 11 & 12: 84%
PAD 8: 89%

4230372/B 04/2025

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

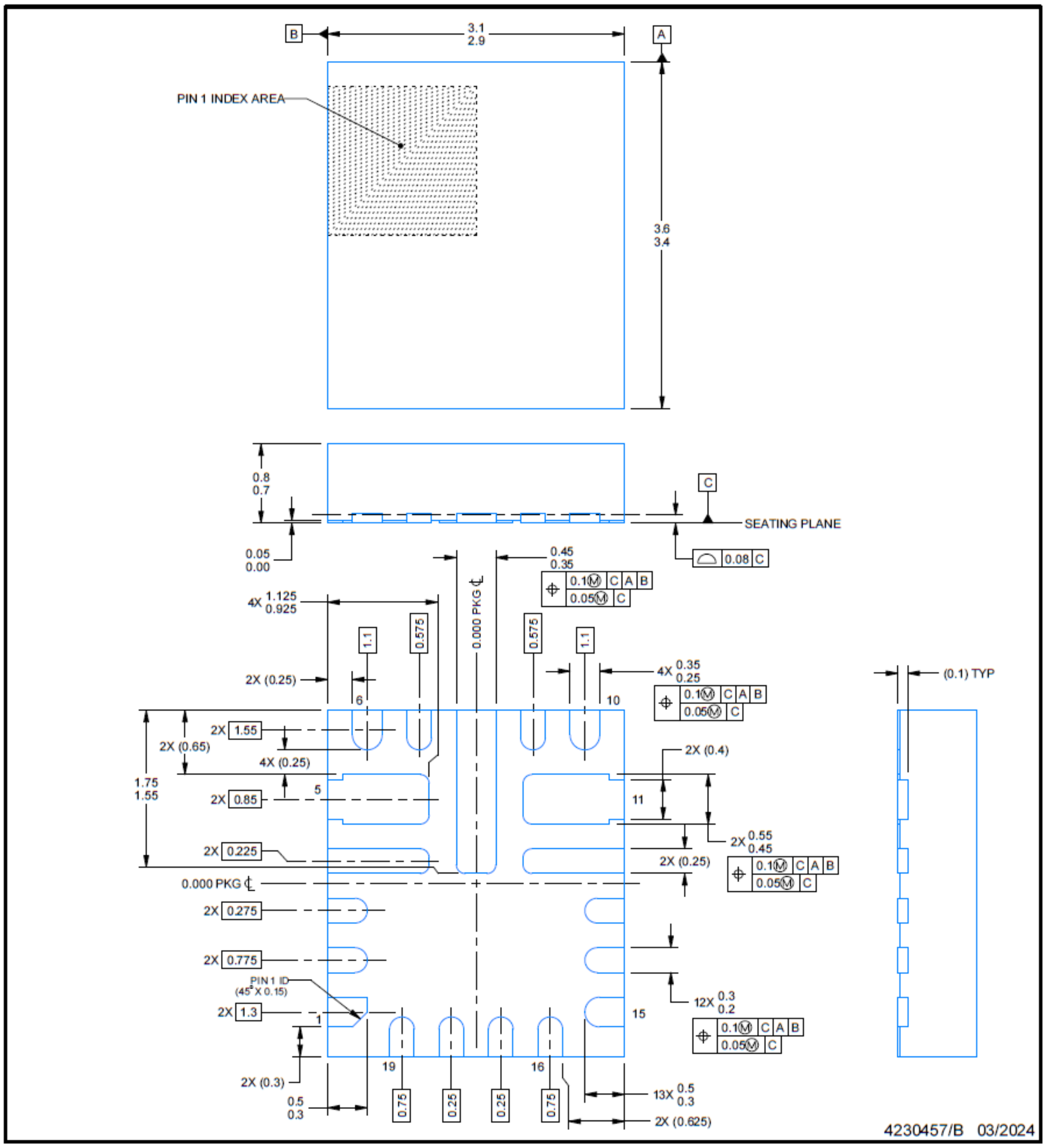
ADVANCE INFORMATION

PACKAGE OUTLINE

RBH0019A

WQFN-HR - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



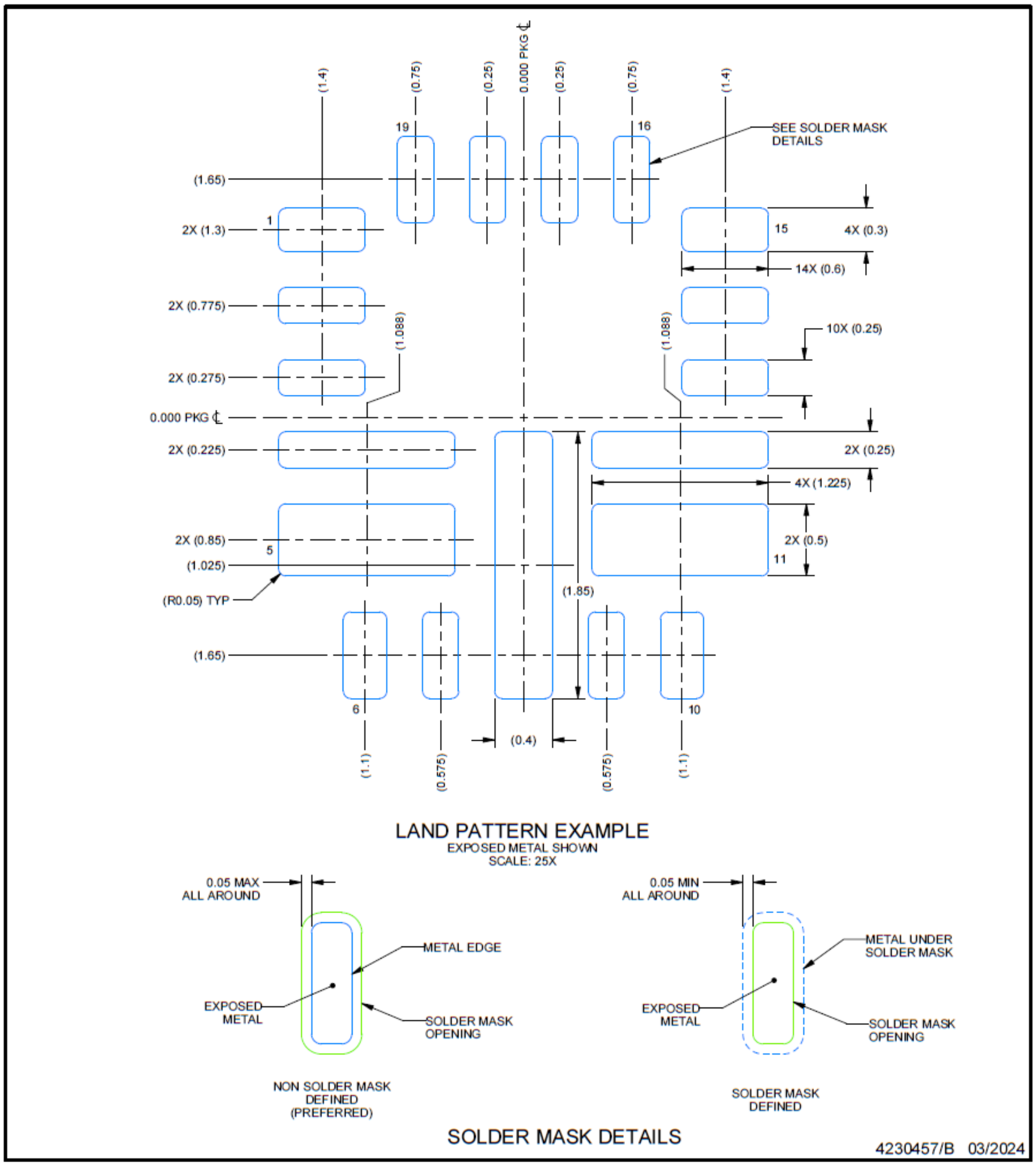
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

RBH0019A **WQFN-HR - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

SOLDER MASK DETAILS

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

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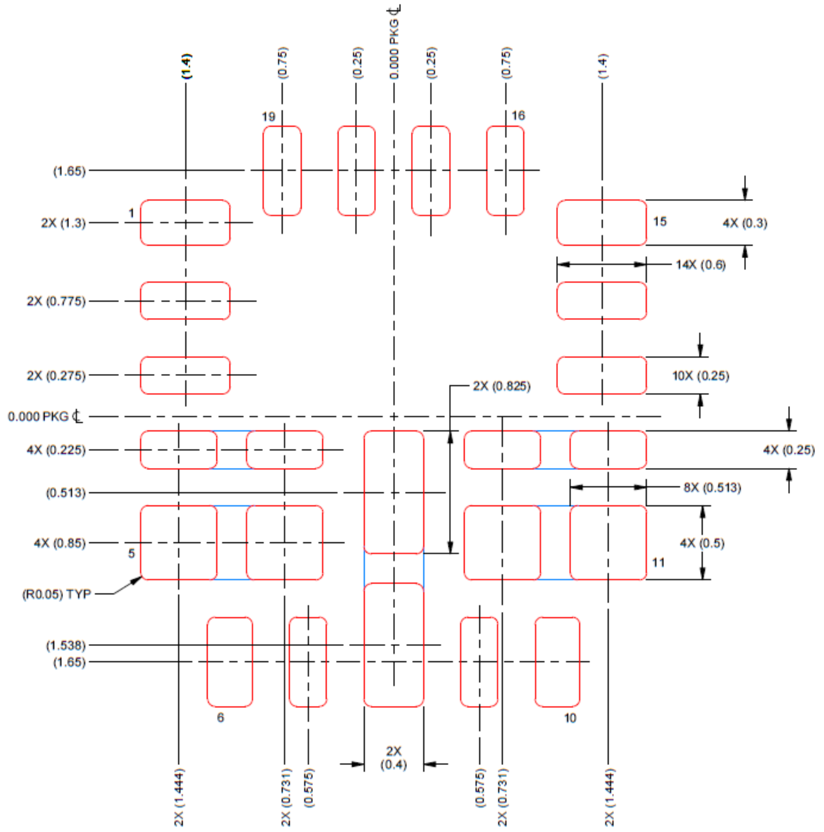
EXAMPLE STENCIL DESIGN

RBH0019A

WQFN-HR - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 4, 5, 11 & 12: 84%
PAD 8: 89%

4230457/B 03/2024

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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