TPS65982BB Dual USB Billboard for USB-PD Devices with Integrated 5-V Load Switch

1 Features

- Port-power switch
  - 5-V, 3-A integrated switch to VBUS
  - Over-current limiter, over-voltage protector
  - Slew-rate control
- USB low-speed endpoint
  - I2C-update capable billboard strings
  - Integrated USB mux supports two Type-C ports
  - I2C control
- Power management
  - Power supply from 3.3-V
- NFBGA package
  - 0.5-mm pitch
  - Through-hole via compatible for all pins

2 Applications

- Docking systems
- Charger adapters
- USB PD devices
- USB PD–enabled bus-powered devices
- DisplayPort, Thunderbolt

3 Description

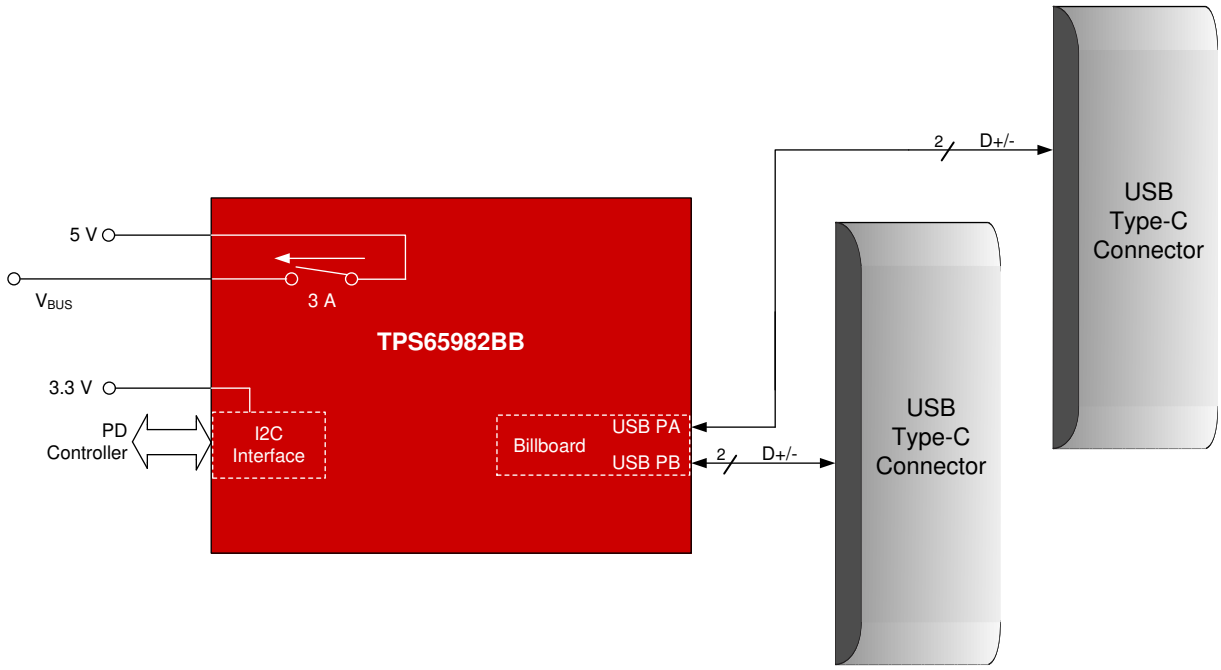
The TPS65982BB device provides a USB billboard endpoint for USB-PD devices implementing alternate modes. The integrated internal USB multiplexor allows the TPS65982BB to support up to two USB Type-C ports. The TPS65982BB communicates with USB-PD port controllers using an I2C interface to enable the billboard as well as update stored billboard strings. An integrated 5-V load switch provides VBUS protection for an optional USB Type-A port.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65982BB	NFBGA (96)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Diagram



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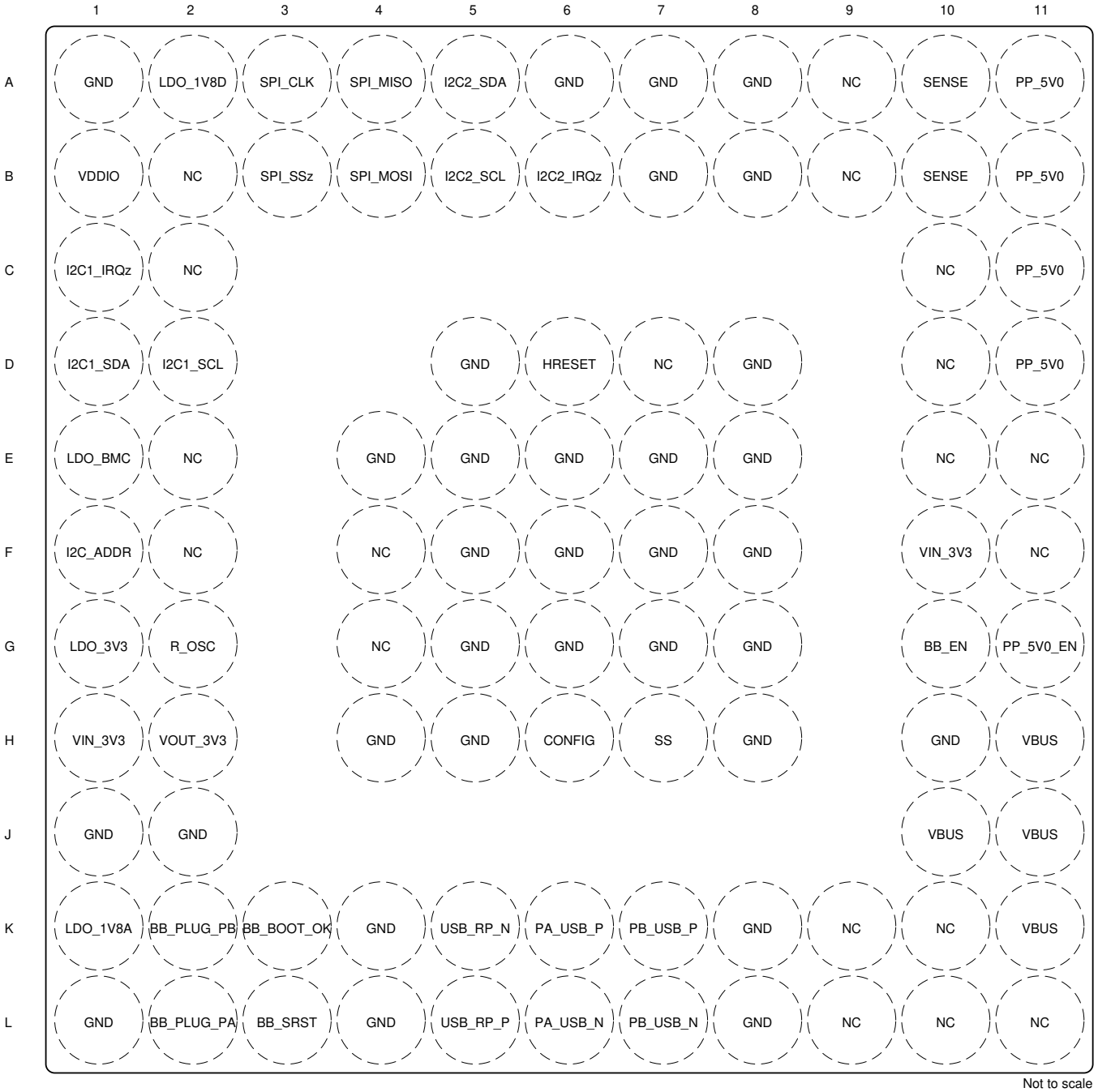
5 Pin Configuration and Functions

ZBH Package
96-Pin NFBGA
Transparent Top View



Not to scale

Pin Functions

PIN		TYPE	POR STATE	DESCRIPTION
NAME	NO.			
PP_5V0	A11, B11, C11, D11	Power	—	5-V supply for VBUS. Bypass with capacitance CPP_5V0 to GND. Tie pin to GND when unused.
VBUS	H11, J10, J11, K11	Power	—	5-V output from PP_5V0. Bypass with capacitance CVBUS to GND.

Pin Functions (continued)

PIN		TYPE	POR STATE	DESCRIPTION
NAME	NO.			
VIN_3V3	H1, F10	Power	—	Supply for core circuitry and I/O. Bypass with capacitance CVIN_3V3 to GND.
VDDIO	B1	Power	—	VDD for I/O.
VOUT_3V3	H2	Power	—	Output of supply switched from VIN_3V3. Bypass with capacitance COUT_3V3 to GND. Float pin when unused.
LDO_3V3	G1	Power	—	Output of the VBUS to 3.3 V LDO or connected to VIN_3V3 by a switch. Main internal supply rail. Used to power optional external flash memory. Bypass with capacitance CLDO_3V3 to GND.
LDO_1V8A	K1	Power	—	Output of the 3.3-V or 1.8-V LDO for core analog circuits. Bypass with capacitance CLDO_1V8A to GND.
LDO_1V8D	A2	Power	—	Output of the 3.3-V or 1.8-V LDO for core digital circuits. Bypass with capacitance CLDO_1V8D to GND.
LDO_BMC	E1	Power	—	Output of the 1.1V output level LDO. Bypass with capacitance CLDO_BMC to GND.
PA_USB_P	K6	Analog I/O	Hi-Z	Port A USB D+ connection.
PA_USB_N	L6	Analog I/O	Hi-Z	Port A USB D- connection.
PB_USB_P	K7	Analog I/O	Hi-Z	Port B USB D+ connection.
PB_USB_N	L7	Analog I/O	Hi-Z	Port B USB D- connection.
USB_RP_P	L5	Analog I/O	Hi-Z	System-side USB2.0 high-speed connection to port multiplexer. Ground pin with between 1-kΩ and 5-MΩ resistance when unused.
USB_RP_N	K5	Analog I/O	Hi-Z	System-side USB2.0 high-speed connection to port multiplexer. Ground pin with between 1-kΩ and 5-MΩ resistance when unused.
SENSE	B10	Analog input	Analog input	Short pin to VBUS.
SENSE	A10	Analog input	Analog input	Short pin to VBUS.
SS	H7	Analog output	Driven low	Soft Start. Tie pin to capacitance CSS to ground.
R_OSC	G2	Analog I/O	Hi-Z	External resistance setting for oscillator accuracy. Connect R_OSC to GND through resistance RR_OSC.
PP_5V0_EN	G11	Digital I/O	Hi-Z	Input enable signal for PP_5V0 power path.
CONFIG	H6	Analog input	Hi-Z	Boot Configuration pin. Tie directly to ground.
BB_BOOT_OK	K3	Digital I/O	Hi-Z	Output. Driven high once the TPS65982BB has completed its boot and configuration routines.
BB_EN	G10	Digital I/O	Hi-Z	Input. When driven high enables billboard output on PA_USB_P and PA_USB_N.
BB_SRST	L3	Digital I/O	Hi-Z	Input. When asserted high, initiates a soft reset of the TPS65982BB.
BB_PLUG_PB	K2	Digital I/O	Hi-Z	Input. Signals the TPS65982BB to enable the USB billboard on the PA_USB pins.
BB_PLUG_PA	L2	Digital I/O	Hi-Z	Input. Signals the TPS65982BB to enable the USB billboard on the PB_USB pins.
HRESET	D6	Digital Input	Hi-Z	Active high hardware reset input. Assertion causes a reboot sequence. Ground pin when HRESET functionality will not be used.
I2C_SDA1	D1	Digital I/O	Digital input	I^2C port 1 serial data. Open-drain output. Tie pin to LDO_3V3 or VDDIO (depending on configuration) through a 10-kΩ resistance when used or unused.
I2C_SCL1	D2	Digital I/O	Digital input	I^2C port 1 serial clock. Open-drain output. Tie pin to LDO_3V3 or VDDIO (depending on configuration) through a 10-kΩ resistance when used or unused.
I2C_IRQ1Z	C1	Digital output	Hi-Z	I^2C port 1 interrupt. Active low. Implement externally as an open drain with a pullup resistance. Float pin when unused.
I2C_SDA2	A5	Digital I/O	Digital input	I^2C port 2 serial data. Open-drain output. Tie pin to LDO_3V3 or VDDIO (depending on configuration) through a 10-kΩ resistance when used or unused.
I2C_SCL2	B5	Digital I/O	Digital input	I^2C port 2 serial clock. Open-drain output. Tie pin to LDO_3V3 or VDDIO (depending on configuration) through a 10-kΩ resistance when used or unused.
I2C_IRQ2Z	B6	Digital output	Hi-Z	I^2C port 2 interrupt. Active low. Implement externally as an open drain with a pullup resistance. Float pin when unused.
I2C_ADDR	F1	Analog I/O	Analog input	Sets the I^2C address for both I^2C ports.
SPI_CLK	A3	Digital output	Digital input	SPI serial clock. Ground pin when unused
SPI_MOSI	B4	Digital output	Digital input	SPI serial master output to slave. Ground pin when unused.
SPI_MISO	A4	Digital input	Digital input	SPI serial master input from slave. This pin is used during boot sequence to determine if the optional flash memory is valid. Refer to the *Device Functional Modes* section for more details. Ground pin when unused.

Pin Functions (continued)

PIN		TYPE	POR STATE	DESCRIPTION
NAME	NO.			
SPI_SSZ	B3	Digital output	Digital input	SPI slave select. Ground pin when unused.
GND	A1, A6, A7, A8, B7, B8, D5, D8, E4, E5, E6, E7, E8, F5, F6, F7, F8, G5, G6, G7, G8, H4, H5, H8, H10, J1, J2, K4, K8, L1, L4, L8	Ground	NA	Ground. Connect all balls to ground plane.
NC	A9, B2, B9, C2, C10, D7, D10, E2, E10, E11, F2, F4, F11, G4, K9, K10, L9, L10, L11	Blank	NA	Populated Ball that must remain unconnected.
No Ball	C3, C4, C5, C6, C7, C8, C9, D3, D4, D9, E3, E9, F3, F9, G3, G9, H3, H9, J3, J4, J5, J6, J7, J8, J9	Blank	NA	Unpopulated Ball for A1 marker and unpopulated inner ring.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_I	Input voltage(2)	PP_5V0	–0.3	6	V
		VIN_3V3	–0.3	3.6	
		SENSE	–0.3	6	
		VDDIO	–0.3	LDO_3V3 + 0.3	
V_{IO}	Output voltage(2)	LDO_1V8A, LDO_1V8D, LDO_BMC	–0.3	2	V
		LDO_3V3	–0.3	3.45	
		VOUT_3V3, I2C _IRQ1Z, I2C_IRQ2Z, SPI_MOSI, SPI_CLK, SPI_SSZ, I2C_ADDR	–0.3	LDO_3V3 + 0.3	
V_{IO}	I/O voltage(2)	VBUS	–0.3	6	V
		I2C_SDA1, I2C_SCL1, SPI_MISO, I2C_SDA2, I2C_SCL2, USB_RP_P, USB_RP_N, CONFIG, PP_5V0_EN, BB_BOOT_OK, BB_SRST, BB_PLUG_PB, BB_PLUG_PA	–0.3	LDO_3V3 + 0.3	
		R_OSC	–0.3	2	
		HRESET	-0.3	LDO_1V8D + 0.3	
		PA_USB_P, PA_USB_N, PB_USB_P, PB_USB_N (Switches Open)	–2	6	
		PA_USB_P, PA_USB_N, PB_USB_P, PB_USB_N (Switches Closed)	–0.3	6	
T_J	Operating junction temperature		–10	125	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network GND. All GND pins must be connected directly to the GND plane of the board.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_I	Input voltage(1)	VIN_3V3	2.85	3.45	V
		PP_5V0	4.75	5.5	
		VDDIO	1.7	3.45	
V_{IO}	I/O voltage(1)	VBUS	4	5.5	V
		PA_USB_P, PA_USB_N, PB_USB_P, PB_USB_N	–2	5.5	
T_A	Ambient operating temperature		–10	85	°C
T_B	Operating board temperature		–10	100	°C
T_J	Operating junction temperature		–10	125	°C

(1) All voltage values are with respect to network GND. All GND pins must be connected directly to the GND plane of the board.

6.4 Thermal Information

THERMAL METRIC(1)		TPS65982BB ZBH (NFBGA) 96 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	12.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Power Supply Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL						
VIN_3V3	Input 3.3-V supply		2.85	3.3	3.45	V
VBUS	Output DC bus voltage.		4	5	5.5	V
PP_5V0	5-V supply input to power VBUS. This supply does not power the TPS65982BB		4.75	5	5.5	V
VDDIO (1)	Optional supply for I/O cells		1.7		3.45	V
INTERNAL						
VLDO_3V3	DC 3.3 V generated internally by either a switch from VIN_3V3, an LDO from PP_CABLE, or an LDO from VBUS		2.7	3.3	3.45	V
VLDO_1V8D	DC 1.8 V generated for internal digital circuitry		1.7	1.8	1.9	V
VLDO_1V8A	DC 1.8 V generated for internal analog circuitry		1.7	1.8	1.9	V
VLDO_BMC	DC voltage generated on LDO_BMC. Setting for USB-PD.		1.05	1.125	1.2	V
IOUT_3V3	External DC current supplied by VOUT_3V3				100	mA
ILDO_1V8D	DC current supplied by LDO_1V8D. This is intended for internal loads only but small external loads may be added				50	mA
ILDO_1V8DEX	External DC current supplied by LDO_1V8D				5	mA
ILDO_1V8A	DC current supplied by LDO_1V8A. This is intended for internal loads only but small external loads may be added				20	mA
ILDO_1V8AEX	External DC current supplied by LDO_1V8A				5	mA
ILDO_BMC	DC current supplied by LDO_BMC. This is intended for internal loads only				5	mA
ILDO_BMCEX	External DC current supplied by LDO_BMC				0	mA
VFWD_DROP	Forward voltage drop across VIN_3V3 to LDO_3V3 switch	I_{LOAD} = 50 mA	25	60	90	mV
RIN_3V3	Input switch resistance from VIN_3V3 to LDO_3V3	$V_{VIN\_3V3} – V_{LDO\_3V3}$ > 50 mV	0.5	1.1	1.75	Ω
ROUT_3V3	Output switch resistance from VIN_3V3 to VOUT_3V3			0.35	0.7	Ω
TR_OUT3V3	10-90% rise time on VOUT_3V3 from switch enable	C_{VOUT_3V3} = 1 µF	35		120	µs

(1) I/O buffers are not fail-safe to LDO_3V3. Therefore, VDDIO may power-up before LDO_3V3. When VDDIO powers up before LDO_3V3, the I/Os shall not be driven high. When VDDIO is low and LDO_3V3 is high, the I/Os may be driven high.

6.6 Power Supervisor Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UV_LDO3V3	Undervoltage threshold for LDO_3V3. Locks out 1.8-V LDOs	LDO_3V3 rising	2.2	2.325	2.45	V
UVH_LDO3V3	Undervoltage hysteresis for LDO_3V3	LDO_3V3 falling	20	80	150	mV
UV_5V0	Undervoltage threshold for PP_5V0	PP_5V0 rising	3.5	3.725	3.95	V
UVH_5V0	Undervoltage hysteresis for PP_P5V0	PP_5V0 falling	20	80	150	mV
OV_VBUS	Overvoltage threshold for VBUS.	VBUS rising	5		24	V
OVLSB_VBUS	Overvoltage threshold step for VBUS. This value is the LSB of the programmable threshold	VBUS rising		328		mV
OVH_VBUS	Overvoltage hysteresis for VBUS	VBUS falling, % of OV_VBUS	0.9%	1.3%	1.7%	
UV_VBUS	Undervoltage threshold for VBUS.	VBUS falling	2.5		18.21	V
UVLSB_VBUS	Undervoltage threshold step for VBUS. This value is the LSB of the programmable threshold	VBUS falling		249		mV
UVH_VBUS	Undervoltage hysteresis for VBUS	VBUS rising, % of UV_VBUS	0.9%	1.3%	1.7%	

6.7 Power Consumption Characteristics

Recommended operating conditions; T_A = 25°C (Room temperature) unless otherwise noted(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IVIN_3V3 in sleep	VIN_3V3 = VDDIO = 3.45 V, VBUS = 0, 100-kHz oscillator running		71		µA
IVIN_3V3 idle	VIN_3V3 = VDDIO = 3.45 V, VBUS=0, 100-kHz oscillator running, 48-MHz oscillator running		2.2		mA
IVIN_3V3 active	VIN_3V3 = VDDIO = 3.45 V, VBUS = 0, 100-kHz Oscillator running, 48-MHz oscillator running		5.3		mA

(1) Application code can result in other power consumption measurements by adjusting enabled circuitry and clock rates. Application code also provisions the wake-up mechanisms (for example, I^2C activity and GPIO activity).

6.8 Port-Power Switch Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
RPP5V	PP_5V0 to VBUS power switch resistance			50	60	mΩ
IPP5VACT	Active quiescent current from PP_5V0				1	mA
IPP5VSD	Shutdown quiescent current from PP_5V0				100	µA
ILIMPP5V	PP_5V0 current limit		3.019	3.355	3.69	
IPP5V_ACC(2)	PP_5V0 current sense accuracy	I = 100 mA, reverse current blocking disabled	1.95	3	4.05	A/V
		I = 200 mA	2.4	3	3.6	A/V
		I = 500 mA	2.64	3	3.36	A/V
		I ≥ 1 A	2.7	3	3.3	A/V
TON_5V	PP_5V0 path turn on time from enable to VBUS = 95% of PP_5V0 voltage	Configured as a source or as a sink with soft start disabled. PP_5V0 = 5 V, CVBUS = 10 µF, ILOAD = 100 mA			2.5	ms
VREV5V0	Reverse-current blocking voltage threshold for PP_5V0 switches		2	6	10	mV
VSAFE0V	Voltage that is a safe 0 V per USB-PD Specifications		0		0.8	V

(1) Maximum capacitance on VBUS when configured as a source must not exceed 12 µF.
(2) The current sense in the ADC does not accurately read below the current VREV5V0/RPP5V or VREVHV/RPPHV because of the reverse blocking behavior. When reverse blocking is disabled, the values given for accuracy are valid.

6.9 Port-Data Multiplexer Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
USB_RP MULTIPLEXER PATH(1)(2)						
USB_RON	On resistance of USB_RP to Px_USB_P/N	V_i = 3 V, I_O = 20 mA		4.5	10	Ω
		V_i = 400 mV, I_O = 20 mA		3	7	
USB_ROND	On-resistance difference between P and N paths of USB_RP to Px_USB_P/N	V_i = 0.4 V to 3 V, I_O = 20 mA	–0.15		0.15	Ω
USB_TON	Switch-on time from enable of USB USB_RP path	Time from enable bit with charge pump off			150	µs
		Time from enable bit at charge-pump steady state			15	
USB_TOFF	Switch-off time from disable of USB_RP path	Time from disable bit at charge-pump steady state			500	ns
USB_BW	3-dB bandwidth of USB_RP path	C_L = 10 pF	850			MHz
USB_ISO	Off isolation of USB_RP path	R_L = 50 Ω, V_I = 800 mV, f = 240 MHz			–19	dB
USB_XTLK	Channel-to-channel crosstalk of USB_RP path	R_L = 50 Ω, f = 240 MHz			–26	dB

(1) All RON specified maximums are the maximum of either of the switches in a pair. All ROND specified maximums are the maximum difference between the two switches in a pair. ROND does not add to RON.
(2) See the *USB Endpoint Characteristics* table for the USB_EP specifications.

6.10 Port-Data Multiplexer Clamp Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCLMP_IND	Clamp voltage triggering indicator to the digital core		3.8	3.95	4.1	V
ICLMP_IND	Clamp current at VCLMP_IND		10		250	µA
TCLMP_PRT(1)	Time from clamp-current crossing ICLMP_IND to interrupt signal assertion	I ≥ ICLMP_IND rising	0		4	µs
ICLMP	USB_EP and USB_RP port-clamp current	V = LDO_3V3			250	nA
		V = VCLMP_IND + 500 mV	3.5		15	mA

(1) The TCLMP_PRT time includes the time through the digital synchronizers. When the clock speed is reduced, the signal assertion time can be longer.

6.11 Port-Data Multiplexer Signal Monitoring Pullup and Pulldown Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RPU05	500-Ω pullup and pulldown resistance	LDO_3V3 = 3.3 V	350	500	650	Ω
RTPU5	5-kΩ pullup and pulldown resistance	LDO_3V3 = 3.3 V	3.5	5	6.5	kΩ
RPU100	100-kΩ pullup and pulldown resistance	LDO_3V3 = 3.3 V	70	100	130	kΩ

6.12 USB Endpoint Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TRANSMITTER(1)						
T_RISE_EP	Rising transition time	Low-speed (1.5 Mbps) data rate only	75		300	ns
T_FALL_EP	Falling transition time	Low-speed (1.5 Mbps) data rate only	75		300	ns
T_RRM_EP	Rise and fall time matching	Low-speed (1.5 Mbps) data rate only	–20%		25%	
V_XOVER_EP	Output crossover voltage		1.3		2	V
RS_EP	Source resistance of driver including 2nd-stage port-data multiplexer			34		Ω
DIFFERENTIAL RECEIVER(1)						
VOS_DIFF_EP	Input offset		–100		100	mV
VIN_CM_EP	Common-mode range		0.8		2.5	V
RPU_EP	D– bias resistance	Receiving	1.425		1.575	kΩ
SINGLE ENDED RECEIVER(1)						
VTH_SE_EP	Single ended threshold	Signal rising or falling	0.8		2	V
VHYS_SE_EP	Single ended threshold hysteresis	Signal falling		200		mV

(1) The USB endpoint PHY is functional across the entire VIN_3V3 operating range, but parameter values are only verified by design for VIN_3V3 ≥ 3.135 V

6.13 Input/Output (I/O) Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPI						
SPI_VIH	High-level input voltage	LDO_3V3 = 3.3 V	2			V
SPI_VIL	Low-level input voltage	LDO_3V3 = 3.3 V			0.8	V
SPI_HYS	Input hysteresis voltage	LDO_3V3 = 3.3 V	0.2			V
SPI_ILKG	Leakage current	Output is Hi-Z, V_{IN} = 0 to LDO_3V3	–1		1	µA
SPI_VOH	SPI output high voltage	I_O = –8 mA, LDO_3V3=3.3 V	2.9			V
		I_O = –15 mA, LDO_3V3=3.3 V	2.5			
SPI_VOL	SPI output low voltage	I_O = 10 mA			0.4	V
		I_O = 20 mA			0.8	
GPIO, MRESET						
GPIO_VIH	High-level input voltage	LDO_3V3 = 3.3 V	2			V
		VDDDIO = 1.8 V	1.25			
GPIO_VIL	Low-level input voltage	LDO_3V3 = 3.3 V			0.8	V
		VDDIO = 1.8 V			0.63	
GPIO_HYS	Input hysteresis voltage	LDO_3V3 = 3.3 V	0.2			V
		VDDIO = 1.8 V	0.09			
GPIO_ILKG	I/O leakage current	INPUT = 0 V to VDD	–1		1	µA
GPIO_RPU	Pullup resistance	Pullup enabled	50	100	150	kΩ
GPIO_RPD	Pulldown resistance	Pulldown enabled	50	100	150	kΩ
GPIO_DG	Digital input path deglitch			20		ns
GPIO_VOH	GPIO output high voltage	IO = –2 mA, LDO_3V3 = 3.3 V	2.9			V
		IO = –2 mA, VDDIO = 1.8 V	1.35			
GPIO_VOL	GPIO output low voltage	IO = 2 mA, LDO_3V3 = 3.3 V			0.4	V
		IO = 2 mA, VDDIO = 1.8 V			0.45	
HRESET						
HRESET_VIH	High-level input voltage		1.25			V
HRESET_VIL	Low-level input voltage				0.63	V
HRESET_HYS	Input hysteresis Voltage		0.09			V
HRESET_ILKG	I/O leakage current	INPUT = 0 V to LDO_1V8D	–1		1	µA

Input/Output (I/O) Characteristics (continued)

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HRESET_THIGH	HRESET minimum high time to assert a reset condition.		0.6			ms
HRESET_TLOW	HRESET minimum low time to deassert a reset condition.		0.6			
I2C_IRQ1Z, I2C_IRQ2Z						
OD_VOL	Low-level output voltage	IOL = 2 mA			0.4	V
OD_LKG	Leakage current	Output is Hi-Z, V_{IN} = 0 to LDO_3V3	–1		1	µA

6.14 I²C Slave Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SDA and SCL COMMON CHARACTERISTICS						
ILEAK	Input leakage current	Voltage on pin = LDO_3V3	-3		3	µA
VOL	SDA output low voltage	IOL = 3 mA, LDO_3V3 = 3.3 V			0.4	V
		IOL = 3 mA, VDDIO = 1.8 V			0.36	
IOL	SDA maximum output-low current	VOL = 0.4 V	3			mA
		VOL = 0.6 V	6			
VIL	Input low signal	LDO_3V3 = 3.3 V			0.99	V
		VDDIO = 1.8 V			0.54	
VIH	Input high signal	LDO_3V3 = 3.3 V	2.31			V
		VDDIO = 1.8 V	1.26			
VHYS	Input hysteresis	LDO_3V3 = 3.3 V	0.17			V
		VDDIO = 1.8 V	0.09			
TSP	I²C pulse width suppressed				50	ns
CI	Pin Capacitance				10	pF
SDA and SCL STANDARD MODE CHARACTERISTICS						
FSCL	I²C clock frequency		0		100	kHz
THIGH	I²C clock high time		4			µs
TLOW	I²C clock low time		4.7			µs
TSUDAT	I²C serial data-setup time		250			ns
THDDAT	I²C serial data-hold time		0			ns
TVDDAT	I²C valid data time	SCL low to SDA output valid			3.4	µs
TVDACK	I²C valid data time of ACK condition	ACK signal from SCL low to SDA (out) low			3.4	µs
TOCF	I²C output fall time	10 pF to 400 pF bus			250	ns
TBUF	I²C bus free time between stop and start		4.7			µs
TSTS	I²C start or repeated start condition setup time		4.7			µs
TSTH	I²C start or repeated start condition hold time		4			µs
TSPS	I²C stop-condition setup time		4			µs
SDA and SCL FAST MODE CHARACTERISTICS						
FSCL	I²C clock frequency		0		400	kHz
THIGH	I²C clock high time		0.6			µs
TLOW	I²C clock low time		1.3			µs
TSUDAT	I²C serial data-setup time		100			ns
THDDAT	I²C serial data-hold time		0			ns
TVDDAT	I²C valid data time	SCL low to SDA output valid			0.9	µs
TVDACK	I²C valid data time of ACK condition	ACK signal from SCL low to SDA (out) low			0.9	µs
TOCF	I²C output fall time	10 pF to 400 pF bus, VDD = 3.3 V	12		250	ns
		10 pF to 400 pF bus, VDD = 1.8 V	6.5		250	
TBUF	I²C bus free time between stop and start		1.3			µs

I²C Slave Characteristics (continued)

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TSTS	I²C start or repeated start condition setup time		0.6			µs
TSTH	I²C start or repeated start condition hold time		0.6			µs
TSPS	I²C stop-condition setup time		0.6			µs

6.15 Thermal Shutdown Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TSD_MAIN	Thermal shutdown temperature of the main thermal shutdown	Temperature rising	145	160	175	°C
TSDH_MAIN	Thermal shutdown hysteresis of the main thermal shutdown	Temperature falling		20		°C
TSD_PWR	Thermal shutdown temperature of the power-path block	Temperature rising	135	150	165	°C
TSDH_PWR	Thermal shutdown hysteresis of the power-path block	Temperature falling		37		°C
TSD_DG	Programmable thermal shutdown detection deglitch time				0.1	ms

6.16 Oscillator Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FOSC_48M	48-MHz oscillator		47.28	48	48.72	MHz
FOSC_100K	100-kHz oscillator		95	100	105	kHz
RR_OSC	External oscillator set resistance (0.2%)		14.985	15	15.015	kΩ

6.17 SPI Master Switching Characteristics

Recommended operating conditions; T_A = –10 to +85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FSPI	Frequency of SPI_CLK		11.82	12	12.18	MHz
TPER	Period of SPI_CLK (1/F_SPI)		82.1	83.33	84.6	ns
TWHI	SPI_CLK high width		30			ns
TWLO	SPI_CLK low width		30			ns
TDACT	SPI_SZZ falling to SPI_CLK rising delay time		30		50	ns
TDINACT	SPI_CLK falling to SPI_SSZ rising delay time		160		180	ns
TDMOSI	SPI_CLK falling to SPI_MOSI Valid delay time		–5		5	ns
TSUMISO	SPI_MISO valid to SPI_CLK falling setup time		21			ns
THDMSIO	SPI_CLK falling to SPI_MISO invalid hold time		0			ns
TRSPI	SPI_SSZ/CLK/MOSI rise time	10% to 90%, C_L = 5 pF to 50 pF, LDO_3V3 = 3.3 V	0.1		8	ns
TFSPI	SPI_SSZ/CLK/MOSI fall time	90% to 10%, C_L = 5 pF to 50 pF, LDO_3V3 = 3.3 V	0.1		8	ns

6.18 Typical Characteristics

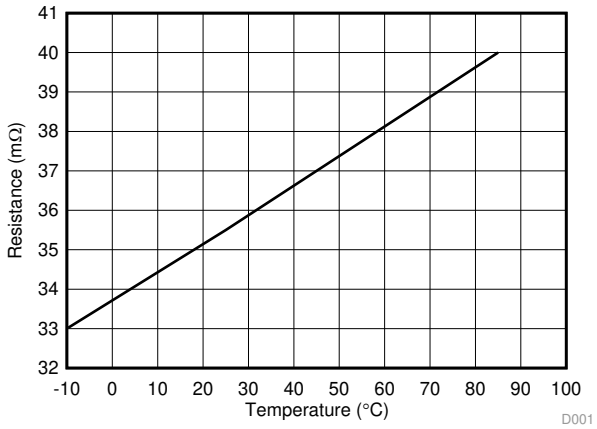


Figure 1. PP_5V0 Switch On-Resistance vs Temperature

7 Parameter Measurement Information

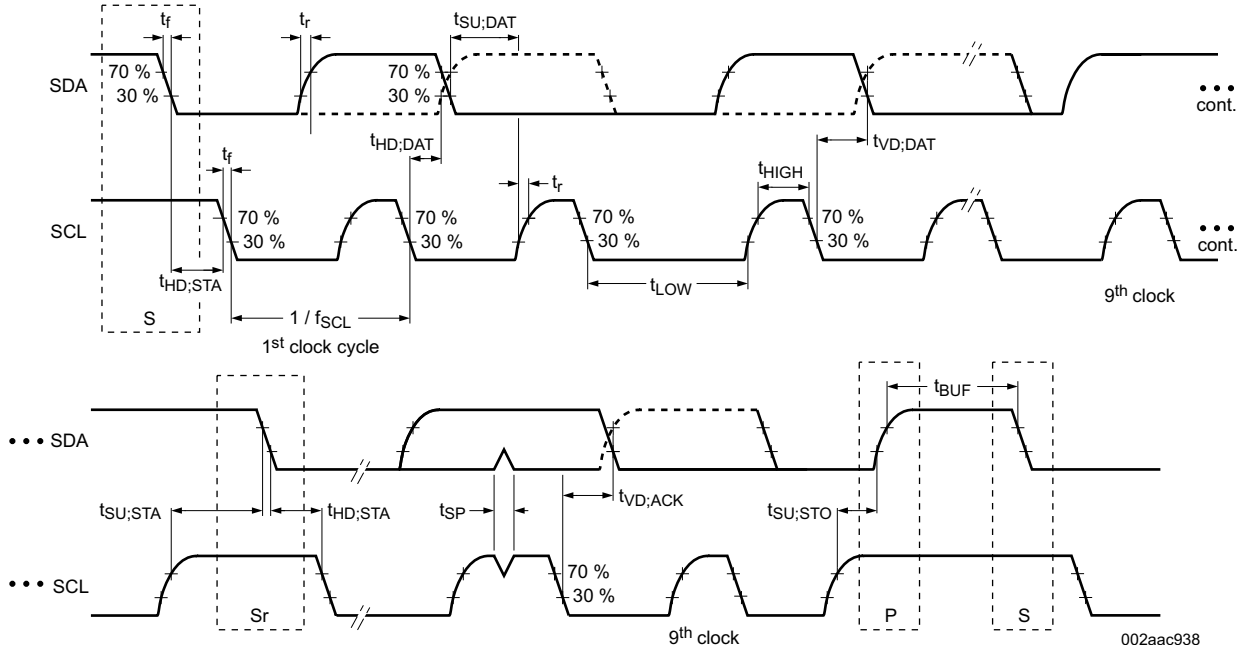


Figure 2. I²C Slave Interface Timing

Parameter Measurement Information (continued)

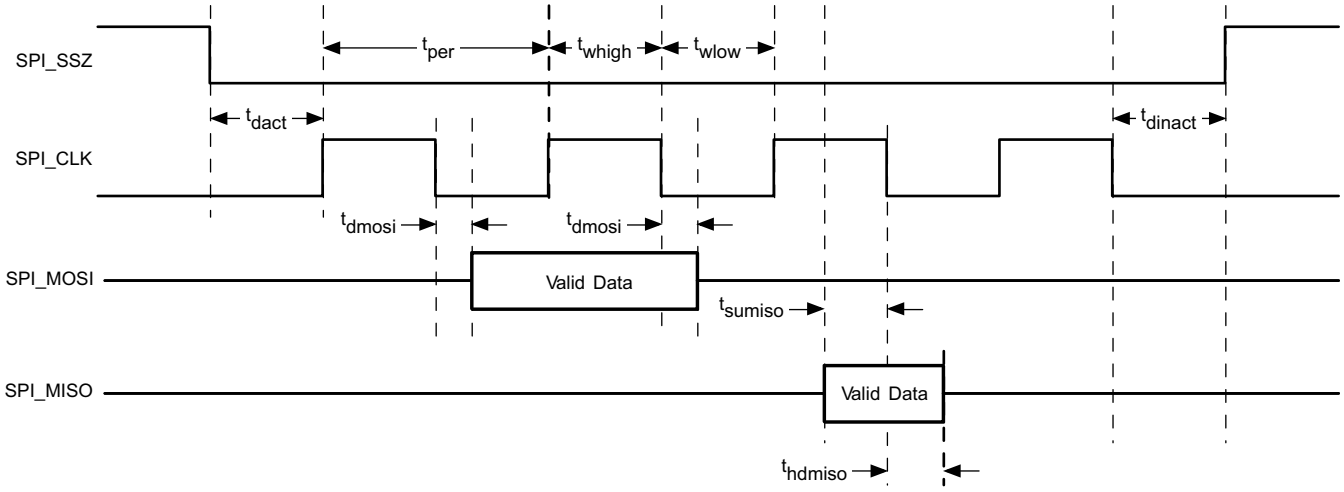


Figure 3. SPI Master Timing

8 Detailed Description

8.1 Overview

The TPS65982BB is a USB billboard controller for USB Type-C systems. The integrated USB2 data multiplexer allows the billboard controller to be switched between two USB Type-C ports or allows a USB2 device controller to be passed through to the ports.

The TPS65982BB includes an integrated 5V load switch that may be used to supply VBUS power to an additional USB Type-A receptacle. See the *Port-Power Switches* section for a high-level block diagram of the port power switch, a description of the features, and more detailed circuitry.

The port-data multiplexer connects various input pairs to the system port through the PA_USB_P, PA_USB_N, PB_USB_P, PB_USB_N pins. For a high-level block diagram of the port-data multiplexer, a description of the features, and more detailed circuitry, refer to the *USB Port-Data Multiplexer* section.

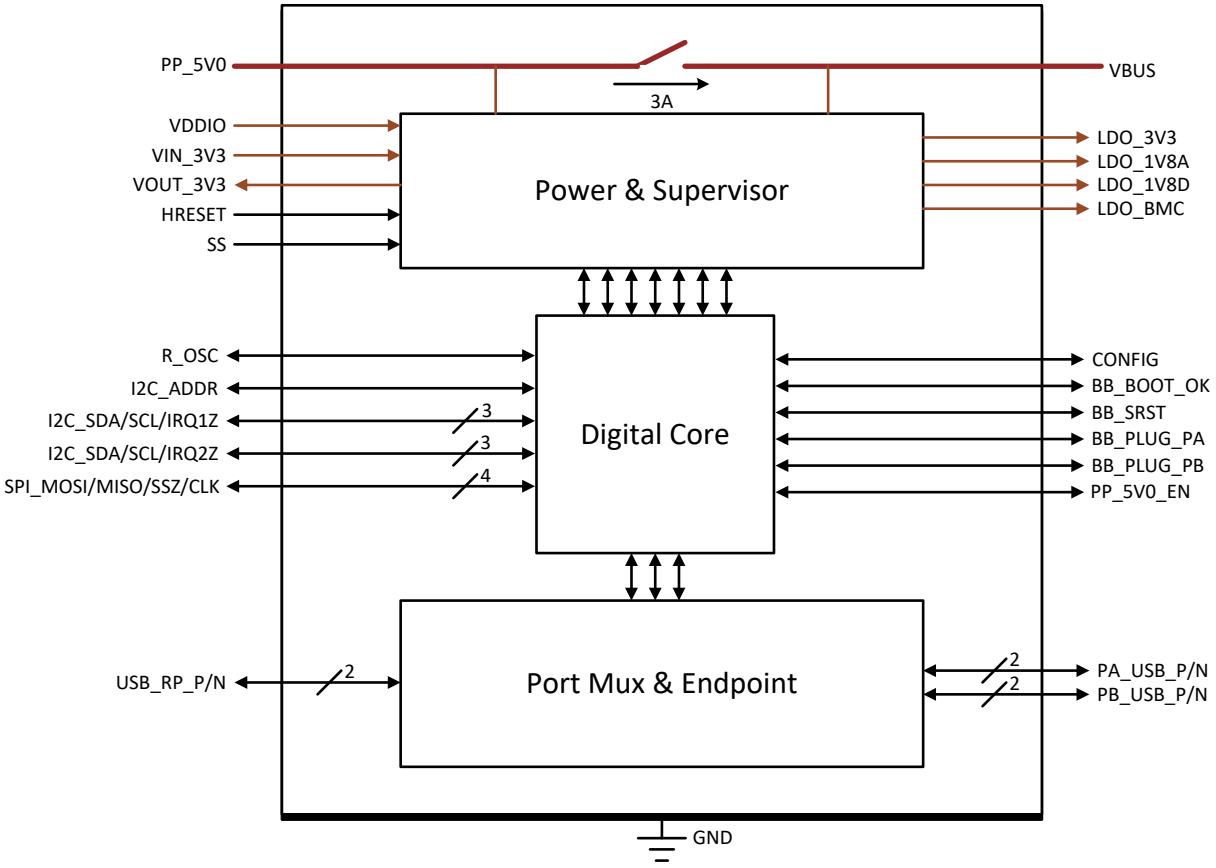
The power-management circuitry receives and provides power to the TPS65982BB internal circuitry and to the VOUT_3V3 and LDO_3V3 outputs. See the *Power Management* section for a high-level block diagram of the power management circuitry, a description of the features, and more detailed circuitry.

The digital core provides the engine for handling control of all other TPS65982BB functionality. A portion of the digital core contains ROM memory which contains all the firmware required to execute USB billboard behavior. In addition, a section of the ROM, called *boot code*, is capable of initializing the TPS65982BB device, loading of device configuration information, and loading any code patches into volatile memory in the digital core. See the *Digital Core* section for a description of the features, and more detailed circuitry.

The TPS65982BB is an I^2C slave to be controlled by a host processor (see the *I^2C Slave Interface* section), and an SPI master to write to and read from an optional external flash memory (see the *SPI Master Interface* section).

The TPS65982BB device also integrates a thermal shutdown mechanism (see the *Thermal Shutdown* section) and runs off of accurate clocks provided by the integrated oscillators (see the *Oscillators* section).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Port-Power Switches

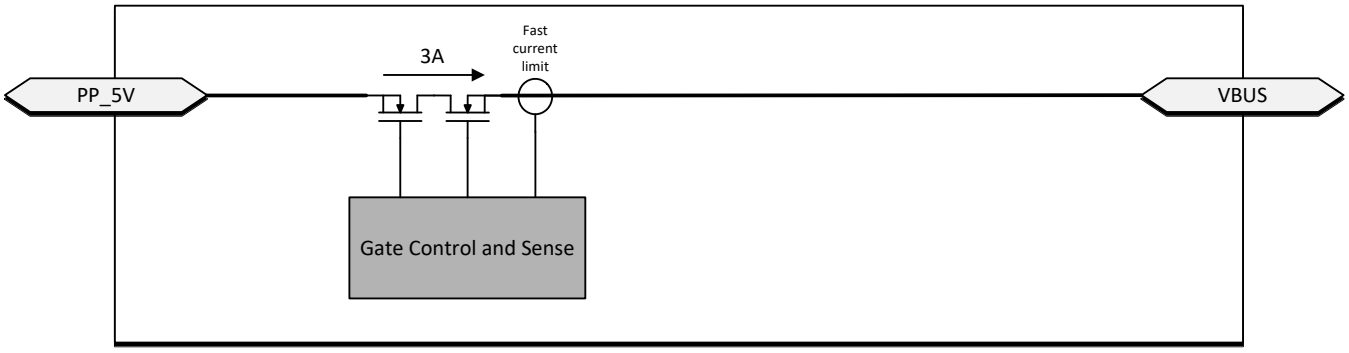


Figure 4. Port-Power Paths

8.3.1.1 5-V Power Delivery

The TPS65982BB device provides a power switch to VBUS from PP_5V0. The switch path provides 5 V at up to 3 A to from PP_5V0 to VBUS. Figure 4 shows a simplified circuit for the switch from PP_5V0 to VBUS.

Feature Description (continued)

8.3.1.2 5-V Power Switch

The PP_5V0 path is unidirectional, only sourcing power from PP_5V0 to VBUS. When the switch is on, the protection circuitry limits reverse current from VBUS to PP_5V0. Figure 5 shows the I-V characteristics of the reverse-current protection feature. Figure 5 and the reverse-current limit can be approximated using Equation 1.

$$IREV5V0 = VREV5V0/RPP5V \quad (1)$$

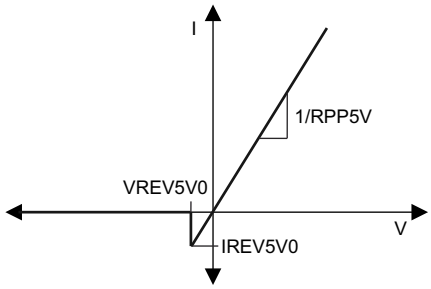


Figure 5. 5V Switch I-V Curve

8.3.1.3 PP_5V0 Current Limit

The current through PP_5V0 to VBUS is limited to ILIMPP5V and is controlled automatically by the digital core. When the current exceeds ILIMPP5V, the current-limit circuit activates. Depending on the severity of the overcurrent condition, the transient response reacts in one of two ways: and Figure 7 show the approximate response time and clamping characteristics of the circuit for a hard short while Figure 8 shows the shows the approximate response time and clamping characteristics for a soft short with a load of 2 Ω.

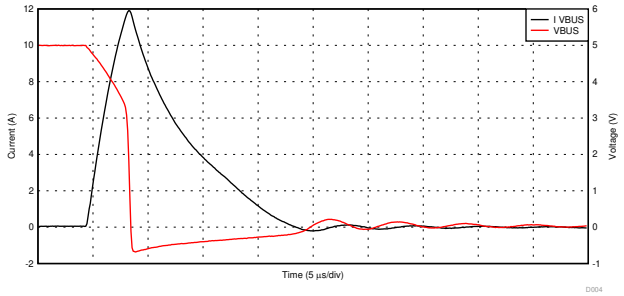


Figure 6. PP_5V0 Current Limit With a Hard Short

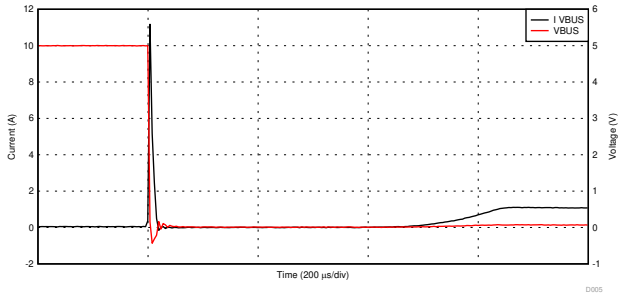


Figure 7. PP_5V0 Current Limit With a Hard Short (Extended Time Base)

Feature Description (continued)

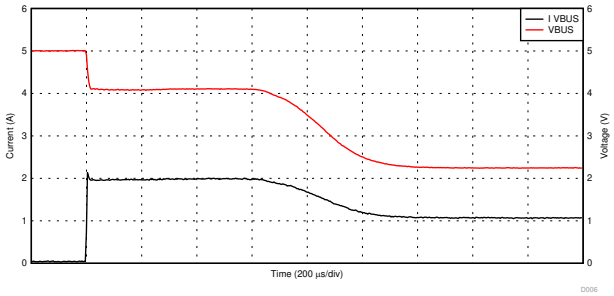


Figure 8. PP_5V0 Current Limit With a Soft Short (2 Ω)

8.3.1.4 VBUS Transition to VSAFE0V

When VBUS transitions to almost 0 V (VSAFE0V), the pulldown circuit in Figure 9 turns on until VBUS reaches VSAFE0V. This transition occurs within the time, TSAFE0V.

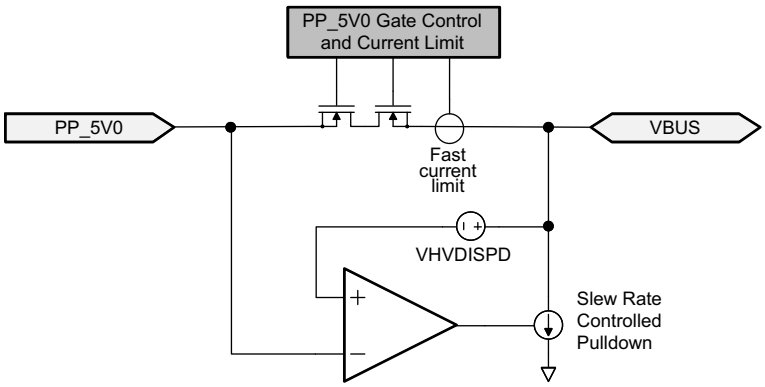


Figure 9. PP_5V0 Slew-Rate Control

8.3.2 USB Port-Data Multiplexer

The includes a USB2 data multiplexor capable of connecting the integrated USB billboard or USB_RP passthrough to the USB2 D+ and D- pins of up to two USB Type-C connectors. The multiplexor connection state is determined by the state of the BB_PLUG_PB and BB_PLUG_PA GPIO inputs. PA_USB_P, PA_USB_N connect to the D+ and D- pins of the "Port A" type-c connector and PB_USB_P, PB_USB_N connect to the D+ and D- pins of the "Port B" type-c connector.

Feature Description (continued)

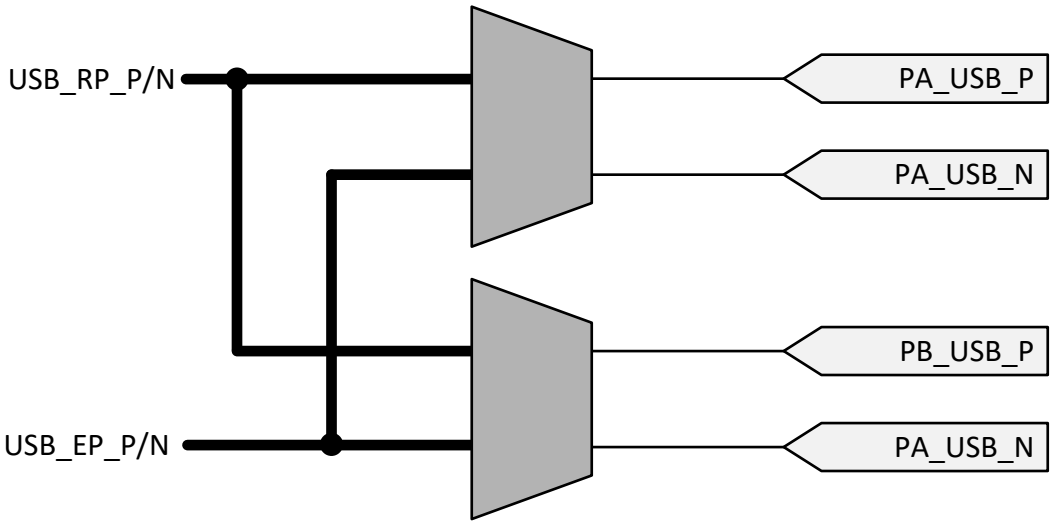


Figure 10. Port-Data Multiplexers

8.3.2.1 Port Multiplexer Clamp

Each input to the multiplexer is clamped to prevent voltages on the port from exceeding the safe operating voltage of circuits attached to the system side of the port data multiplexer. Figure 11 shows the simplified clamping circuit. When a path through the multiplexer is closed, the clamp is connected to the one of the port pins (PA_USB_P/N, PB_USB_P/N). When a path through the multiplexer is not closed, then the port pin is not clamped. As the pin voltage rises above the VCLMP_IND voltage, the clamping circuit activates, and sinks current to ground, preventing the voltage from rising further.

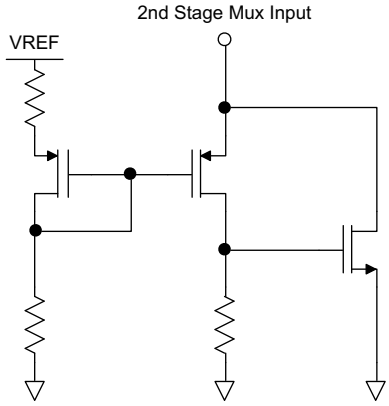


Figure 11. Port Mux Clamp

8.3.2.2 USB2.0 Low-Speed Endpoint

The USB low-speed endpoint is a USB 2.0 low-speed (1.5 Mbps) interface used to support HID class-based accesses. The TPS65982BB device supports control of endpoint EP0. This endpoint enumerates to a USB 2.0 bus to provide USB-Billboard information to a host system as defined in the USB Type-C standard. EP0 is used for advertising the Billboard Class. When a host is connected to a device that provides Alternate Modes that cannot be supported by the host, the Billboard class allows a means for the host to report back to the user without any silent failures.

Figure 12 shows the physical layer of the USB endpoint. The physical layer consists of the analog transceiver, the serial interface engine, and the endpoint FIFOs. The physical layer supports low-speed operation.

Feature Description (continued)

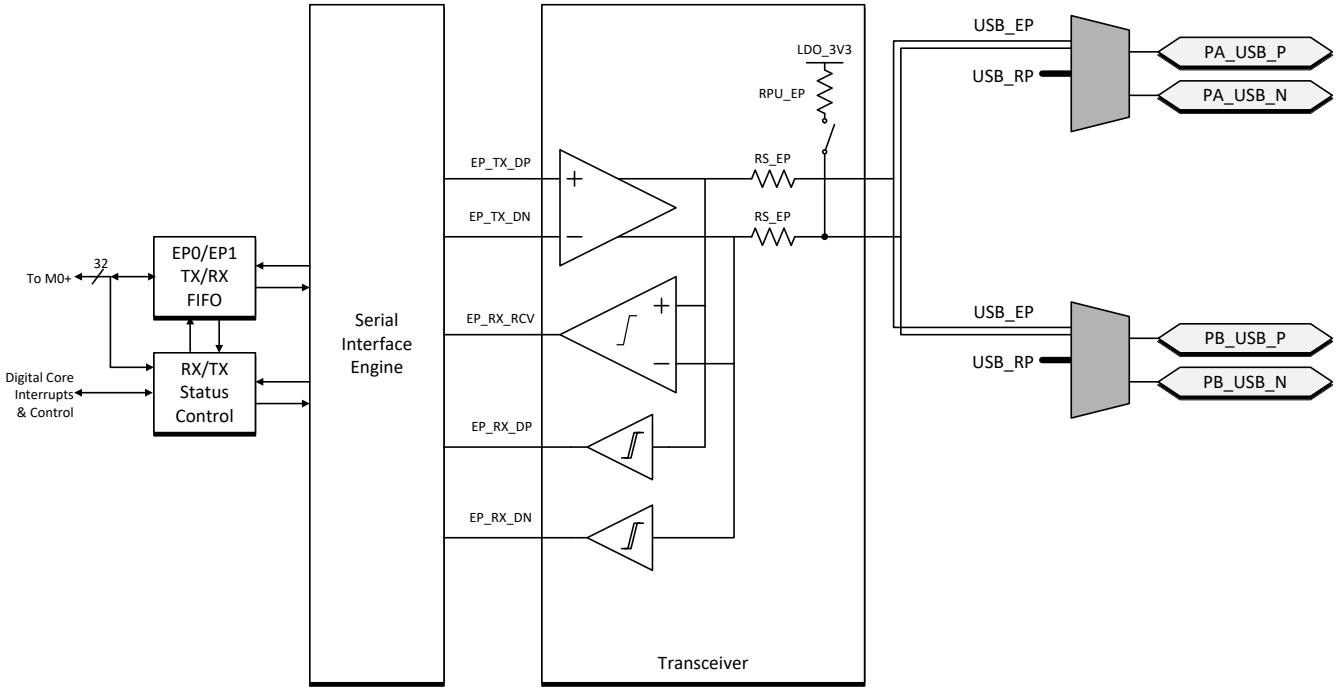


Figure 12. USB Endpoint PHY

The transceiver is made up of a fully-differential output driver, a differential to single-ended receive buffer and two single-ended receive buffers on the D+/D– independently. The output driver drives the D+/D– of the selected output of the port multiplexer. The signals pass through the port-data multiplexer to the port pins. When driving, the signal is driven through a source resistance RS_EP. RS_EP is shown as a single resistor in the USB endpoint PHY but this resistance also includes the resistance of the port-data multiplexer defined in the *Port-Data Multiplexer Characteristics* table. RPU_EP is disconnected during transmit mode of the transceiver.

When the endpoint is in receive mode, the resistance RPU_EP is connected to the D– pin of the A or B port (PA_USB_N or PB_USB_N) depending on the detected orientation of the cable. The RPU_EP resistance advertises low-speed mode only.

8.3.3 Power Management

The TPS65982BB power management block receives power and generates voltages to provide power to the TPS65982BB internal circuitry. These generated power rails are LDO_3V3, LDO_1V8A, and LDO_1V8D. The LDO_3V3 power rail is also a low power output to load an optional external flash memory. The VOUT_3V3 power rail is a low-power output that does not power internal circuitry that is controlled by the application code and can be used to power other ICs in some applications. Figure 13 shows the power-supply path.

Feature Description (continued)

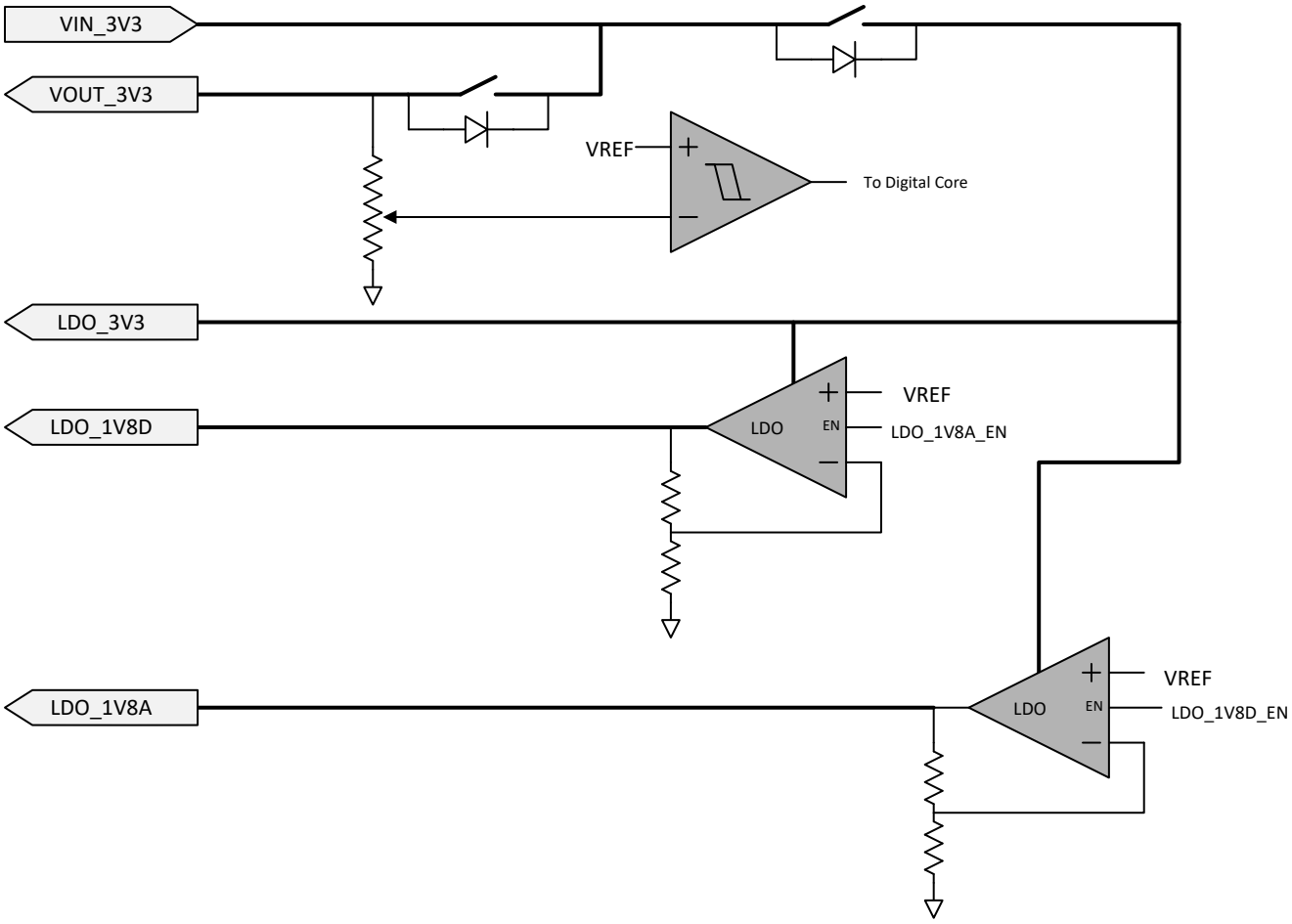


Figure 13. Power Supply Path

The TPS65982BB device is powered from VIN_3V3. Current flows from VIN_3V3 to LDO_3V3 to power the core 3.3-V circuitry and the 3.3-V I/Os. A second LDO steps the voltage down from LDO_3V3 to LDO_1V8D and LDO_1V8A to power the 1.8-V core digital circuitry and 1.8-V analog circuits.

8.3.3.1 Power-On and Supervisory Functions

A power-on-reset (POR) circuit monitors each supply. This POR allows the active circuitry to turn on only when a good supply is present. In addition to the POR and supervisory circuits for the internal supplies, a separate programmable voltage supervisor monitors the VOUT_3V3 voltage.

8.3.4 Digital Core

8.3.5 Power Reset-Control Module (PRCM)

The PRCM implements all clock management, reset control, and sleep-mode control.

8.3.6 Interrupt Monitor

The interrupt control module handles all interrupt from the external GPIO as well as interrupts from internal analog circuits.

Feature Description (continued)

8.3.7 I²C Slave

Two I²C interfaces provide interface to the digital core from the system. These interfaces operate as a slave and support low-speed and full-speed signaling. See the *I²C Slave Interface* section for more information.

8.3.8 SPI Master

The SPI master provides a serial interface to an optional, external flash memory. The optional flash memory can be used to store code patches and or device configurations. The recommended memory is the W25X05CL (64 KB) serial-flash memory. A memory of at least (24 KB) is required for the TPS65982BB device (shared or unshared) if device configuration and patch memory features are used. See the *SPI Master Interface* section for more information.

8.3.9 Thermal Shutdown

The TPS65982BB device has both a central thermal shutdown to the chip and a local thermal shutdown for the power-path block. The central thermal shutdown monitors the temperature of the center of the die and disables all functions except for supervisory circuitry. This shutdown also halts digital core when die temperature goes above a rising temperature of TSD_MAIN. The temperature shutdown has a hysteresis of TSDH_MAIN and when the temperature falls back below this value, the device resumes normal operation. The power-path block has a local thermal-shutdown circuit to detect an overtemperature condition because of overcurrent, and quickly turns off the power switches. The power-path thermal shutdown values are TSD_PWR and TSDH_PWR. The output of the thermal shutdown circuit is deglitched by TSD_DG before triggering. The thermal shutdown circuits generate interrupt events to the digital core.

8.3.10 Oscillators

The TPS65982BB device has two independent oscillators for generating internal clock domains. A 48-MHz oscillator generates clocks for the core during normal operation and clocks for the USB 2.0 endpoint physical layer. An external resistance is placed on the R_OSC pin to set the oscillator accuracy. A 100-kHz oscillator generates clocks for various timers and clocking the core during low-power states.

8.4 Device Functional Modes

8.4.1 SPI Master Interface

The TPS65982BB device loads any ROM patch, configuration or both from flash memory during the sequence. The SPI master electrical characteristics are defined in *SPI Master Switching Characteristics* and timing characteristics are defined in Figure 3. The TPS65982BB device is designed to power the flash from LDO_3V3, and therefore pullup resistors used for the flash memory must be tied to LDO_3V3. The flash memory IC must support a 12-MHz SPI clock frequency. The size of the flash must be at least 24 KB to hold the maximum ROM patch and configuration code outlined in the section. The SPI master of the TPS65982BB device supports SPI Mode 0. For Mode 0, data delay is defined such that data is output on the same cycle as the chip select (SPI_SSZ pin) becomes active. The chip select polarity is active-low. The clock phase is defined such that data (on the SPI_MISO and SPI_MOSI pins) is shifted out on the falling edge of the clock (SPI_CLK pin) and data is sampled on the rising edge of the clock. The clock polarity for chip select is defined such that when data is not being transferred the SPI_CLK pin is held (or idling) low. The minimum erasable sector size of the flash must be 4 KB. The W25X05CL device or similar is recommended.

8.4.2 I^2C Slave Interface

The TPS65982BB device has two I^2C interface ports. I^2C port 1 is comprised of the I2C_SDA1, I2C_SCL1, and I2C_IRQ1Z pins. I^2C port 2 is comprised of the I2C_SDA2, I2C_SCL2, and I2C_IRQ2Z pins. These interfaces provide general-status information about the TPS65982BB device and about the ability to control the TPS65982BB behavior.

8.4.2.1 I^2C Interface Description

The TPS65982BB device supports standard and fast mode I^2C interface. The bidirectional I^2C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a supply through a pullup resistor. The data transfer can only be initiated when the bus is not busy.

A master sending a start condition (a high-to-low transition on the SDA I/O) while the SCL input is high initiates I^2C communication. After the Start Condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA I/O during the high of the ACK-related clock pulse. On the I^2C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period as changes in the data line at this time are interpreted as control conditions (START or STOP). The master sends a Stop Condition, a low-to-high transition on the SDA I/O while the SCL input is high.

Any number of data bytes can be transferred from the transmitter to receiver between the start and the stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges, must pull down the SDA line during the ACK clock pulse, so that the SDA line remains low during the high pulse of the ACK-related clock period. When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. The master receiver holding the SDA line high does this. In this event, the transmitter must release the data line to enable the master to generate a stop condition.

Figure 14 shows the start and stop conditions of the transfer. Figure 15 shows the SDA and SCL signals for transferring a bit. Figure 16 shows a data transfer sequence with the ACK or NACK at the last clock pulse.

Device Functional Modes (continued)

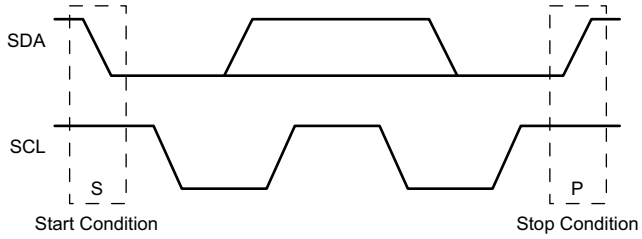


Figure 14. I²C Definition of Start and Stop Conditions

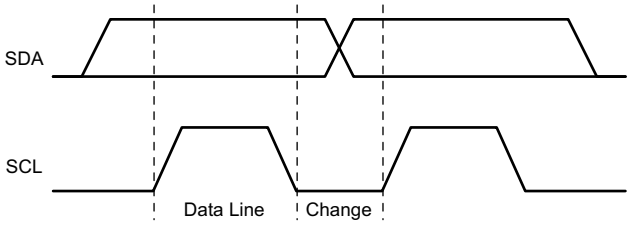


Figure 15. I²C Bit Transfer

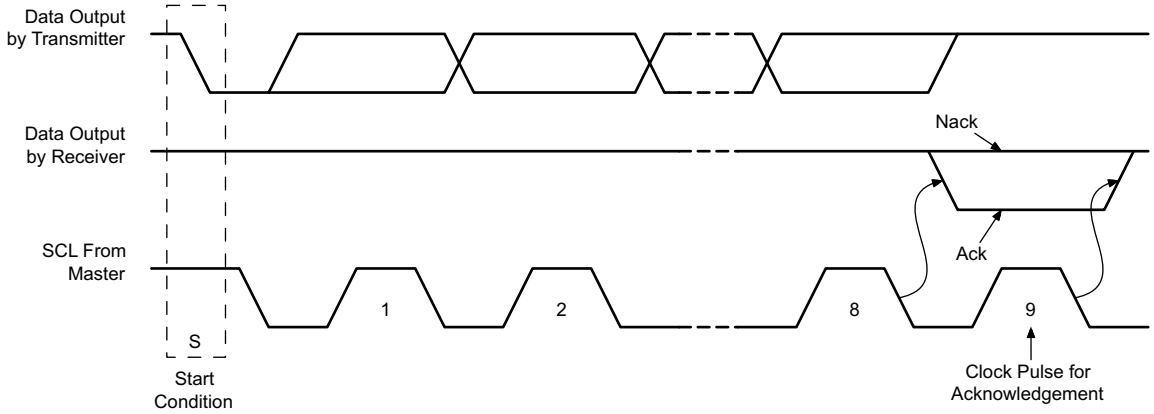


Figure 16. I²C Acknowledgment

8.4.2.2 I²C Clock Stretching

The TPS65982BB device features clock stretching for the I²C protocol. The TPS65982BB slave I²C port can hold the clock line (SCL) low after receiving (or sending) a byte, indicating that the slave is not yet ready to process more data. The master communicating with the slave must not finish the transmission of the current bit and must wait until the clock line actually goes high. When the slave is clock stretching, the clock line remains low.

The master must wait until it observes the clock line transitioning high plus an additional minimum time (4 μs for standard 100 kbps I²C) before pulling the clock low again.

Any clock pulse can be stretched but typically it is the interval before or after the acknowledgment bit.

8.4.2.3 I²C Address Setting

The boot code sets the hardware configurable unique I²C address of the TPS65982BB device before the port is enabled to respond to I²C transactions. For the I2C1 interface, the unique I²C address is determined by the analog level set by the analog I2C_ADDR strap pin (three bits) as listed in Table 1.

Device Functional Modes (continued)

Table 1. I²C Default Unique Address I2C1 (1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	1	I2C_ADDR_DECODE[2:0]			R/W

(1) Any bit is maskable for each port independently providing firmware override of the I²C address.

For the I2C2 interface, the unique I²C address is determined by the analog level set by the analog I2C_ADDR strap pin (three bits) as listed in Table 2.

Table 2. I²C Default Unique Address I2C2 (1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	I2C_ADDR_DECODE[2:0]			R/W

(1) ny bit is maskable for each port independently, providing firmware override of the I²C address.

8.4.2.4 Unique-Address Interface

The unique-address interface allows for complex interaction between an I²C master and a single TPS65982BB device. The I²C slave sub-address is used to receive or respond to the protocol commands of the host interface. Figure 17 and Figure 18 show the write and read protocol for the I²C slave interface. Figure 19 provides a key to explain the terminology used. The key to the protocol diagrams is in the SMBus specification and is repeated here in part.

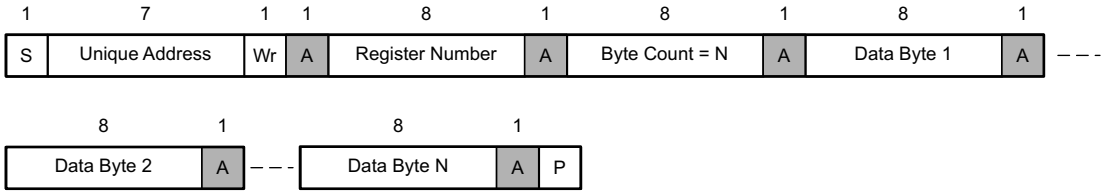


Figure 17. I²C Unique Address-Write Register Protocol

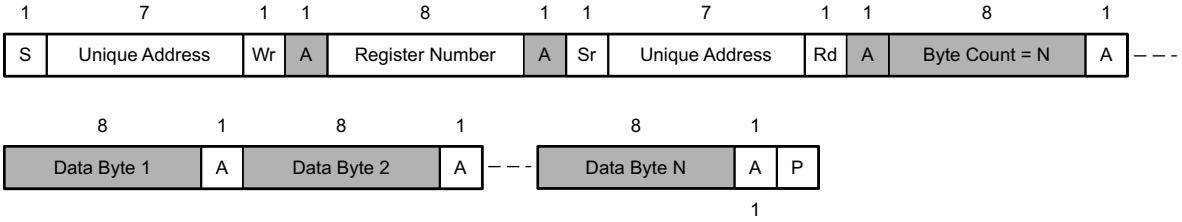


Figure 18. I²C Unique Address-Read Register Protocol

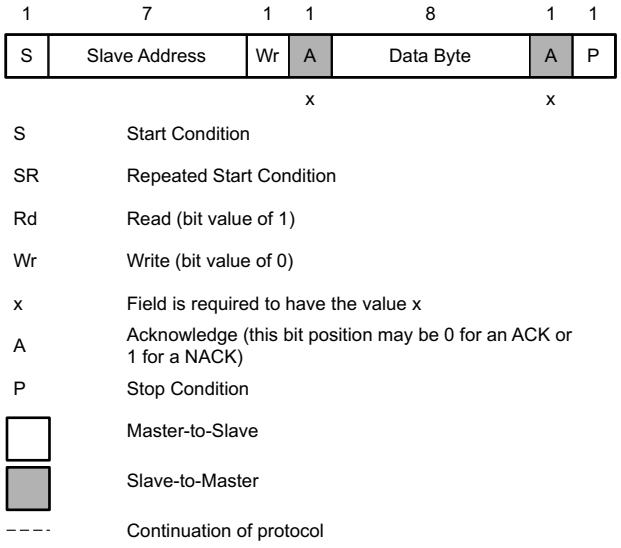


Figure 19. I²C Read/Write Protocol Key

8.4.2.5 I²C Pin Address Setting

To enable the setting of multiple I²C addresses using a single TPS65982BB pin, a resistance is placed externally on the I2C_ADDR pin. The internal ADC then decodes the address from this resistance value. Figure 20 shows the decoding.

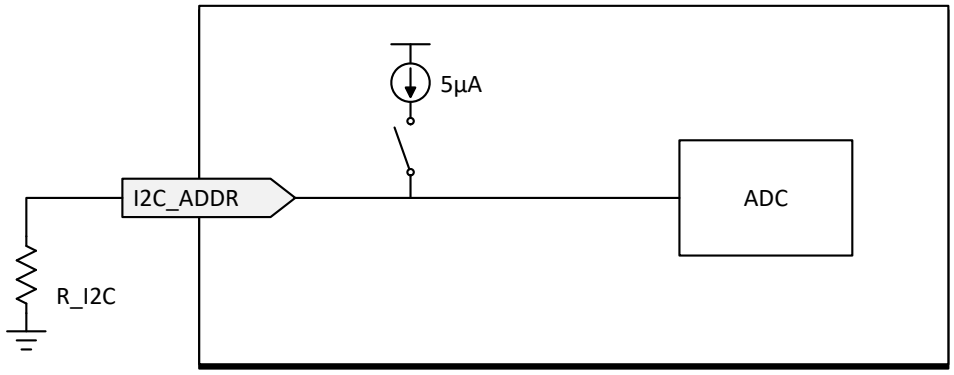


Figure 20. I²C Address Decode

Table 3 lists the external resistance required to set bits [3:1] of the I²C unique address.

Table 3. I²C Address Resistance

TPS65982BB DEVICE	EXTERNAL RESISTANCE (1%)	I²C UNIQUE ADDRESS [3:1]
Device 0	0	0x00
Device 7	38.3k	0x01
Device 6	84.5k	0x02
Device 5	140k	0x03
Device 4	205k	0x04
Device 3	280k	0x05
Device 2	374k	0x06
Device 1	Open	0x07

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS65982BB is controlled through I^2C and GPIO to perform the billboard function for two USB Type-C ports. The external flash is connected through SPI to the TPS65982BB and contains the firmware to execute the billboard function. Alternatively, an embedded controller (EC) or PD controller is capable of loading the firmware to the TPS65982BB through I^2C. Generally the PD controller is used to control the TPS65982BB through GPIO and I^2C as the PD controller is managing the USB Type-C ports.

9.2 Typical Application

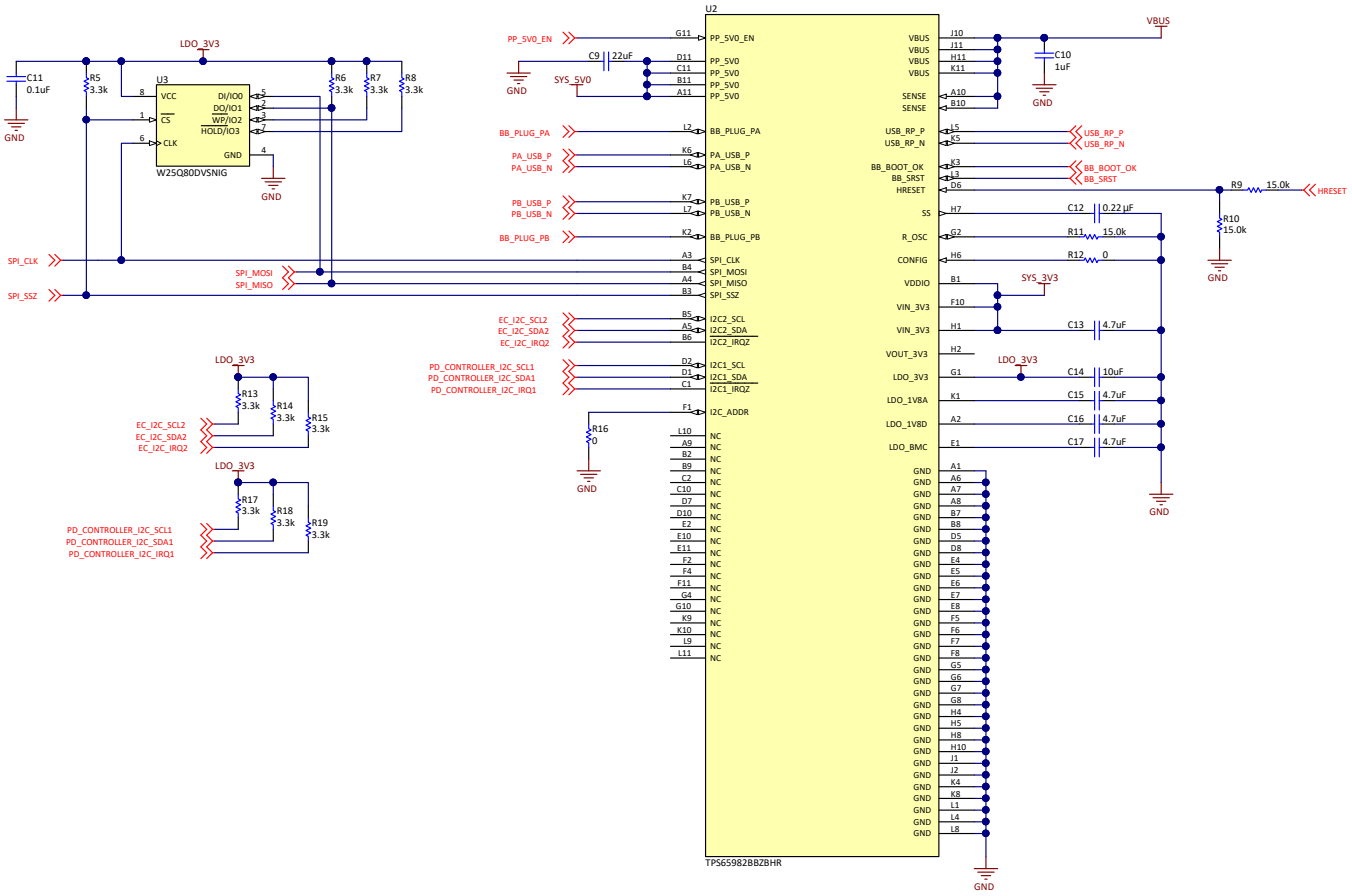


Figure 21. Example Schematic

9.2.1 VBUS Load Switch

The load switch is capable of providing up to 3A for multiple USB Type-A receptacles. The 22uF capacitance on PP_5V0 is for the local PP_5V0 pins. There should be additional capacitance on the SYS_5V0 that should be able to support load transients for the number of ports used in the system. The VBUS side capacitance should be less than PP_5V0 to optimize the over current protection.

Typical Application (continued)

9.2.2 HRESET

HRESET is the hardware reset on the TPS65982BB and it is a 1.8V (Max) pin. Most PD Controllers and ECs will drive to 3.3V and will require a resistor divider to drive the HRESET pin.

9.2.3 Dual Port Billboard Support

The TPS65982BB will route the USB2 paths from two USB Type-C ports and provide VBUS with over current protection to a USB Type-A receptacle or a USB Hub. The TPS65982BB implements a “first come – first serve” with the two USB2 paths, where the USB2 connection to the USB Type-A or USB Hub is connected to the USB Type-C port that was connected first. The device will maintain that connection until all connections are removed. When the PD controller fails to enter an alternate mode, the PD controller will communicate to the TPS65982BB through I^2C to enable the billboard function. Upon receiving the I^2C command, the TPS65982BB will connect its USB endpoint to the connected Type-C port and will be able to send the proper billboard message. The block diagram below shows the system application for billboard support for two Type-C ports.

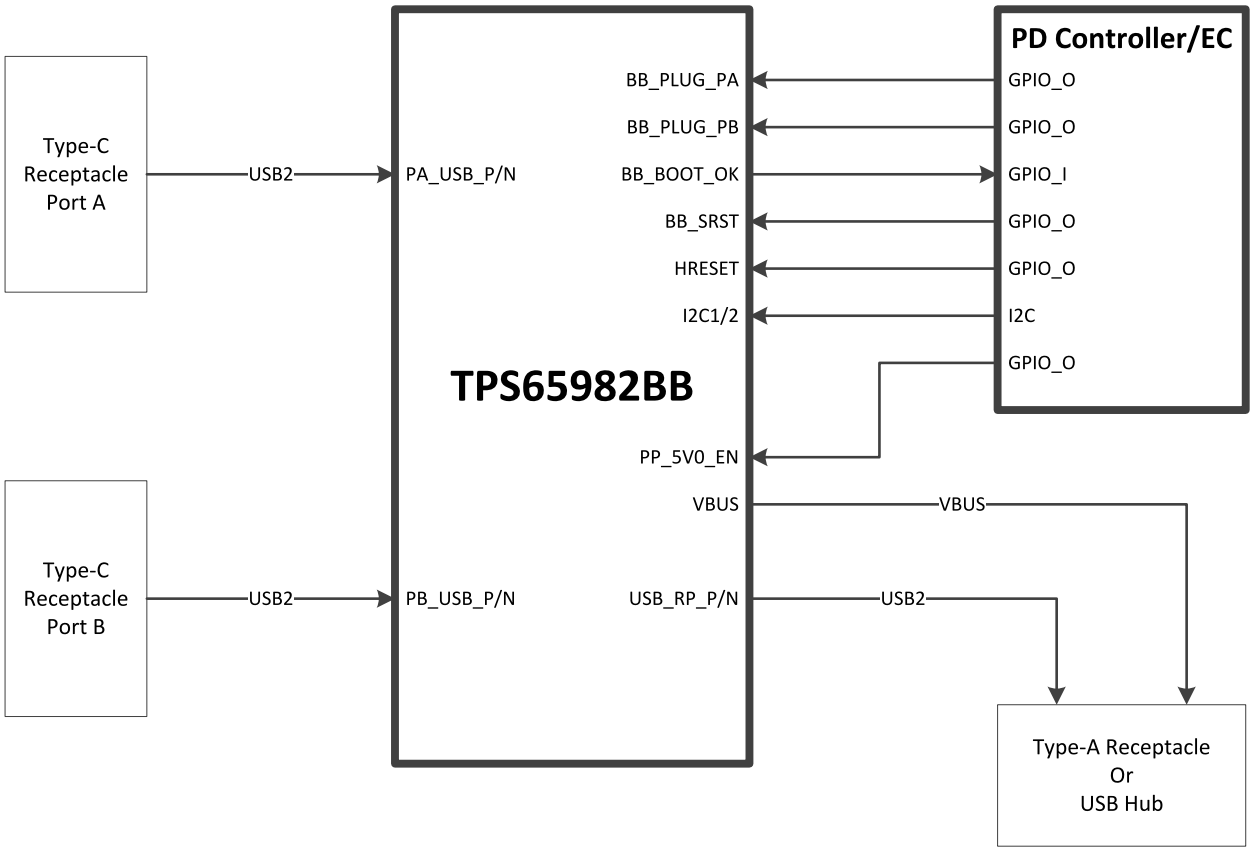


Figure 22. Application Block Diagram

10 Power Supply Recommendations

10.1 3.3-V Power

10.1.1 1VIN_3V3 Input Switch

The VIN_3V3 input is the main supply to the TPS65982BB device. The VIN_3V3 switch (S1 in Figure 13) is a unidirectional switch from VIN_3V3 to LDO_3V3, not allowing current to flow backwards from LDO_3V3 to VIN_3V3. This switch is on when 3.3 V is available. See Table 4 for the recommended external capacitance on the VIN_3V3 pin.

10.1.2 VOUT_3V3 Output Switch

The VOUT_3V3 output switch (S2 in Figure 13) enables a low-current auxiliary supply to an external element. This switch is controlled by and is off by default. See Table 4 for the recommended external capacitance on the VOUT_3V3 pin.

10.2 1.8-V Core Power

The internal circuitry is powered from 1.8 V. Two LDOs step the voltage down from LDO_3V3 to 1.8 V. One LDO powers the internal digital circuits. The other LDO powers the internal low-voltage analog circuits.

10.2.1 1.8-V Digital LDO

The 1.8-V digital LDO provides power to all internal low-voltage digital circuits which includes the digital core, memory, and other digital circuits. See Table 4 for the recommended external capacitance on the LDO_1V8D pin.

10.2.2 1.8-V Analog LDO

The 1.8-V analog LDO provides power to all internal low-voltage analog circuits. See Table 4 for the recommended external capacitance on the LDO_1V8A pin.

10.3 VDDIO

The VDDIO pin provides a secondary input allowing some I/Os to be powered by a source other than LDO_3V3. The default state is power from LDO_3V3. The memory stored in the flash configures the I/Os to use LDO_3V3 or VDDIO as a source. The application code automatically scales the input and output voltage thresholds of the I/O buffer accordingly. See the section for more information on the I/O buffer circuitry. See Table 4 for the recommended external capacitance on the VDDIO pin.

10.3.1 Recommended Supply Load Capacitance

Table 4 lists the recommended board capacitances for the various supplies. The typical capacitance is the nominally rated capacitance that must be placed on the board as close to the pin as possible. The maximum capacitance must not be exceeded on pins for which it is specified. The minimum capacitance is minimum capacitance allowing for tolerances and voltage derating ensuring proper operation.

Table 4. Recommended Supply Load Capacitance

PARAMETER	DESCRIPTION	VOLTAGE RATING	CAPACITANCE		
			MIN (ABS MIN)	TYP (TYP PLACED)	MAX (ABS MAX)
CVIN_3V3	Capacitance on VIN_3V3	6.3 V	5 µF	10 µF	
CLDO_3V3	Capacitance on LDO_3V3	6.3 V	5 µF	10 µF	25 µF
CVOUT_3V3	Capacitance on VOUT_3V3	6.3 V	0.1 µF	1 µF	2.5 µF
CLDO_1V8D	Capacitance on LDO_1V8D	4 V	500 nF	2.2 µF	12 µF
CLDO_1V8A	Capacitance on LDO_1V8A	4 V	500 nF	2.2 µF	12 µF
CLDO_BMC	Capacitance on LDO_BMC	4 V	1 µF	2.2 µF	4 µF
CVDDIO	Capacitance on VDDIO. When shorted to LDO_3V3, the CLDO_3V3 capacitance may be shared.	6.3 V	0.1 µF	1 µF	
CVBUS	Capacitance on VBUS	25 V	0.5 µF	1 µF	12 µF
CPP_5V0	Capacitance on PP_5V0	10 V	2.5 µF	4.7 µF	
CSS	Capacitance on soft start pin	6.3 V		220 nF	

11 Layout

11.1 Layout Guidelines

Proper placement and routing will maintain signal integrity for the high speed signals and power integrity for the VBUS power switch. The following guidelines show the recommended methodology to properly route all required signals. Board manufacturing capabilities must be taken into account with any layout to guarantee manufacturability.

11.2 Layout Example

The layout example is based on the schematic below. Other system components are not shown as they have their own layout recommendations.

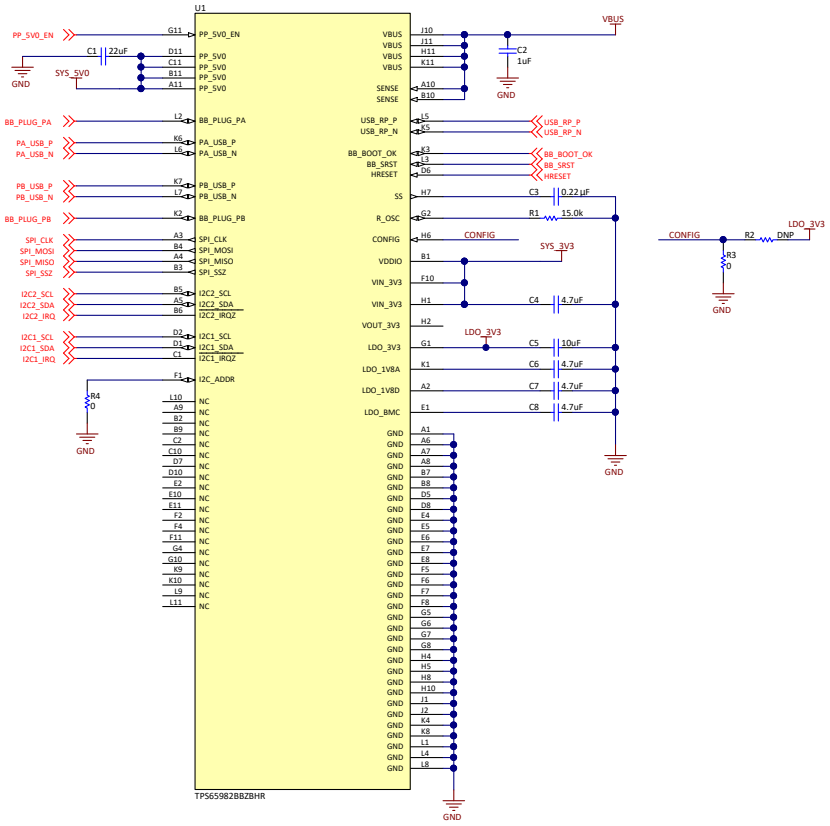


Figure 23. Layout Example Schematic

11.2.1 Component Placement

The recommended placement is to have the TPS65982BB on the Top Layer and have all of the passive components on the opposite layer of the PCB. This will significantly reduce solution size and allows for more clearance for the high speed and interface signals. The figures below show the top and bottom placement.

Layout Example (continued)

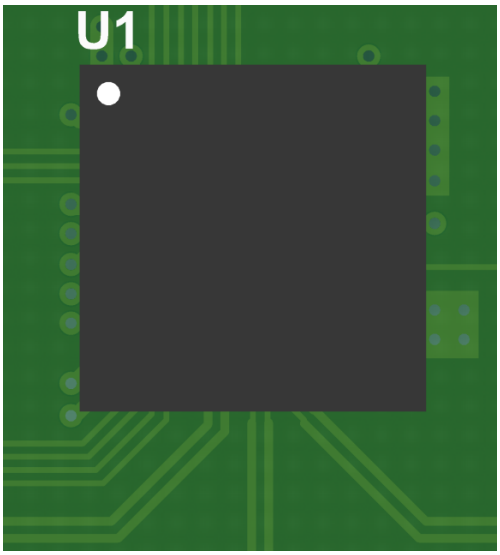


Figure 24. Top Placement

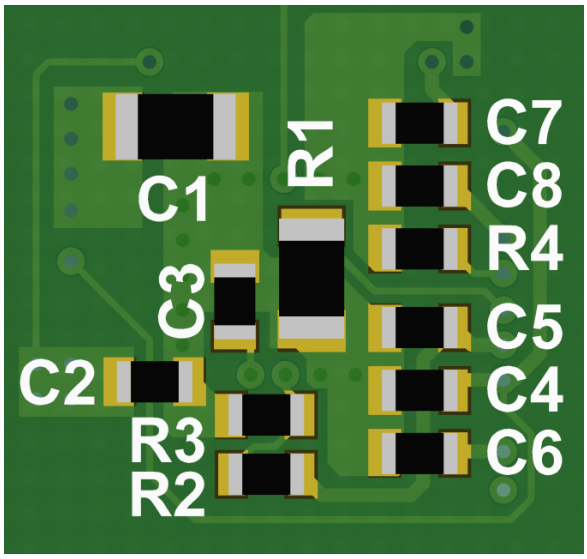


Figure 25. Bottom Placement

11.2.2 Recommended Via Size and Trace Widths

For all LDO voltages, GPIO, Interface (I^2C/SPI) and VIN_3V3 a single via connection to the pads on the TPS65982BB is sufficient. For PP_5V0 and VBUS it is recommended to use 4 vias to reduce inductance through the VBUS switch and to have low resistive connection to the bulk cap on the opposite layer. The recommended via is a 16mil diameter / 8mil hole that is filled (epoxy fill or Cu fill) and tented on both sides of the PCB. The tenting will help reduce solder from wicking and lifting the BGA package. The figure below shows the recommended via size.

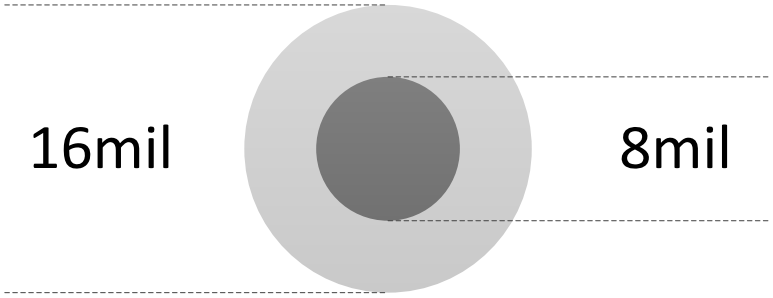


Figure 26. Recommended Via Size

The table below shows the minimum trace widths. It is recommended to take into account any losses that may be present such as resistance from system supplies to input supply pins (VIN_3V3).

Table 5. Minimum Trace Widths

Signal	Minimum Width (mil)
VIN_3V3 (H1, B1)	6
LDO_3V3, LDO_1V8A, LDO_1V8D, LDO_BMC	6
GPIO, VIN_3V3 (F10)	4
Component GND	8

11.2.3 USB2 Routing

It is important to reduce the number of vias use when routing USB2 signals from the two Type-C receptacles and to the USB Type-A receptacle or USB hub. Routing on the top and bottom layers only will reduce the amount of antenna created when using a through hole via to connect an outer layer to an inner layer. When fanning out the BGA it is recommended to use 4mil traces to get enough clearance to route the width and gap requirements for impedance matching. Follow the USB2 specification and USB Hub requirements for complete routing rules.

11.2.4 Oval Pad for BGA Fanout

The footprint below uses an oval footprint for the outer pads of the BGA. This allows for routing the inner pads through the outer pads. The figure below shows the pad size for the out oval pads.

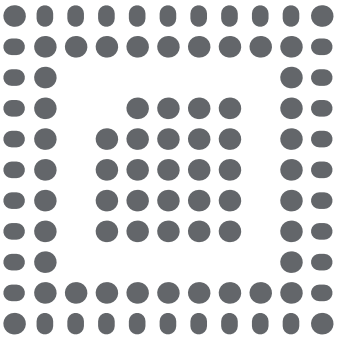


Figure 27. Example Footprint

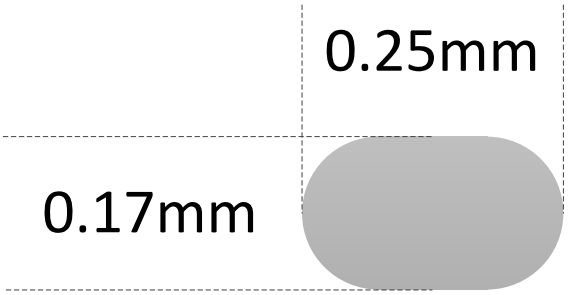


Figure 28. Oval Pad Sizing

11.2.5 Top and Bottom Layer Complete Routing

The figures below incorporate the guidelines to route all of the required TPS65982BB signals on the top and bottom layer only. For GND and the VBUS switch (PP_5V0 & VBUS) they are connected all with planes/pours. Follow the amount of vias used and placement to ensure proper grounding and heat dissipation. All vias must be connected to a GND plane.

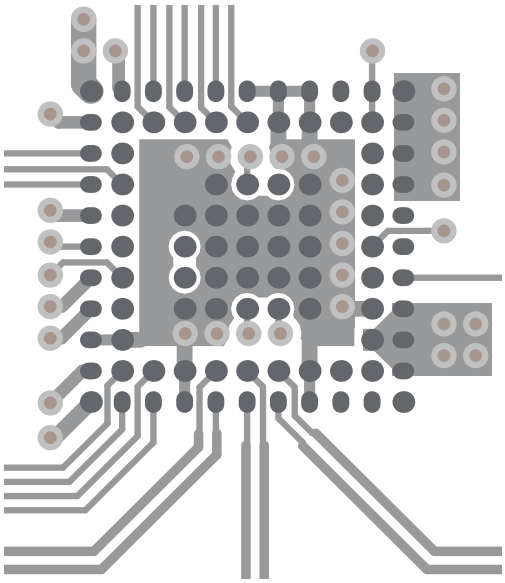


Figure 29. Top Layer Routing

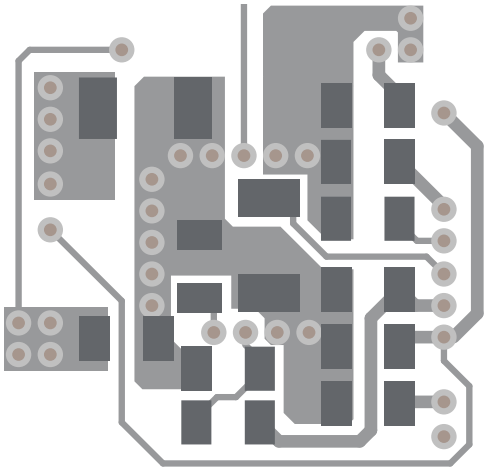


Figure 30. Bottom Layer Routing

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- NSR20F30NXT5G data sheet, *Schottky Barrier Diode*, http://www.onsemi.com/PowerSolutions/product.do?id=NSR20F30NX
- USB Power Delivery Specification Revision 3.0, V2.0 (August 2019)
- USB Type-C Specification Release 2.0 (August 2019)
- Billboard Device Class Spec Revision 1.21 (September 2016)
- USB Battery Charging Specification Revision 1.2 (December 7th, 2010)
- W25X05CL data sheet, *2.5 / 3 / 3.3 V 512K-Bit Serial Flash Memory With 4KB Sectors and Dual I/O SPI*, www.winbond.com/hq/product/code-storage-flash-memory/serial-nor-flash/?__locale=en&partNo=W25X05CL

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS65982BBZBHR	NRND	Production	NFBGA (ZBH) | 96	2500 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-10 to 85	TPS65982BB BH
TPS65982BBZBHR.A	NRND	Production	NFBGA (ZBH) | 96	2500 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-10 to 85	TPS65982BB BH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

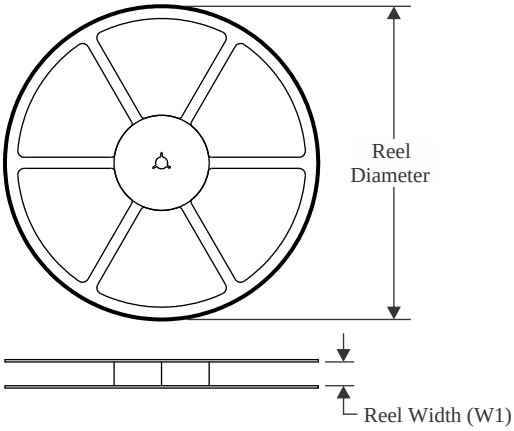
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

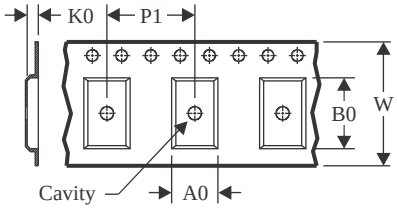
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

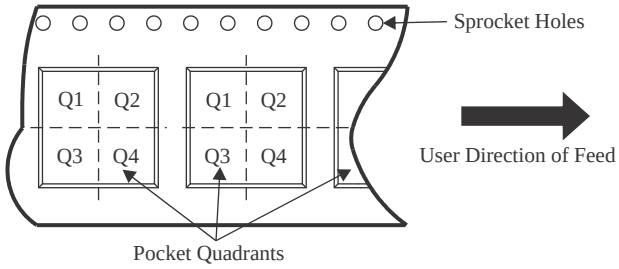


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

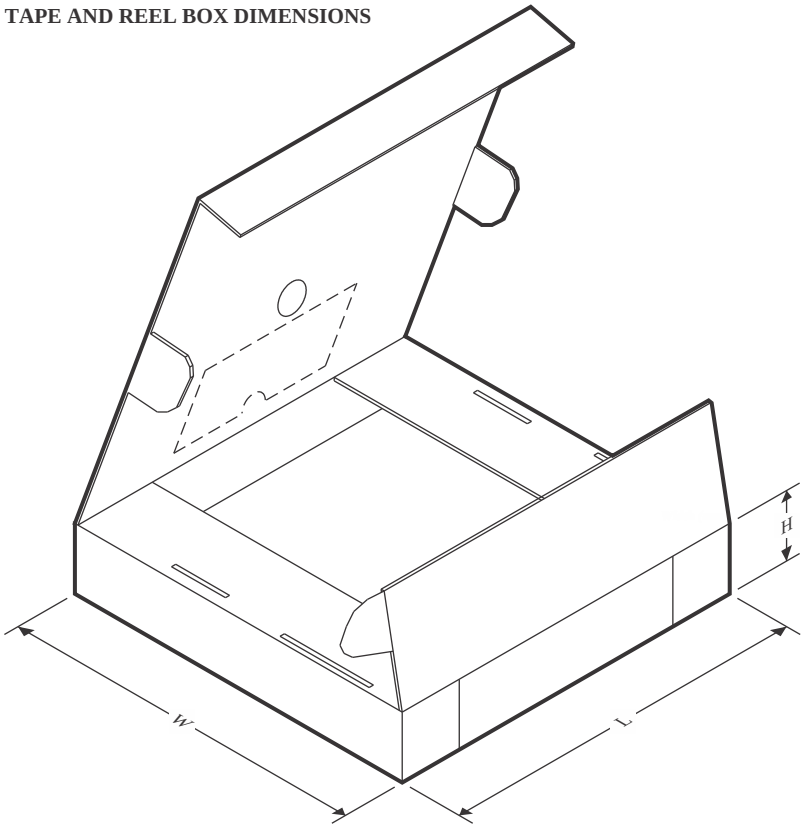
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65982BBZBHR	NFBGA	ZBH	96	2500	330.0	16.4	6.3	6.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

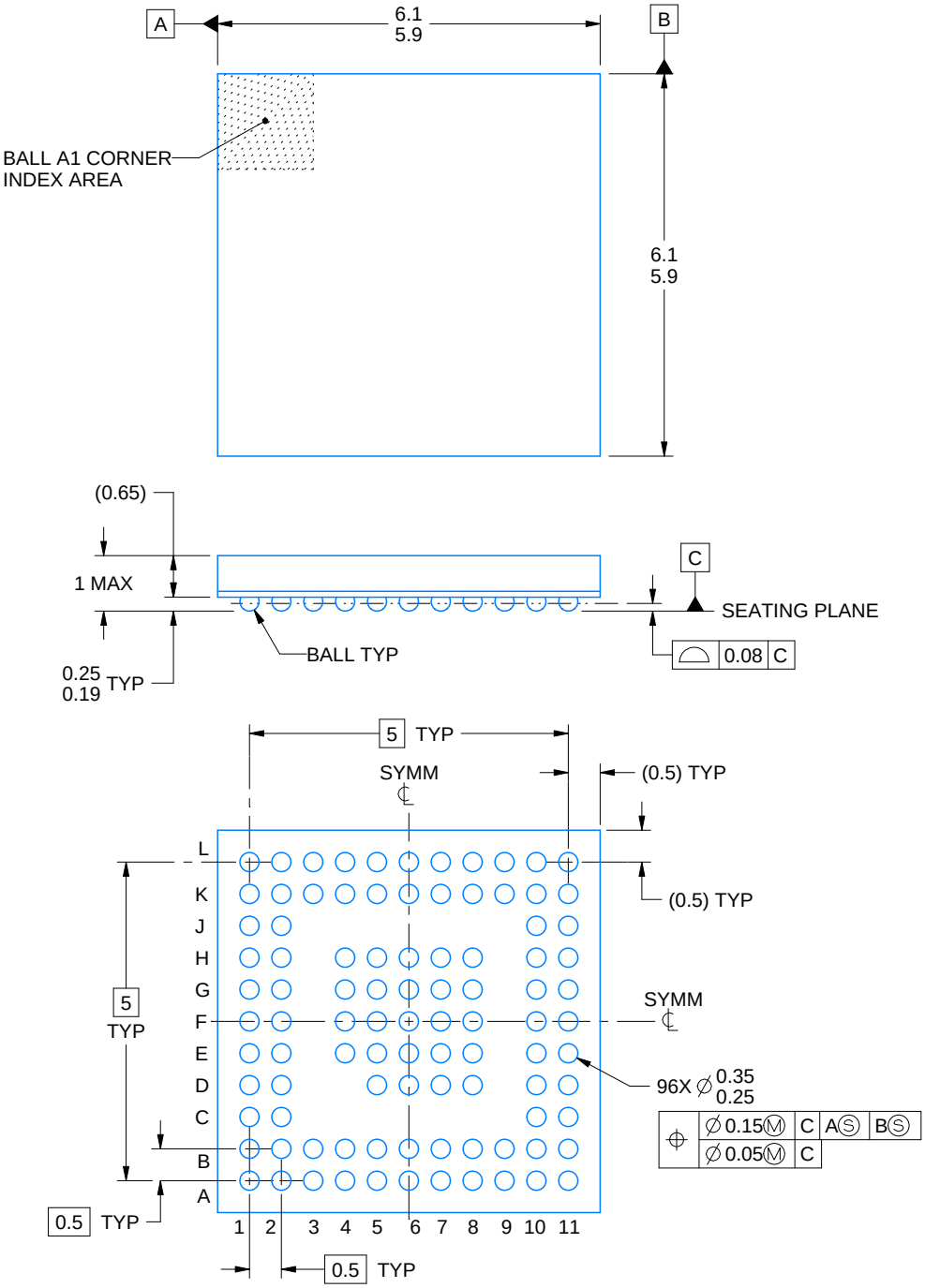
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65982BBZBHR	NFBGA	ZBH	96	2500	336.6	336.6	31.8

PACKAGE OUTLINE

ZBH0096A

NFBGA - 1 mm max height

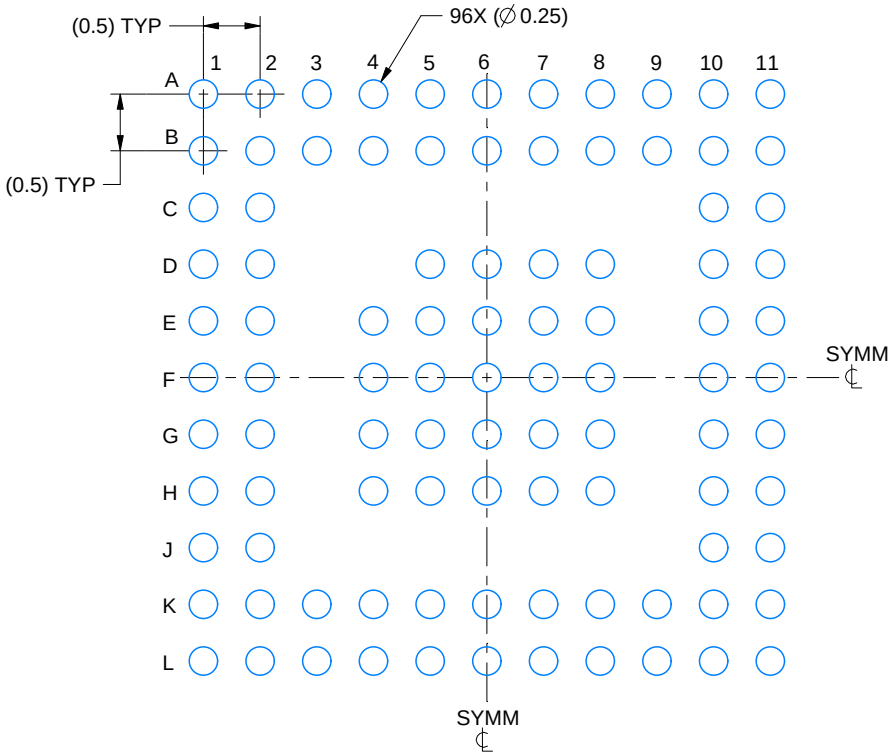
PLASTIC BALL GRID ARRAY



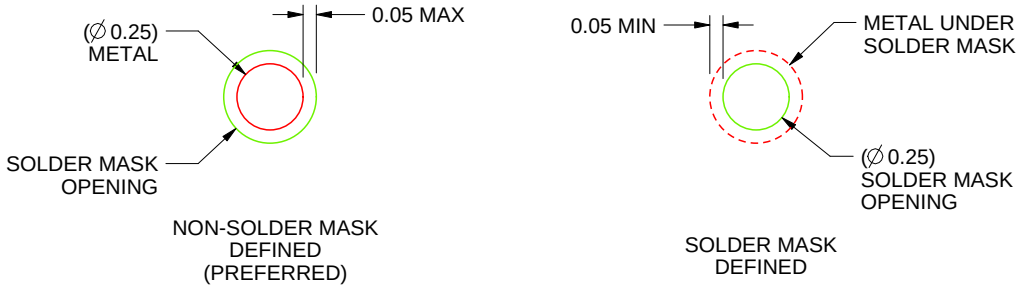
4221754/B 09/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:15X

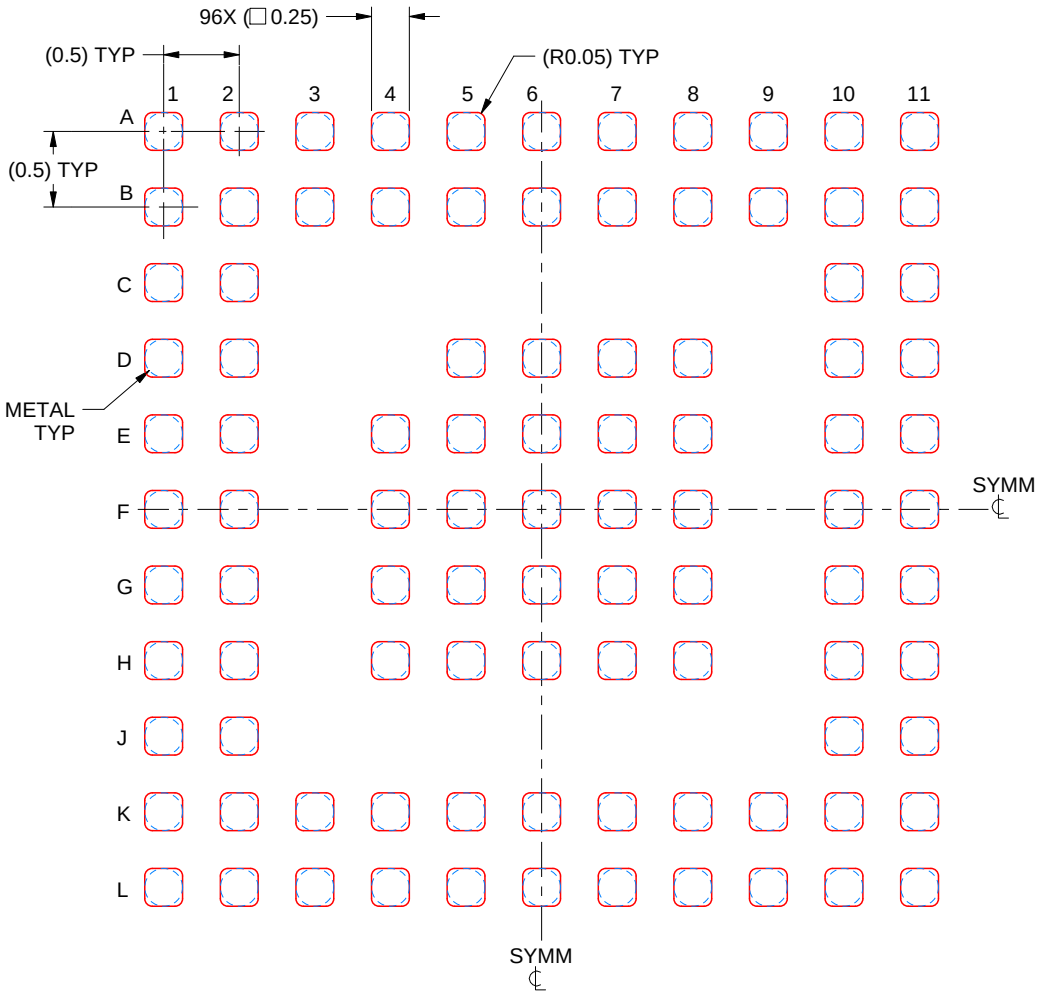


SOLDER MASK DETAILS
NOT TO SCALE

4221754/B 09/2018

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:20X

4221754/B 09/2018

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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Last updated 10/2025