# TPSM82843x 1.8V to 5.5V, 600mA, Ultra-Low 275nA $I_Q$, High Efficiency, Step-Down Converter With Integrated Inductor in a QFN Package

## 1 Features

- 1.8V to 5.5V input voltage range
- 0.4V to 3.6V output voltage range
- 275nA typical quiescent current, 4nA shutdown
- Zero feedback error from integrated output divider
- 1.2V logic compliant EN (Enable) pin
- 600mA output current and output discharge
- 1% accurate voltage selection with single resistor on VSET-pin
  - TPSM828436: 0.4V to 0.8V
  - TPSM828437: 0.8V to 1.8V
  - TPSM828438: 1.8V to 3.6V
- Cost and size optimized passive components
  - Down to 4.7µF $C_{IN}$ and $C_{OUT}$
  - 0402 and 0201 capacitors supported
- Low output voltage ripple in power save mode
- RF-friendly and fast transient DCS-Control
- Automatic transition to no ripple 100% mode
- Small QFN package with 2.45mm × 2.70mm × 1.29mm

## 2 Applications

- Bluetooth® low energy BLE (BTLE) remote controls, wireless sensors, beacons
- IoT Wi-Fi® battery driven nodes
- Smart meter, heat meter, telemetry
- Datalogger, predictive maintenance
- Programmable logic controller (PLC) point of load
- Wearable electronics
- Headsets, headphones, and earbuds
- Hearing aid
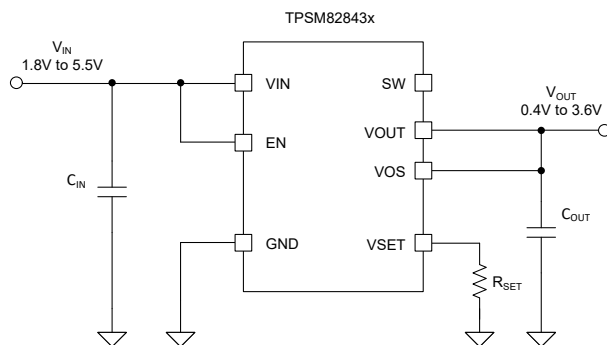
## 3 Description

The high efficiency TPSM82843x step-down converter family supports an ultra-low $I_Q$ (typical operating quiescent current) of 275nA and a typical shutdown current of only 4nA. The inductor is integrated into the QFN package improving ease of use and reducing the bill of material down to only three passive components.
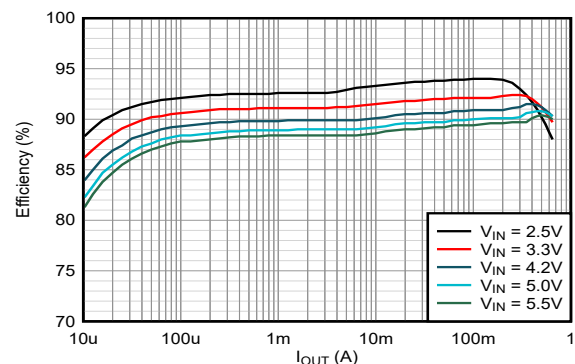
The RF-friendly device uses DCS-Control for a low output voltage ripple. The device is designed to power wireless applications like Wi-Fi or Bluetooth. The device switches at 1.5MHz and has high efficiency even at light load current down to 10µA for long battery life and easy thermal management. Humidity, temperature or vibration have no influence on the output voltage accuracy due to the integrated feedback divider. Therefore, the device is also an excellent choice for industrial point of load applications.

18 predefined output voltages per part number with 1% accuracy selected through a standard E48 (2%) or E96 (1%) resistor on the VSET pin support a large variety of applications.

### Device Information

| PART NUMBER[3] | $V_{OUT}$ RANGE | PACKAGE[1] | PACKAGE SIZE[2] |
|---|---|---|---|
| TPSM828436 | 0.4V – 0.8V | VCF (QFN-FCMOD, 7) | 2.45mm × 2.7mm |
| TPSM828437 | 0.8V – 1.8V | | |
| TPSM828438 | 1.8V – 3.6V | | |

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) See the *Device Comparison Table*.



**Typical Application**



**Efficiency vs Output Current at 1.8V$_{OUT}$**

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Product Folder Links: *TPSM82843*

## 4 Device Comparison Table

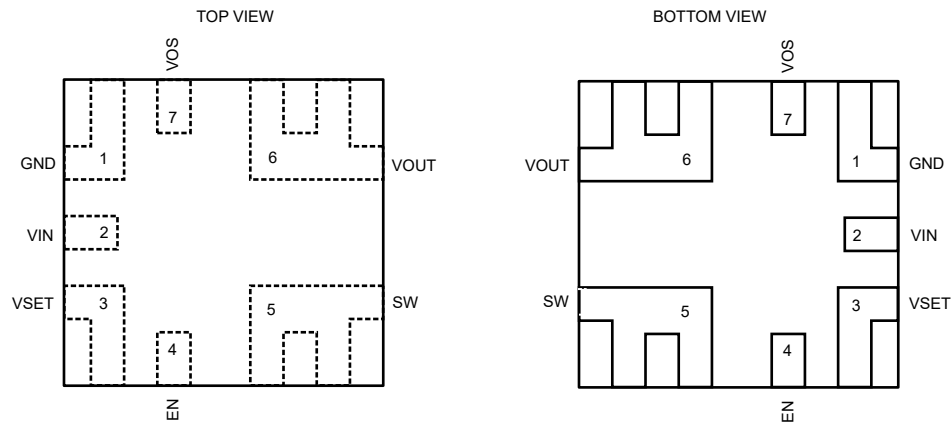| Device | Fixed $V_{OUT}$ VSET = GND | Selectable Output Voltages | $f_{SW}$ [MHz] | Soft Start $t_{SS}$ |
|---|---|---|---|---|
| TPSM828436VCFR | 1.0V | 0.4V – 0.8V in 25mV steps | 1.5 | 0.45ms |
| TPSM828437VCFR | 1.8V | 0.8V – 1.6V in 50mV steps | 1.5 | 1ms |
| TPSM828438VCFR | 3.6V | 1.8V – 3.4V in 100mV steps | 1.5 | 0.7ms |

## 5 Pin Configuration and Functions



**Figure 5-1. VCF, 7-Pin QFN-FCMOD Package**

**Table 5-1. Pin Functions**

| PIN NAME | PIN NO. | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| GND | 1 | PWR | GND supply pin. Connect this pin close to the GND terminal of the input and output capacitor. |
| VIN | 2 | PWR | $V_{IN}$ power supply pin. Connect the input capacitor close to this pin for best noise and voltage spike suppression. A ceramic capacitor is required. |
| VOUT | 6 | PWR | Output voltage of the module. Connect this pin to the output capacitor. |
| VSET | 3 | I | Connecting a resistor to GND selects a pre-defined output voltage. |
| VOS | 7 | I | Output voltage sense pin for the internal feedback divider network and regulation loop. This pin also discharges $V_{OUT}$ by an internal MOSFET when the converter is disabled. Connect this pin directly to the output capacitor with a short trace. |
| SW | 5 | O | This pin is the switch pin of the converter. This pin connects to the internal power MOSFET and the inductor. Avoid connecting this pin to larger traces as this action can increase EMI. This pin can stay unconnected or be soldered to a small pad for thermal improvement. |
| EN | 4 | I | A high level enables the devices and a low level turns the device off. The pin features an internal pulldown resistor, which is disabled after the device has started up. |

(1)    I = input, O = output, PWR = power

# 6 Specifications

## 6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) [1]

|  |  | MIN | MAX | UNIT |
|---|---|---|---|---|
| Pin voltage | VIN | −0.3 | 6 | V |
| Pin voltage | SW, VOUT at DC condition | −0.3 | $V_{IN}$ + 0.3V | V |
| Pin voltage | SW, transient < 10ns, while switching | −2.5 | 9 | V |
| Pin voltage | EN, VSET | −0.3 | 6 | V |
| Pin voltage | VOS | −0.3 | 5 | V |
| $T_J$ | Operating junction temperature | −40 | 150 | °C |
| $T_{stg}$ | Storage temperature | −55 | 150 | °C |

(1)  Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

## 6.2 ESD Ratings

|  |  |  | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1] | ±2000 | V |
|  |  | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 [2] | ±500 | |

(1)  JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2)  JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

|  |  | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Supply voltage $V_{IN}$ | 1.8 | | 5.5 | V |
| $I_{OUT}$ | Output current | | | 0.6 | A |
| $C_{OUT}$ | Effective output capacitance | 4 | | 25 | µF |
| $C_{IN}$ | Effective input capacitance | 0.5 | 4.7 | | µF |
| $C_{VSET}$ | External parasitic capacitance at VSET pin | | | 30 | pF |
| $R_{SET}$ | Resistance range for external resistor at VSET pin (E96 1% resistor values) | 10 | | 249 | kΩ |
|  | External resistor tolerance E96 series at VSET pin | | | 1% | |
|  | E96 resistor series temperature coefficient (TCR) | −200 | | +200 | ppm/°C |
| $T_J$ | Operating junction temperature range | −40 | | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | TPSM82843x VCF (QFN-FCMOD) 7 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 72.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 57.2 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 21.2 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | (–4.2)[2] | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 21.2 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | – | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) Case top temperature can be higher than temperature of active circuit because of inductor power dissipation. This results in a negative Junction-to-top characterization parameter.

## 6.5 Electrical Characteristics

$T_J$ = –40°C to +125°C, $V_{IN}$ = 1.8V to 5.5V. Typical values are at $T_J$ = 25°C, $V_{IN}$ = 3.6V and $V_{OUT}$ = 0.7V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY** | | | | | | |
| $I_Q$ | Operating quiescent current in PFM mode while output voltage > set output voltage | Non-switching, $V_{EN}$ = $V_{IN}$, $I_{OUT}$ = 0µA, $T_J$ = –40°C to 85°C | | 275 | 1500 | nA |
| $I_{SD}$ | Shutdown current | $V_{EN}$ = 0 V, VSET = GND, $T_J$ = –40°C to 85°C | | 4 | 850 | nA |
| **UVLO** | | | | | | |
| $V_{UVLO(R)}$ | Undervoltage lockout rising threshold | $V_{IN}$ rising, $I_{OUT}$ = 0µA | | 1.75 | 1.8 | V |
| $V_{UVLO(F)}$ | Undervoltage lockout falling threshold | $V_{IN}$ falling, $I_{OUT}$ = 0µA | | 1.65 | 1.7 | V |
| $V_{UVLO(H)}$ | Undervoltage lockout hysteresis | | | 100 | | mV |
| **VSET PIN** | | | | | | |
| $V_{SET(LKG)}$ | VSET input leakage current | $T_J$ = –40°C to 85°C | | 10 | 800 | nA |
| $V_{SET(H)}$ | VSET high-level detection | Voltage at VSET during startup | 1.0 | | | V |
| $R_{SET}$ | RSET accuracy | $T_J$ = –20°C to 125°C | –4 | | 4 | % |
| $R_{SET}$ | RSET accuracy | $T_J$ = –40°C to 125°C | –3.5 | | 3.5 | % |
| **ENABLE** | | | | | | |
| $V_{EN(R)}$ | EN voltage rising threshold | EN rising, enable switching | 0.8 | | | V |
| $V_{EN(F)}$ | EN voltage falling threshold | EN falling, disable switching | | | 0.4 | V |
| $V_{EN(LKG)}$ | EN input leakage current | $V_{EN}$ > 0.8V, $T_J$ = –40°C to 85°C | | 1 | 25 | nA |
| $R_{EN;PD}$ | EN internal pull-down resistance | EN pin to GND | 425 | 500 | | kΩ |
| **VOUT VOLTAGE** | | | | | | |
| $V_{OUT}$ | DC output voltage accuracy | PWM operation, $T_J$ = –20°C to 125°C | –1 | | +1 | % |
| $V_{OUT}$ | DC output voltage accuracy | PWM operation, $T_J$ = –40°C to 125°C | –1.5 | | +1.5 | % |
| $V_{OUT}$ | TPSM828436 | | 0.4 | | 0.8 | V |
| | TPSM828437 | | 0.8 | | 1.8 | V |
| | TPSM828438 | | 1.8 | | 3.6 | V |
| $I_{VOS(LKG)}$ | VOS input leakage current | TPSM828436, $V_{EN}$ = $V_{IN}$, $V_{VOS}$ = 0.7V, $T_J$ = –40°C to 85°C | | | 100 | nA |
| | | TPSM828437, $V_{EN}$ = $V_{IN}$, $V_{VOS}$ = 1.2V, $T_J$ = –40°C to 85°C | | 100 | 250 | nA |
| | | TPSM828438, $V_{EN}$ = $V_{IN}$, $V_{VOS}$ = 3.3V, $T_J$ = –40°C to 85°C | | 275 | 450 | nA |

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## 6.5 Electrical Characteristics (continued)

$T_J$ = –40°C to +125°C, $V_{IN}$ = 1.8V to 5.5V. Typical values are at $T_J$ = 25°C, $V_{IN}$ = 3.6V and $V_{OUT}$ = 0.7V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SW}$ | | $I_{OUT}$ = 400mA | | 1.5 | | MHz |
| **STARTUP** | | | | | | |
| $t_{SS}$ | TPSM828436 soft-start time | From $V_{OUT}$ = 0% to $V_{OUT}$ = 95% of $V_{OUT}$ nominal | | 0.45 | 0.6 | ms |
| | TPSM828438 soft-start time | | | 1.0 | 1.4 | |
| | TPSM828437 soft-start time | | | 0.7 | 1.0 | |
| $t_{Startup\_delay}$ | EN HIGH to start of switching delay | R2D = GND | | 330 | 560 | µs |
| **POWER STAGE** | | | | | | |
| $R_{DSON(HS)}$ | High-side MOSFET on-resistance | $V_{IN}$ = 3.6V, $I_{OUT}$ = 300mA | | 170 | 260 | mΩ |
| $R_{DSON(LS)}$ | Low-side MOSFET on-resistance | $V_{IN}$ = 3.6V, $I_{OUT}$ = 300mA | | 70 | 115 | mΩ |
| $R_{DROPOUT}$ | Dropout resistance high-side MOSFET $R_{DSON}$ + $L_{DCR}$ | $V_{IN}$ = 3.6V, $I_{OUT}$ = 300mA, typ at 25°C | | 280 | | mΩ |
| $I_{LKG\_SW}$ | Leakage current into SW-Pin | $V_{SW}$ = 0.7V, $T_J$ = –40°C to 85°C | | 0 | 35 | nA |
| $I_{LKG\_SW}$ | Leakage current into SW-Pin | $V_{SW}$ = 1.2V, $T_J$ = –40°C to 85°C | | 0 | 45 | nA |
| $I_{LKG\_SW}$ | Leakage current into SW-Pin | $V_{VIN > VSW}$, $V_{SW}$ = 3.3V, $T_J$ = –40°C to 85°C | | 0 | 45 | nA |
| **OVERCURRENT PROTECTION** | | | | | | |
| $I_{HS(OC)}$ | High-side peak current limit | $V_{IN}$ ≧ 2.2V | 0.9 | 1.1 | 1.3 | A |
| $I_{LS(OC)}$ | Low-side valley current limit | $V_{IN}$ ≧ 2.2V | 0.79 | 1.0 | 1.11 | A |
| **OUTPUT DISCHARGE** | | | | | | |
| $R_{DSCH\_VOS}$ | Output discharge resistor on VOS pin | $V_{EN}$ = GND, I(VOS) = –10mA | | 7 | 22 | Ω |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{J(SD)}$ | Thermal shutdown threshold | Temperature rising | | 160 | | °C |
| $T_{J(HYS)}$ | Thermal shutdown hysteresis | | | 20 | | °C |

Product Folder Links: *TPSM82843*
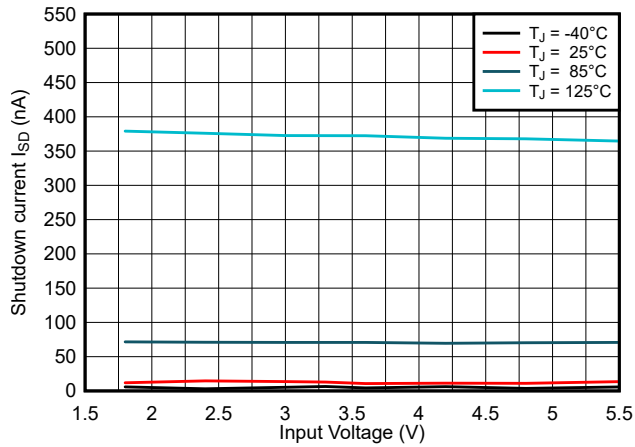
## 6.6 Typical Characteristics



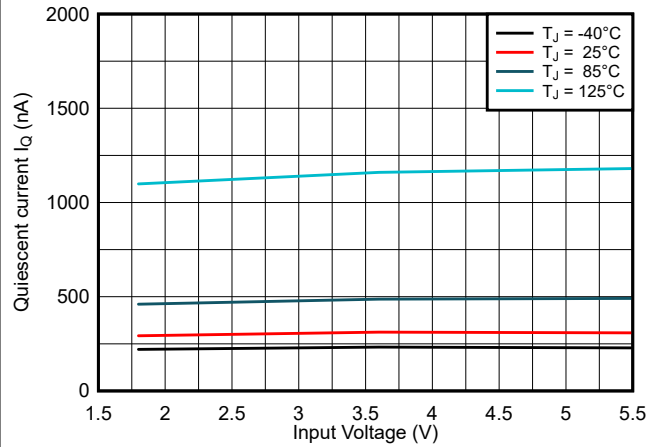Figure 6-1. Shutdown Current $I_{SD}$
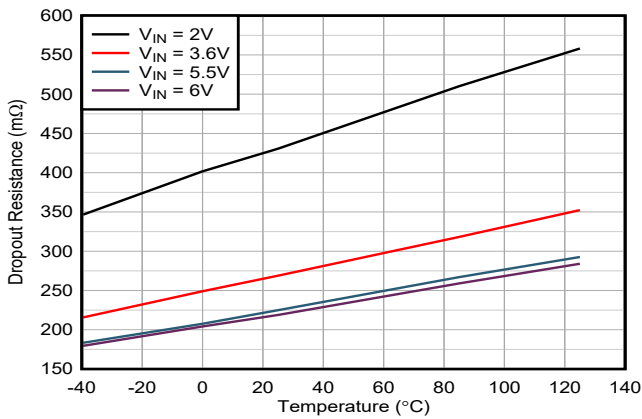


Figure 6-2. Quiescent Current $I_Q$



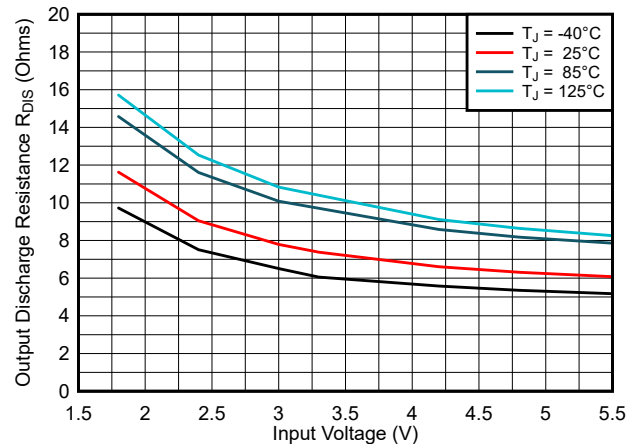Figure 6-3. Dropout Resistance $R_{DS(ON)}$



Figure 6-4. VOS Discharge Switch Drain Source Resistance $R_{DIS}$

# 7 Detailed Description

## 7.1 Overview

The TPSM82843 is a high-frequency, synchronous step-down converter with integrated inductor and ultra-low quiescent current of typically 275nA. The device operates with a 4.7µF input capacitor and 10µF output capacitor over the entire recommended operation range to provide very small design size.

Using TI's DCS-Control topology, the device extends the high efficiency operation area down to microamperes of load current during power saving in Pulse Frequency Modulation (PFM) mode. TI's DCS-Control (Direct Control with Seamless Transition into PFM mode) is an advanced regulation topology that combines the advantages of hysteretic and voltage mode control. Characteristics of DCS-Control are excellent AC load regulation and transient response, low output ripple voltage, and a seamless transition between PFM and Pulse Width Modulation (PWM) mode operation. DCS-Control includes an AC loop that senses the output voltage (VOS pin) and directly feeds the information to a fast comparator stage. This comparator sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To achieve accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low-ESR capacitors.

## 7.2 Functional Block Diagram
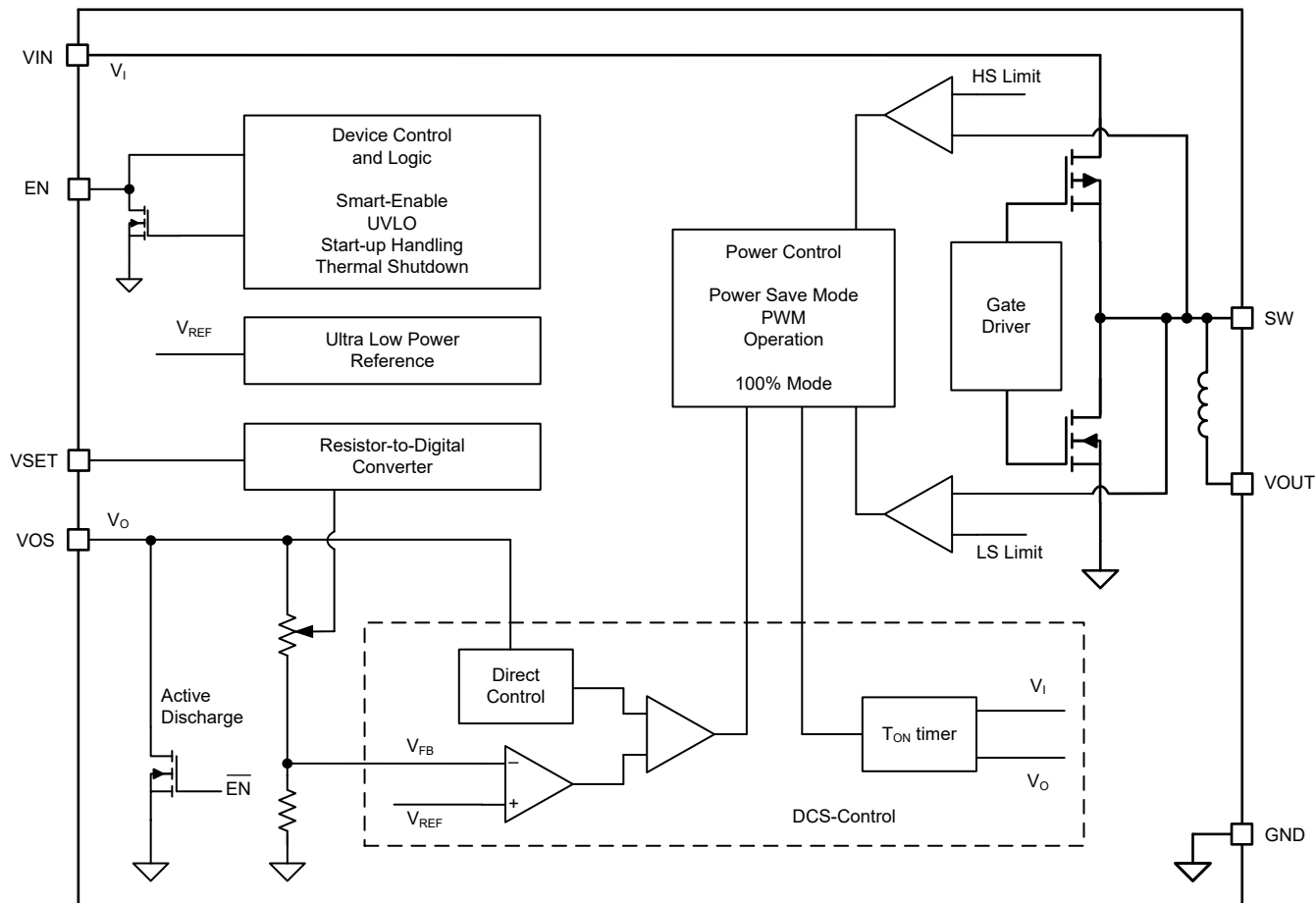
## 7.3 Feature Description

### 7.3.1 Smart Enable and Shutdown (EN)

An internal 500kΩ resistor pulls the EN pin to GND and avoids floating the pin. This action prevents an uncontrolled start-up of the device in case the EN pin cannot be driven to low level safely. With EN low, the device is in shutdown mode. The device is turned on with EN set to a high level. The pulldown control circuit disconnects the pulldown resistor on the EN pin after the internal control logic and the reference have been powered up. With EN set to a low level, the device enters shutdown mode and the pulldown resistor is activated again.

### 7.3.2 Soft Start

After the device has been enabled with EN high, the device initializes and powers up the internal circuits. This action occurs during the regulator start-up delay time, $t_{Startup\_delay}$. After $t_{Startup\_delay}$ expires, the internal soft-start circuitry ramps up the output voltage within the soft-start time, $t_{ss}$. See Figure 7-1.

The start-up delay time, $t_{Startup\_delay}$, varies depending on the selected VSET value. The start-up delay is shortest with VSET = 0 and longest with VSET = 16.



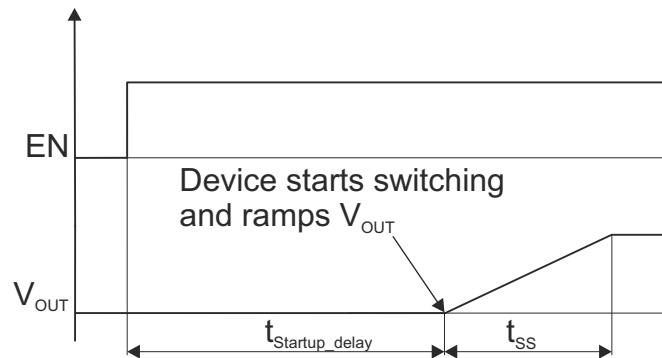**Figure 7-1. Device Start-Up**

### 7.3.3 VSET Pin: Output Voltage Selection

The output voltage is set with a single external resistor connected between the VSET pin and GND. After the device has been enabled and the control logic as well as the internal reference have been powered up, a R2D (resistor-to-digital) conversion is started to detect the external resistor, $R_{SET}$, within the regulator start-up delay time, $t_{Startup\_delay}$. An internal current source applies current through the external resistor and an internal ADC reads back the resulting voltage level. Depending on the level, an internal feedback divider network is selected to set the correct output voltage. After this R2D conversion is finished, the current source is turned off to avoid current flow through the external resistor. The circuit can detect resistive values, high-level, low-level, and a pin-open.

For a proper reading, make sure that there is no additional current path or capacitance greater than 30pF total to GND during R2D conversion. Otherwise, the additional current to GND is interpreted as a lower resistor value and a false output voltage is set. Table 7-1 lists the correct resistor values for $R_{SET}$ to set the appropriate output voltages. The R2D converter is designed to operate with resistor values out of the E96 table and requires 1% resistor value accuracy. The external resistor $R_{SET}$ is not a part of the regulator feedback loop and has therefore no impact on the output voltage accuracy. Make sure that there is no other leakage path than the $R_{SET}$ resistor at the VSET pin during an undervoltage lockout event. Otherwise, a false output voltage is set.

**Table 7-1. Output Voltage Setting**

| VSET | Output Voltage Setting [V] | | | $R_{SET}$ [Ω] |
|---|---|---|---|---|
| | TPSM828436 | TPSM828437 | TPSM828438 | |
| 1 | 0.400 | 0.80 | 1.8 | 10.0 k |
| 2 | 0.425 | 0.85 | 1.9 | 12.1 k |
| 3 | 0.450 | 0.90 | 2.0 | 15.4 k |
| 4 | 0.475 | 0.95 | 2.1 | 18.7 k |
| 5 | 0.500 | 1.00 | 2.2 | 23.7 k |
| 6 | 0.525 | 1.05 | 2.3 | 28.7 k |
| 7 | 0.550 | 1.10 | 2.4 | 36.5 k |
| 8 | 0.575 | 1.15 | 2.5 | 44.2 k |
| 9 | 0.600 | 1.20 | 2.6 | 56.2 k |
| 10 | 0.625 | 1.25 | 2.7 | 68.1 k |
| 11 | 0.650 | 1.30 | 2.8 | 86.6 k |
| 12 | 0.675 | 1.35 | 2.9 | 105.0 k |
| 13 | 0.700 | 1.40 | 3.0 | 133.0 k |
| 14 | 0.725 | 1.45 | 3.1 | 162.0 k |
| 15 | 0.750 | 1.50 | 3.2 | 205.0 k |
| 16 | 0.775 | 1.55 | 3.3 | 249.0 k or larger |
| 17 | 0.8 | 1.6 | 3.4 | VIN |
| 0 | 1.0 | 1.8 | 3.6 | GND |

### 7.3.4 Undervoltage Lockout (UVLO)

To avoid misoperation of the device at low input voltages, an undervoltage lockout (UVLO) comparator monitors the supply voltage. The UVLO comparator shuts down the device at an input voltage of 1.7V (maximum) with falling $V_{IN}$. The device starts at an input voltage of 1.8V (maximum) rising $V_{IN}$. After the device re-enters operation out of an undervoltage lockout condition, the device behaves like being enabled. The internal control logic is powered up and the external resistor at the VSET pin is read out.

### 7.3.5 Switch Current Limit, Short-Circuit Protection

The TPSM82843 integrates a current limit on the high-side and low-side MOSFETs to protect the device against overload or short circuit conditions. The current in the switches is monitored cycle by cycle. If the high-side MOSFET current limit, $I_{LIMF}$ trips, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. After the inductor current through the low-side switch decreases beneath the low-side MOSFET current limit, $I_{LIMF}$, the low-side MOSFET is turned off and the high-side MOSFET turns on again.

### 7.3.6 Thermal Shutdown

The junction temperature ($T_J$) of the device is monitored by an internal temperature sensor. If $T_J$ exceeds the thermal shutdown temperature, $T_{SD}$, of 160°C (typical), the device enters thermal shutdown. Both the high-side and low-side power FETs are turned off. When $T_J$ decreases below the hysteresis amount of typically 20°C, the converter resumes operation, beginning with a soft start to the originally set $V_{OUT}$ (there is no R2D conversion of $R_{SET}$). The thermal shutdown is not active in power save mode.

### 7.3.7 Output Voltage Discharge

The purpose of the output discharge function is to make sure of a defined down-ramp of the output voltage when the device is disabled and to keep the output voltage close to 0V.

The internal discharge resistor is connected to the VOS pin. The discharge function is enabled as soon as the device is disabled. The minimum supply voltage required to keep the discharge function active is $V_{IN} > V_{TH\_UVLO}$.

## 7.4 Device Functional Modes

### 7.4.1 Power Save Mode Operation

The DCS-Control topology supports power save mode operation. At light loads, the device operates in PFM (pulse frequency modulation) mode that generates a single switching pulse to ramp up the inductor current and recharge the output capacitor, followed by a sleep period where most of the internal circuits are shut down to achieve the lowest operating quiescent current. During this time, the load current is supported by the output capacitor. The duration of the sleep period depends on the load current and the inductor peak current. During the sleep periods, the current consumption is reduced to typically 275nA. This low quiescent current consumption is achieved by an ultra-low power voltage reference, an integrated high impedance feedback divider network, and an optimized power save mode operation.

In PFM mode, the switching frequency varies linearly with the load current. At medium and high load conditions, the device enters automatically PWM (pulse width modulation) mode and operates in continuous conduction mode with a nominal switch frequency $f_{sw}$ of typically 1.5MHz. The switching frequency in PWM mode is controlled and depends on $V_{IN}$ and $V_{OUT}$. The boundary between PWM and PFM mode is when the inductor current becomes discontinuous.

If the load current decreases, the converter seamlessly enters PFM mode to maintain high efficiency down to very light loads. Because DCS-Control supports both operation modes within one single building block, the transition from PWM to PFM mode is seamless with minimum output voltage ripple.

### 7.4.2 100% Mode Operation

The duty cycle of the buck converter operating in PWM mode is given as $D = V_{OUT}/V_{IN}$. The duty cycle increases as the input voltage comes close to the output voltage. In 100% duty cycle mode, the device keeps the high-side switch on continuously. The high-side switch stays turned on as long as the output voltage is below the internal set point. This action allows the conversion of small input to output voltage differences.

# 8 Application and Implementation

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**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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## 8.1 Application Information

The following sections discuss the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

## 8.2 Typical Application

The following schematics show the typical application circuit for minimal footprint. The TPSM82843 has been designed to accommodate output capacitance values from 4µF (effective) to 25µF (effective). The output capacitance has influence on the application curves, especially light load efficiency and load step. A smaller output capacitance causes a higher switching frequency and lower efficiency at equal light load. This outcome can help however keeping the switching frequency out of the audio band. This outcome also results in a larger voltage change during load transients while a larger capacitance reduces the voltage change. The application curves have been taken with 10µF output capacitor which is equivalent to an effective capacitance of 8µF at $V_{OUT}$ of 1.2V with the output capacitor type in the BOM table.
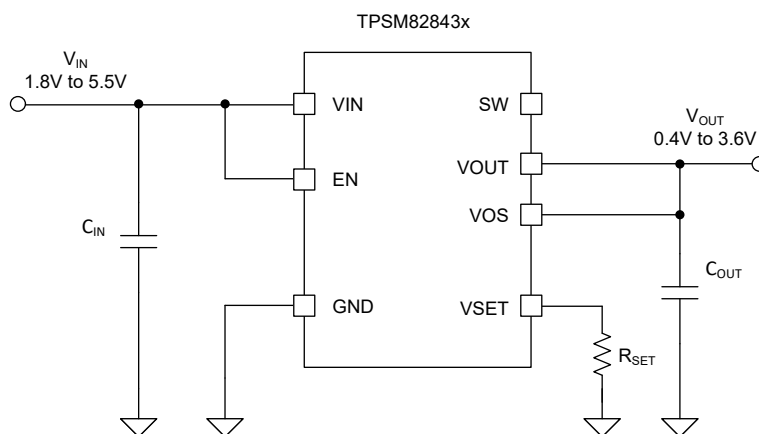


**Figure 8-1. TPSM82843 Typical Application Circuit**

### 8.2.1 Design Requirements

The following table shows the list of components for the application circuit and the characteristic application curves.

**Table 8-1. Components for Application Characteristic Curves**

| Reference | Description | Value | Size Code Inch [Metric L × W × T] | Manufacturer |
|---|---|---|---|---|
| TPSM828436, TPSM828437, TPSM828438 | 275nA-$I_Q$ buck converter module | | [2.45mm × 2.7mm × 1.29mm] | TI |
| $C_{IN}$ | Ceramic capacitor GRM155R60J475ME47D | 4.7µF | 0402 [1.0mm × 0.5mm × 0.5mm] | Murata |
| $C_{OUT}$ | Ceramic capacitor GRM155R60J106ME15D | 10µF | 0402 [1.0mm × 0.5mm × 0.5mm] | Murata |
| $R_{SET}$ | See voltage setting table | | 0402 [1.0mm × 0.5mm × 0.5mm] | |

Product Folder Links: *TPSM82843*

### 8.2.2 Detailed Design Procedure

Follow the passive component selection per the typical application circuit.
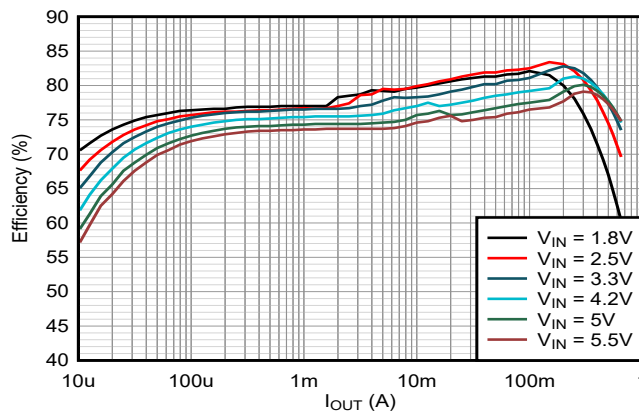
### 8.2.3 Application Curves
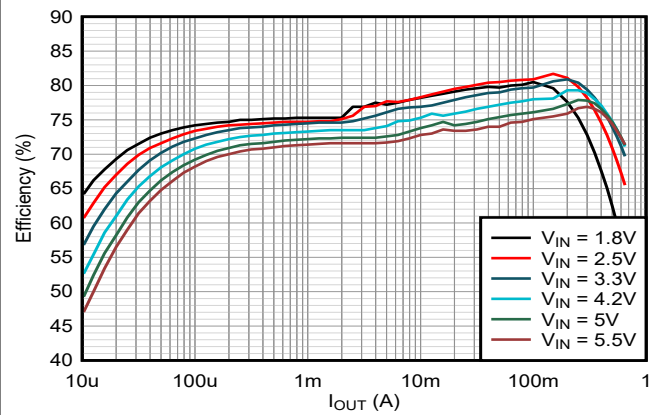


**Figure 8-2. Efficiency at 0.4 V$_{OUT}$ and 25°C**
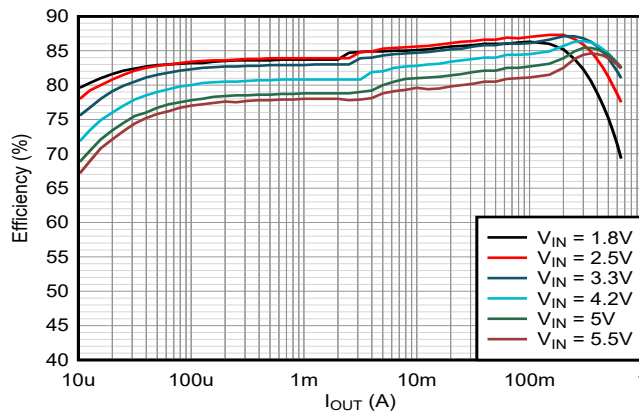


**Figure 8-3. Efficiency at 0.4 V$_{OUT}$ and 85°C**



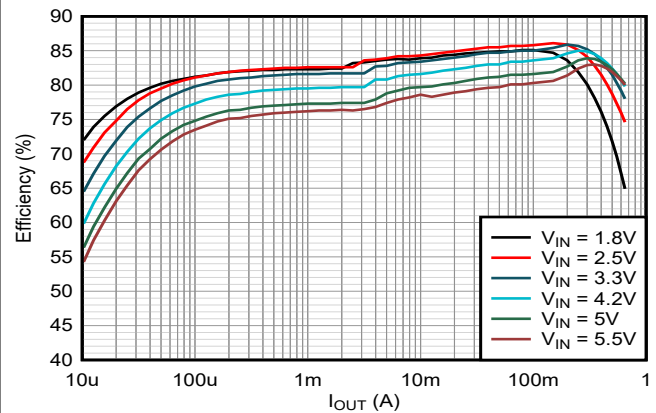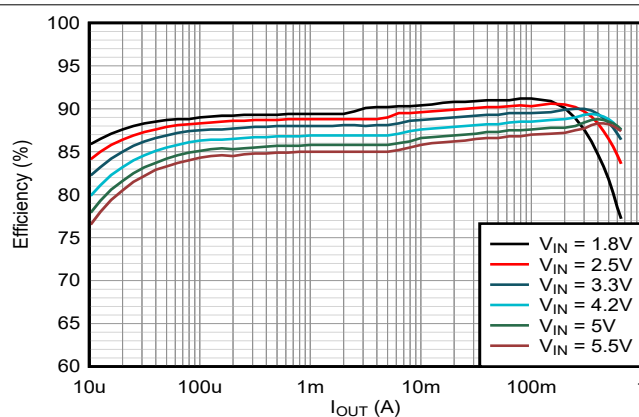**Figure 8-4. Efficiency at 0.7 V$_{OUT}$ and 25°C**



**Figure 8-5. Efficiency at 0.7 V$_{OUT}$ and 85°C**



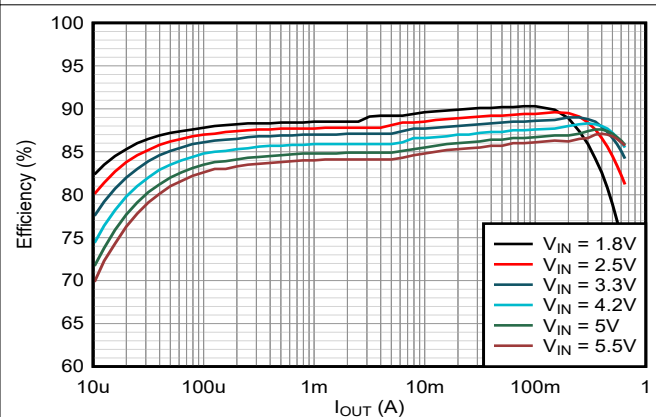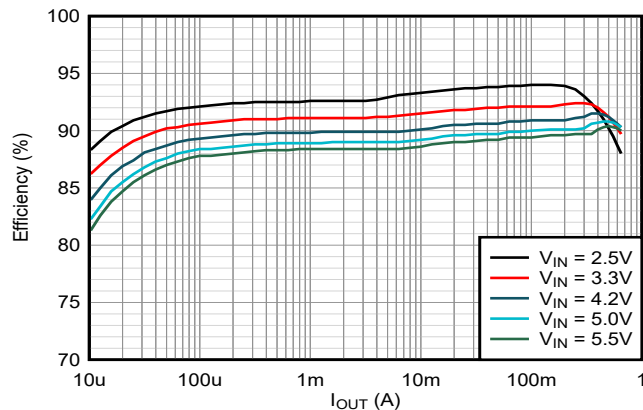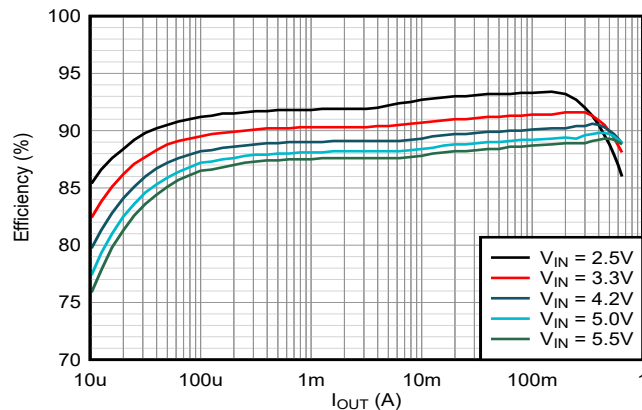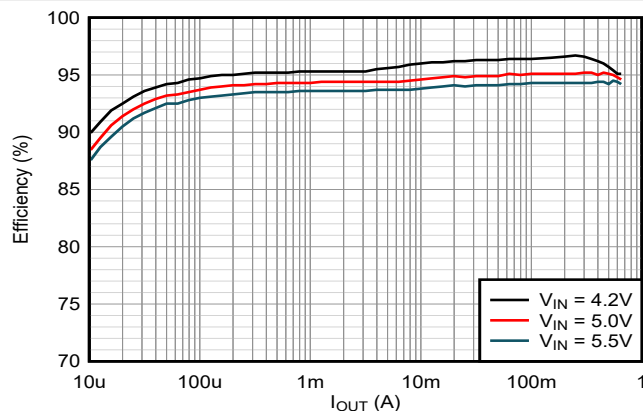**Figure 8-6. Efficiency at 1.2 V$_{OUT}$ and 25°C**



**Figure 8-7. Efficiency at 1.2 V$_{OUT}$ and 85°C**

Product Folder Links: TPSM82843

**Figure 8-8. Efficiency at 1.8 V_OUT and 25°C**

**Figure 8-9. Efficiency at 1.8 V_OUT and 85°C**

**Figure 8-10. Efficiency at 3.6 V_OUT and 25°C**
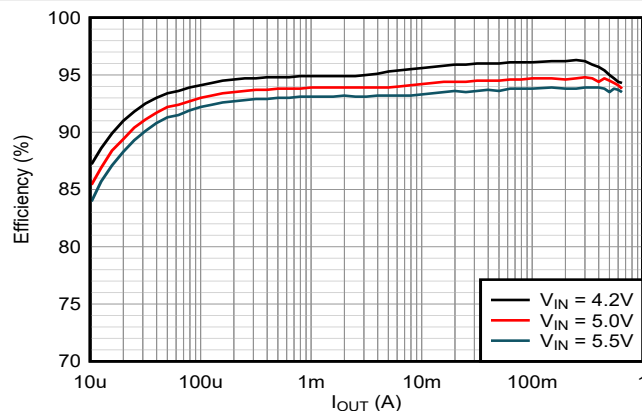
**Figure 8-11. Efficiency at 3.6 V_OUT and 85°C**
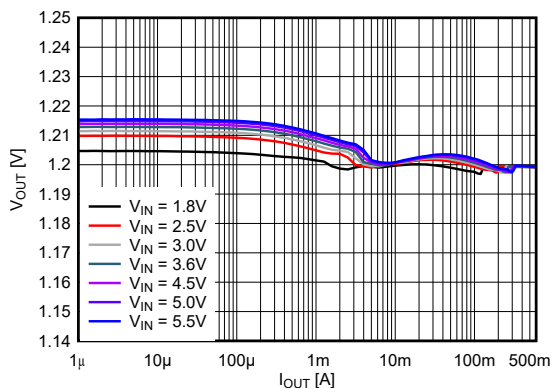
**Figure 8-12. Output Voltage vs Output Current at 1.2 V_OUT**
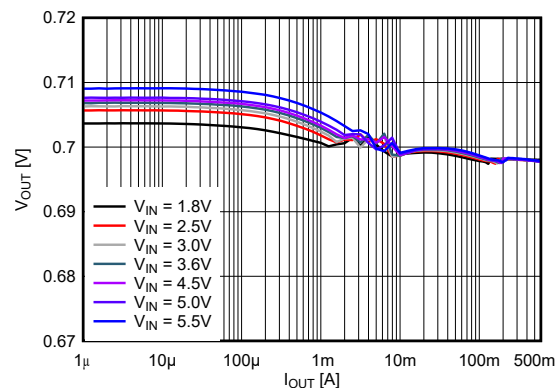
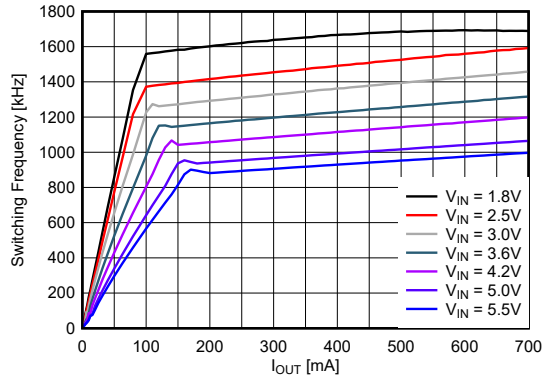**Figure 8-13. Output Voltage vs Output Current at 0.7 V_OUT**

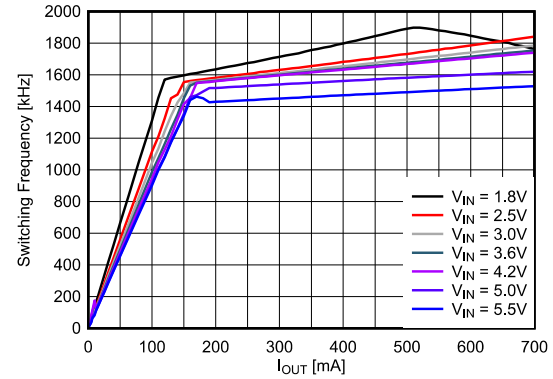Figure 8-14. Switching Frequency vs Output Current at 0.4 $V_{OUT}$



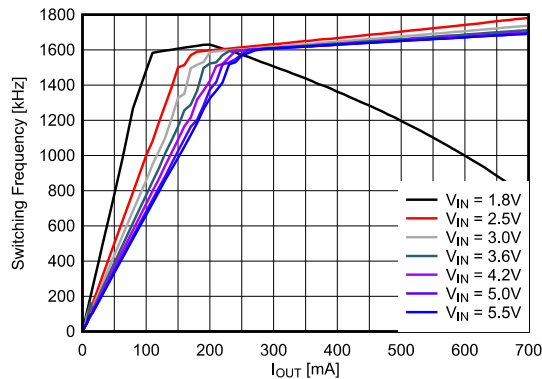Figure 8-15. Switching Frequency vs Output Current at 0.7 $V_{OUT}$



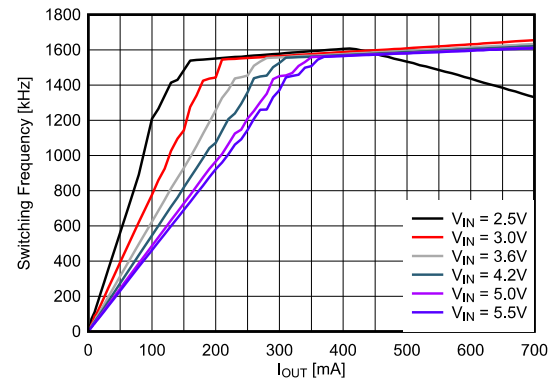Figure 8-16. Switching Frequency vs Output Current at 1.2 $V_{OUT}$



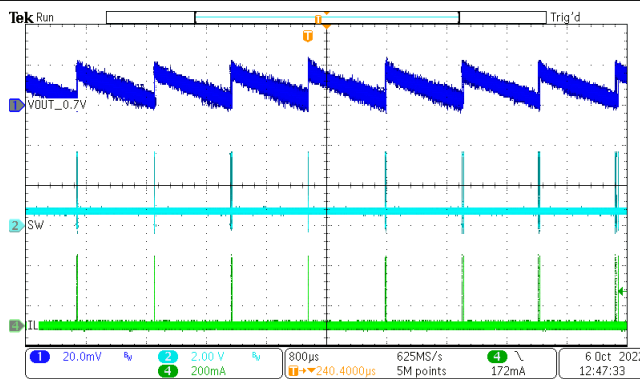Figure 8-17. Switching Frequency vs Output Current at 1.8 $V_{OUT}$



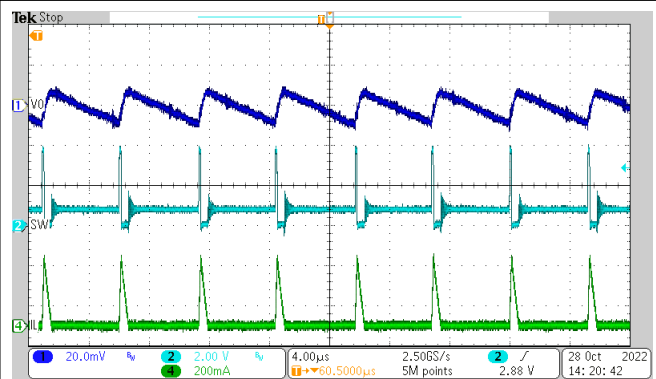Figure 8-18. Typical Operation at 0.7 $V_{OUT}$, 100 µA $I_{OUT}$



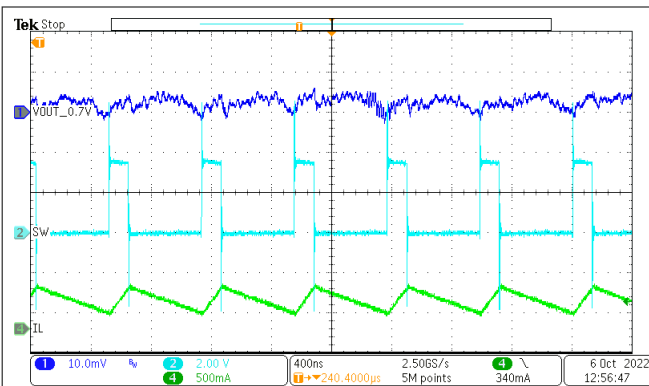Figure 8-19. Typical Operation at 0.7 $V_{OUT}$, 20 mA $I_{OUT}$

Product Folder Links: *TPSM82843*

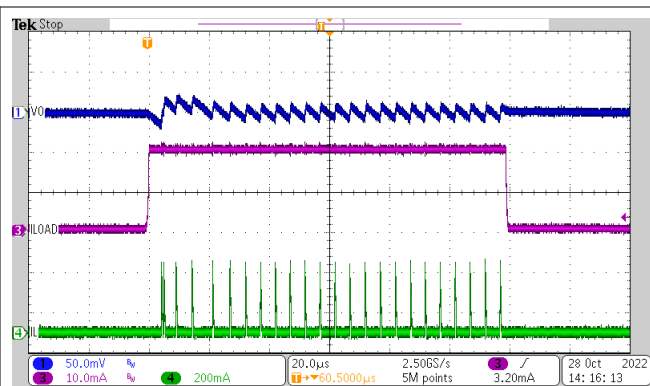**Figure 8-20. Typical Operation at 0.7 V$_{OUT}$, 400 mA I$_{OUT}$**



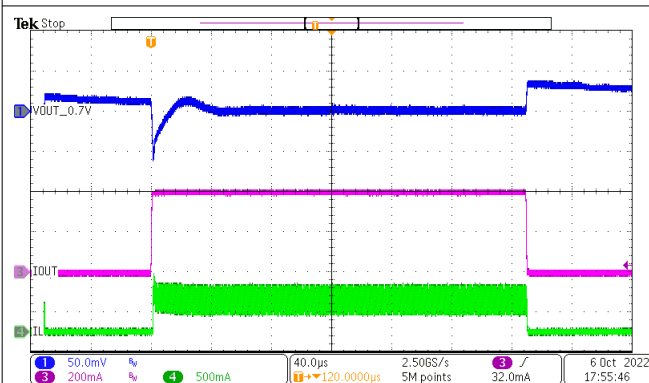**Figure 8-21. Load Transient at 0.7 V$_{OUT}$, I$_{OUT}$ = 100µA to 20mA**



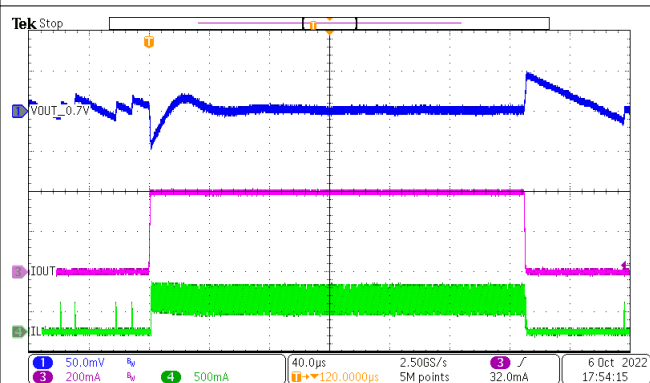**Figure 8-22. Load Transient at 0.7 V$_{OUT}$, I$_{OUT}$ = 100µA to 400mA**



**Figure 8-23. Load Transient at 0.7 V$_{OUT}$, I$_{OUT}$ = 5mA to 400mA**



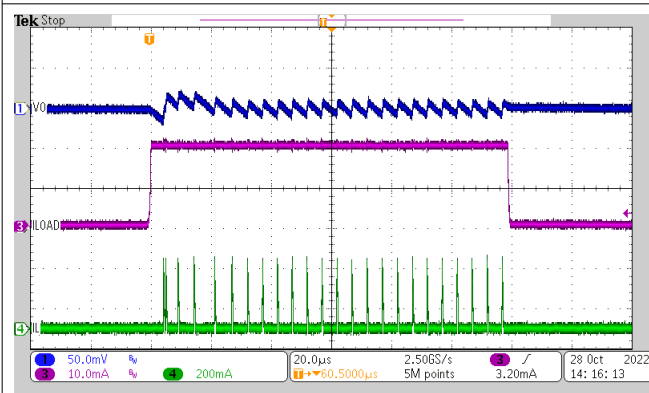**Figure 8-24. Load Transient at 1.2 V$_{OUT}$, I$_{OUT}$ = 100µA to 20mA**
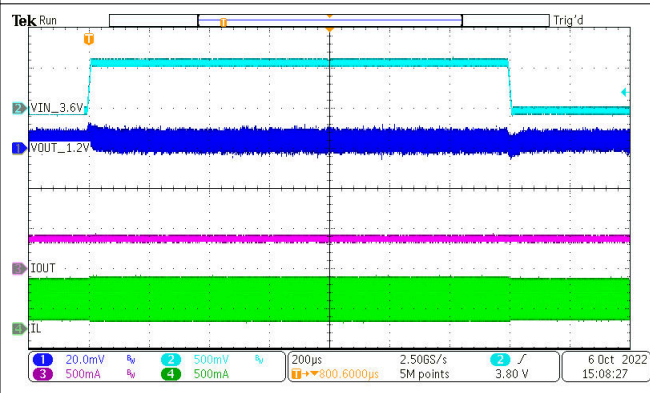


**Figure 8-25. Load Transient at 1.2 V$_{OUT}$, I$_{OUT}$ = 100µA to 400mA**

Product Folder Links: *TPSM82843*
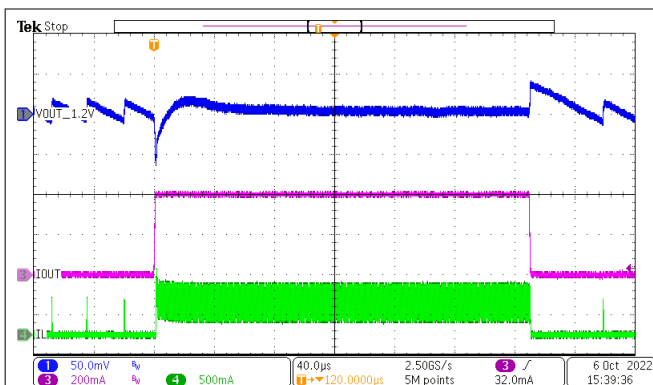
**Figure 8-26. Load Transient at 1.2 V_OUT, I_OUT = 5mA to 400mA**



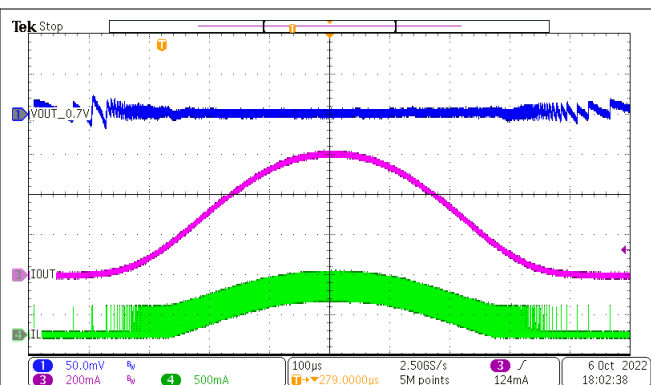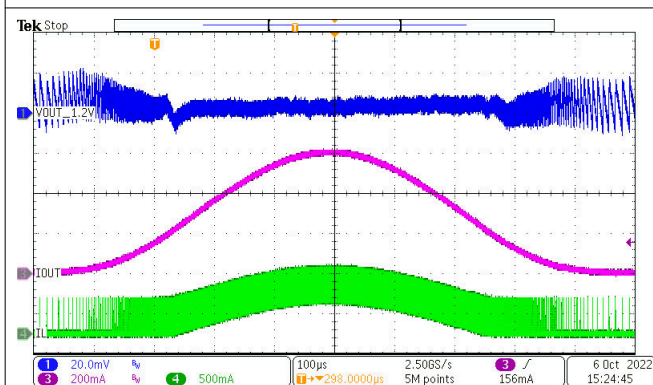**Figure 8-27. AC Load Sweep at 0.7 V_OUT, I_OUT = 1mA to 600mA**



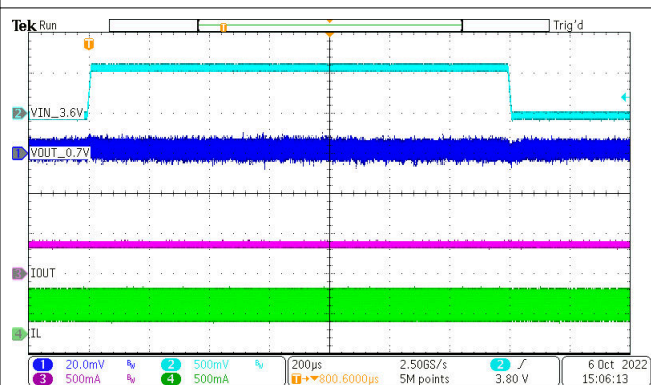**Figure 8-28. AC Load Sweep at 1.2 V_OUT, I_OUT = 1mA to 600mA**



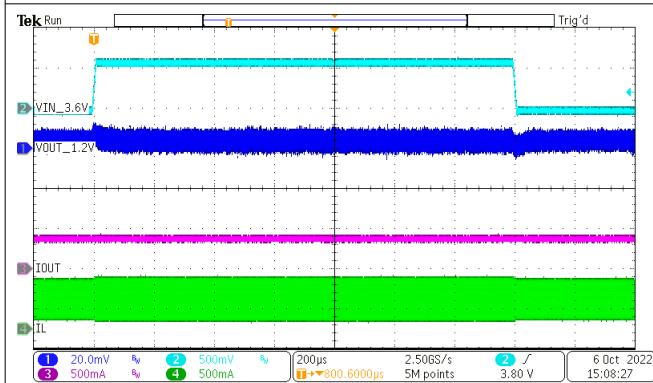**Figure 8-29. Line Transient at 0.7 V_OUT, I_OUT = 400mA, V_IN = 3.6V to 4.2V**



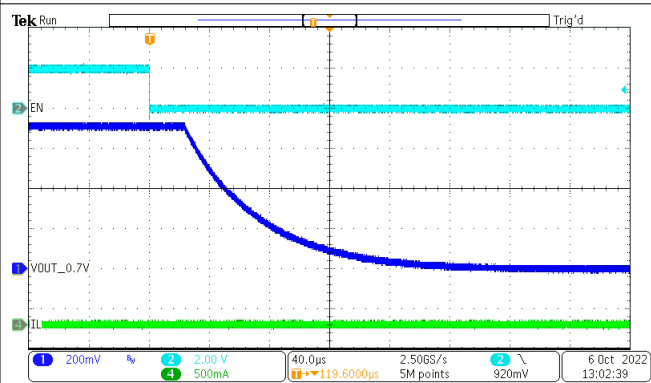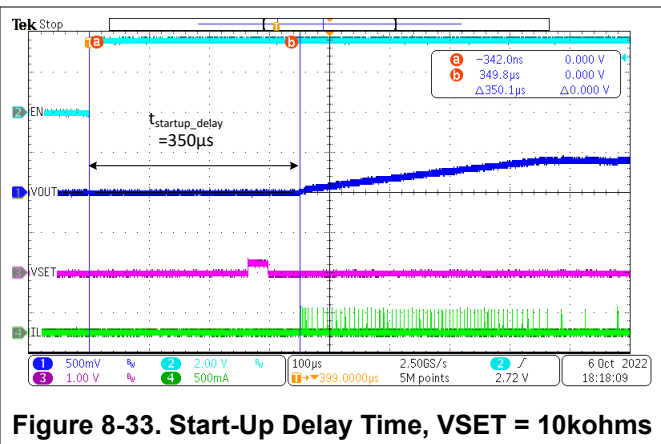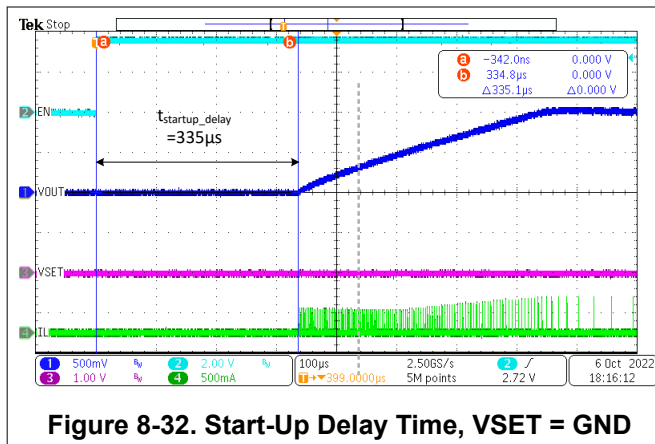**Figure 8-30. Line Transient at 1.2 V_OUT, I_OUT = 400mA, V_IN = 3.6V to 4.2V**



**Figure 8-31. Shutdown, Output Discharge at 0.7 V_OUT**

Product Folder Links: *TPSM82843*

**Figure 8-32. Start-Up Delay Time, VSET = GND**



**Figure 8-33. Start-Up Delay Time, VSET = 10kohms**

## 8.3 Power Supply Recommendations

The power supply must provide a current rating according to the supply voltage, output voltage, and output current of the TPSM82843.

## 8.4 Layout

### 8.4.1 Layout Guidelines

The pinout of TPSM82843 has been designed to enable a single top layer PCB routing of the IC and the critical passive components such as CIN, COUT, and VSET resistor. Furthermore, this pinout allows the user to connect tiny components such as 0201 (0603 metric) size capacitors and resistors. As for all switching power supplies, the layout is an important step in the design. Care must be taken in board layout to get the specified performance. Providing a low inductance, low impedance ground path is critical. Therefore, use wide and short traces for the main current paths. Place the input capacitor as close as possible to the VIN of the IC and GND pins. This placement is the most critical component placement. Then place the output capacitor without via as close as possible to the VOUT and GND pin as shown in the following layout diagram. The VOS line is a sensitive, high impedance input and must be connected to the output capacitor with a direct trace from the output capacitor solder pad to the device pin. The VOS line must stay away from noisy components and traces (for example, the SW line) or other noise sources. For bode measurements in the evaluation board, a via is placed on the trace to allow connection of a 10Ohm resistor between the capacitor pad and VOS on the bottom side of the PCB. The connection between capacitor pad and via must be cut for this measurement. For the final circuit, no vias can be present and all capacitors must be placed on the top layer.
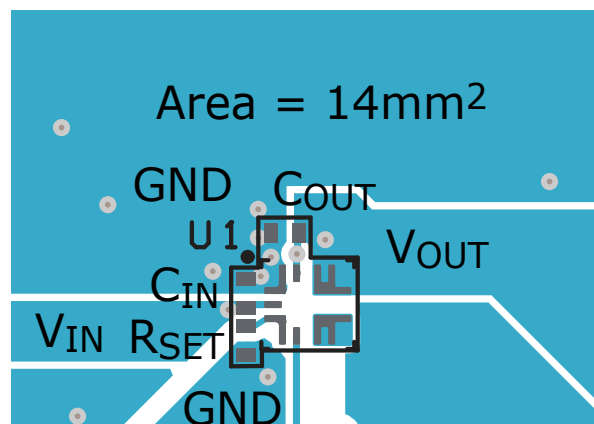
### 8.4.2 Layout Example



**Figure 8-34. Layout Example**

# 9 Device and Documentation Support

## 9.1 Device Support

### 9.1.1 Third-Party Products Disclaimer

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## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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## 9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

TI Glossary    This glossary lists and explains terms, acronyms, and definitions.

# 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision * (September 2024) to Revision A (November 2024)** — **Page**
- Changed document status from Advance Information to Production Data.........................................................1

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: *TPSM82843*

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPSM828436VCFR | Active | Production | QFN-FCMOD (VCF) \| 7 | 3000 \| LARGE T&R | Yes | Call TI | Call TI | -40 to 125 | 88436 |
| TPSM828436VCFR.A | Active | Production | QFN-FCMOD (VCF) \| 7 | 3000 \| LARGE T&R | Yes | Call TI | Call TI | -40 to 125 | 88436 |
| TPSM828437VCFR | Active | Production | QFN-FCMOD (VCF) \| 7 | 3000 \| LARGE T&R | Yes | Call TI | Call TI | -40 to 125 | 88437 |
| TPSM828437VCFR.A | Active | Production | QFN-FCMOD (VCF) \| 7 | 3000 \| LARGE T&R | Yes | Call TI | Call TI | -40 to 125 | 88437 |
| TPSM828438VCFR | Active | Production | QFN-FCMOD (VCF) \| 7 | 3000 \| LARGE T&R | Yes | Call TI | Call TI | -40 to 125 | 88438 |
| TPSM828438VCFR.A | Active | Production | QFN-FCMOD (VCF) \| 7 | 3000 \| LARGE T&R | Yes | Call TI | Call TI | -40 to 125 | 88438 |

**(1) Status:** For more details on status, see our product life cycle.

**(2) Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

**(3) RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
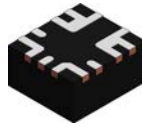
**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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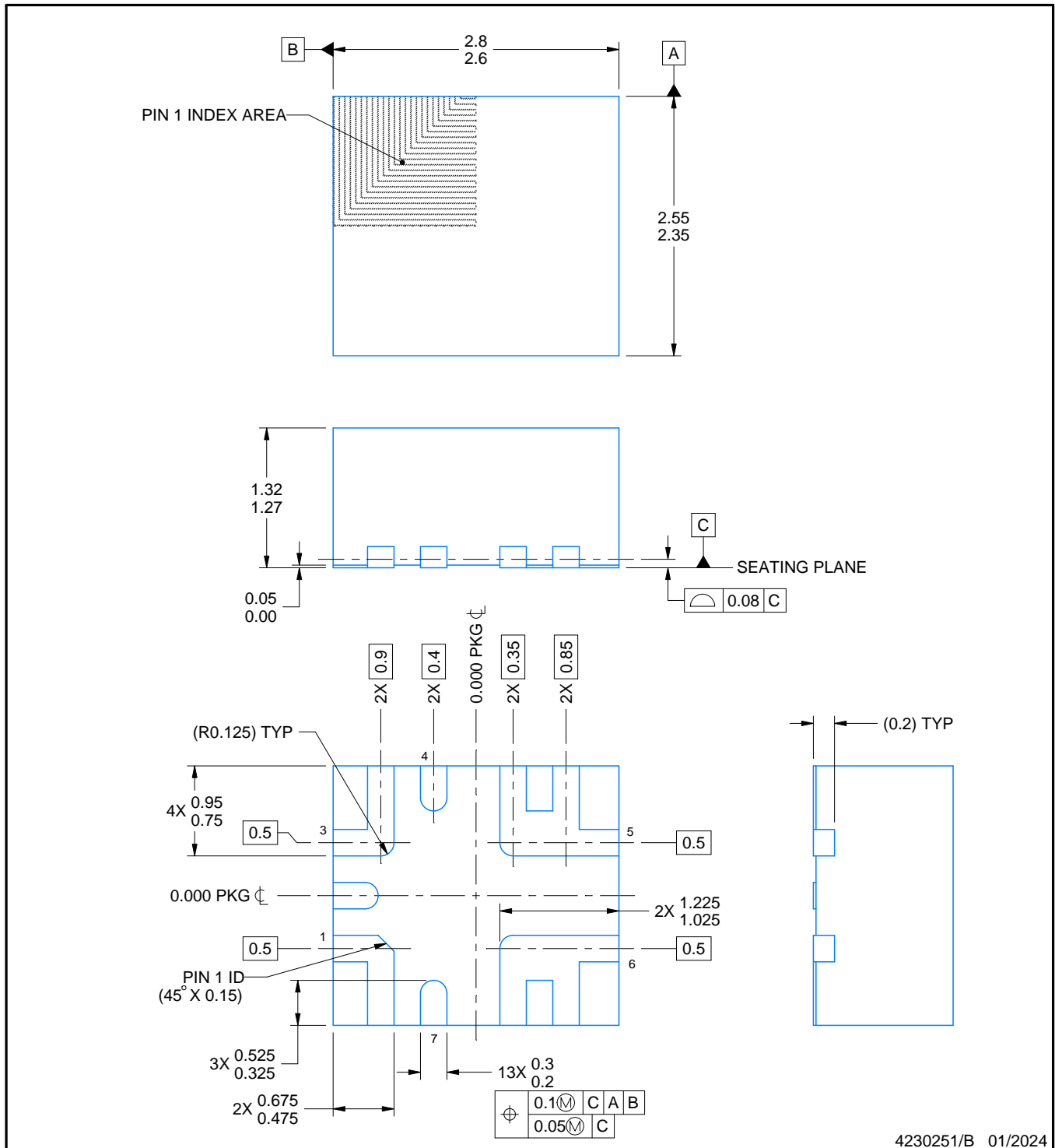
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

B | 2.8 / 2.6 | A

PIN 1 INDEX AREA

2.55 / 2.35

1.32 / 1.27

0.05 / 0.00

C

SEATING PLANE

0.08 | C

2X 0.9

2X 0.4

0.000 PKG ₵

2X 0.35

2X 0.85

(R0.125) TYP

(0.2) TYP

4X 0.95 / 0.75

0.5 | 3

4

0.5 | 5

0.000 PKG ₵

2X 1.225 / 1.025

0.5 | 1

0.5 | 6

PIN 1 ID
(45° X 0.15)

3X 0.525 / 0.325

7

13X 0.3 / 0.2

2X 0.675 / 0.475

⌖ | 0.1 Ⓜ | C | A | B
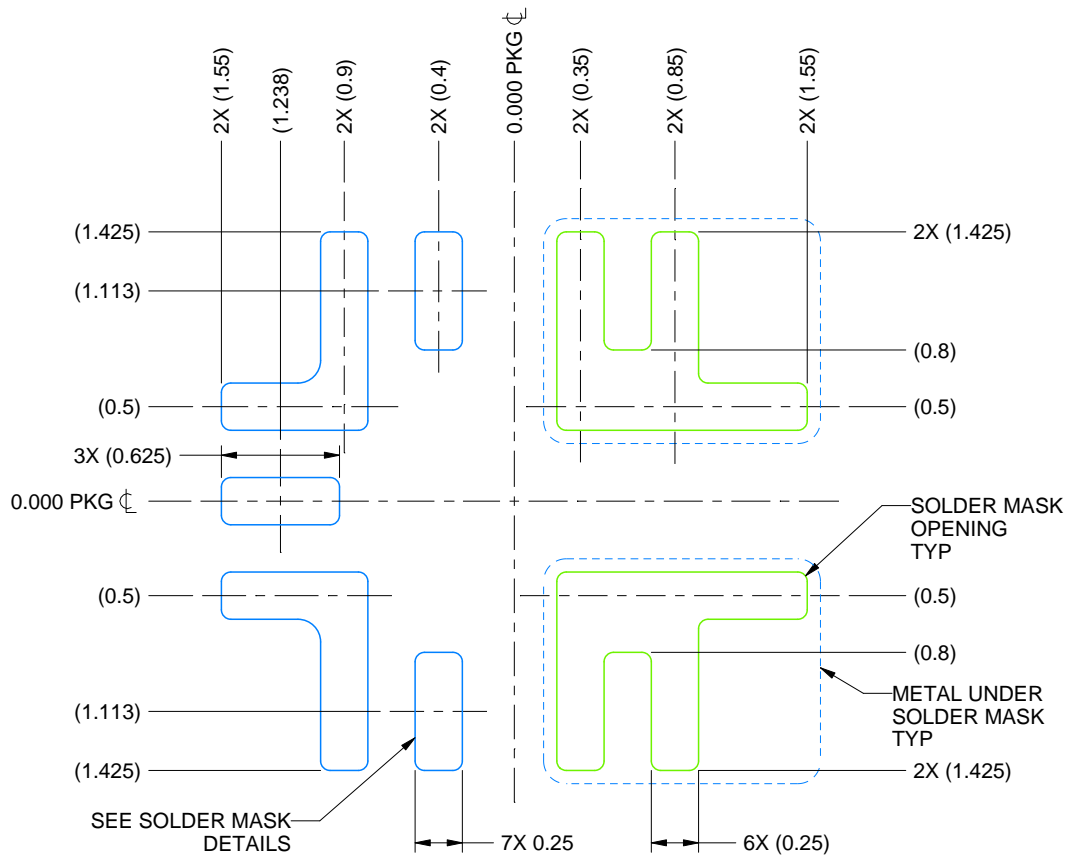| 0.05 Ⓜ | C

4230251/B   01/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

LAND PATTERN EXAMPLE
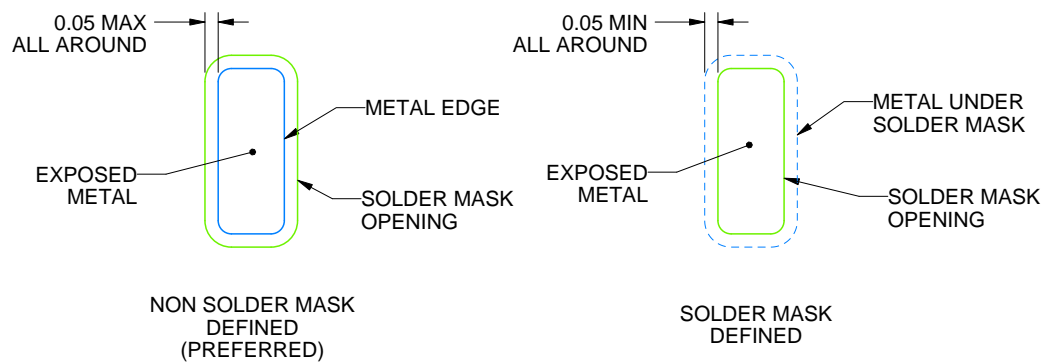SCALE: 25X

Dimensions and callouts in the land pattern:
- 2X (1.55)
- (1.238)
- 2X (0.9)
- 2X (0.4)
- 0.000 PKG ℄
- 2X (0.35)
- 2X (0.85)
- 2X (1.55)
- (1.425)
- (1.113)
- (0.5)
- 3X (0.625)
- 0.000 PKG ℄
- 2X (1.425)
- (0.8)
- (0.5)
- SOLDER MASK OPENING TYP
- METAL UNDER SOLDER MASK TYP
- 2X (1.425)
- SEE SOLDER MASK DETAILS
- 7X 0.25
- 6X (0.25)



SOLDER MASK DETAILS

Left detail:
- 0.05 MAX ALL AROUND
- METAL EDGE
- EXPOSED METAL
- SOLDER MASK OPENING
- NON SOLDER MASK DEFINED (PREFERRED)

Right detail:
- 0.05 MIN ALL AROUND
- METAL UNDER SOLDER MASK
- EXPOSED METAL
- SOLDER MASK OPENING
- SOLDER MASK DEFINED

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NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

2X (1.55)
(1.238)
2X (0.9)
2X (0.4)
0.000 PKG ℄
2X (0.35)
2X (0.85)
2X (1.55)

(1.425)

(1.113)

(0.5)

3X (0.625)

0.000 PKG ℄

(0.5)

(1.113)

(1.425)

2X (1.425)

(0.8)

(0.5)

METAL UNDER
SOLDER MASK
TYP

(0.5)

(0.8)

2X (1.425)

7X (0.25)

6X (0.25)
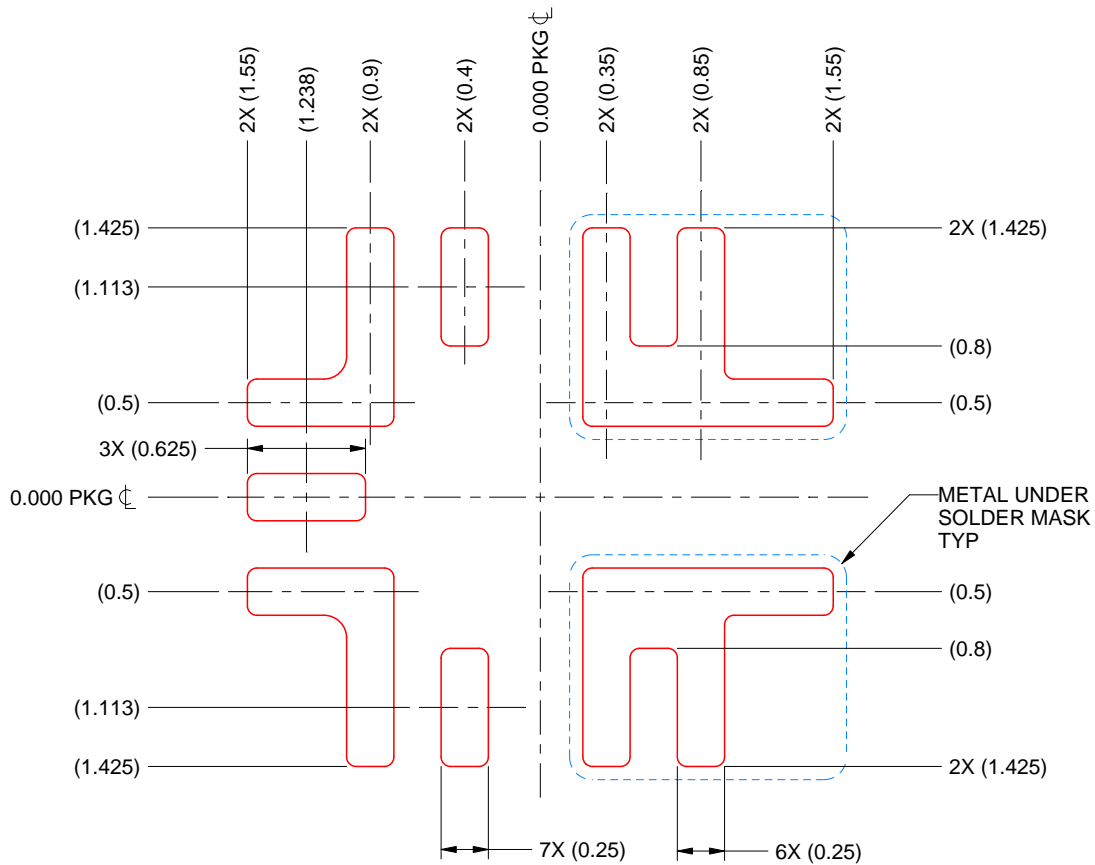
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE 25.000

4230251/B   01/2024

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.

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