

## TSV91x Rail-to-Rail Input/Output, 8-MHz Operational Amplifiers

### 1 Features

- Rail-to-rail input and output
- Low noise: 18 nV/ $\sqrt{\text{Hz}}$  at 1 kHz
- Low power consumption: 550  $\mu\text{A}$  (typical)
- High-gain bandwidth: 8 MHz
- Operating supply voltage from 2.5 V to 5.5 V
- Low input bias current: 1 pA (typical)
- Low input offset voltage: 1.5 mV (maximum)
- Low offset voltage drift:  $\pm 0.5 \mu\text{V}/^\circ\text{C}$  (typical)
- ESD internal protection:  $\pm 4\text{-kV}$  human-body model (HBM)
- Extended temperature range:  $-40^\circ\text{C}$  to  $125^\circ\text{C}$

### 2 Applications

- Battery-powered applications
- Motor control
- Power modules
- HVAC: heating, ventilating, and air conditioning
- Washing machines
- Refrigerators
- Medical instrumentation
- Active filters
- Sensor signal conditioning
- Audio receiver
- Automotive infotainment

### 3 Description

The TSV91x family, which includes single-, dual-, and quad-channel operational amplifiers (op amps), is specifically designed for general-purpose applications. Featuring rail-to-rail input and output (RRIO) swings, wide bandwidth (8 MHz), and low offset voltage (0.3 mV, typical), this family is designed for a variety of applications that require a good balance between speed and power consumption. The op amps are unity-gain stable and feature an ultra-low input bias current, which enables the family to be used in applications with high-source impedances. The low input bias current allows the devices to be used for sensor interfaces, battery-supplied and portable applications, and active filtering.

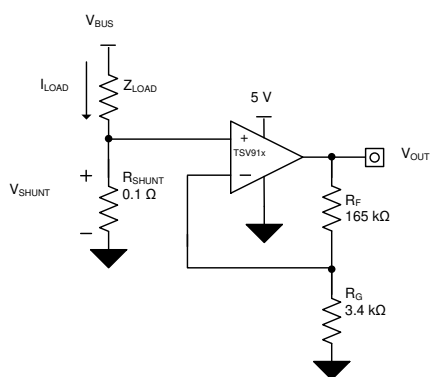
The robust design of the TSV91x provides ease-of-use to the circuit designer. Features include a unity-gain stable, integrated RFI-EMI rejection filter, no phase reversal in overdrive condition, and high electrostatic discharge (ESD) protection (4-kV HBV).

#### Device Information<sup>(1)</sup>

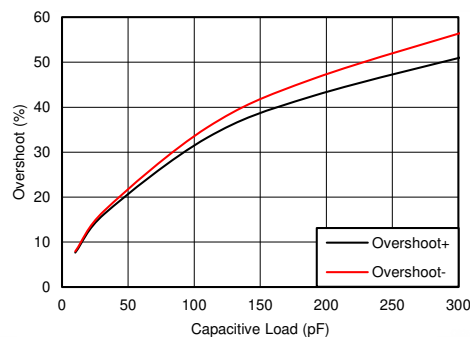
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TSV911	SOT-23 (5)	1.60 mm x 2.90 mm
	SC70 (5)	1.25 mm x 2.00 mm
TSV912	SOIC (8)	3.91 mm x 4.90 mm
	WSON (8)	2.00 mm x 2.00 mm
	SOT-23 (8)	1.60 mm x 2.90 mm
TSV914	SOIC (14)	8.65 mm x 3.91 mm
	TSSOP (14)	4.40 mm x 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Low-Side Motor Control



#### Small-Signal Overshoot vs Load Capacitance



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## 4 Revision History

Changes from Revision C (January 2019) to Revision D	Page
• Added SOT-23 (8) (DDF) package information to data sheet .....	1

Changes from Revision B (April 2018) to Revision C	Page
• Deleted preview notations for TSV911IDBV .....	1
• Added SC70 package information to <i>Device Information</i> table .....	1
• Deleted package preview notation from TSV911 DBV (SOT-23) package .....	4
• Added DCK (SC70) package information to <i>Device Comparison Table</i> .....	4
• Deleted TSV911 DBV (SOT-23) package preview notation from <i>Pin Configuration and Functions</i> section .....	5
• Added TSV911 DCK (SC70) package drawing and pin functions .....	5
• Added TSV911 DBV and DCK package thermal information .....	8

Changes from Revision A (October 2017) to Revision B	Page
• Changed TSV914 14-pin TSSOP package from preview to production data in <i>Device Information</i> table .....	1
• Deleted package preview note from 8-pin WSON package in <i>Device Information</i> table .....	1
• Deleted package preview note from PW (TSSOP) package from <i>Device Comparison</i> table .....	4
• Deleted package preview note from DSG (WSON) package from <i>Device Comparison</i> table .....	4
• Deleted package preview note from TSV912 DSG package pinout drawing in <i>Pin Configuration and Functions</i> section .....	6
• Added DGK (VSSOP) thermal information to <i>Thermal Information: TSV912</i> table .....	9
• Deleted package preview note to TSV914 PW (TSSOP) package <i>Thermal Information</i> table .....	9
• Added PW (TSSOP) package information to <i>Thermal Information: TSV914</i> table .....	9
• Changed TSV914 PW (TSSOP) junction-to-ambient thermal resistance from 135.8°C/W to 205.8°C/W .....	9
• Changed TSV914 PW (TSSOP) junction-to-case(top) thermal resistance from 64°C/W to 106.7°C/W .....	9
• Changed TSV914 PW (TSSOP) junction-to-board thermal resistance from 79°C/W to 133.9°C/W .....	9

- Changed TSV914 PW (TSSOP) junction-to-top characterization parameter from 15.7°C/W to 34.4°C/W ..... 9
  - Changed TSV914 PW (TSSOP) junction-to-board characterization parameter from 78.4°C/W to 132.6°C/W ..... 9
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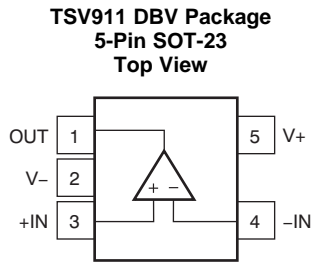
**Changes from Original (July 2017) to Revision A**
**Page**

- Changed TSV914 14-pin SOIC package from preview to production data in *Device Information* table ..... 1
  - Deleted TSV911 SC70, SOT-553 and SOIC packages from *Device Information* table ..... 1
  - Deleted TSV912 VSSOP packages from *Device Information* table ..... 1
  - Deleted TSV911 SC70 and SOIC packages from pinout drawings and *Pin Functions* table ..... 5
  - Deleted TSV912 DGK and DGS packages from pinout images *Pin Functions* table ..... 6
  - Deleted package preview note from TSV914 pinout drawing and *Pin Functions* table ..... 7
  - Added TSV914 *Thermal Information* table ..... 9
  - Added 2017 copyright notice to [Figure 35](#)..... 20
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## 5 Device Comparison Table

DEVICE	NO. OF CHANNELS	PACKAGE LEADS					
		DBV	DCK	D	DSG	PW	DDF
TSV911	1	5	5	—	—	—	—
TSV912	2	—	—	8	8	—	8
TSV914	4	—	—	14	—	14	—

## 6 Pin Configuration and Functions



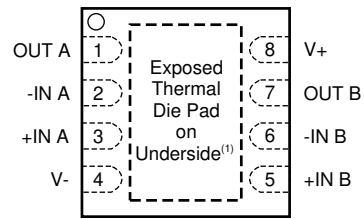
**Pin Functions: TSV911**

NAME	PIN NO.		I/O	DESCRIPTION
	DBV (SOT-23)	DCK (SC70)		
-IN	4	3	I	Inverting input
+IN	3	1	I	Noninverting input
OUT	1	4	O	Output
V-	2	2	—	Negative (lowest) supply or ground (for single-supply operation)
V+	5	5	—	Positive (highest) supply

**TSV912 D, DGK, DDF Packages  
8-Pin SOIC, VSSOP  
Top View**



**TSV912 DSG Package (1)  
8-Pin WSON With Exposed Thermal Pad  
Top View**

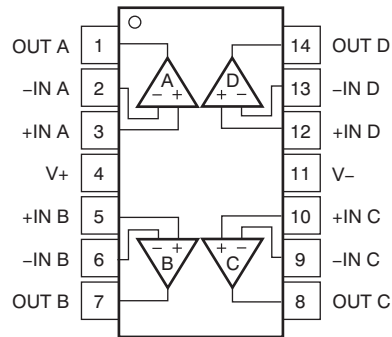


(1) Connect exposed thermal pad to V-. See [Packages with an Exposed Thermal Pad](#) section for more information.

**Pin Functions: TSV912**

PIN		I/O	DESCRIPTION
NAME	NO.		
-IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
-IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V-	4	—	Negative (lowest) supply or ground (for single-supply operation)
V+	8	—	Positive (highest) supply

**TSV914 D, PW Packages  
14-Pin SOIC, TSSOP  
Top View**



**Pin Functions: TSV914**

PIN		I/O	DESCRIPTION
NAME	NO.		
-IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
-IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
-IN C	9	I	Inverting input, channel C
+IN C	10	I	Noninverting input, channel C
-IN D	13	I	Inverting input, channel D
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V-	11	—	Negative (lowest) supply or ground (for single-supply operation)
V+	4	—	Positive (highest) supply

## 7 Specifications

### 7.1 Absolute Maximum Ratings

 over operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
Supply voltage				6	V
Signal input pins	Voltage <sup>(2)</sup>	Common-mode	(V <sup>-</sup> ) – 0.5	(V <sup>+</sup> ) + 0.5	V
		Differential	(V <sup>+</sup> ) – (V <sup>-</sup> ) + 0.2		
	Current <sup>(2)</sup>		–10	10	mA
Output short-circuit <sup>(3)</sup>			Continuous		mA
Specified, T <sub>A</sub>			–40	125	°C
Junction, T <sub>J</sub>				150	°C
Storage, T <sub>stg</sub>			–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.
- (3) Short-circuit to ground, one amplifier per package.

### 7.2 ESD Ratings

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>S</sub>	Supply voltage		2.5	5.5	V
	Specified temperature		–40	125	°C

### 7.4 Thermal Information: TSV911

THERMAL METRIC <sup>(1)</sup>		TSV911		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	221.7	263.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case(top) thermal resistance	144.7	75.5	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	49.7	51.0	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	26.1	1.0	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	49.0	50.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Thermal Information: TSV912

THERMAL METRIC <sup>(1)</sup>		TSV912				UNIT
		D (SOIC)	DGK (VSSOP)	DSG (WSON)	DDF (SOT-23)	
		8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	157.6	201.2	94.4	184.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	104.6	85.7	116.5	112.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	99.7	122.9	61.3	99.9	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	55.6	21.2	13	18.7	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	99.2	121.4	61.7	99.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	34.4	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.6 Thermal Information: TSV914

THERMAL METRIC <sup>(1)</sup>		TSV914		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106.9	205.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69	106.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63	133.9	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	25.9	34.4	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	62.7	132.6	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.7 Electrical Characteristics: $V_S$ (Total Supply Voltage) = $(V_+) - (V_-) = 2.5\text{ V to }5.5\text{ V}$

 at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>						
$V_{OS}$	Input offset voltage	$V_S = 5\text{ V}$		$\pm 0.3$	$\pm 1.5$	mV
		$V_S = 5\text{ V}$ $T_A = -40^\circ\text{C to }125^\circ\text{C}$			$\pm 3$	
$dV_{OS}/dT$	Drift	$V_S = 5\text{ V}$ $T_A = -40^\circ\text{C to }125^\circ\text{C}$		$\pm 0.5$		$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	$V_S = 2.5\text{ V} - 5.5\text{ V}$ , $V_{CM} = (V_-)$		$\pm 7$		$\mu\text{V/V}$
	Channel separation, DC	At DC		100		dB
<b>INPUT VOLTAGE RANGE</b>						
$V_{CM}$	Common-mode voltage range	$V_S = 2.5\text{ V to }5.5\text{ V}$	$(V_-) - 0.1$		$(V_+) + 0.1$	V
CMRR	Common-mode rejection ratio	$V_S = 5.5\text{ V}$ $(V_-) - 0.1\text{ V} < V_{CM} < (V_+) - 1.4\text{ V}$ $T_A = -40^\circ\text{C to }125^\circ\text{C}$	80	103		dB
		$V_S = 5.5\text{ V}$ , $V_{CM} = -0.1\text{ V to }5.6\text{ V}$ $T_A = -40^\circ\text{C to }125^\circ\text{C}$	57	87		
		$V_S = 2.5\text{ V}$ , $(V_-) - 0.1\text{ V} < V_{CM} < (V_+) - 1.4\text{ V}$ $T_A = -40^\circ\text{C to }125^\circ\text{C}$		88		
		$V_S = 2.5\text{ V}$ , $V_{CM} = -0.1\text{ V to }1.9\text{ V}$ $T_A = -40^\circ\text{C to }125^\circ\text{C}$		81		
<b>INPUT BIAS CURRENT</b>						
$I_B$	Input bias current			$\pm 1$		pA
$I_{OS}$	Input offset current			$\pm 0.05$		pA
<b>NOISE</b>						
$E_n$	Input voltage noise (peak-to-peak)	$V_S = 5\text{ V}$ , $f = 0.1\text{ Hz to }10\text{ Hz}$		4.77		$\mu\text{V}_{PP}$
$e_n$	Input voltage noise density	$V_S = 5\text{ V}$ , $f = 10\text{ kHz}$		12		$\text{nV}/\sqrt{\text{Hz}}$
		$V_S = 5\text{ V}$ , $f = 1\text{ kHz}$		18		
$i_n$	Input current noise density	$f = 1\text{ kHz}$		10		$\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT CAPACITANCE</b>						
$C_{ID}$	Differential			2		pF
$C_{IC}$	Common-mode			4		pF
<b>OPEN-LOOP GAIN</b>						
$A_{OL}$	Open-loop voltage gain	$V_S = 2.5\text{ V}$ , $(V_-) + 0.04\text{ V} < V_O < (V_+) - 0.04\text{ V}$ $R_L = 10\text{ k}\Omega$		100		dB
		$V_S = 5.5\text{ V}$ , $(V_-) + 0.05\text{ V} < V_O < (V_+) - 0.05\text{ V}$ $R_L = 10\text{ k}\Omega$	104	130		
		$V_S = 2.5\text{ V}$ , $(V_-) + 0.06\text{ V} < V_O < (V_+) - 0.06\text{ V}$ $R_L = 2\text{ k}\Omega$		100		
		$V_S = 5.5\text{ V}$ , $(V_-) + 0.15\text{ V} < V_O < (V_+) - 0.15\text{ V}$ $R_L = 2\text{ k}\Omega$		130		
<b>FREQUENCY RESPONSE</b>						
GBP	Gain bandwidth product	$V_S = 5\text{ V}$ , $G = 1$		8		MHz
$\phi_m$	Phase margin	$V_S = 5\text{ V}$ , $G = 1$		55		°
SR	Slew rate	$V_S = 5\text{ V}$ , $G = 1$ $R_L = 2\text{ k}\Omega$ $C_L = 100\text{ pF}$		4.5		V/ $\mu\text{s}$
$t_s$	Settling time	To 0.1%, $V_S = 5\text{ V}$ , 2-V step, $G = 1$ $C_L = 100\text{ pF}$		0.5		$\mu\text{s}$
		To 0.01%, $V_S = 5\text{ V}$ , 2-V step, $G = 1$ $C_L = 100\text{ pF}$		1		
$t_{OR}$	Overload recovery time	$V_S = 5\text{ V}$ , $V_{IN} \times \text{gain} > V_S$		0.2		$\mu\text{s}$
THD + N	Total harmonic distortion + noise <sup>(1)</sup>	$V_S = 5\text{ V}$ , $V_O = 1\text{ V}_{RMS}$ , $G = 1$ , $f = 1\text{ kHz}$		0.0008%		
<b>OUTPUT</b>						
$V_O$	Voltage output swing from supply rails	$V_S = 5.5\text{ V}$ , $R_L = 10\text{ k}\Omega$			15	mV
		$V_S = 5.5\text{ V}$ , $R_L = 2\text{ k}\Omega$			50	

(1) Third-order filter; bandwidth = 80 kHz at -3 dB.

**Electrical Characteristics:  $V_S$  (Total Supply Voltage) = (V+) – (V–) = 2.5 V to 5.5 V (continued)**

 at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{SC}$	Short-circuit current	$V_S = 5\text{ V}$		$\pm 50$		mA
$Z_O$	Open-loop output impedance	$V_S = 5\text{ V}$ , $f = 10\text{ MHz}$		100		$\Omega$
<b>POWER SUPPLY</b>						
$I_Q$	Quiescent current per amplifier	$V_S = 5.5\text{ V}$ , $I_O = 0\text{ mA}$		550	750	$\mu\text{A}$
		$V_S = 5.5\text{ V}$ , $I_O = 0\text{ mA}$ , $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$			1100	

## 7.8 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)

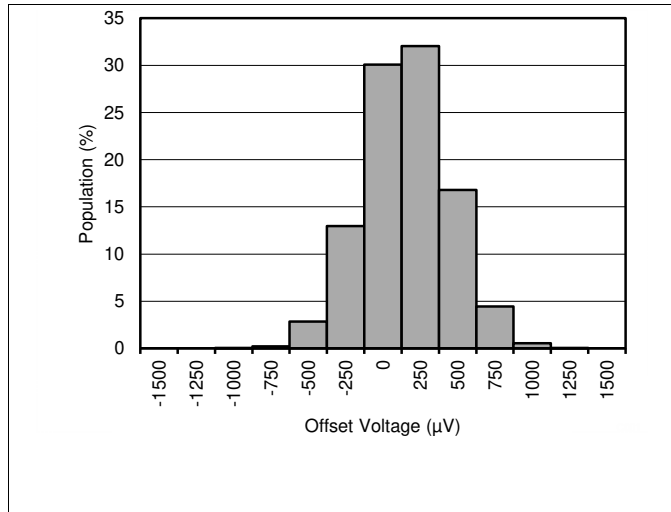


Figure 1. Offset Voltage Production Distribution

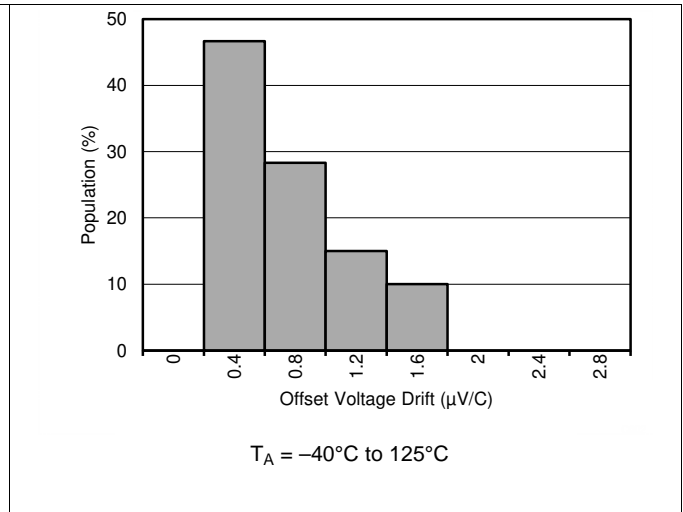


Figure 2. Offset Voltage Drift Distribution

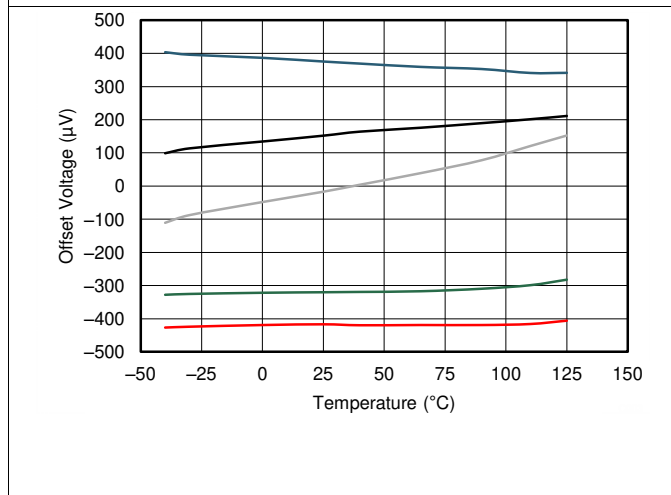


Figure 3. Offset Voltage vs Temperature

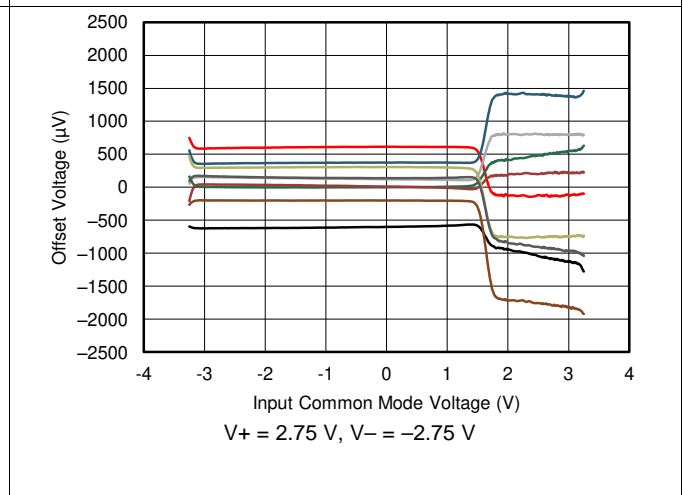


Figure 4. Offset Voltage vs Common-Mode Voltage

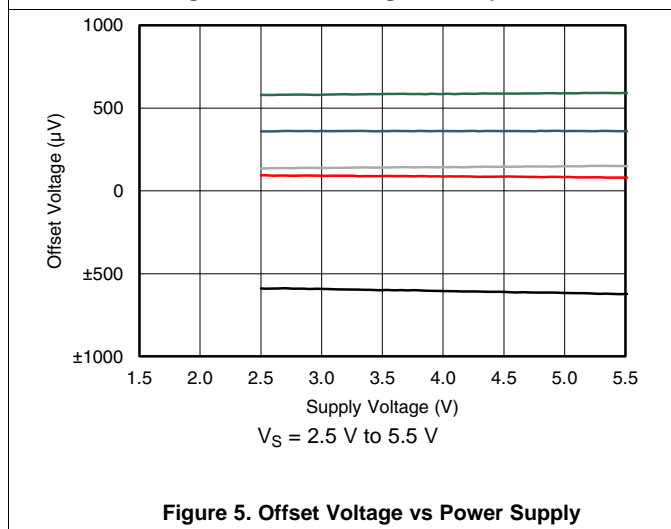


Figure 5. Offset Voltage vs Power Supply

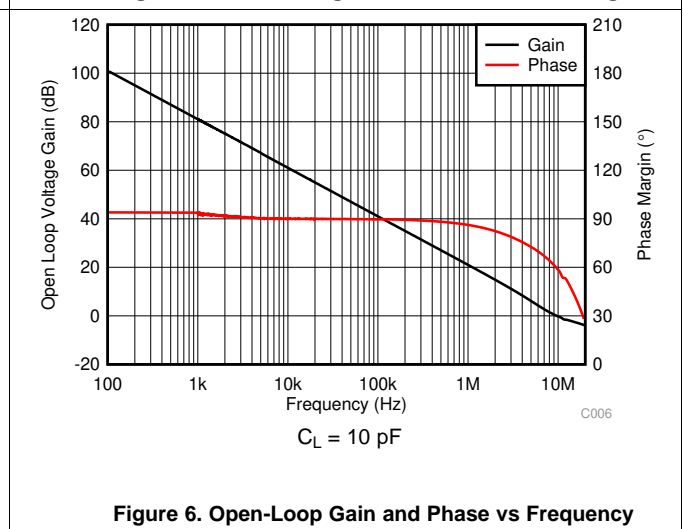


Figure 6. Open-Loop Gain and Phase vs Frequency

Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)

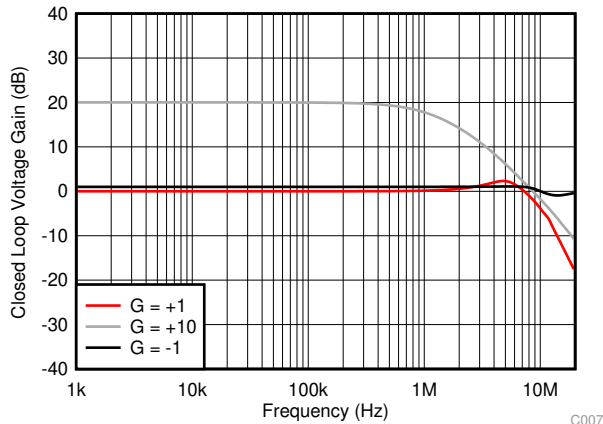


Figure 7. Closed-Loop Gain vs Frequency

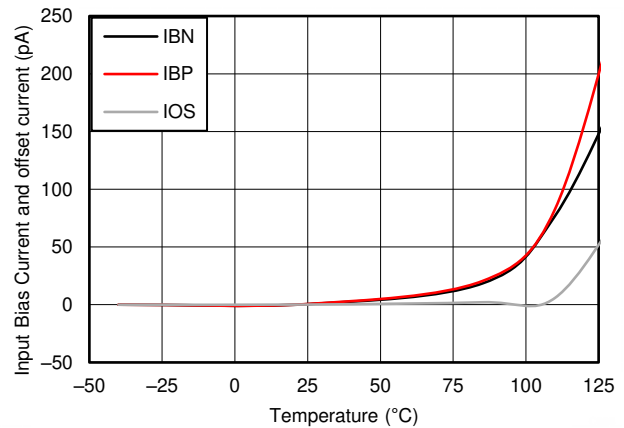


Figure 8. Input Bias Current vs Temperature

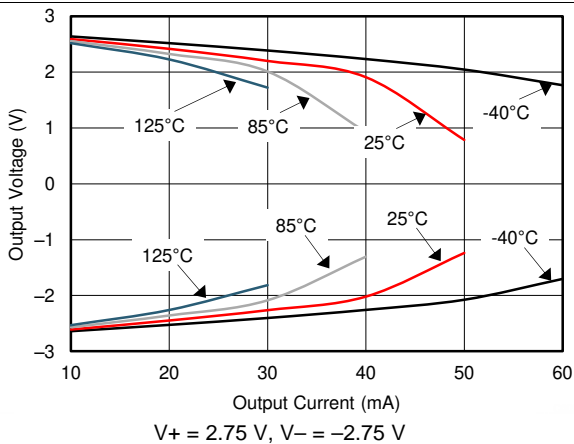


Figure 9. Output Voltage Swing vs Output Current

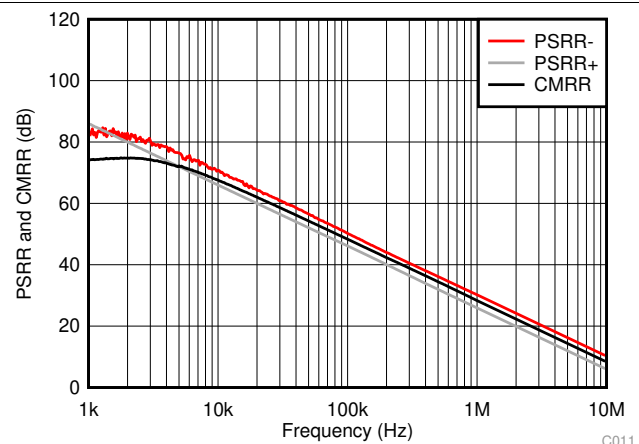


Figure 10. CMRR and PSRR vs Frequency (Referred to Input)

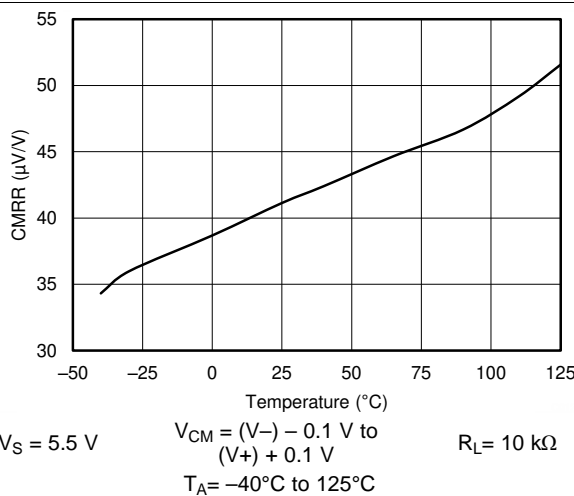


Figure 11. CMRR vs Temperature

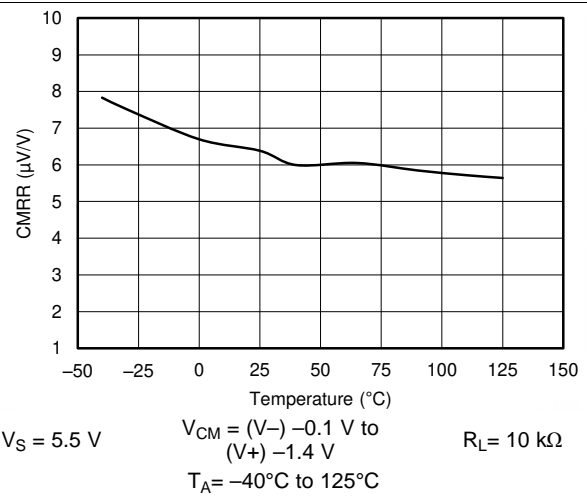


Figure 12. CMRR vs Temperature

### Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)



Figure 13. PSRR vs Temperature

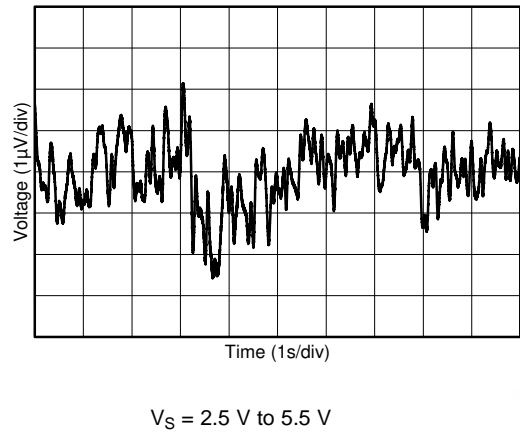


Figure 14. 0.1-Hz to 10-Hz Input Voltage Noise

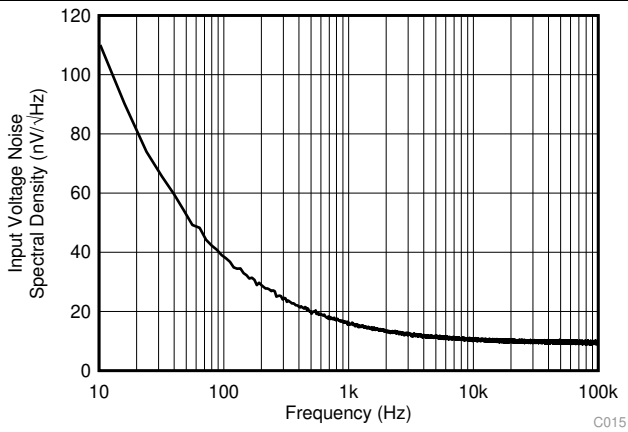


Figure 15. Input Voltage Noise Spectral Density vs Frequency

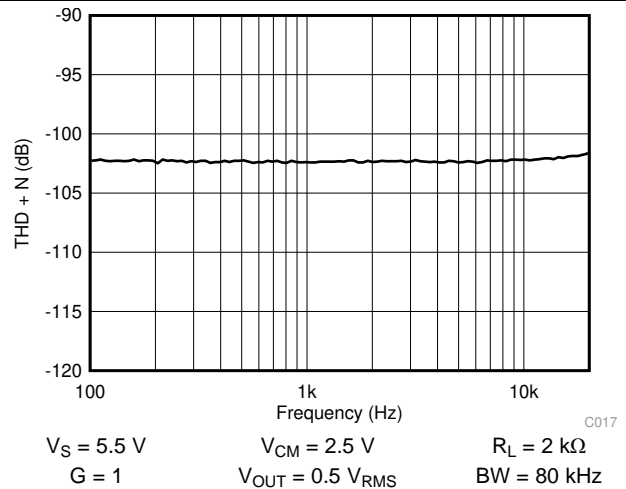


Figure 16. THD + N vs Frequency

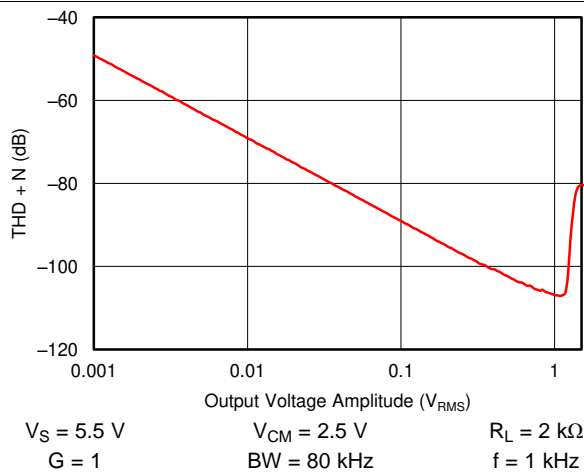


Figure 17. THD + N vs Amplitude

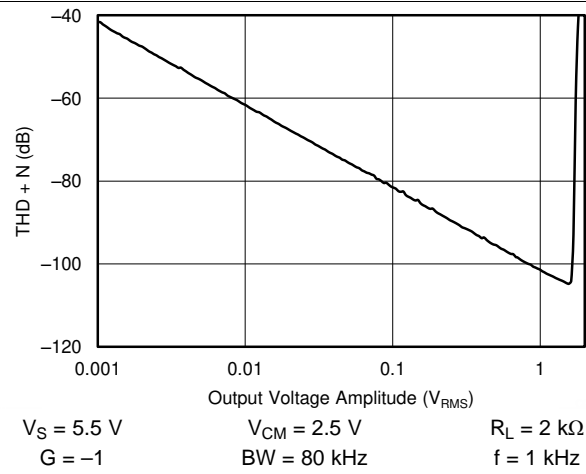
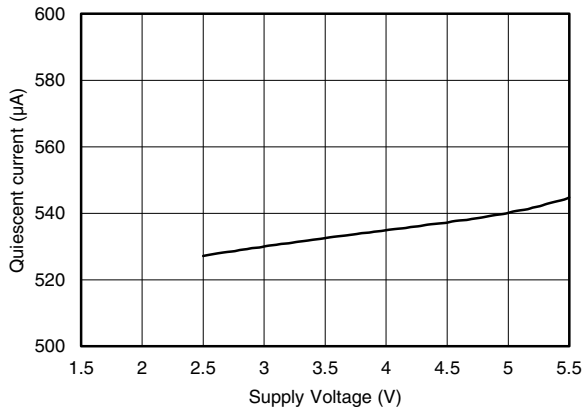


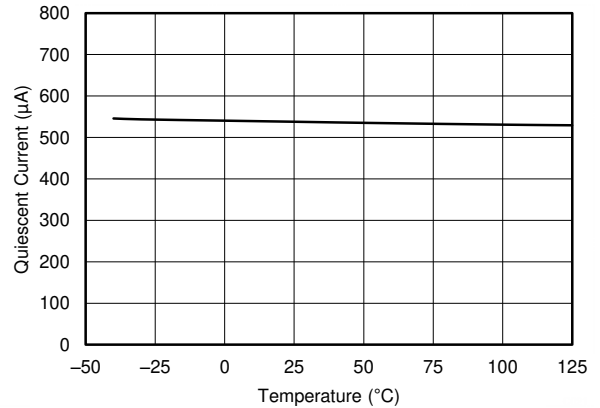
Figure 18. THD + N vs Amplitude

**Typical Characteristics (continued)**

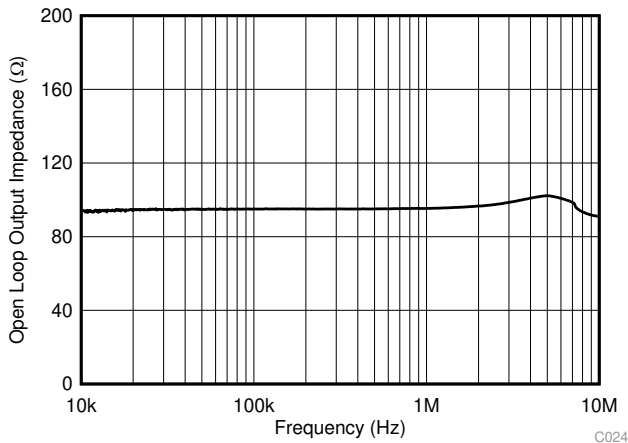
at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)



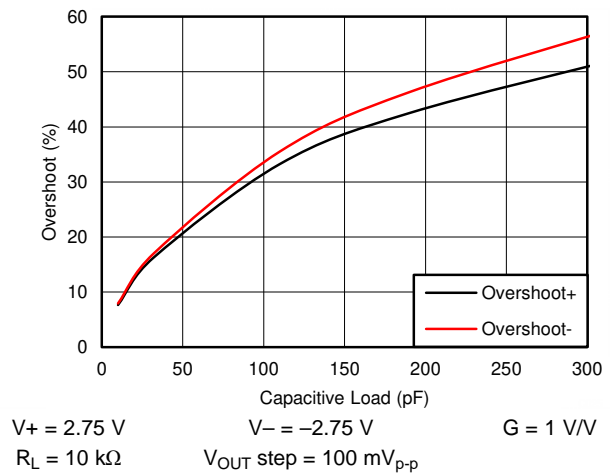
**Figure 19. Quiescent Current vs Supply Voltage**



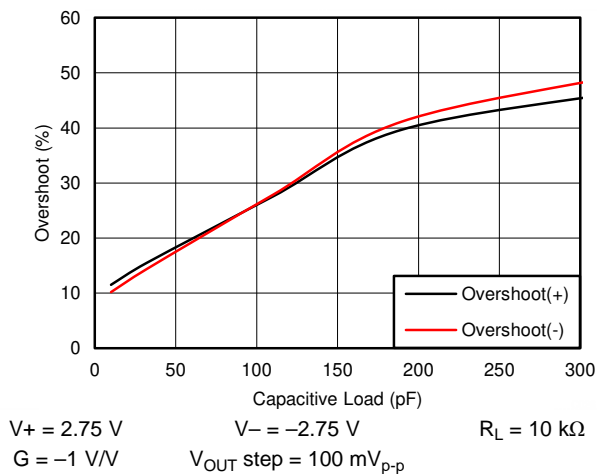
**Figure 20. Quiescent Current vs Temperature**



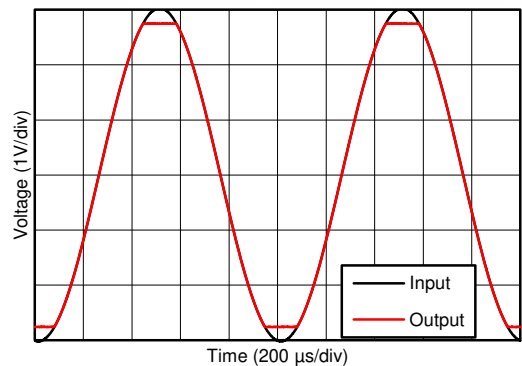
**Figure 21. Open-Loop Output Impedance vs Frequency**



**Figure 22. Small-Signal Overshoot vs Load Capacitance**



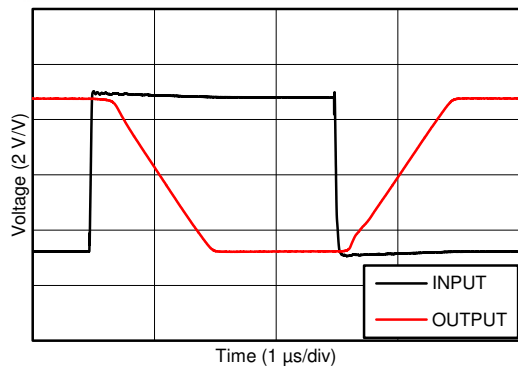
**Figure 23. Small-Signal Overshoot vs Load Capacitance**



**Figure 24. No Phase Reversal**

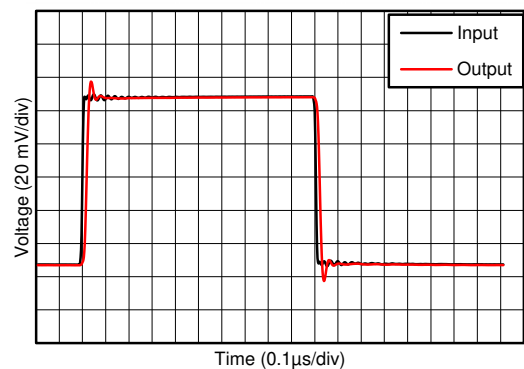
### Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)



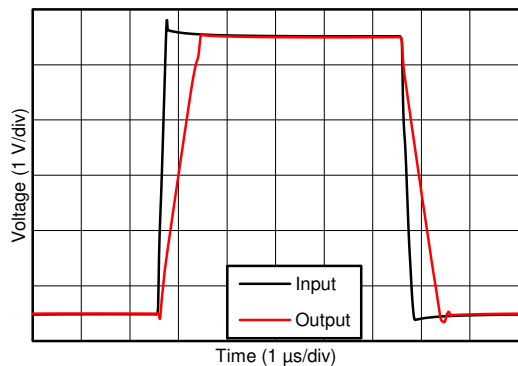
$V_+ = 2.75\text{ V}$ ,  $V_- = -2.75\text{ V}$ ,  $G = -10\text{ V/V}$

Figure 25. Overload Recovery



$V_+ = 2.75\text{ V}$ ,  $V_- = -2.75\text{ V}$ ,  $G = 1\text{ V/V}$

Figure 26. Small-Signal Step Response



$V_+ = 2.75\text{ V}$        $V_- = -2.75\text{ V}$        $C_L = 100\text{ pF}$   
 $G = 1\text{ V/V}$

Figure 27. Large-Signal Step Response

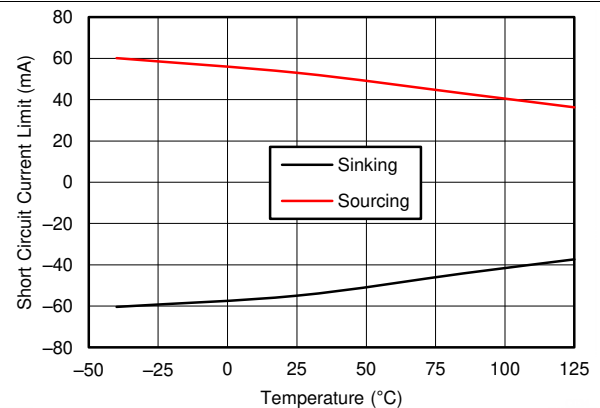


Figure 28. Short-Circuit Current vs Temperature

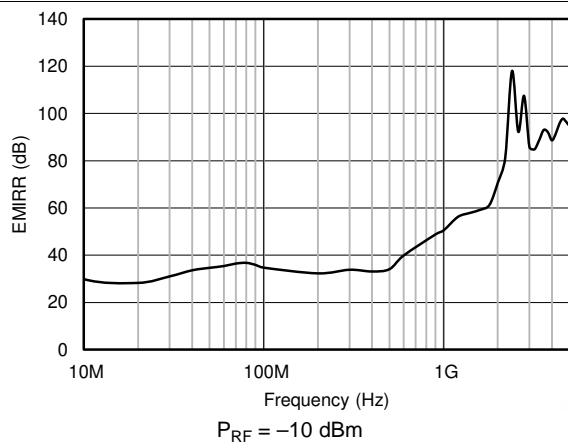


Figure 29. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

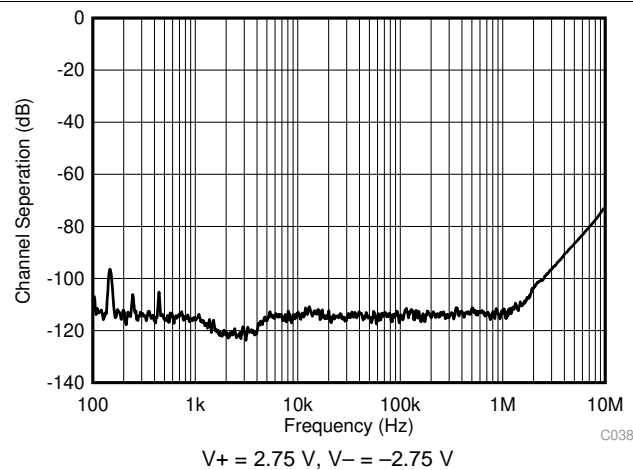
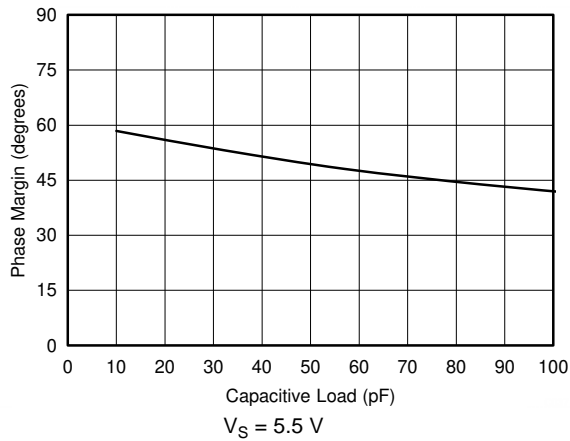


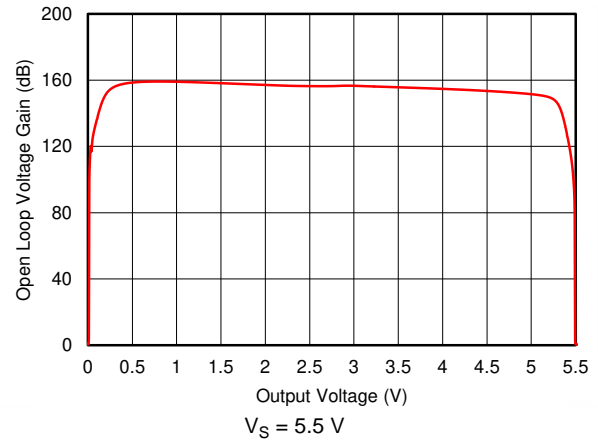
Figure 30. Channel Separation vs Frequency

**Typical Characteristics (continued)**

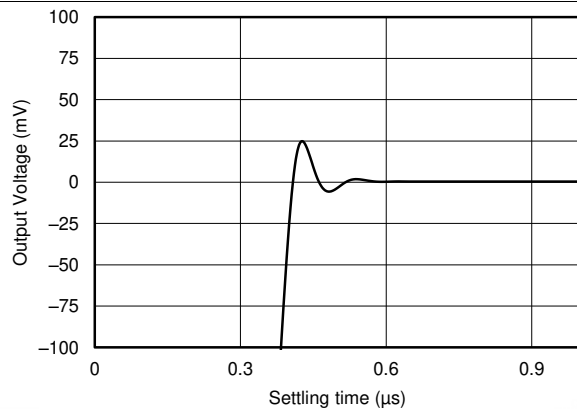
at  $T_A = 25^\circ\text{C}$ ,  $V_S = 5.5\text{ V}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)



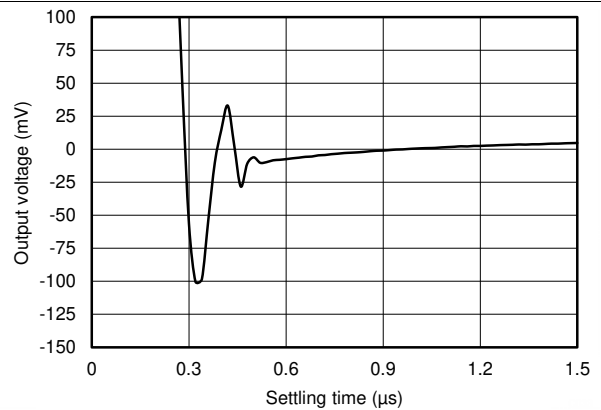
**Figure 31. Phase Margin vs Capacitive Load**



**Figure 32. Open Loop Voltage Gain vs Output Voltage**



**Figure 33. Large Signal Settling Time (Positive)**



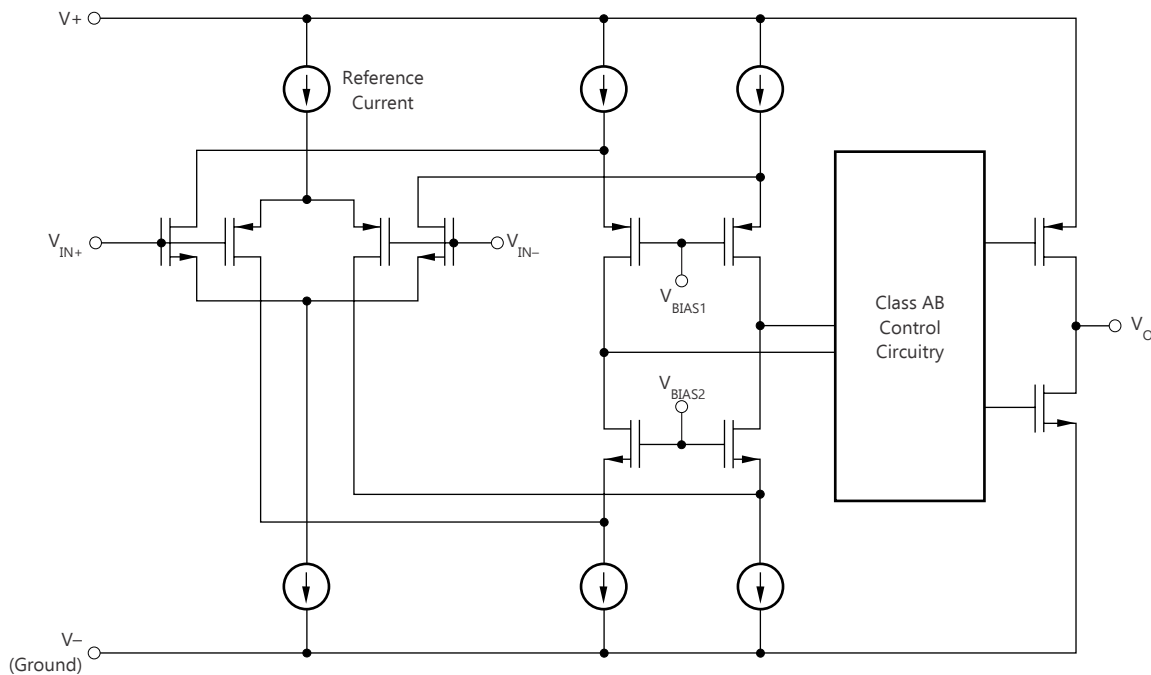
**Figure 34. Large Signal Settling Time (Negative)**

## 8 Detailed Description

### 8.1 Overview

The TSV91x series is a family of low-power, rail-to-rail input and output op amps. These devices operate from 2.5 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the TSV91x series to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications and are designed for driving sampling analog-to-digital converters (ADCs).

### 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Rail-to-Rail Input

The input common-mode voltage range of the TSV91x family extends 100 mV beyond the supply rails for the full supply voltage range of 2.5 V to 5.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the [Functional Block Diagram](#). The N-channel pair is active for input voltages close to the positive rail, typically  $(V+) - 1.4$  V to 100 mV above the positive supply, whereas the P-channel pair is active for inputs from 100 mV below the negative supply to approximately  $(V+) - 1.4$  V. There is a small transition region, typically  $(V+) - 1.2$  V to  $(V+) - 1$  V, in which both pairs are on. This 200-mV transition region can vary up to 200 mV with process variation. Thus, the transition region (with both stages on) can range from  $(V+) - 1.4$  V to  $(V+) - 1.2$  V on the low end, and up to  $(V+) - 1$  V to  $(V+) - 0.8$  V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

### 8.3.2 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the TSV91x series delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10 k $\Omega$ , the output swings to within 15 mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

### 8.3.3 Packages with an Exposed Thermal Pad

The TSV91x family is available in packages such as the WSON-8 (DSG) which feature an exposed thermal pad. Inside the package, the die is attached to this thermal pad using an electrically conductive compound. For this reason, when using a package with an exposed thermal pad, the thermal pad must either be connected to  $V-$  or left floating. Attaching the thermal pad to a potential other than  $V-$  is not allowed, and the performance of the device is not assured when doing so.

### 8.3.4 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TSV91x series is approximately 200 ns.

## 8.4 Device Functional Modes

The TSV91x family has a single functional mode. These devices are powered on as long as the power-supply voltage is between 2.5 V ( $\pm 1.25$  V) and 5.5 V ( $\pm 2.75$  V).

## 9 Application and Implementation

### NOTE

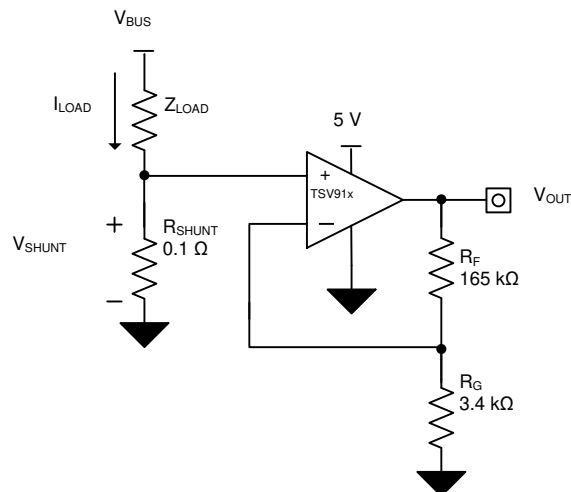
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TSV91x series features 8-MHz bandwidth and 4.5-V/ $\mu$ s slew rate with only 550  $\mu$ A of supply current per channel, providing good AC performance at low power consumption. DC applications are well served with a low input noise voltage of 18 nV /  $\sqrt{\text{Hz}}$  at 1 kHz, low input bias current, and a typical input offset voltage of 0.3 mV.

### 9.2 Typical Application

Figure 35 shows the TSV91x configured in a low-side, motor-control application.



**Figure 35. TSV91x in a Low-Side, Motor-Control Application**

#### 9.2.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.95 V
- Maximum shunt voltage: 100 mV

## Typical Application (continued)

### 9.2.2 Detailed Design Procedure

The transfer function of the circuit in [Figure 35](#) is shown in [Equation 1](#).

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times \text{Gain} \quad (1)$$

The load current ( $I_{LOAD}$ ) produces a voltage drop across the shunt resistor ( $R_{SHUNT}$ ). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using [Equation 2](#).

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100\text{mV}}{1\text{A}} = 100\text{m}\Omega \quad (2)$$

Using [Equation 2](#),  $R_{SHUNT}$  is 100 m $\Omega$ . The voltage drop produced by  $I_{LOAD}$  and  $R_{SHUNT}$  is amplified by the TSV91x to produce an output voltage of approximately 0 V to 4.95 V. The gain required by the TSV91x to produce the necessary output voltage is calculated using [Equation 3](#):

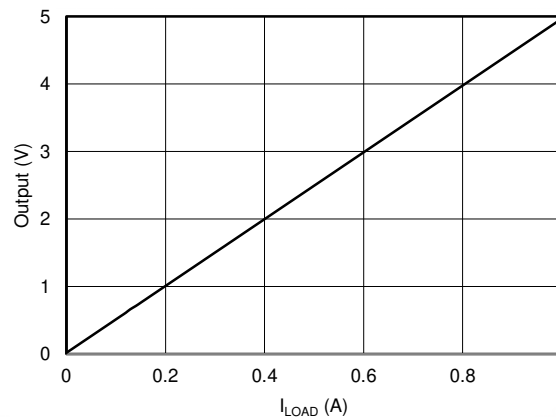
$$\text{Gain} = \frac{(V_{OUT\_MAX} - V_{OUT\_MIN})}{(V_{IN\_MAX} - V_{IN\_MIN})} \quad (3)$$

Using [Equation 3](#), the required gain is calculated to be 49.5 V/V, which is set with resistors  $R_F$  and  $R_G$ . [Equation 4](#) is used to size the resistors,  $R_F$  and  $R_G$ , to set the gain of the TSV91x to 49.5 V/V.

$$\text{Gain} = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

Selecting  $R_F$  as 165 k $\Omega$  and  $R_G$  as 3.4 k $\Omega$  provides a combination that equals roughly 49.5 V/V. [Figure 36](#) shows the measured transfer function of the circuit shown in [Figure 35](#).

### 9.2.3 Application Curve



**Figure 36. Low-Side, Current-Sense, Transfer Function**

## 10 Power Supply Recommendations

The TSV91x series is specified for operation from 2.5 V to 5.5 V ( $\pm 1.25$  V to  $\pm 2.75$  V); many specifications apply from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The [Typical Characteristics](#) section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

### CAUTION

Supply voltages larger than 6 V can permanently damage the device; see the [Absolute Maximum Ratings](#) table.

Place 0.1- $\mu\text{F}$  bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the [Layout Example](#) section.

### 10.1 Input and ESD Protection

The TSV91x series incorporates internal ESD protection circuits on all pins. For input and output pins, this protection consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10-mA, as stated in the [Absolute Maximum Ratings](#) table. [Figure 37](#) shows how a series input resistor is added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.



**Figure 37. Input Current Protection**

## 11 Layout

### 11.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see [Circuit Board Layout Techniques](#).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in [Figure 39](#), keeping RF and RG close to the inverting input minimizes parasitic capacitance on the inverting input.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

### 11.2 Layout Example



Figure 38. Schematic Representation for [Figure 39](#)

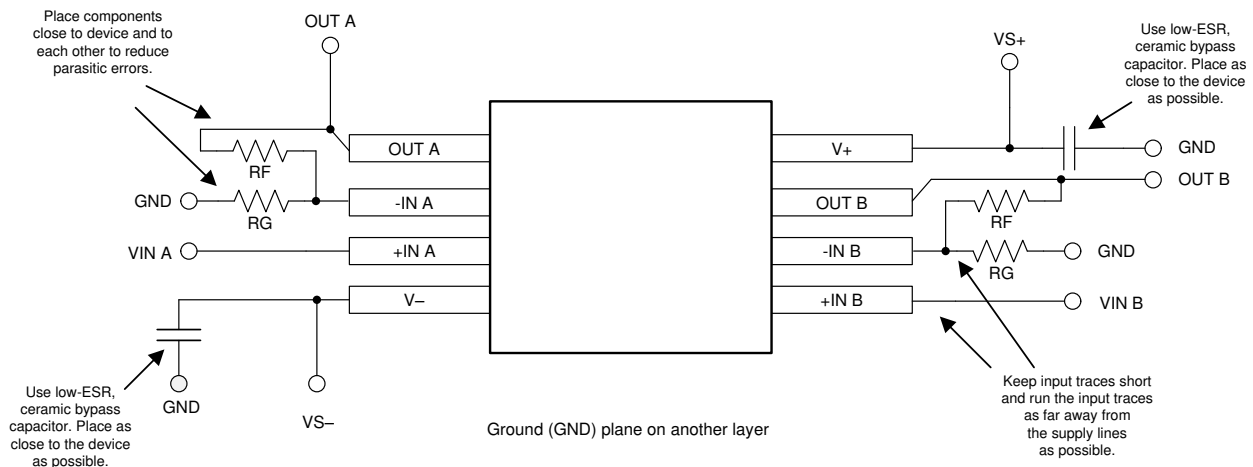


Figure 39. Layout Example

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

Texas Instruments, [Circuit Board Layout Techniques](#), SLOA089

### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

**Table 1. Related Links**

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TSV911	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TSV912	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TSV914	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.4 Community Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 12.5 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TSV911AIDBVR</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	1U2F
TSV911AIDBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1U2F
TSV911AIDBVRG4	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1U2F
TSV911AIDBVRG4.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1U2F
<a href="#">TSV911AIDCKR</a>	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1EK
TSV911AIDCKR.A	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1EK
<a href="#">TSV912AIDDFR</a>	Active	Production	SOT-23-THIN (DDF)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T12A
TSV912AIDDFR.A	Active	Production	SOT-23-THIN (DDF)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T12A
TSV912AIDDFRG4	Active	Production	SOT-23-THIN (DDF)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T12A
TSV912AIDDFRG4.A	Active	Production	SOT-23-THIN (DDF)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T12A
<a href="#">TSV912AIDGKR</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU   SN   NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	T912
TSV912AIDGKR.A	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T912
<a href="#">TSV912AIDGKT</a>	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU   SN   NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	T912
TSV912AIDGKT.A	Active	Production	VSSOP (DGK)   8	250   SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T912
<a href="#">TSV912AIDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TSV912
TSV912AIDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TSV912
TSV912AIDRG4	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TSV912
TSV912AIDRG4.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TSV912
<a href="#">TSV912AIDSGR</a>	Active	Production	WSON (DSG)   8	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T912
TSV912AIDSGR.A	Active	Production	WSON (DSG)   8	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T912
<a href="#">TSV912AIDSGT</a>	Active	Production	WSON (DSG)   8	250   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T912
TSV912AIDSGT.A	Active	Production	WSON (DSG)   8	250   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	T912
<a href="#">TSV912AIPWR</a>	Active	Production	TSSOP (PW)   8	2000   LARGE T&R	Yes	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	TSV912
TSV912AIPWR.A	Active	Production	TSSOP (PW)   8	2000   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TSV912
<a href="#">TSV914AIDR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TSV914AD
TSV914AIDR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TSV914AD
TSV914AIDRG4	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TSV914AD
TSV914AIDRG4.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TSV914AD

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TSV914AIPWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	TSV914
TSV914AIPWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TSV914
<a href="#">TSV914AIPWT</a>	Active	Production	TSSOP (PW)   14	250   SMALL T&R	Yes	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	TSV914
TSV914AIPWT.A	Active	Production	TSSOP (PW)   14	250   SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	TSV914

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

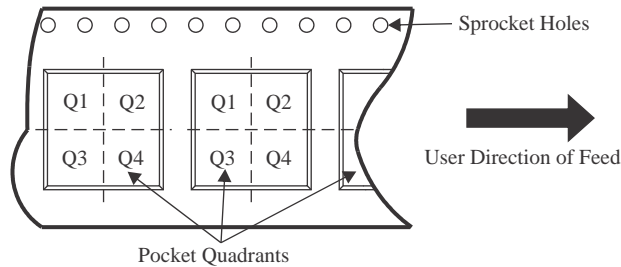
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSV911AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TSV911AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TSV911AIDBVRG4	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TSV911AIDCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
TSV912AIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TSV912AIDDFRG4	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TSV912AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TSV912AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TSV912AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TSV912AIDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TSV912AIDSGR	WSO	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TSV912AIDSGT	WSO	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TSV912AIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TSV914AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TSV914AIDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSV914AIDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
TSV914AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TSV914AIPWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSV911AIDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TSV911AIDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TSV911AIDBVRG4	SOT-23	DBV	5	3000	210.0	185.0	35.0
TSV911AIDCKR	SC70	DCK	5	3000	210.0	185.0	35.0
TSV912AIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TSV912AIDDFRG4	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TSV912AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TSV912AIDGKT	VSSOP	DGK	8	250	353.0	353.0	32.0
TSV912AIDR	SOIC	D	8	2500	353.0	353.0	32.0
TSV912AIDRG4	SOIC	D	8	2500	353.0	353.0	32.0
TSV912AIDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TSV912AIDSGT	WSON	DSG	8	250	210.0	185.0	35.0
TSV912AIPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TSV914AIDR	SOIC	D	14	2500	353.0	353.0	32.0
TSV914AIDRG4	SOIC	D	14	2500	353.0	353.0	32.0
TSV914AIDRG4	SOIC	D	14	2500	356.0	356.0	36.0
TSV914AIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TSV914AIPWT	TSSOP	PW	14	250	353.0	353.0	32.0

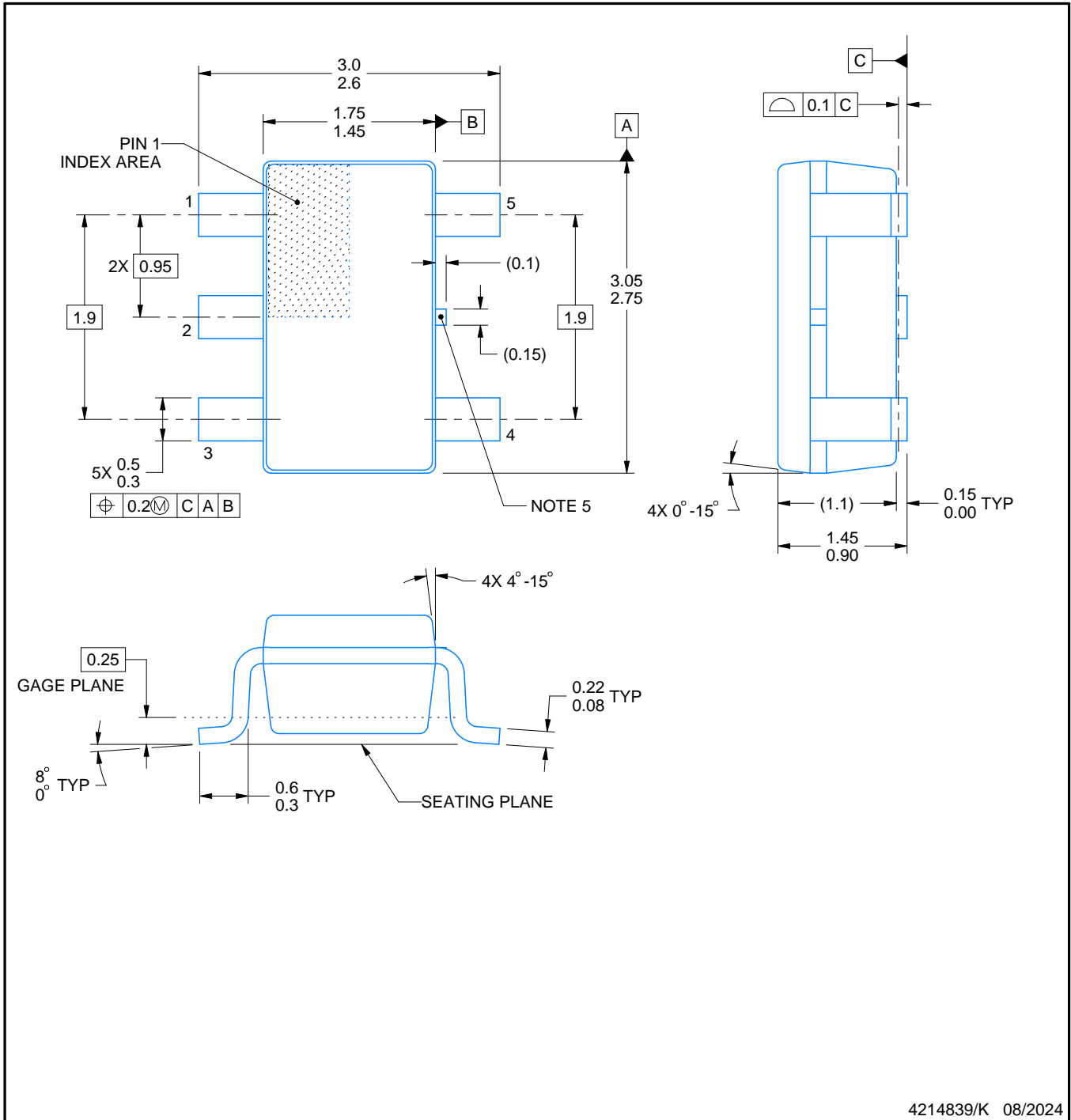


DBV0005A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. Reference JEDEC MO-178.
- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



# D0014A

# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

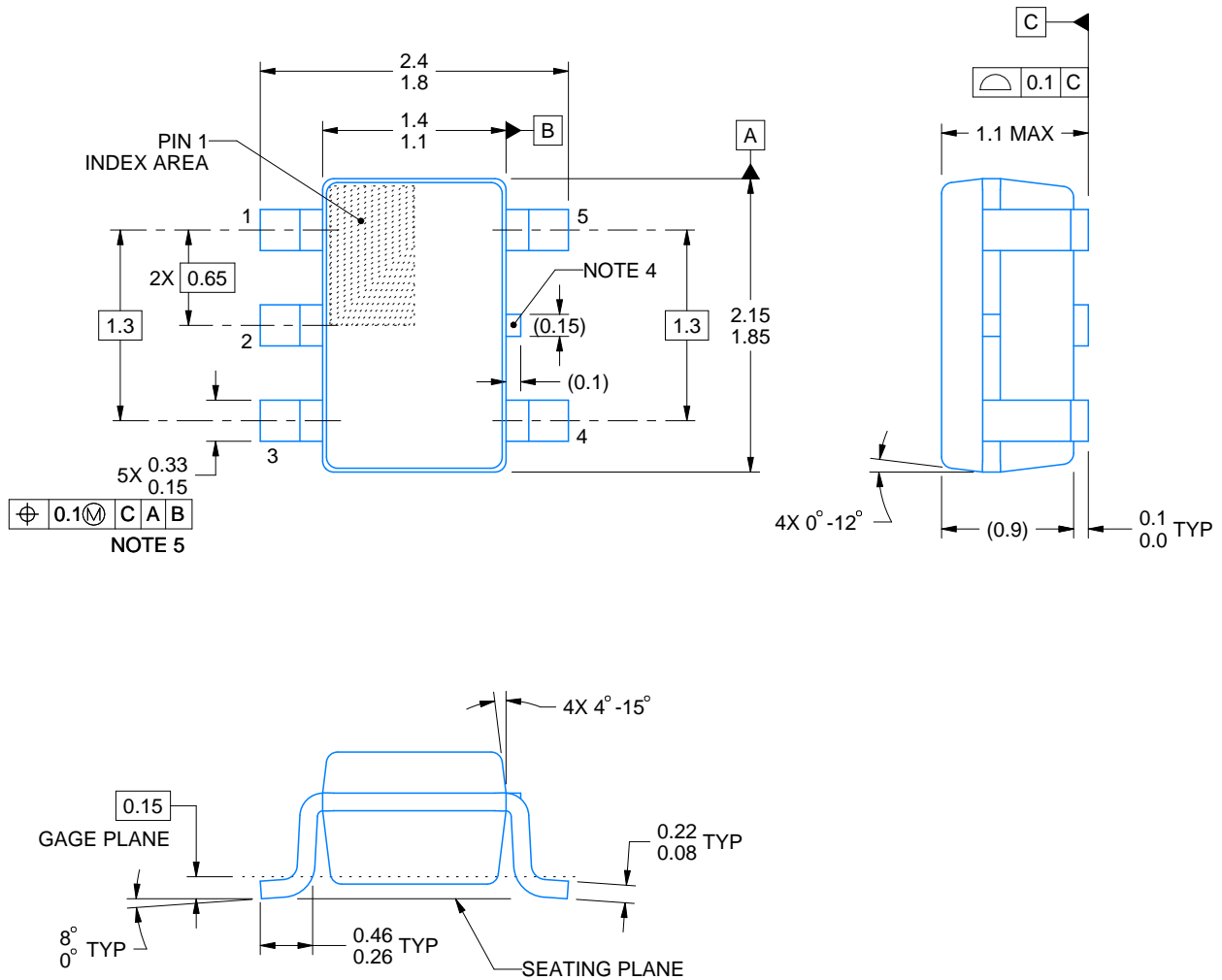
# DCK0005A



## PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/G 11/2024

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

# EXAMPLE BOARD LAYOUT

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE: 18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

# DDF0008A



# PACKAGE OUTLINE

## SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



4222047/E 07/2024

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

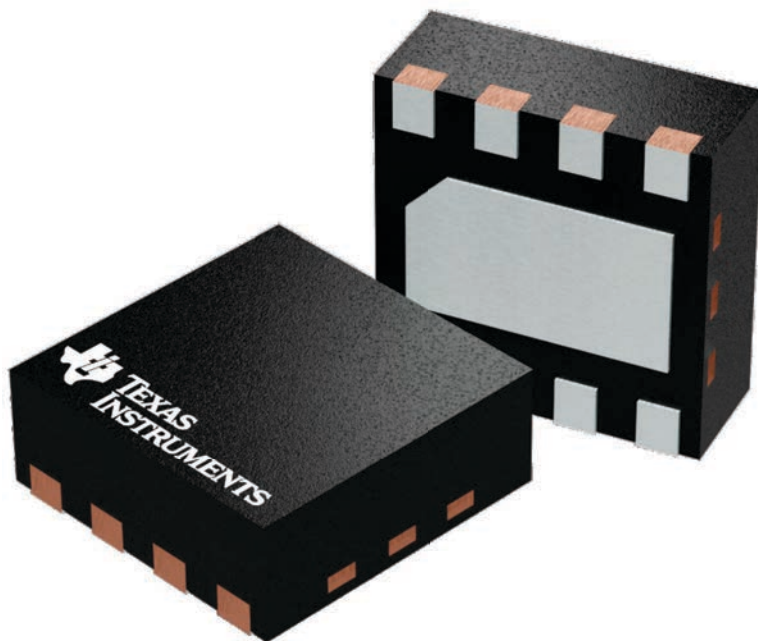
**DSG 8**

**WSON - 0.8 mm max height**

2 x 2, 0.5 mm pitch

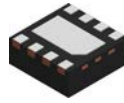
PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224783/A

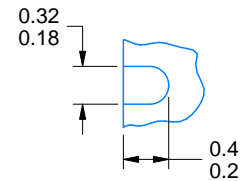
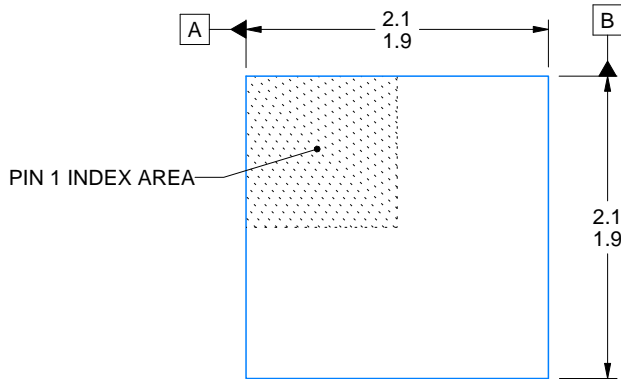
# DSG0008A



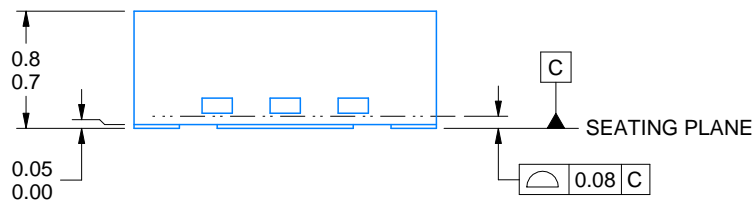
# PACKAGE OUTLINE

## WSON - 0.8 mm max height

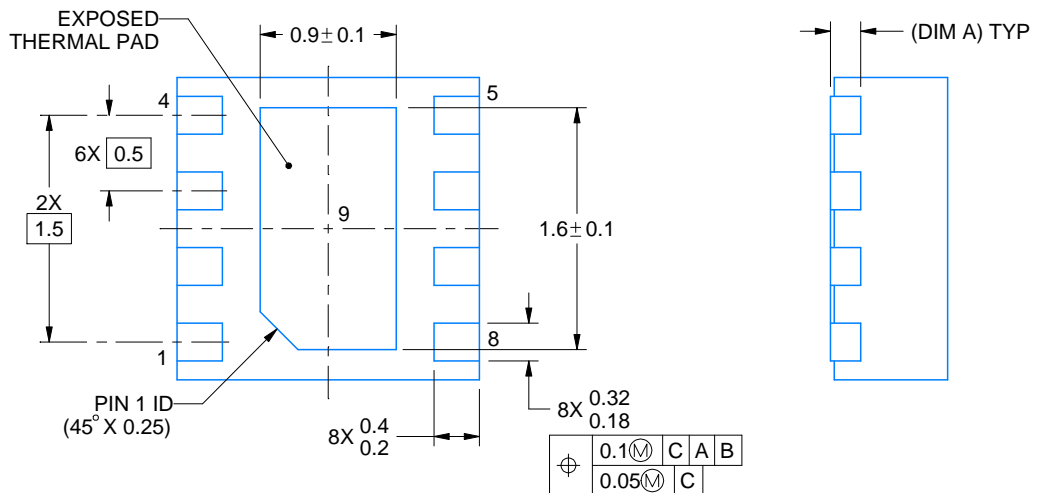
PLASTIC SMALL OUTLINE - NO LEAD



ALTERNATIVE TERMINAL SHAPE TYPICAL



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



4218900/E 08/2022

### NOTES:

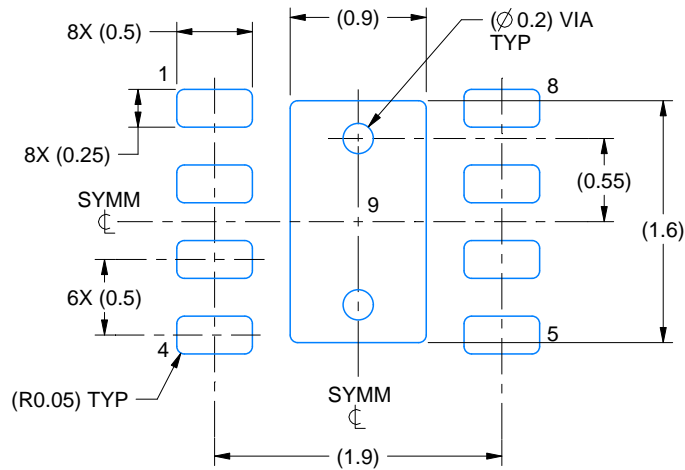
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

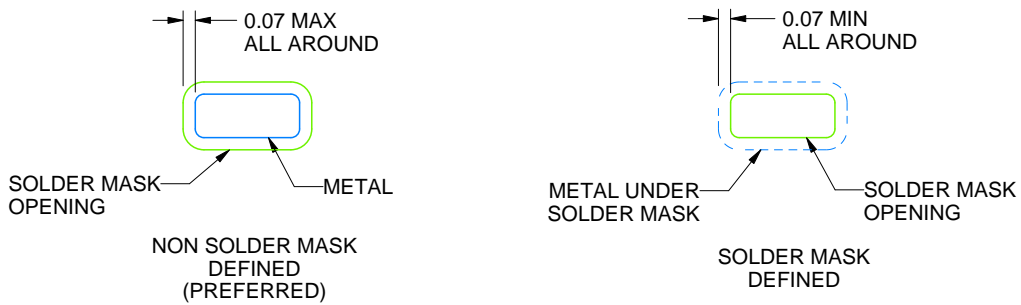
DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

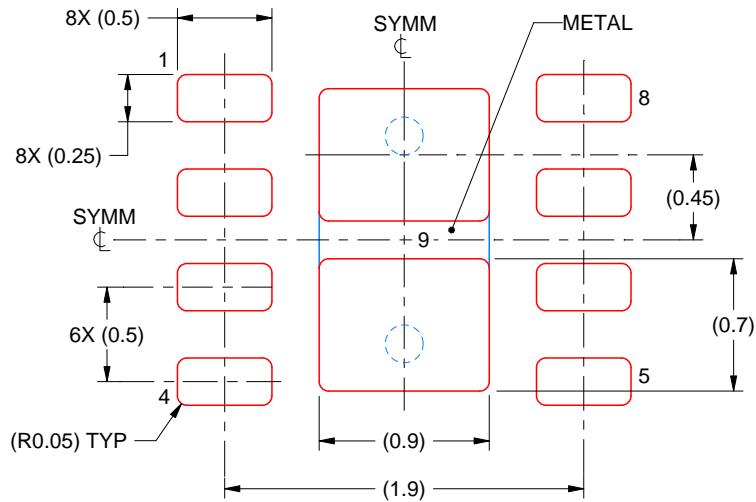
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:  
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

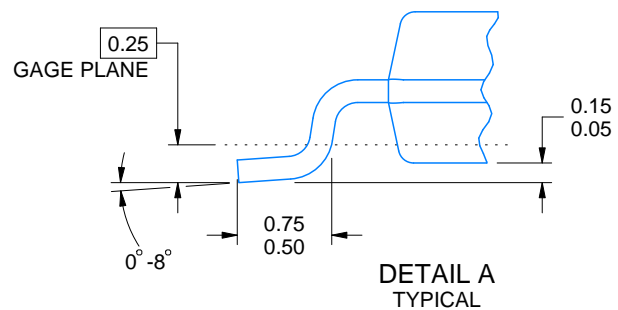
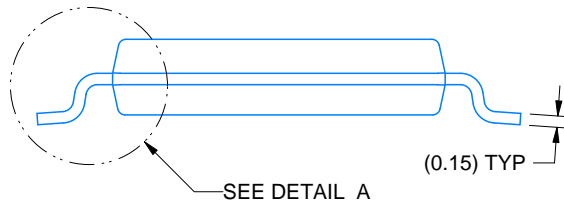
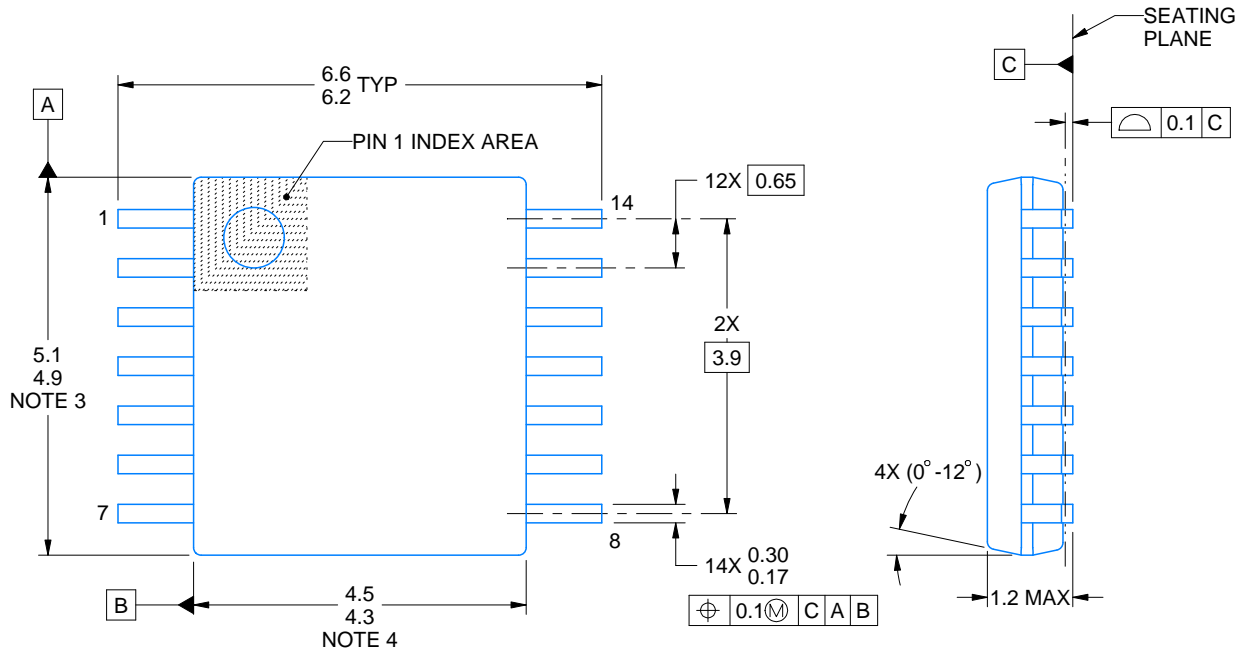
PW0014A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0008A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



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NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153, variation AA.

# EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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