

# High Speed PWM Controller

## FEATURES

- Compatible with Voltage or Current-Mode Topologies
- Practical Operation @ Switching Frequencies to 1.0MHz
- 50ns Propagation Delay to Output
- High Current Totem Pole Output (1.5A peak)
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start/Max. Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Low Start Up Current (1.1mA)
- Trimmed Bandgap Reference (5.1V  $\pm 1\%$ )

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pins 15, 13).....	30V
Output Current, Source or Sink (Pin14)	
DC.....	0.5A
Pulse (0.5 $\mu$ s).....	2.0A
Analog Inputs (Pins 1, 2, 7, 8, 9, 11).....	-0.3V to +6V
Clock Output Current (Pin 4) .....	-5mA
Error Amplifier Output Current (Pin 3) .....	5mA
Soft Start Sink Current (Pin 8) .....	20mA

## DESCRIPTION

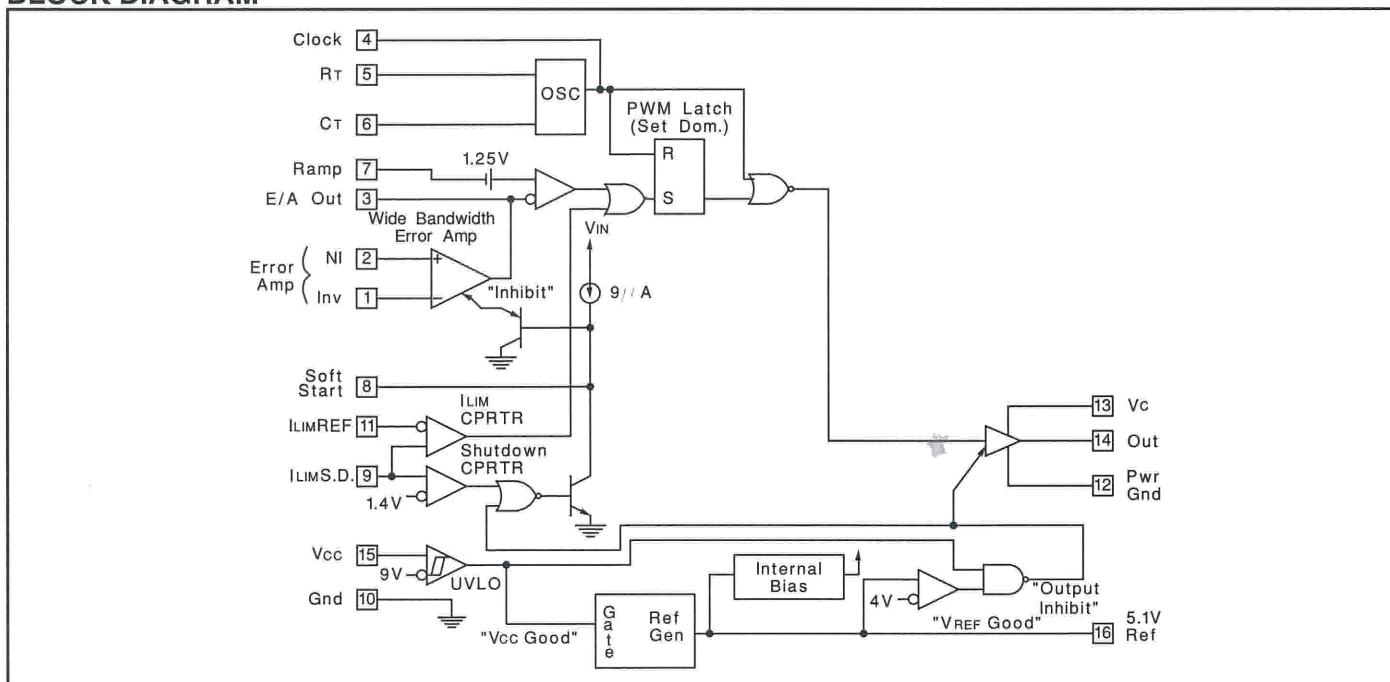
The UC1823 family of PWM control ICs is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current-mode or voltage-mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at the output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the output is high impedance. The current limit reference (pin 11) is a DC input voltage to the current limit comparator. Consult specifications for details.

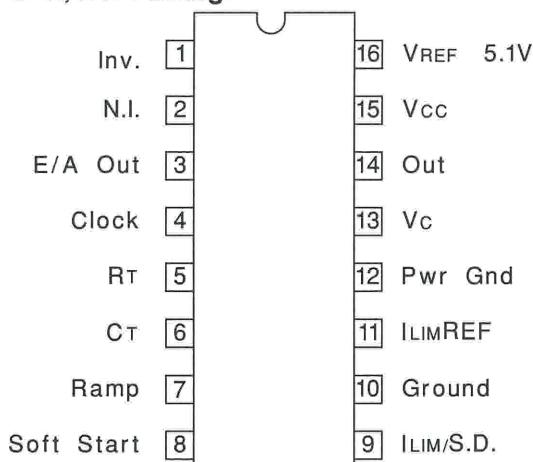
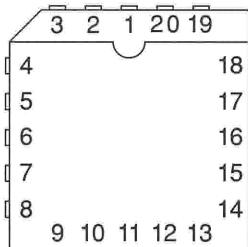
These devices feature a totem pole output designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is defined as a high level.

Oscillator Charging Current (Pin 5) .....	-5mA
Power Dissipation at $T_A = 60^\circ\text{C}$ .....	1W
Storage Temperature Range .....	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds) .....	300°C
Note: All voltages are with respect to ground, Pin 10.	
Currents are positive into the specified terminal.	
Consult Packaging Section of Databook for thermal	
limitations	

## BLOCK DIAGRAM



## CONNECTION DIAGRAMS

DIL-16, SOIC-16 (TOP VIEW)  
J or N, DW PackagePLCC-20, LCC-20 (TOP VIEW)  
Q, L Package

PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Inv.	2
N.I.	3
E/A Out	4
Clock	5
N/C	6
RT	7
CT	8
Ramp	9
Soft start	10
N/C	11
ILIM/S.D.	12
Ground	13
ILIM REF	14
PWR Gnd	15
N/C	16
Vc	17
OUT	18
VCC	19
VREF 5.1V	20

## THERMAL PACKAGING INFORMATION

PACKAGE	$\theta_{JA}$	$\theta_{JC}$
J-16	80 - 120	28 (Note2)
N-16	90 (Note1)	45
DW-16	45 - 90 (Note1)	25
PLCC-20 Q Package	43 - 75 (Note1)	34
LCC-20 L Package	70 - 80	20 (Note2)

Note 1. Specified  $\theta_{JA}$  (junction to ambient) is for devices mounted to 5-in-2 FR4 PC board with one ounce copper where noted. When resistance range is given, lower values are for 5-in-2 aluminum PC board. Test PWB was 0.062 in thick and typically used 0.635 mm trace widths for power pkgs and 1.3 mm trace widths for non-power pkgs with a 100 x 100 mil probe land area at the end of each trace.

Note 2.  $\theta_{JC}$  data values stated were derived from MIL-STD-1835B. MIL-STD-1835B states that "The baseline values shown are worst case (mean + 2s) for a 60 x 60 mil microcircuit device silicon die and applicable for devices with die sizes up to 14400 square mils. For device die sizes greater than 14400 square mils use the following values; dual-in-line, 11°C/W; flat pack, 10°C/W; pin grid array, 10°C/W"

UC1823

UC2823

UC3823

**ELECTRICAL CHARACTERISTICS:** Unless otherwise noted, these specifications apply for  $R_T = 3.65k$ ,  $C_T = 1nF$ ,  $V_{CC} = 15V$ ,  $0^\circ C < T_A < +70^\circ C$  for the UC3823,  $-25^\circ C < T_A < +85^\circ C$  for the UC2823, and  $-55^\circ C < T_A < +125^\circ C$  for the UC1823,  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	UC1823 UC2823			UC3823			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>Reference Section</b>								
Output Voltage	$T_J = 25^\circ C$ , $I_O = 1mA$	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	$10 < V_{CC} < 30V$		2	20		2	20	mV
Load Regulation	$1 < I_O < 10mA$		5	20		5	20	mV
Temperature Stability*	$T_{MIN} < T_A < T_{MAX}$		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation*	Line, Load, Temp.	5.00		5.20	4.95		5.25	
Output Noise Voltage*	$10Hz < f < 10kHz$		50			50		µV
Long Term Stability*	$T_J = 125^\circ C$ , 1000 hrs.		5	25		5	25	mV
Short Circuit Current	$V_{REF}=0V$	-15	-50	-100	-15	-50	-100	mA
<b>Oscillator Section</b>								
Initial Accuracy*	$T_J=25^\circ C$	360	400	440	360	400	440	kHz
Voltage Stability*	$10 < V_{CC} < 30V$		0.2	2		0.2	2	%
Temperature Stability*	$T_{MIN} < T_A < T_{MAX}$ (UC1823)		12					%
	$T_{MIN} < T_A < T_{MAX}$ (UC2823)		5					%
	$T_{MIN} < T_A < T_{MAX}$ (UC3823)					5		%
Total Variation*	Line, Temp.	340		460	340		460	kHz
Clock Out High		3.9	4.5		3.9	4.5		V
Clock Out Low			2.3	2.9		2.3	2.9	V
Ramp Peak*		2.6	2.8	3.0	2.6	2.8	3.0	V
Ramp Valley*		0.7	1.0	1.25	0.7	1.0	1.25	V
<b>Error Amplifier Section</b>								
Input Offset Voltage				10			15	mV
Input Bias Current			0.6	3		0.6	3	µA
Input Offset Current			0.1	1		0.1	1	µA
Open Loop Gain	$1 < V_O < 4V$	60	95		60	95		dB
CMRR	$1.5 < V_{CM} < 5.5V$	75	95		75	95		dB
PSRR	$10 < V_{CC} < 30V$	85	110		85	110		dB
Output Sink Current	$V_{PIN\ 3}=1V$	1	2.5		1	2.5		mA
Output Source Current	$V_{PIN\ 3}=4V$	-0.5	-1.3		-0.5	-1.3		mA
Output High Voltage	$I_{PIN\ 3} = -0.5mA$	4.0	4.7	5.0	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN\ 3} = 1mA$	0	0.5	1.0	0	0.5	1.0	V
Unity Gain Bandwidth*		3	5.5		3	5.5		MHz
Slew Rate*		6	12		6	12		V/µS
Ramp Valley to Peak*		1.6	1.8	2.0	1.6	1.8	2.0	V

\* These parameters are ensured by design but not 100% tested in production.



UC1823

UC2823

UC3823

**ELECTRICAL CHARACTERISTICS:** Unless otherwise noted, these specifications apply for  $R_T = 3.65k$ ,  $C_T = 1nF$ ,  $V_{CC} = 15V$ ,  $0^\circ C < T_A < +70^\circ C$  for the UC3823,  $-25^\circ C < T_A < +85^\circ C$  for the UC2823, and  $-55^\circ C < T_A < +125^\circ C$  for the UC1823,  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	UC1823 UC2823			UC3823			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>PWM Comparator Section</b>								
Pin 7 Bias Current	$V_{PIN\ 7} = 0V$		-1	-5		-1	-5	$\mu A$
Duty Cycle Range		0		80	0		85	%
Pin 3 Zero D.C. Threshold	$V_{PIN\ 7} = 0V$	1.1	1.25		1.1	1.25		V
Delay to Output*			50	80		50	80	ns
<b>Soft-Start Section</b>								
Charge Current	$V_{PIN\ 8} = 0.5V$	3	9	20	3	9	20	$\mu A$
Discharge Current	$V_{PIN\ 8} = 1V$	1			1			mA
<b>Current Limit/Shutdown Section</b>								
Pin 9 Bias Current	$0 < V_{PIN\ 9} < 4V$			$\pm 10$			$\pm 10$	$\mu A$
Current Limit Offset	$V_{PIN\ 11} = 1.1V$			15			15	mV
Current Limit Common Mode Range (V <sub>PIN</sub> 11)		1.0		1.25	1.0		1.25	V
Shutdown Threshold		1.25	1.40	1.55	1.25	1.40	1.55	V
Delay to Output*			50	80		50	80	ns
<b>Output Section</b>								
Output Low Level	$I_{OUT} = 20mA$		0.25	0.40		0.25	0.40	V
	$I_{OUT} = 200mA$		1.2	2.2		1.2	2.2	V
Output High Level	$I_{OUT} = -20mA$	13.0	13.5		13.0	13.5		V
	$I_{OUT} = -200mA$	12.0	13.0		12.0	13.0		V
Collector Leakage	$V_C = 30V$		100	500		100	500	$\mu A$
Rise/Fall Time*	$C_L = 1nF$		30	60		30	60	ns
<b>Under-Voltage Lockout Section</b>								
Start Threshold		8.8	9.2	9.6	8.8	9.2	9.6	V
UVLO Hysteresis		0.4	0.8	1.2	0.4	0.8	1.2	V
<b>Supply Current</b>								
Start Up Current	$V_{CC} = 8V$		1.1	2.5		1.1	2.5	mA
I <sub>CC</sub>	$V_{PIN\ 1}, V_{PIN\ 7}, V_{PIN\ 9} = 0V, V_{PIN\ 2} = 1V$		22	33		22	33	mA

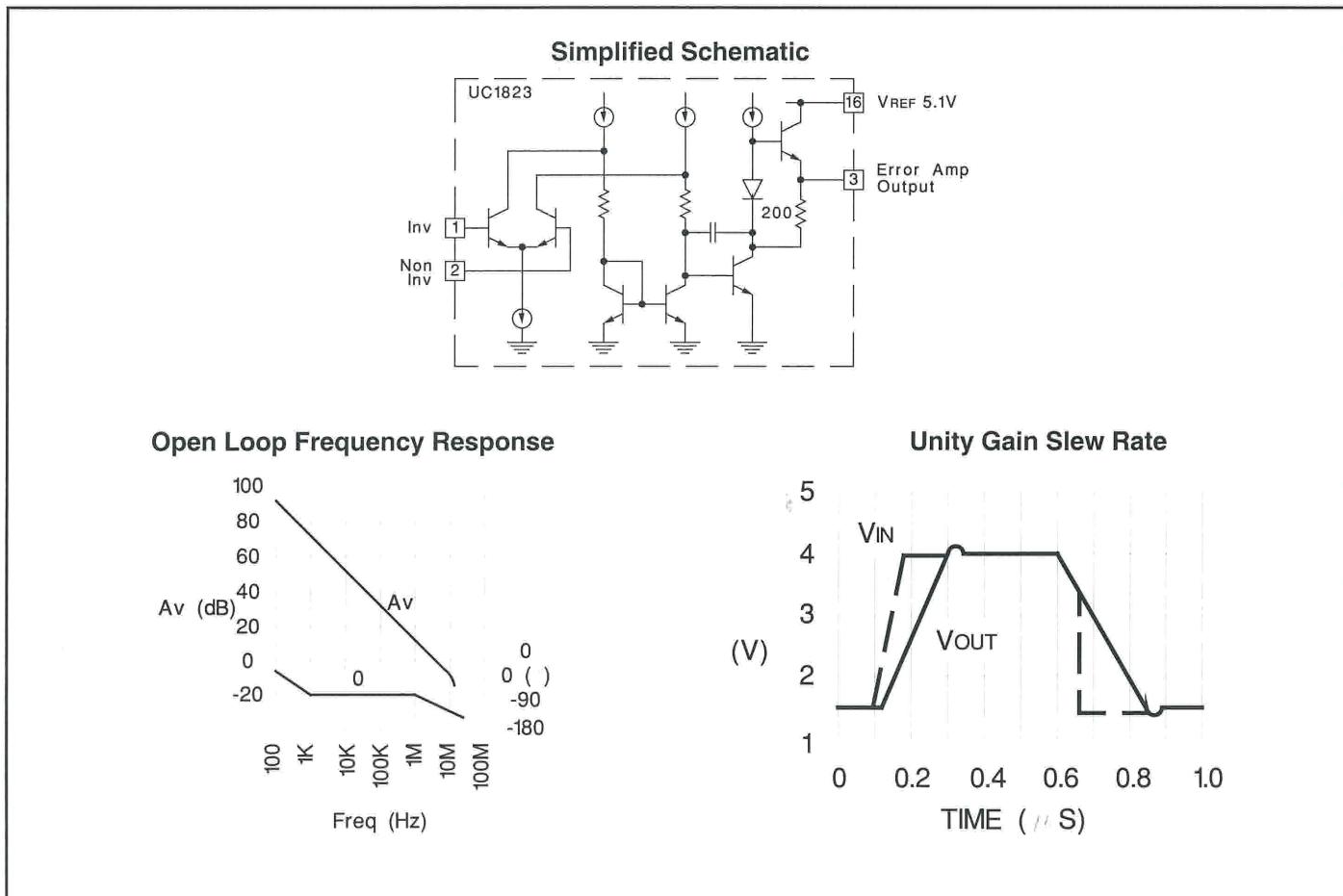
\* These parameters are ensured by design but not 100% tested in production.

## UC1823 PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

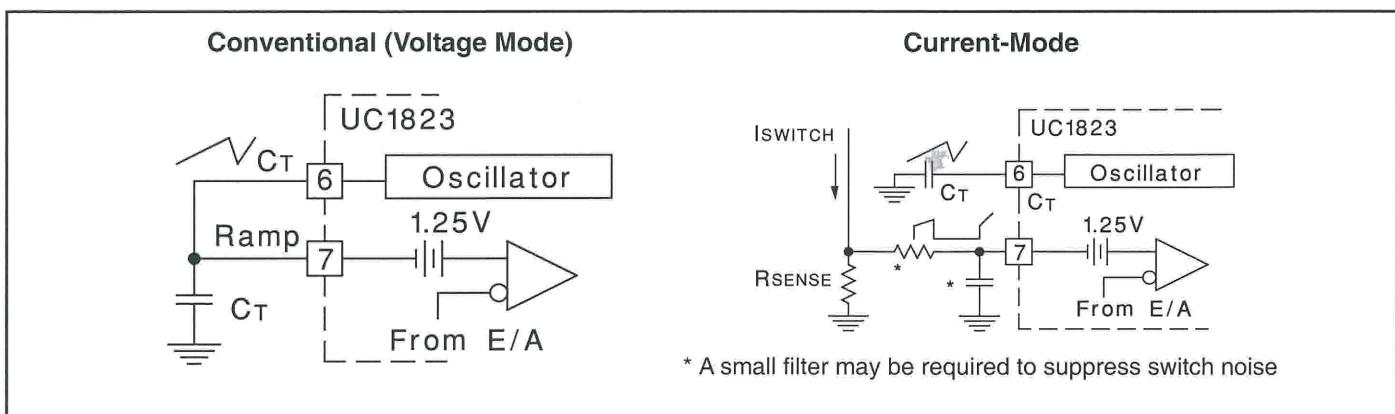
High speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC1823, follow these rules. 1) Use a ground plane. 2) Damp or clamp parasitic inductive kick energy from the gate of driven MOSFET. Don't allow the output pins to ring below ground. A series gate resistor or a shunt 1 Amp Schottky diode at the output pin will serve

this purpose. 3) Bypass V<sub>CC</sub>, V<sub>C</sub>, and V<sub>REF</sub>. Use 0.1 $\mu$ F monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane. 4) Treat the timing capacitor, C<sub>T</sub>, like a bypass capacitor.

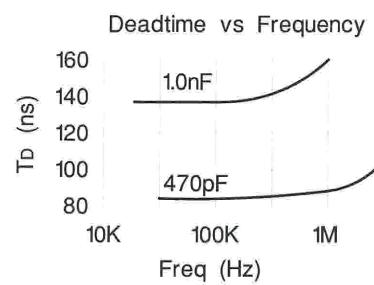
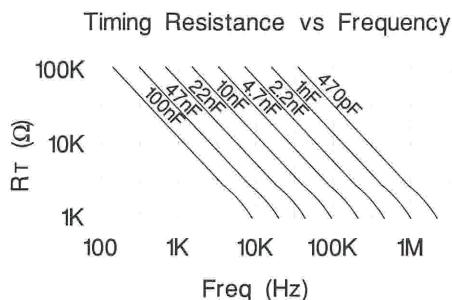
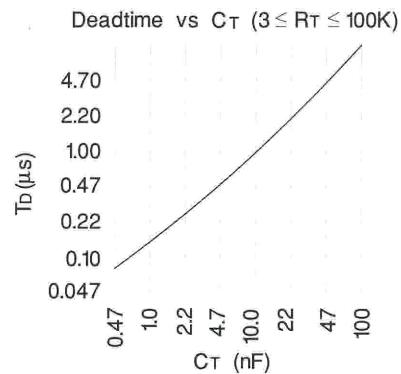
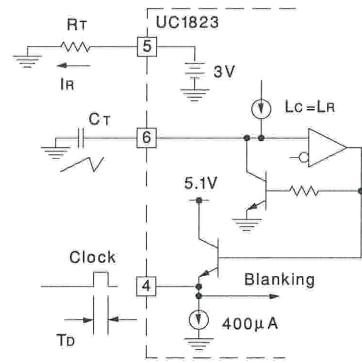
## ERROR AMPLIFIER CIRCUIT



## PWM APPLICATIONS

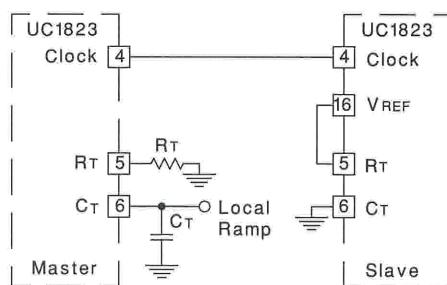


## OSCILLATOR CIRCUIT

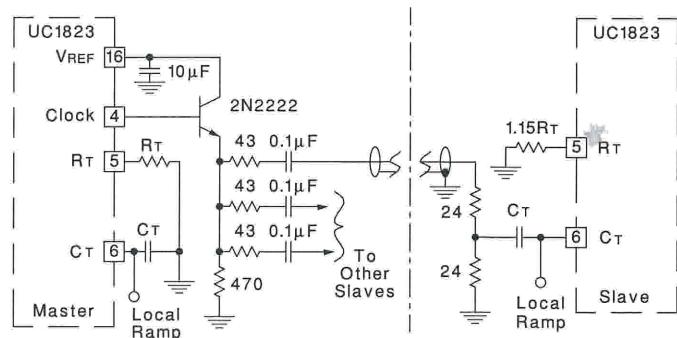


## SYNCHRONIZED OPERATION

### Two Units in Close Proximity

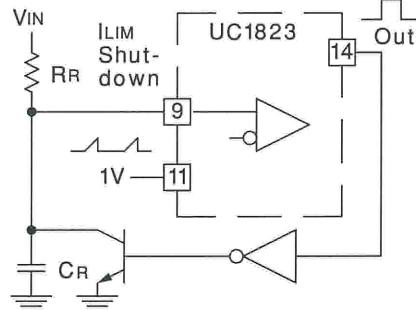


### Generalized Synchronization

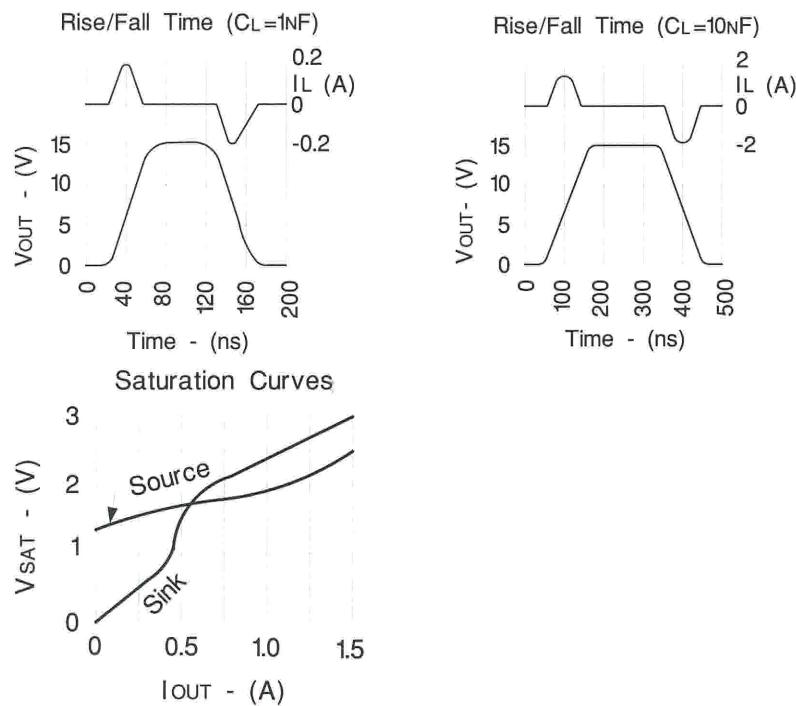
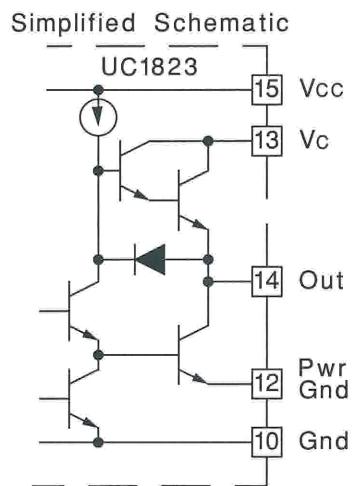


## CONSTANT VOLT-SECOND CLAMP CIRCUIT

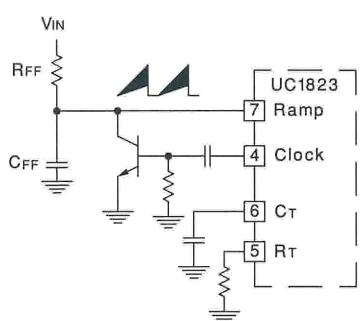
The circuit shown here will achieve a constant volt-second product clamp over varying input voltages. The ramp generator components,  $R_T$  and  $C_R$  are chosen so that the ramp at Pin 9 crosses the 1V threshold at the same time the desired maximum volt-second product is reached. The delay through the inverter must be such that the ramp capacitor can be completely discharged during the minimum deadtime.



## OUTPUT SECTION



## FEED FORWARD TECHNIQUE FOR OFF-LINE VOLTAGE MODE APPLICATION



**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-89905012A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-89905012A UC1823L/883B
5962-8990501EA	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8990501EA UC1823J/883B
UC1823J	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1823J
UC1823J.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1823J
UC1823J883B	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8990501EA UC1823J/883B
UC1823J883B.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8990501EA UC1823J/883B
UC1823L	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1823L
UC1823L.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	UC1823L
UC1823L883B	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-89905012A UC1823L/883B
UC1823L883B.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-89905012A UC1823L/883B
UC2823DW	Active	Production	SOIC (DW)   16	40   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	UC2823DW
UC2823DW.A	Active	Production	SOIC (DW)   16	40   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	UC2823DW
UC2823DWTR	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	UC2823DW
UC2823DWTR.A	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	UC2823DW
UC2823N	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-25 to 85	UC2823N
UC2823N.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-25 to 85	UC2823N
UC3823DW	Active	Production	SOIC (DW)   16	40   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3823DW
UC3823DW.A	Active	Production	SOIC (DW)   16	40   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3823DW
UC3823DWG4	Active	Production	SOIC (DW)   16	40   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3823DW
UC3823DWTR	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3823DW

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UC3823DWTR.A	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3823DW
<a href="#">UC3823N</a>	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3823N
UC3823N.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3823N
UC3823NG4	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3823N

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF UC1823, UC3823 :

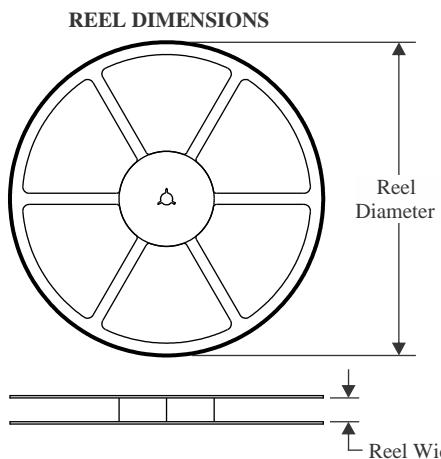
- Catalog : [UC3823](#)

---

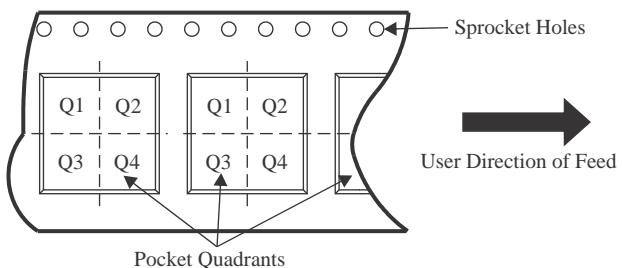
- Military : [UC1823](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


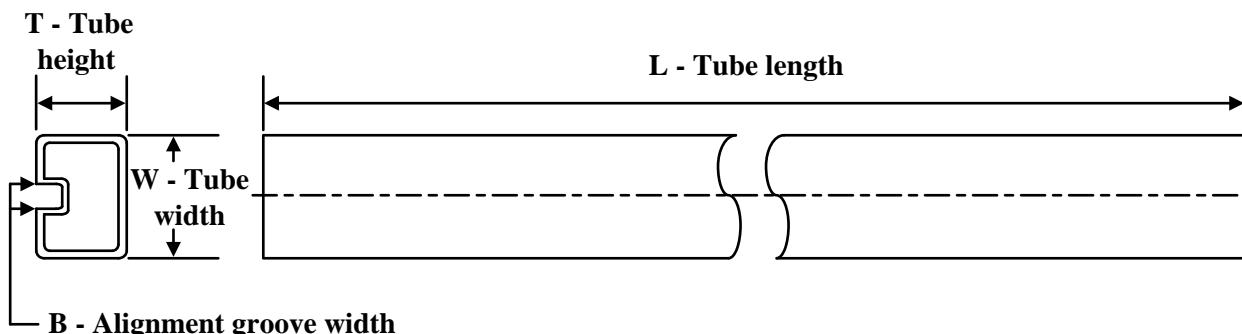
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2823DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UC3823DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2823DWTR	SOIC	DW	16	2000	353.0	353.0	32.0
UC3823DWTR	SOIC	DW	16	2000	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-89905012A	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1823L	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1823L.A	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1823L883B	FK	LCCC	20	55	506.98	12.06	2030	NA
UC1823L883B.A	FK	LCCC	20	55	506.98	12.06	2030	NA
UC2823DW	DW	SOIC	16	40	507	12.83	5080	6.6
UC2823DW.A	DW	SOIC	16	40	507	12.83	5080	6.6
UC2823N	N	PDIP	16	25	506	13.97	11230	4.32
UC2823N.A	N	PDIP	16	25	506	13.97	11230	4.32
UC3823DW	DW	SOIC	16	40	507	12.83	5080	6.6
UC3823DW.A	DW	SOIC	16	40	507	12.83	5080	6.6
UC3823DWG4	DW	SOIC	16	40	507	12.83	5080	6.6
UC3823N	N	PDIP	16	25	506	13.97	11230	4.32
UC3823N.A	N	PDIP	16	25	506	13.97	11230	4.32
UC3823NG4	N	PDIP	16	25	506	13.97	11230	4.32

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025