

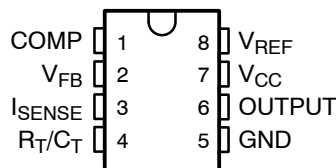
UC1842A-EP, UC1843A-EP, UC1844A-EP, UC1845A-EP CURRENT-MODE PWM CONTROLLER

SGLS134D – SEPTEMBER 2002 – REVISED JANUARY 2013

- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree†**
- **Optimized for Off-line and DC-to-DC Converters**
- **Low Start Up Current (<0.5 mA)**
- **Trimmed Oscillator Discharge Current**
- **Automatic Feed Forward Compensation**
- **Pulse-by-Pulse Current Limiting**
- **Enhanced Load Response Characteristics**
- **Under-Voltage Lockout With Hysteresis**
- **Double Pulse Suppression**
- **High Current Totem Pole Output**
- **Internally Trimmed Bandgap Reference**
- **500 kHz Operation**
- **Low R_O Error Amp**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

D PACKAGE
(TOP VIEW)



description

The UC1842A/3A/4A/5A family of control ICs is a pin-for-pin compatible improved version of the UC3842/3/4/5 family. Providing the necessary features to control current mode switched mode power supplies, this family has the following improved features. Start up current is guaranteed to be less than 0.5 mA. Oscillator discharge is trimmed to 8.3 mA. During under voltage lockout, the output stage can sink at least 10 mA at less than 1.2 V for V_{CC} over 5 V.

The difference between members of this family are shown in the table below.

PART NUMBER	UVLO ON	UVLO OFF	MAXIMUM DUTY CYCLE
UC1842A	16 V	10 V	<100%
UC1843A	8.5 V	7.9 V	<100%
UC1844A	16 V	10 V	<50%
UC1845A	8.5 V	7.9 V	<50%

ORDERING INFORMATION‡

T _A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOP – D	Tape and reel	UC1842AMDREP	1842AME
–55°C to 125°C	SOP – D	Tape and reel	UC1843AMDREP	1843AME
–55°C to 125°C	SOP – D	Tape and reel	UC1844AMDREP	1844AME
–55°C to 125°C	SOP – D	Tape and reel	UC1845AMDREP	1845AME

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

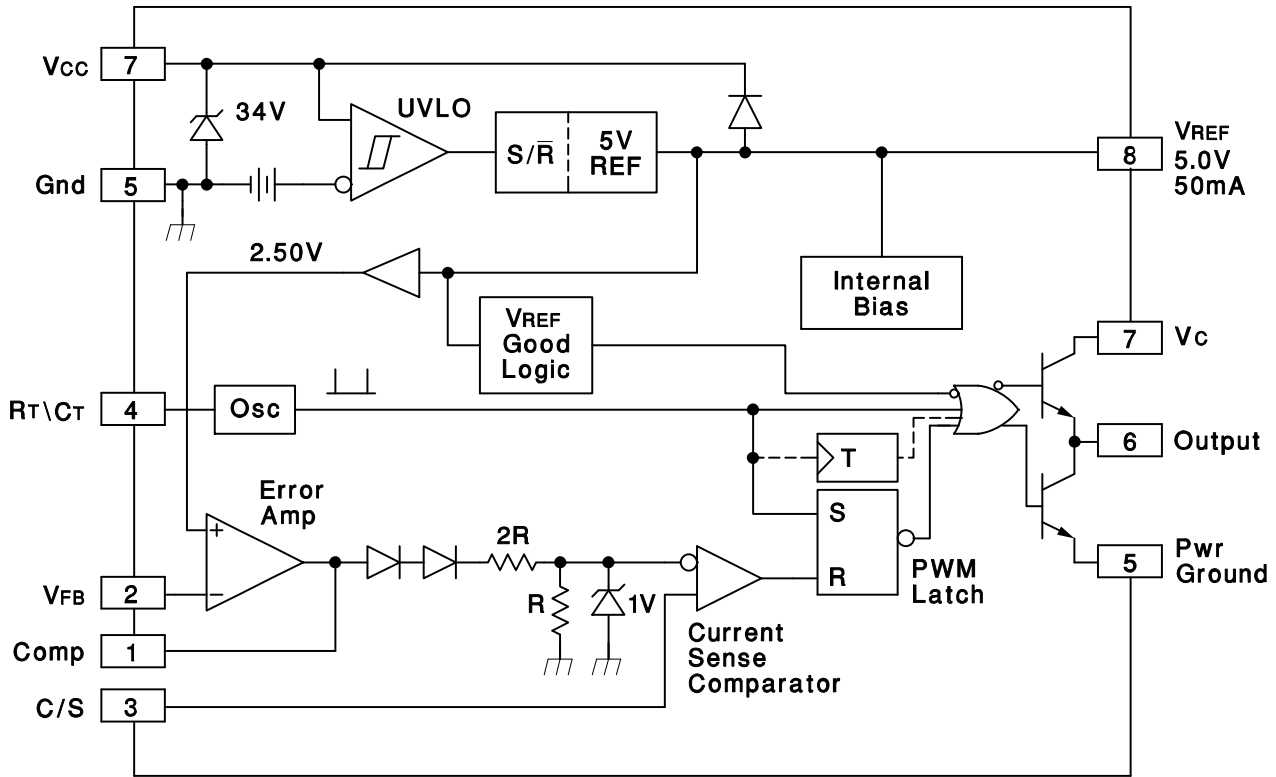
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UC1842A-EP, UC1843A-EP, UC1844A-EP, UC1845A-EP CURRENT-MODE PWM CONTROLLER

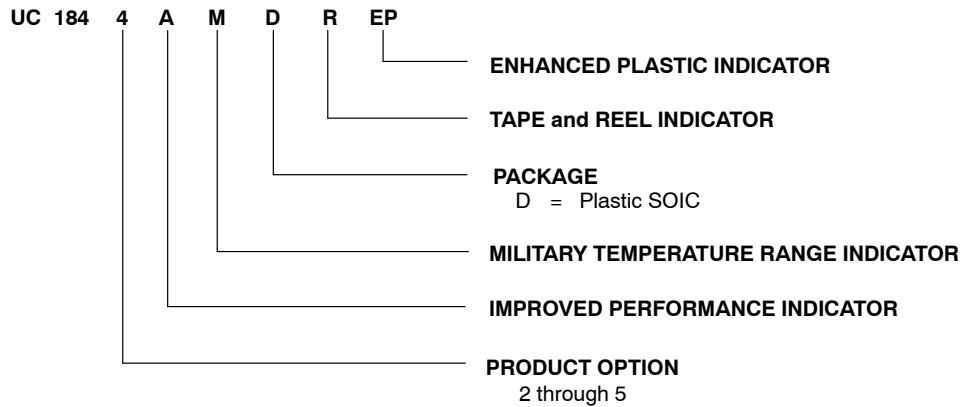
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block diagram



NOTES: 1. Toggle flip flop used only in 1844A and 1845A.

Ordering Information



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UC1842A-EP, UC1843A-EP, UC1844A-EP, UC1845A-EP CURRENT-MODE PWM CONTROLLER

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)^{†‡}

V _{CC} voltage (low impedance source)	30 V
V _{CC} voltage (I _{CC} mA)	self limiting
Output current, I _O	±1 A
Output energy (capacitive load)	5 μJ
Analog Inputs (pins 2, 3)	–0.3 V to 6.3 V
Error Amp Output Sink current	10 mA
Power Dissipation at T _A < 25°C	1 W
Package thermal impedance, θ _{JA} (see Note 1):	97°C/W
Storage temperature range, T _{stg}	–65°C to 150°C
Maximum junction temperature, T _J	150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] Unless otherwise indicated, voltages are reference to ground and currents are positive into and negative out of the specified terminals.

NOTE 1: Long term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

electrical characteristics, T_A = –55°C to 125°C for the UC184xAM-EP, V_{CC} = 15 V (see Note 1), R_T = 10 kΩ, C_T = 3.3 nF, and T_A = T_J (unless otherwise stated)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS		
Reference Section							
Output voltage	T _J = 25°C, I _O = 1 mA	4.95	5	5.05	V		
Line regulation voltage	V _{IN} = 12 V to 25 V		6	20	mV		
Load regulation voltage	I _O = 1 mA to 20 mA		6	25	mV		
Temperature stability	See Notes NO TAG and NO TAG		0.2	0.4	mV/°C		
Total output variation voltage	Line, Load, Temp.	4.9		5.1	V		
Output noise voltage	f = 10 Hz to 10 kHz, See Note NO TAG		50		μV		
Long term stability	1000 hours, See Note 2		5	25	mV		
Output short-circuit current		–30	–100	–180	mA		
Oscillator Section							
Initial accuracy	See Note NO TAG		47	52	57	kHz	
Voltage stability	V _{CC} = 12 V to 25 V		0.2%	1%			
Temperature stability	T _A = MIN to MAX, See Note 2		5%				
Amplitude peak-to-peak	V pin 4, See Note 2		1.7		V		
Discharge current	V pin 4 = 2 V, See Note 3		T _J = 25°C	7.8	8.3	8.8	mA
			T _J = Full range	7.5		8.8	

- NOTES: 1. Adjust V_{CC} above the start threshold before setting at 15 V.
 2. Not production tested.
 3. This parameter is measured with R_T = 10 kΩ to V_{REF}. This contributes approximately 300 μA of current to the measurement. The total current flowing into the R_{T/C} pin will be approximately 300 μA higher than the measured value.



UC1842A-EP, UC1843A-EP, UC1844A-EP, UC1845A-EP CURRENT-MODE PWM CONTROLLER

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electrical characteristics, $T_A = -55^\circ\text{C}$ to 125°C for the UC184xAM-EP, $V_{CC} = 15\text{ V}$ (see Note 1), $R_T = 10\text{ k}\Omega$, $C_T = 3.3\text{ nF}$, and $T_A = T_J$ (unless otherwise stated)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Error Amplifier Section						
Input voltage	COMP = 2.5 V		2.45	2.5	2.55	V
Input bias current				-0.3	-1	μA
Open loop voltage gain (A_{VOL})	$V_O = 2\text{ V}$ to 4 V		65	90		dB
Unity gain bandwidth	See Note 2	$T_J = 25^\circ\text{C}$	0.7	1		MHz
PSRR	$V_{CC} = 12\text{ V}$ to 25 V		60	70		dB
Output sink current	FB = 2.7 V, COMP = 1.1 V		2	6		mA
Output source current	FB = 2.3 V, COMP = 5 V		-0.5	-0.8		mA
V_{OUT} high	FB = 2.3 V, $R_L = 15\text{ k}\Omega$ to GND		5	6		V
V_{OUT} low	FB = 2.7 V, $R_L = 15\text{ k}\Omega$ to V_{REF}			0.7	1.1	V
Current Sense Section						
Gain	See Note 3 and Note 4		2.85	3	3.15	V/V
Maximum input signal	COMP = 5 V, See Note 3		0.9	1	1.1	V
PSRR	$V_{CC} = 12\text{ V}$ to 25 V , See Note 3			70		dB
Input bias current				-2	-10	μA
Delay to output	$I_{SENSE} = 0\text{ V}$ to 2 V , See Note 2			150	300	ns
Output Section (OUT)						
Low-level output voltage	$I_{OUT} = 20\text{ mA}$			0.1	0.4	V
	$I_{OUT} = 200\text{ mA}$			15	2.2	
High-level output voltage	$I_{OUT} = -20\text{ mA}$		13	13.5		V
	$I_{OUT} = -200\text{ mA}$		12	13.5		
Rise time	$C_L = 1\text{ nF}$, See Note 2	$T_J = 25^\circ\text{C}$		50	150	ns
Fall time	$C_L = 1\text{ nF}$, See Note 2	$T_J = 25^\circ\text{C}$		50	150	ns
UVLO saturation	$V_{CC} = 5\text{ V}$, $I_{OUT} = 10\text{ mA}$			0.7	1.2	V
Undervoltage Lockout Section						
Start threshold	UC1842A, UC1844A		15	16	17	V
	UC1843A, UC1845A		7.8	8.4	9	
Minimum operation voltage after turn on	UC1842A, UC1844A		9	10	11	V
	UC1843A, UC1845A		7	7.6	8.2	

- NOTES: 1. Adjust V_{CC} above the start threshold before setting at 15 V.
 2. Not production tested.
 3. Parameter measured at trip point of latch with V_{FB} at 0 V.
 4. Gain is defined by: $A = \frac{\Delta V_{COMP}}{\Delta V_{SENSE}}$; $0 \leq V_{SENSE} \leq 0.8\text{ V}$.



UC1842A-EP, UC1843A-EP, UC1844A-EP, UC1845A-EP CURRENT-MODE PWM CONTROLLER

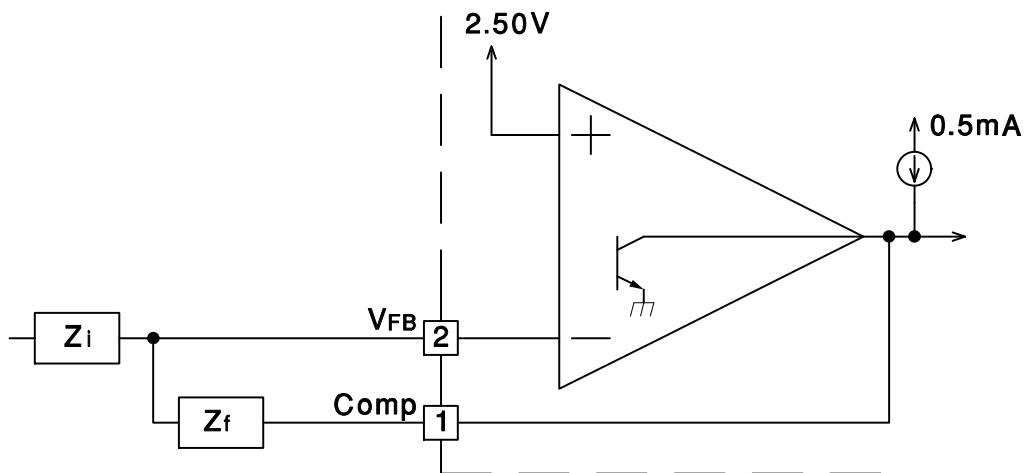
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electrical characteristics, $T_A = -55^\circ\text{C}$ to 125°C for the UC184xAM-EP, $V_{CC} = 15\text{ V}$ (see Note 1), $R_T = 10\text{ k}\Omega$, $C_T = 3.3\text{ nF}$, and $T_A = T_J$ (unless otherwise stated)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PWM Section					
Maximum duty cycle	UC1842A, UC1843A	94%	96%	100%	
	UC1844A, UC1845A	47%	48%	50%	
Minimum duty cycle				0%	
Total Standby Current					
Start-up current			0.3	0.5	mA
Operating supply current	FB = 0 V, SENSE = 0 V		11	17	mA
V_{CC} internal zener voltage	$I_{CC} = 25\text{ mA}$	30	34		V

NOTES: 1. Adjust V_{CC} above the start threshold before setting at 15 V.

PARAMETER MEASUREMENT INFORMATION



Error Amp can source and sink up to 0.5 mA and sink up to 2 mA.

Figure 1. Error Amp Configuration

UC1842A-EP, UC1843A-EP, UC1844A-EP, UC1845A-EP CURRENT-MODE PWM CONTROLLER

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PARAMETER MEASUREMENT INFORMATION

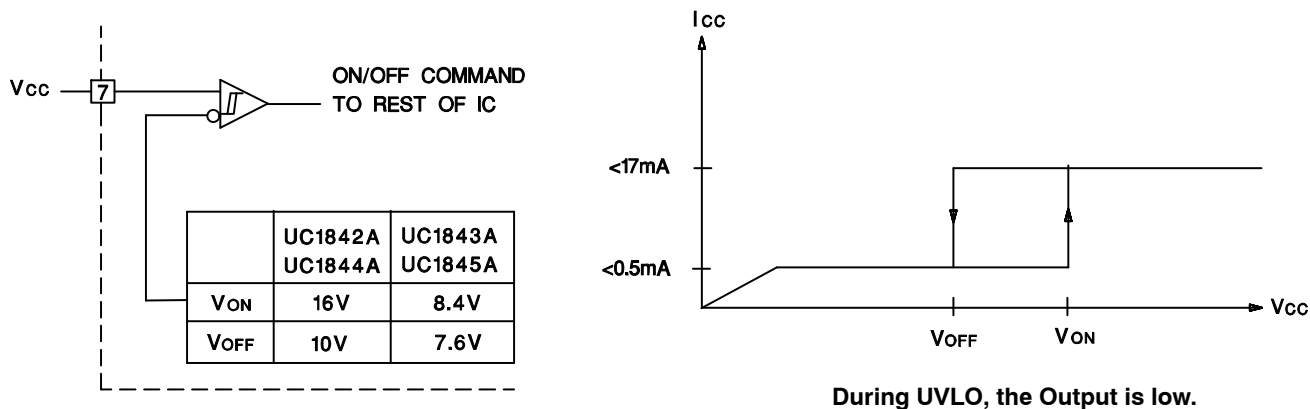
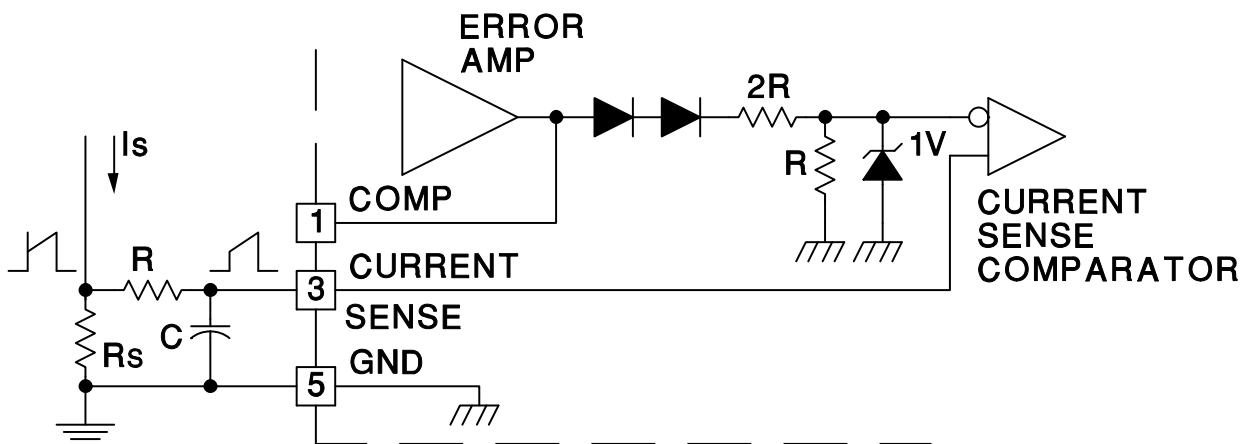


Figure 2. Under Voltage Lockout



Peak Current (I_s) is determined by the following formula:

$$I_{smax} = \frac{1V}{R_S}$$

A small RC filter may be required to suppress switch transients.

Figure 3. Current Sense Circuit

PARAMETER MEASUREMENT INFORMATION

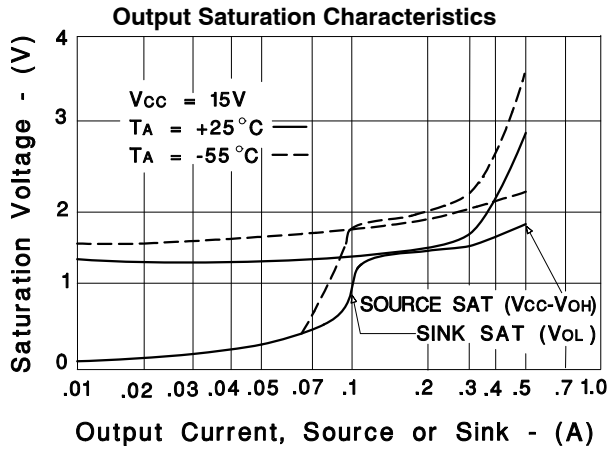


Figure 4

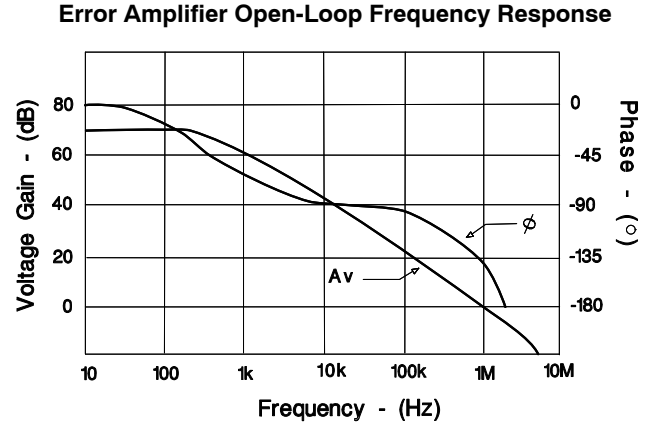


Figure 5

APPLICATION INFORMATION

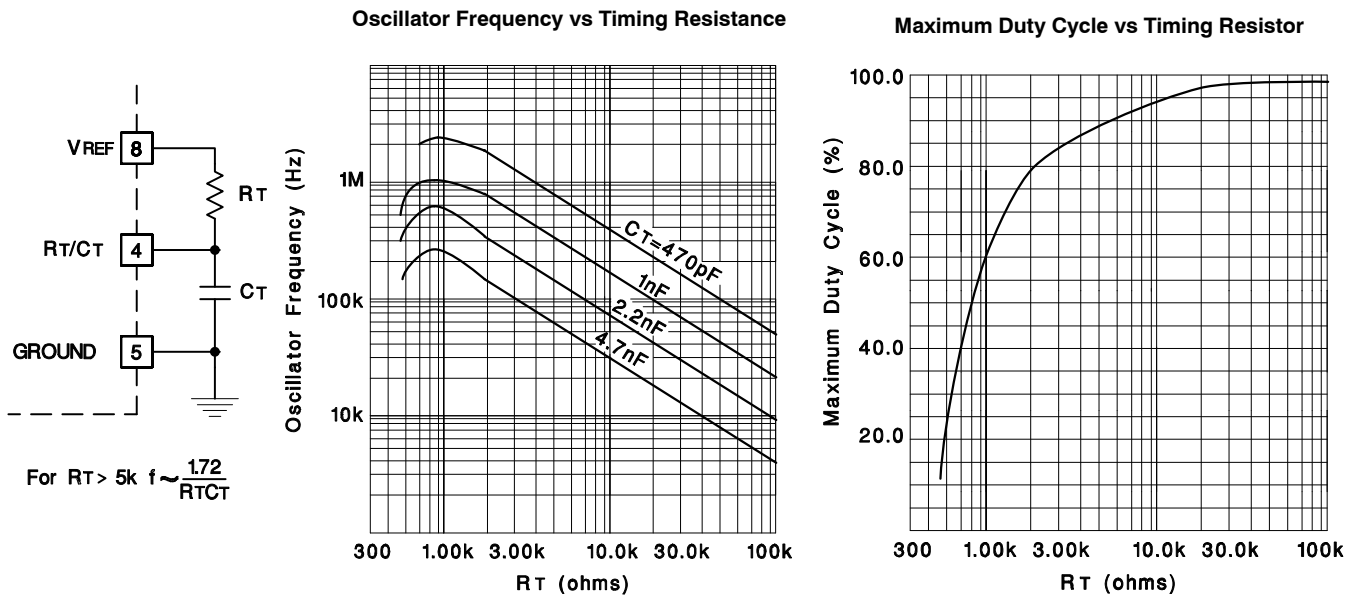
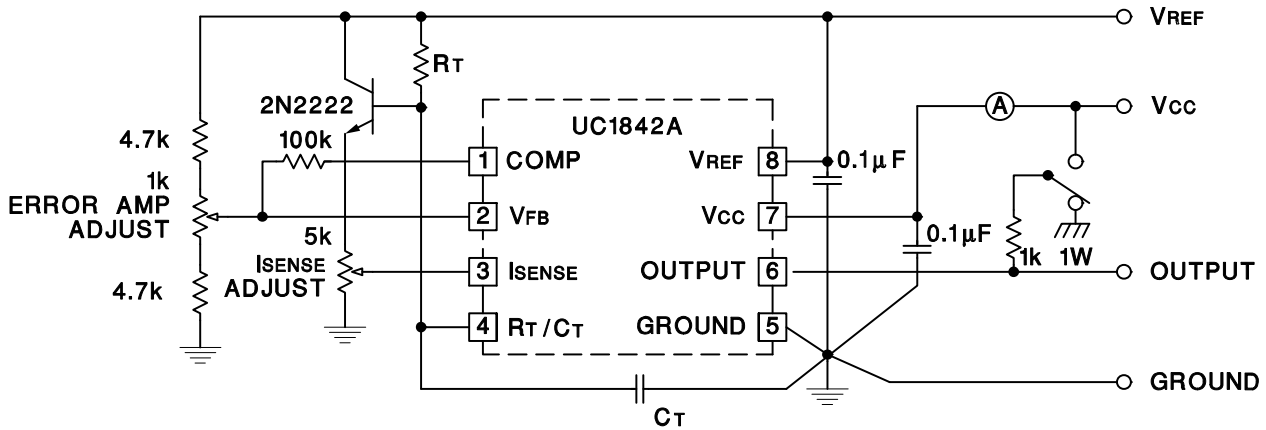


Figure 6. Oscillator

UC1842A-EP, UC1843A-EP, UC1844A-EP, UC1845A-EP CURRENT-MODE PWM CONTROLLER

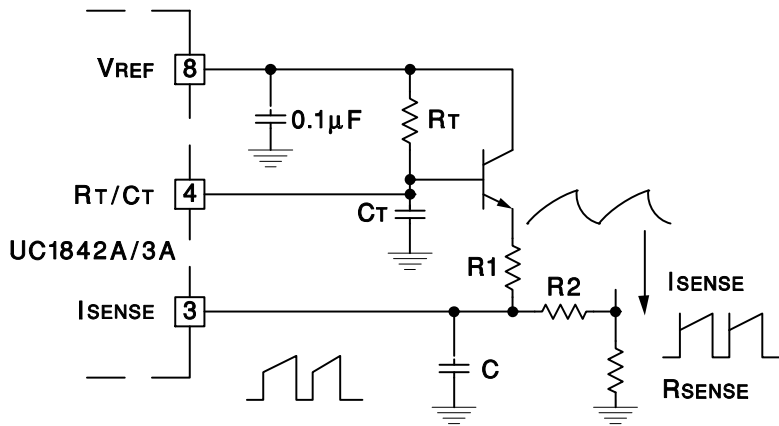
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APPLICATION INFORMATION



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Figure 7. Open-Loop Laboratory Text Fixture



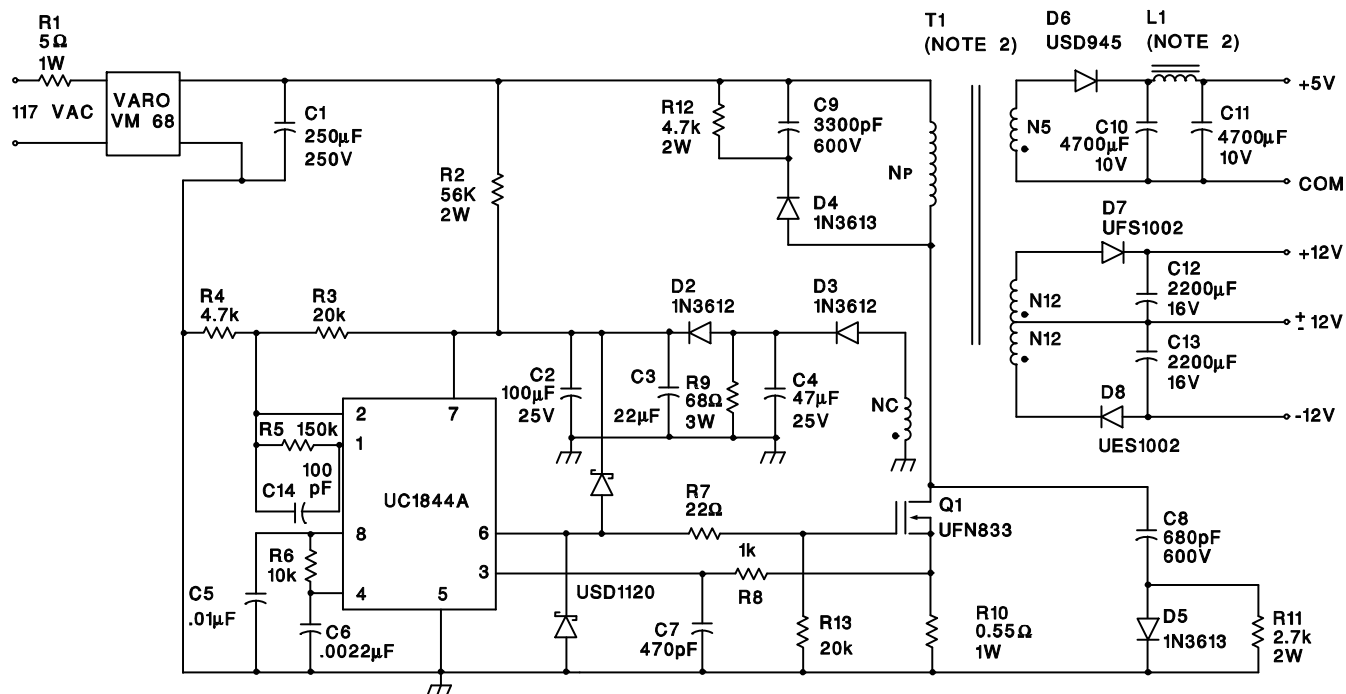
A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%. Note that capacitor, C, forms a filter with R2 to suppress the leading edge switch spikes.

Figure 8. Slope Compression

UC1842A-EP, UC1843A-EP, UC1844A-EP, UC1845A-EP CURRENT-MODE PWM CONTROLLER

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APPLICATION INFORMATION



Power Supply Specifications

1. Input Voltage 95VAC to 130VAC (50 Hz/60 Hz)
2. Line Isolation 3750 V
3. Switching Frequency 40 kHz
4. Efficiency, Full Load 70%
5. Output Voltage:
 - A. +5V, $\pm 5\%$; 1A to 4A Load
 - B. +12V, $\pm 3\%$; 0.1A to 0.3A Load Ripple voltage: 100 mV P-P Max
 - C. -12V, $\pm 3\%$; 0.1A to 0.3A Load Ripple voltage: 100 mV P-P Max

Figure 9. Off-Line Flyback Regulator

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UC1842AMDREP	NRND	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1842AME
UC1842AMDREP.A	NRND	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1842AME
UC1843AMDREP	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1843AME
UC1843AMDREP.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1843AME
UC1844AMDREP	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1844AME
UC1844AMDREP.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1844AME
UC1845AMDREP	NRND	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	(1845AE, 1845AME)
UC1845AMDREP.A	NRND	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	(1845AE, 1845AME)
UC1845AMDREPG4	NRND	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	(1845AE, 1845AME)
V62/03625-01YE	NRND	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1842AME
V62/03625-02YE	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1843AME
V62/03625-03YE	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	1844AME
V62/03625-04YE	NRND	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	(1845AE, 1845AME)

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF UC1842A-EP, UC1843A-EP, UC1844A-EP, UC1845A-EP :

- Catalog : [UC1842A](#), [UC1843A](#), [UC1844A](#), [UC1845A](#)
- Space : [UC1842A-SP](#), [UC1843A-SP](#), [UC1844A-SP](#), [UC1845A-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC1842AMDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC1843AMDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC1844AMDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC1845AMDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC1842AMDREP	SOIC	D	8	2500	350.0	350.0	43.0
UC1843AMDREP	SOIC	D	8	2500	350.0	350.0	43.0
UC1844AMDREP	SOIC	D	8	2500	350.0	350.0	43.0
UC1845AMDREP	SOIC	D	8	2500	350.0	350.0	43.0



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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