



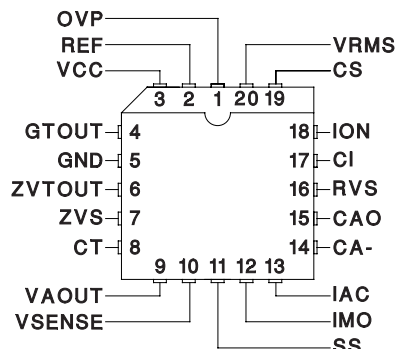
### ABSOLUTE MAXIMUM RATINGS

Supply Voltage VCC	Internally Limited
VCC Supply Clamp Current	20mA
PFC Gate Driver Current (continuous)	± 0.5A
PFC Gate Driver Current (peak)	± 1.5A
ZVT Drive Current (continuous)	± 0.25A
ZVT Drive Current (peak)	± 0.75A
Input Current (IAC, RT, RVA)	5mA
Analog Inputs (except Peak Limit)	-0.3 to 10V
Peak Limit Input	-0.3 to 6.5V
Softstart Sinking Current	1.5mA
Storage Temperature	-65°C to +150°C
Junction Temperature	-55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

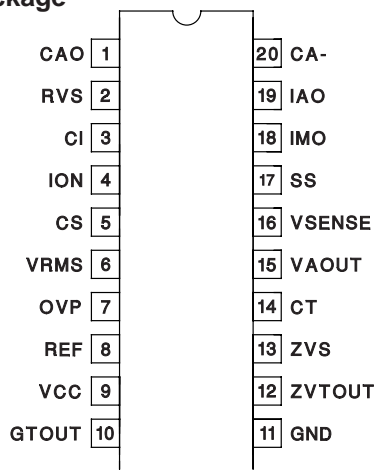
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

### CONNECTION DIAGRAMS

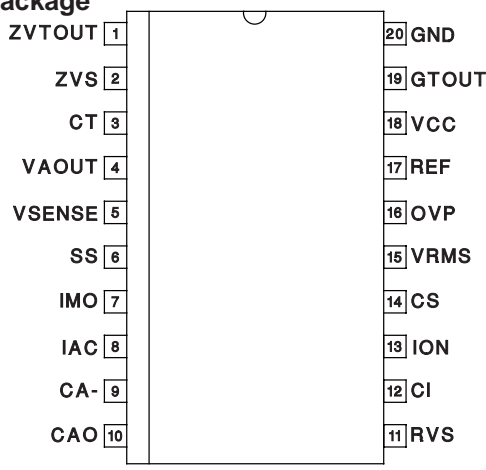
PLCC-20 & LCC-20 (Top View)  
Q or L Package



DIL-20 (Top View)  
J or N Package



SOIC-20 (Top View)  
DW Package



**ELECTRICAL CHARACTERISTICS:** Unless otherwise specified: VCC = 18V, RVS = 23k, CT = 470pF, CI = 150pF, VRMS = 1.5V, IAC = 100µA, ISENSE = 0V, CAO = 4V, VAOUT = 3.5V, VSENSE = 3V. -40°C to 85°C (UC2855A/B), 0°C to 70°C (UC3855A/B).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>Overall</b>					
Supply Current, OFF	CAO, VAOUT = 0V, VCC = UVLO -0.3V		150	500	µA
Supply Current, OPERATING			17	25	mA
VCC Turn-On Threshold	UC3855A		15.5	17.5	V
VCCTurn-Off Threshold	UC3855A,B	9	10		V
VCC Turn-On Threshold	UC3855B		10.5	10.8	V
VCC Clamp	I(VCC) = ICC(on) + 5mA	18	20	22	V
<b>Voltage Amplifier</b>					
Input Voltage		2.9		3.1	V
VSENSE Bias Current		-500	25	500	nA
Open Loop Gain	VOUT = 2 to 5V	65	80		dB
VOUT High	ILOAD = -300µA	5.75	6	6.25	V
VOUT Low	ILOAD = 300µA		0.3	0.5	V
Output Short Circuit Current	VOUT = 0V		0.6	3	mA

**ELECTRICAL CHARACTERISTICS:** Unless otherwise specified: VCC = 18V, RVS = 23k, CT = 470pF, CI = 150pF, VRMS = 1.5V, IAC = 100μA, ISENSE = 0V, CAO = 4V, VAOUT = 3.5V, VSENSE = 3V. -40°C to 85°C (UC2855A/B), 0°C to 70°C (UC3855A/B).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>Current Amplifier</b>					
Input Offset Voltage	V <sub>CM</sub> = -2.5V	-4		4	mV
Input Bias Current (Sense)	V <sub>CM</sub> = 2.5V	-500		500	nA
Open Loop Gain	V <sub>CM</sub> = 2.5V, V <sub>OUT</sub> = 2 to 6V	80	110		dB
V <sub>OUT</sub> High	I <sub>LOAD</sub> = -500μA		6		V
V <sub>OUT</sub> Low	I <sub>LOAD</sub> = 500μA		0.3	0.5	V
Output Short Circuit Current	V <sub>OUT</sub> = 0V		1	3	mA
Common Mode Range		-0.3		5	V
Gain Bandwidth Product	F <sub>IN</sub> = 100kHz, 10mV, P-P, T <sub>A</sub> = 25°C	2.5	5		MHz
<b>Reference</b>					
Output Voltage	I <sub>REF</sub> = 0mA, T <sub>A</sub> = 25°C	7.388	7.5	7.613	V
	I <sub>REF</sub> = 0mA	7.313	7.5	7.688	V
Load Regulation	I <sub>REF</sub> = 1 to 10 mA	-15		15	mV
Line Regulation	V <sub>CC</sub> = 15 to 35V	-10		10	mV
Short Circuit Current	REF = 0V	20	45	65	mA
<b>Oscillator</b>					
Initial Accuracy	T <sub>A</sub> = 25°C	170	200	230	kHz
Voltage Stability	V <sub>CC</sub> = 12 to 18V		1		%
Total Variation	Line, Temp.	160		240	kHz
Ramp Amplitude (P-P)	Outputs at 0% duty cycle	4.7		5.7	V
Ramp Valley Voltage		1.1		1.6	V
<b>Enable/OVP/Current Limit</b>					
Enable Threshold			1.8	2.2	V
OVP Threshold			7.5	7.66	V
OVP Hysteresis		200	400	600	mV
OVP Propagation Delay			200		ns
OVP Input Bias Current	V = 7.5V		1	10	μA
PKLIMIT Threshold		1.25	1.5	1.75	V
PKLIMIT Input Current	V <sub>PKLIMIT</sub> = 1.5V		100		μA
PKLIMIT Prop. Delay			100		ns
<b>Soft Start</b>					
Soft Start Charge Current		-10	-13	-20	μA
Soft Start Discharge Current		2	10	20	mA
<b>Multiplier</b>					
Output Current - IAC Limited	IAC = 100μA, VRMS = 1V	-235	-205	-175	μA
Output Current - Zero	IAC = 0μA	-2	-0.2	2	μA
Output Current - Power Limited	VRMS = 1.5V, VAOUT = 5.5V	-250	-209	-160	μA
Output Current	VRMS = 1.5V, VAOUT = 2V		-26		μA
	VRMS = 1.5V, VAOUT = 5V		-190		μA
	VRMS = 5V, VAOUT = 2V		-3		μA
	VRMS = 5V, VAOUT = 5V		-17		μA
Gain Constant	Refer to Note 1	-0.95	-0.85	-0.75	1/V

**ELECTRICAL CHARACTERISTICS:** Unless otherwise specified: VCC = 18V, RVS = 23k, CT = 470pF, CI = 150pF, VRMS = 1.5V, IAC = 100μA, ISENSE = 0V, CAO = 4V, VAOUT = 3.5V, VSENSE = 3V. -40°C to 85°C (UC2855A/B), 0°C to 70°C (UC3855A/B).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>Gate Driver Output</b>					
Output High Voltage	I <sub>OUT</sub> = -200mA, VCC = 15V	12	12.8		V
Output Low Voltage	I <sub>OUT</sub> = 200mA		1	2.2	V
Output Low Voltage	I <sub>OUT</sub> = 10mA		300	500	mV
Output Low (UVLO)	I <sub>OUT</sub> = 50mA, VCC = 0V		0.9	1.5	V
Output RISE/FALL Time	C <sub>LOAD</sub> = 1nF		35		ns
Output Peak Current	C <sub>LOAD</sub> = 10nF	0.5	1.5		A
<b>ZVT</b>					
ZVS Threshold		2.3	2.6	2.9	V
Input Bias Current	V = 2.5V, V <sub>CT</sub> = 0		6	20	μA
Propagation Delay	Measured at ZVTOUT		100		ns
Maximum Pulse Width			400		ns
Output High Voltage	I <sub>OUT</sub> = -100mA, VCC = 15V	12	12.8		V
Output Low Voltage	I <sub>OUT</sub> = 100mA		1	2.2	V
Output Low Voltage	I <sub>OUT</sub> = 10mA		300	900	mV
Output Low (UVLO)	I <sub>OUT</sub> = 50mA, VCC = 0V		0.9	1.5	V
Output RISE/FALL Time	C <sub>LOAD</sub> = 1nF		35		ns
Output Peak Current	C <sub>LOAD</sub> = 10nF	0.25	0.75		A
<b>Current Synthesizer</b>					
ION to CS Offset	V <sub>ION</sub> = 0V		30	50	mV
CI Discharge Current	IAC = 50μA	105	118	140	μA
	IAC = 500μA		5		μA
IAC Offset Voltage		0.3	0.65	1.1	V
ION Buffer Slew Rate			10		V/μs
ION Input Bias Current	V <sub>ION</sub> = 2V		2	15	μA
RVS Output Voltage	23k from RVS to GND	2.87	3	3.13	V

Note 1: Gain constant (K) =  $\frac{IAC \cdot (VA_{OUT} - 1.5V)}{(V_{RMS}^2 \cdot IMO)}$  at V<sub>RMS</sub> = 1.5V, VA<sub>OUT</sub> = 5.5V.

## PIN DESCRIPTIONS

**CA** This is the inverting input to the current amplifier. Connect the required compensation components between this pin and CAOUT. The common mode operating range for this input is between -0.3V and 5V.

**CAO:** This is the output of the wide bandwidth current amplifier and one of the inputs to the PWM duty cycle comparator. The output signal generated by this amplifier commands the PWM to force the correct input current. The output can swing from 0.1V to 7.5V.

**CI:** The level shifted current sense signal is impressed upon a capacitor connected between this pin and GND. The buffered current sense transformer signal charges the capacitor when the boost switch is on. When the switch is off, the current synthesizer discharges the capacitor at a rate proportional to the di/dt of the boost inductor current. In this way, the discharge current is approximately equal to

$$\frac{3V}{RRVS} - \frac{IAC}{4}$$

Discharging the CI capacitor in this fashion, a “reconstructed” version of the inductor current is generated using only one current sense transformer.

**PIN DESCRIPTIONS (cont.)**

**CS:** The reconstructed inductor current waveform generated on the CI pin is level shifted down a diode drop to this pin. Connect the current amplifier input resistor between CS and the inverting input of the current amplifier. The waveform on this pin is compared to the multiplier output waveform through the average current sensing current amplifier. The input to the peak current limiting comparator is also connected to this pin. A voltage level greater than 1.5 volts on this pin will trip the comparator and disable the gate driver output.

**CT:** A capacitor from CT to GND sets the PWM oscillator frequency according to the following equation:

$$f \approx \frac{1}{11200 \bullet CT}$$

Use a high quality ceramic capacitor with low ESL and ESR for best results. A minimum CT value of 200pF insures good accuracy and less susceptibility to circuit layout parasitics. The oscillator and PWM are designed to provide practical operation to 500kHz.

**GND:** All voltages are measured with respect to this pin. All bypass and timing capacitors connected to GND should have leads as short and direct as possible.

**GTOUT:** The output of the PWM is a 1.5A peak totem pole MOSFET gate driver on GTOUT. A series resistor between GTOUT and the MOSFET gate of at least 10 ohms should be used to limit the overshoot on GTOUT. In addition, a low Vf Schottky diode should be connected between GTOUT and GND to limit undershoot and possible erratic operation.

**IAC:** This is a current input to the multiplier. The current into this pin should correspond to the instantaneous value of the rectified AC input line voltage. This is accomplished by connecting a resistor directly between IAC and the rectified input line voltage. The nominal 650mV level present on IAC negates the need for any additional compensating resistors to accommodate for the zero crossings of the line. A current equal to one fourth of the IAC current forms one of the inductor current synthesizer inputs.

**IMO:** This is the output of the multiplier, and the non-inverting input of the current amplifier. Since this output is a current, connect a resistor between this pin and ground equal in value to the input resistor of the current amplifier. The common mode operating range for this pin is -0.3V to 5V.

**ION:** This pin is the current sensing input. It should be connected to the secondary side output of a current sensing transformer whose primary winding is in series with the boost switch. The resultant signal applied to this input is buffered and level shifted up a diode to the CI capacitor on the CI pin. The ION buffer has a source only output. Discharge of the CI cap is enabled through the current synthesizer circuitry. The current sense transformer termination resistor should be designed to obtain a 1V input signal amplitude at peak switch current.

**OVP:** This pin senses the boost output voltage through a voltage divider. The enable comparator input is TTL compatible and can be used as a remote shutdown port. A voltage level below 1.8V, disables VREF, oscillator, and the PWM circuitry via the enable comparator. Between 1.8V and VREF (7.5V) the UC is enabled. Voltage levels above 7.5V will set the PWM latch via the hysteretic OVP comparator and disable both ZVTOUT and GTOUT until the OVP level has decayed by the nominal hysteresis of 400mV. If the voltage divider is designed to initiate an OVP fault at 5% of OV, the internal hysteresis enables normal operation again when the output voltage has reached its nominal regulation level. Both the OVP and enable comparators have direct logical connections to the PWM output and exhibit typical propagation delays of 200ns.

**REF:** REF is the output of the precision reference. The output is capable of supplying 25mA to peripheral circuitry and is internally short circuit current limited. REF is disabled and low whenever VCC is below the UVLO threshold, and when OVP is below 1.8V. A REF "GOOD" comparator senses REF and disables the stage until REF has attained approximately 90% of its nominal value. Bypass REF to GND with a 0.1μF or larger ceramic capacitor for best stability.

**RVS:** The nominal 3V signal present on the VSENSE pin is buffered and brought out to the RVS pin. A current proportional to the output voltage is generated by connecting a resistor between this pin and GND. This current forms the second input to the current synthesizer.

**SS:** Soft-start V<sub>SS</sub> is discharged for V<sub>VCC</sub> low conditions. When enabled, SS charges an external capacitor with a current source. This voltage is used as the voltage error signal during start-up, enabling the PWM duty cycle to increase slowly. In the event of a V<sub>VCC</sub> dropout, the OVP/EN is forced below 1.8V (typ), SS quickly discharges to disable the PWM.

### PIN DESCRIPTIONS (cont.)

**VAO:** This is the output of the voltage amplifier. At a given input RMS voltage, the voltage on this pin will vary directly with the output load. The output swing is limited from approximately 100mV to 6V. Voltage levels below 1.5V on this pin will inhibit the multiplier output.

**VCC:** Positive supply rail for the IC. Bypass this pin to GND with a 1 $\mu$ F low ESL, ESR ceramic capacitor. This pin is internally clamped to 20V. Current into this clamp should be limited to less than 10mA. The UC3855A has a 15.5V (nominal) turn on threshold with 6 volts of hysteresis while the UC3855B turns on at 10.5V with 500mV of hysteresis.

**VRMS:** This pin is the feedforward line voltage compensation input to the multiplier. A voltage on VRMS proportional to the AC input RMS voltage commands the multiplier to alter the current command signal by  $1/VRMS^2$  to maintain a constant power balance. The input to VRMS is generally derived from a two pole low pass filter/voltage divider connected to the rectified AC input voltage. This feature allows universal input supply voltage operation and faster response to input line fluctuations for the PFC boost preregulator. For most designs, a voltage level of 1.5V on this pin should correspond to low line, and 4.7V for high line. The input range for this pin extends from 0 to 5.5V.

**VSENSE:** This pin is the inverting input of the voltage amplifier and serves as the output voltage feedback point for the PFC boost converter. It senses the output voltage through a voltage divider which produces a nominal 3V. The voltage loop compensation is normally connected between this pin and VAO. The VSENSE pin must be above 1.5V at 25°C, (1.9V at -55°C) for the current synthesizer to work properly.

**ZVS:** This pin senses when the drain voltage of the main MOSFET switch has reached approximately zero volts, and resets the ZVT latch via the ZVT comparator. A minimum and maximum ZVTOUT pulse width are programmable from this pin. To directly sense the  $\approx 400V$  drain voltage of the main switch, a blocking diode is connected between ZVS and the high voltage drain. When the drain reaches 0V, the level on ZVS is  $\approx 0.7V$  which is below the 2.6V ZVT comparator threshold. The maximum ZVTOUT pulse width is approximately equal to the oscillator blanking period time.

**ZVTOUT:** The output of the ZVT block is a 750mA peak totem pole MOSFET gate driver on ZVTOUT. Since the ZVT MOSFET switch is typically 3X smaller than the main switch, less peak current is required from this output. Like GTOUT, a series gate resistor and Schottky diode to GND are recommended. This pin may also be used as a high current synchronization output driver.

For more information see Unitrode Applications Note U-153.

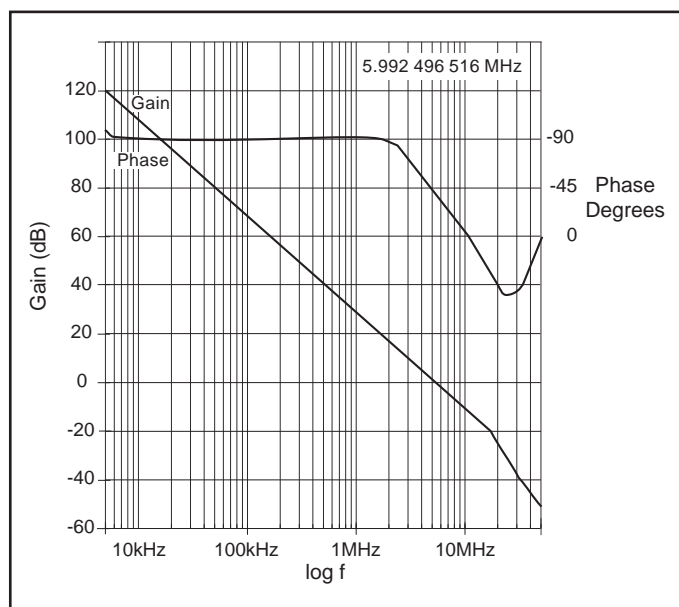


Figure 1. Current Amplifier Frequency Response

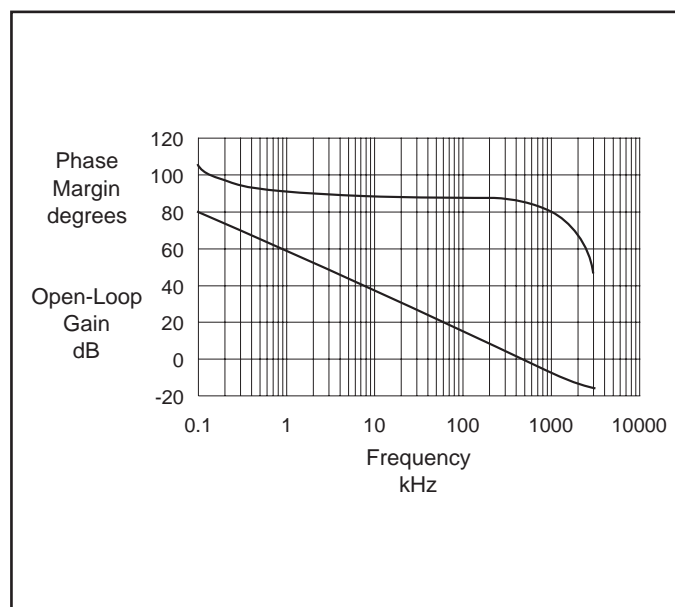


Figure 2. Voltage Amplifier Gain Phase vs Frequency

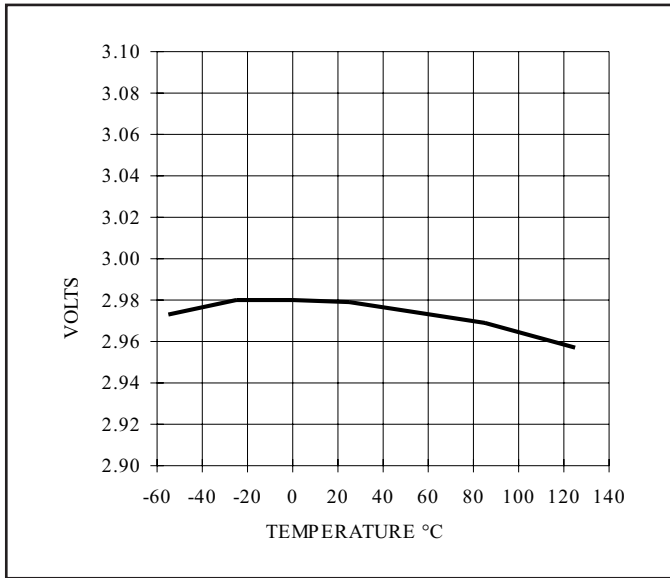


Figure 3. Voltage Amplifier Input Threshold

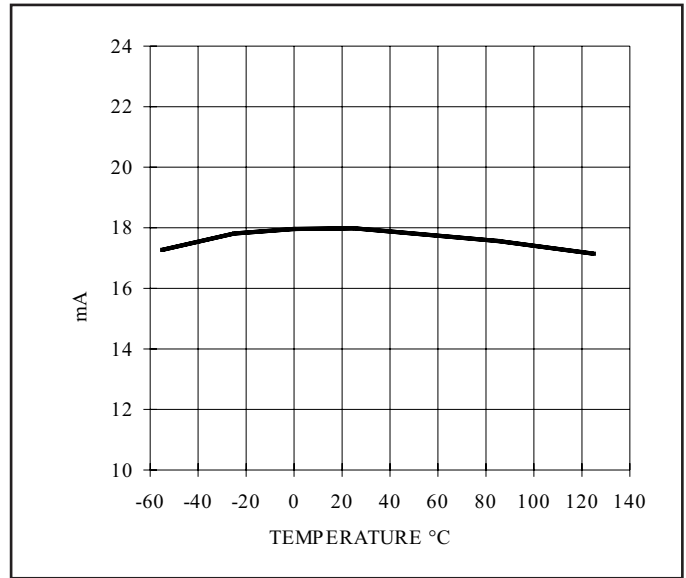


Figure 4. Supply Current ON

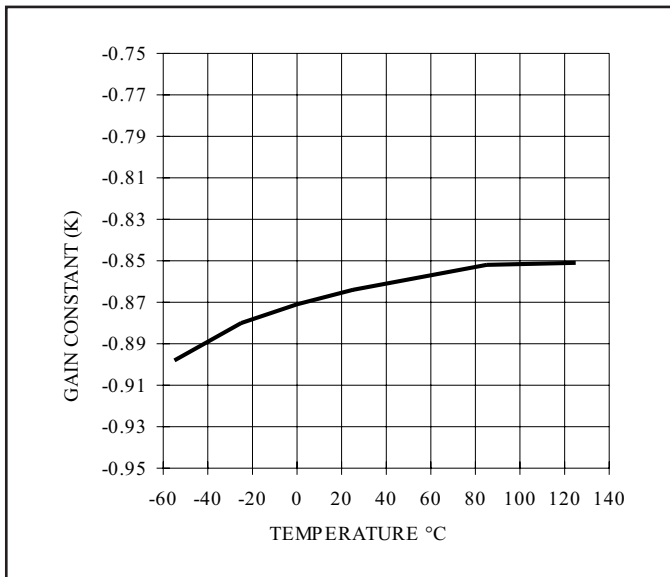


Figure 5. Multiplier Current Gain Constant

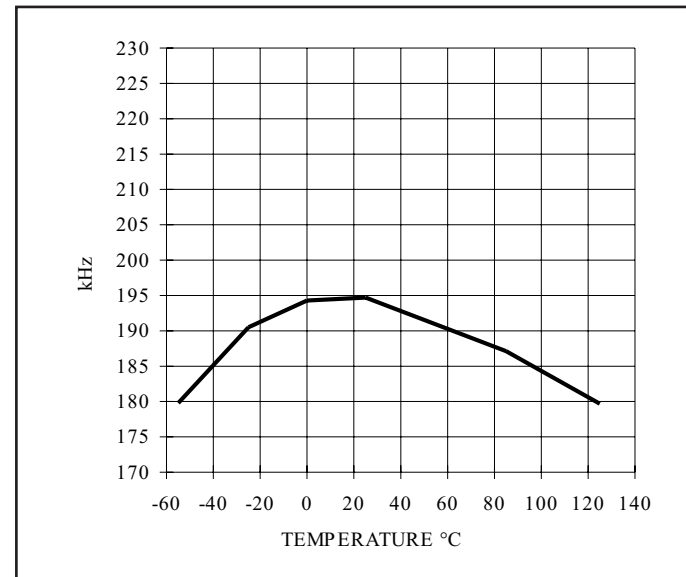
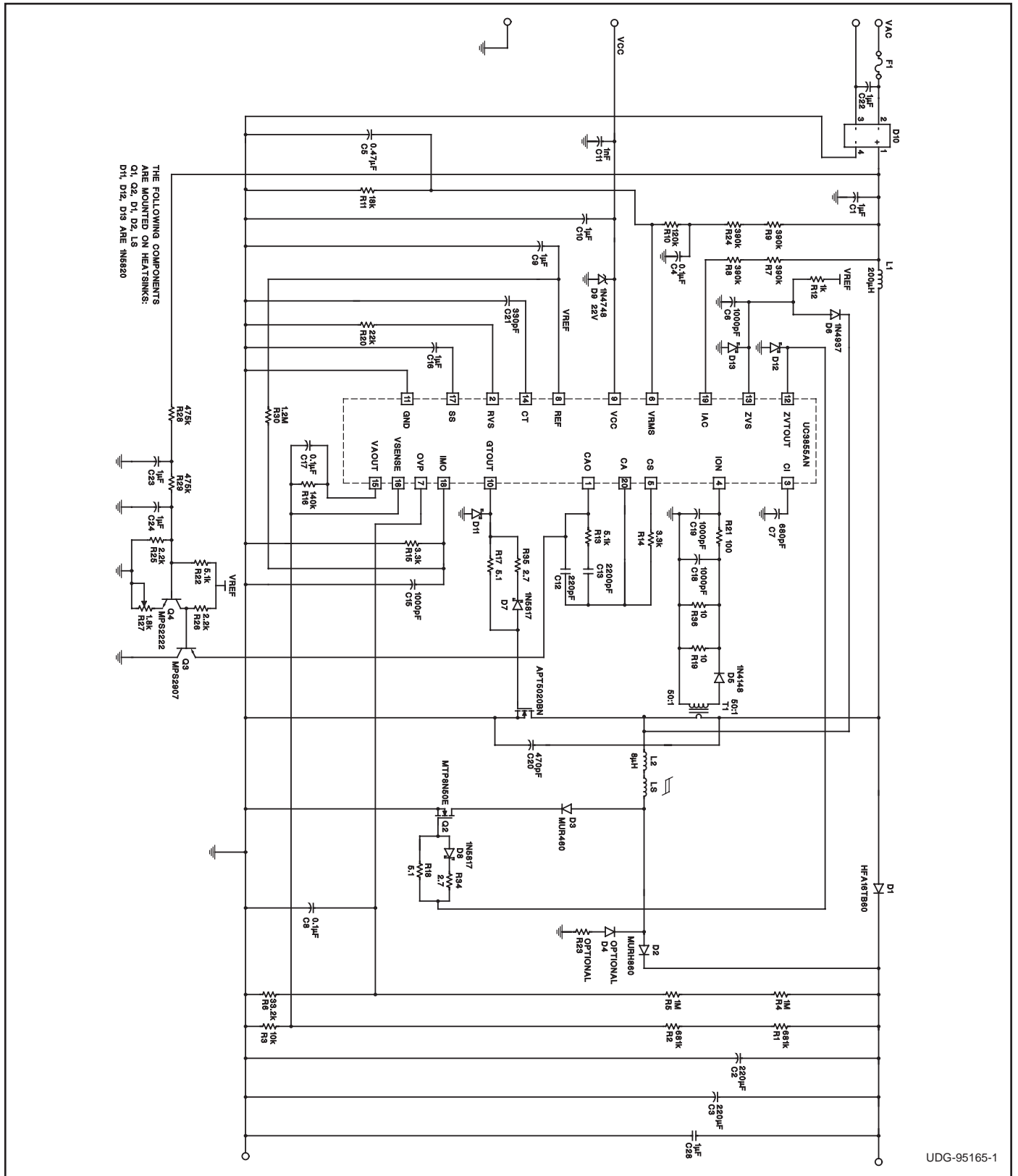


Figure 6. Oscillator Initial Accuracy

TYPICAL APPLICATION



UDG-95165-1

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">UC2855ADW</a>	NRND	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2855ADW
UC2855ADW.A	NRND	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2855ADW
<a href="#">UC2855BDW</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2855BDW
UC2855BDW.A	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2855BDW
<a href="#">UC2855BDWTR</a>	NRND	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2855BDW
UC2855BDWTR.A	NRND	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UC2855BDW
<a href="#">UC2855BN</a>	NRND	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2855BN
UC2855BN.A	NRND	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	UC2855BN
<a href="#">UC3855ADW</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3855ADW
UC3855ADW.A	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3855ADW
<a href="#">UC3855ADWTR</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3855ADW
UC3855ADWTR.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3855ADW
<a href="#">UC3855BDW</a>	NRND	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3855BDW
UC3855BDW.A	NRND	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3855BDW
UC3855BDWG4	NRND	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3855BDW
<a href="#">UC3855BDWTR</a>	NRND	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3855BDW
UC3855BDWTR.A	NRND	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UC3855BDW
<a href="#">UC3855BN</a>	NRND	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3855BN
UC3855BN.A	NRND	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3855BN
UC3855BNG4	NRND	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	UC3855BN

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

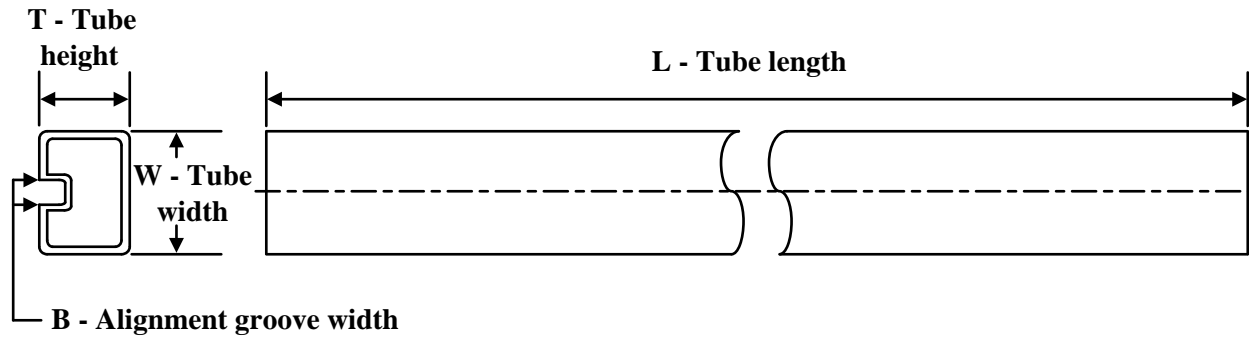

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2855BDWTR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
UC3855ADWTR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
UC3855BDWTR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2855BDWTR	SOIC	DW	20	2000	356.0	356.0	45.0
UC3855ADWTR	SOIC	DW	20	2000	356.0	356.0	45.0
UC3855BDWTR	SOIC	DW	20	2000	356.0	356.0	45.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UC2855ADW	DW	SOIC	20	25	507	12.83	5080	6.6
UC2855ADW.A	DW	SOIC	20	25	507	12.83	5080	6.6
UC2855BDW	DW	SOIC	20	25	507	12.83	5080	6.6
UC2855BDW.A	DW	SOIC	20	25	507	12.83	5080	6.6
UC2855BN	N	PDIP	20	20	506	13.97	11230	4.32
UC2855BN.A	N	PDIP	20	20	506	13.97	11230	4.32
UC3855ADW	DW	SOIC	20	25	507	12.83	5080	6.6
UC3855ADW.A	DW	SOIC	20	25	507	12.83	5080	6.6
UC3855BDW	DW	SOIC	20	25	507	12.83	5080	6.6
UC3855BDW.A	DW	SOIC	20	25	507	12.83	5080	6.6
UC3855BDWG4	DW	SOIC	20	25	507	12.83	5080	6.6
UC3855BN	N	PDIP	20	20	506	13.97	11230	4.32
UC3855BN.A	N	PDIP	20	20	506	13.97	11230	4.32
UC3855BNG4	N	PDIP	20	20	506	13.97	11230	4.32

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025