Application Report

DLP3021-Q1 Dynamic Ground Projection System Design

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ABSTRACT

To be used in the widest variety of areas around the vehicle, projector systems must be compact and low cost. In many applications, a projector accepts a standard video signal over HDMI or FPD-Link. However, in many areas of the vehicle where it would be desirable to place a projector, there is no access to a high-speed bus to relay video information. In some cases, there may not even be CAN or LIN available to communicate with a remote projector. Due to these limitations, a new system architecture was developed that addresses these issues. By removing the need for a microcontroller or GPU to provide content to the projection system, a projector can be placed wherever needed around the vehicle and the only wiring required is power and ground. This enables new opportunities for vehicle customization and communication that were previously unavailable or limited to static, single-image projection. This application report introduces the dynamic ground projection (DGP) system architecture and will address the major electrical differences between it and traditional projection systems used in head-up displays or headlights.

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Trademarks

1 Typical Automotive System Architecture

A typical DLP® automotive projector system as shown in Figure 1-1 uses solid state illumination and a DMD controller such as the DLPC120 or DLPC230 for applications similar to head-up display (HUD) or high-resolution headlight. The controller has an input for video data and an output for DMD data, DMD control signals, and illumination control signals. Each frame of video is read by the controller, processed, and converted to a set of DMD native format bit-planes. These bit-planes set the state of the DMD mirrors and cause light to be reflected toward the projection optics or away from the projection optics. Each bit-plane is associated with an illumination color. Each time a bit-plane is loaded and displayed control signals from the DMD controller enable the correct illuminator. As each bit-plane is loaded, the viewer's vision system combines the bit-planes into a single full color video frame.

While this approach provides the maximum flexibility for system design, it also leads to a number of system requirements that may increase system cost and complexity. This type of system requires a video source such as a CPU/GPU combo that generates the video content or loads it from memory. It may also require a host microcontroller to bring up and configure the DMD controller. The DMD controller itself also requires RAM for either an external or internal frame buffer depending on the controller architecture. If space is a concern then the host processor and GPU may need be located remotely. This requires that a high-speed video bus be added to the system which may include serializers/deserializers along with specialized cables and connectors. While all of this is appropriate where you have a system critical display that requires constantly updated information from the ADAS system such as a HUD, it may not be appropriate for dynamic ground projection displays where only a limited subset of information needs to be displayed for a short period of time.

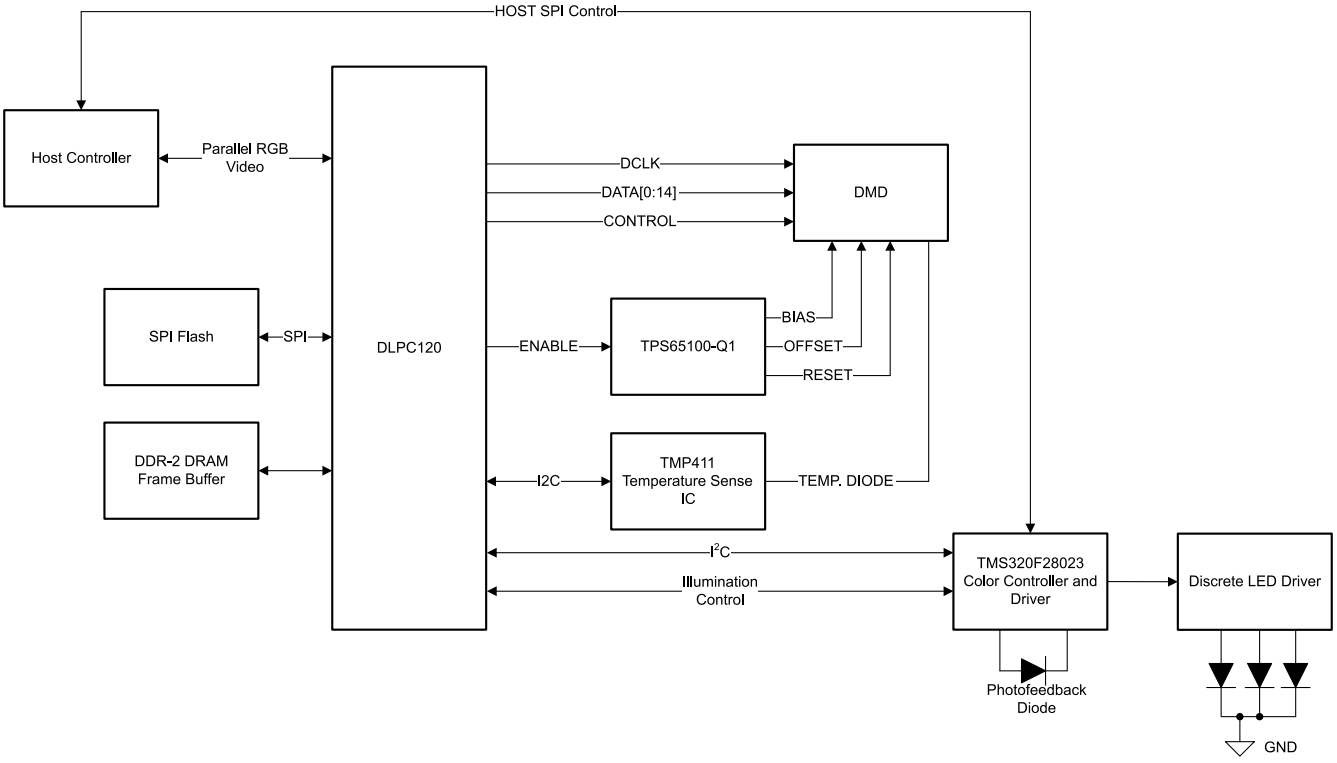

Figure 1-1. HUD Simplified Schematic

2 Dynamic Ground Projection

Figure 2-1 shows a simplified block diagram for a DLP3021-Q1 based dynamic ground projector. The DLP3021-Q1 dynamic ground projection system architecture is designed to reduce the need for external components while still supporting high quality, full color images and animations. To remove the need for a GPU to generate content, the DLPC120-Q1 DMD controller has been replaced with an automotive qualified Xilinx Spartan®-7 FPGA that streams content from SPI flash directly to the DMD.

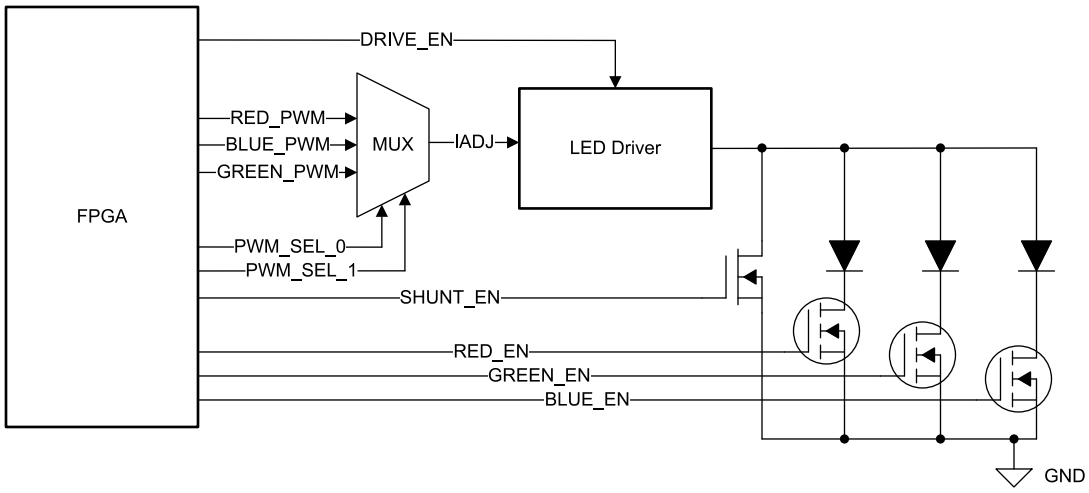

Figure 2-1. Dynamic Ground Projection Simplified Schematic

Rather than processing an arbitrary video stream from a GPU, the FPGA loads pre-processed content directly from a flash device to the DMD array. To load the high resolution DMD quickly enough, a SPI flash part with an octal interface is used to support the bandwidth required. On power-up the FPGA automatically begins loading video content and on power loss the FPGA automatically executes the DMD power down sequence. The overall design and operation process is shown in Figure 2-2.

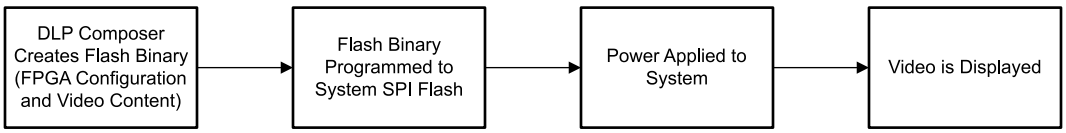

Figure 2-2. System Programming Flow

Videos can be loaded into a tool called DLP Composer which takes each frame of video content and pre-renders them into individual bit-planes in DMD native format. DLP Composer then compresses and combines the individual bit planes, any default start-up conditions, and the FPGA configuration into a single flash binary as shown in Figure 2-3.

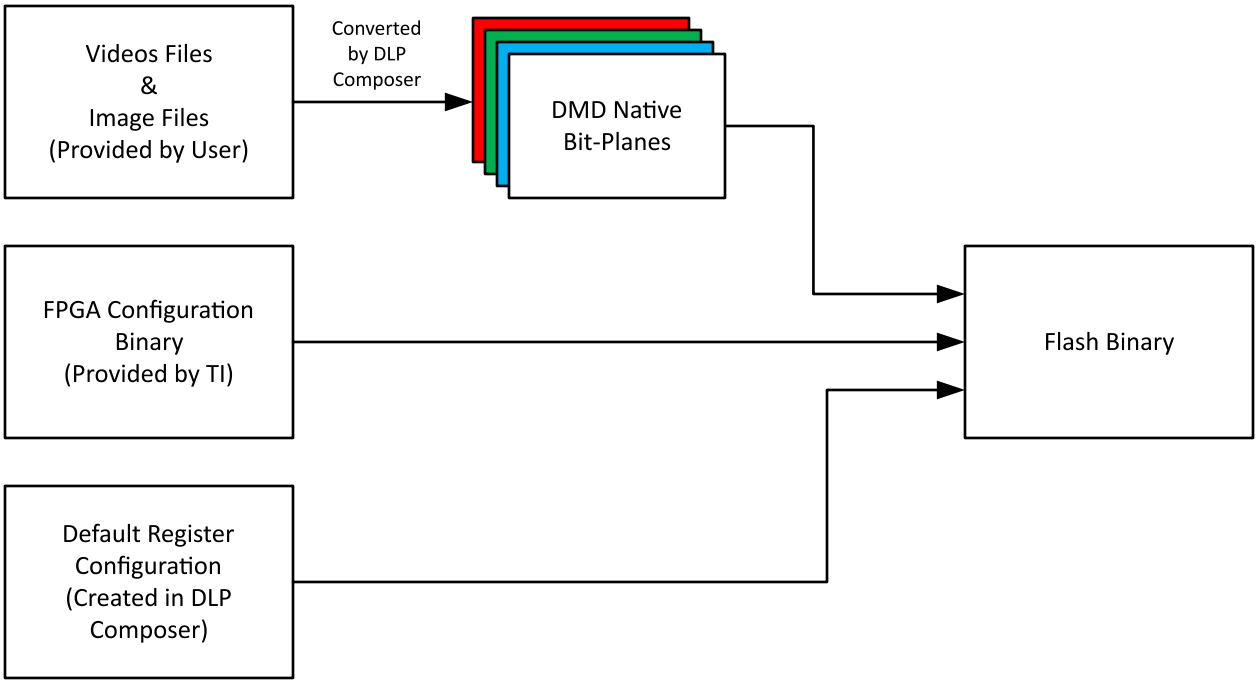

Figure 2-3. DLP Composer DGP Process Example

When power is applied to the system, the FPGA configuration is loaded to the FPGA. Depending on the default configuration, the FPGA begins loading bit-planes to the DMD and sequencing the LED enables for each bit plane loaded. Alternatively, a microcontroller can issue commands to the FPGA via SPI to enable video playback, change videos, read DMD temperature via the TMP411, or adjust current levels to the LEDs.

3 LED Driver

To achieve a high quality image, the LED illumination must be precisely timed with the image displayed on the DMD. The FPGA generates signals to support the required timing as shown in Figure 3-1. There is an LED enable signal for the overall LED driver and an individual enable for each LED color. This signal drives a low side driver MOSFET for each color as well as a shunt MOSFET for quickly turning off the illumination. The FPGA also generates a PWM for each color and two PMW select signals, allowing the 3 PWMs to be muxed to the current control pin of the LED driver. This gives the ability to select different current limits for each of the colors, which is important for color calibration and dimming the image for thermal derating. For example, if the projector is left on for an extended period of time, you may want to reduce the LED current but still allow an image to be displayed. The DGP reference design uses an LM3409 current control buck LED driver and is powered directly from the vehicle battery voltage. If another LED driver is selected, it's important that the driver can support shunt FET dimming; so a boost regulator could not be used here.

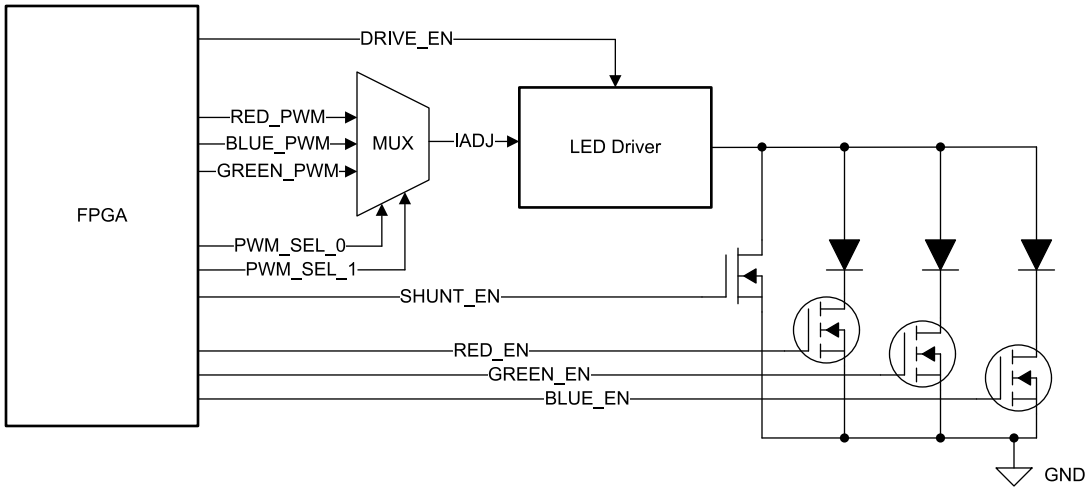

Figure 3-1. LED Driver Simplified Schematic

4 Flash Storage Space Requirements

The SPI flash device in the DGP system needs to be fast enough to support loading content directly from flash to the DMD. Due to the high bandwidth requirements, an octal-SPI flash device compatible with the JEDEC xSPI protocol was chosen for this application. In the DGP application all of the content for a dynamic ground projection system is pre-processed into DMD native format and compressed using RLE (run length encoding) on a PC and then loaded onto the SPI flash. Ideally an arbitrarily large flash part would be used but to optimize system bill of materials cost it's important to minimize the amount of flash storage in the system.

To estimate the amount of storage space required for each frame of video the required parameters are:

- DMD Array Width, W
- DMD Array Height, H
- Number of bit-planes, BP
- Compression Ratio, C

The storage space required (in bits) can be calculated by:

$$\frac{W \times H \times BP}{C} \quad (1)$$

For the DLP3021-Q1 DLP Composer project and FPGA configuration in the DLP3021-Q1 product folder on TI.com, the following values can be used

- W = 608
- H = 684
- BP = 20
- C = 2.1 (estimated, depending on content see Table 4-1)

The width and height is set by the number of mirrors on the DMD. For the dynamic ground application, every mirror location must be loaded with data. The number of bit-planes is not fixed and can be adjusted depending on the system requirements. For example, in the case of a single illumination source, white light only module, you may only need to use six to eight total bit-planes. The RLE compression ratio is dependent on content. Images with fine detail such as live video may not compress as well as image with large solid fields of color such as animations. The compression ratio of 2.1:1 is used as a rough estimate of what you may expect to see across various types of content, although the worst case would always be slightly less than 1:1. Table 4-1 shows a few examples of how different image content compresses. The "1x1 checkerboard" pattern is an image where every alternating pixel is black or white. This is a type of worst case image where the content is not compressible and you still have the overhead from the compression algorithm causing the resulting compressed frame to be slightly larger than the uncompressed frame. This is for example only and is not typical of real-world images.

Table 4-1. Compression Examples

Image	Description	Size (Bytes)	Compression Factor
	Any Uncompressed	1,070,080	1.0
	1 x 1 checkerboard	1,102,000	0.97
	Complex	520,683	2.1
	Animation	273,963	3.9
	Simple BW (Rendered with RGB)	162,897	6.6

When the approximate storage size of each frame of video is determined, you can multiply it by the typical 25Hz frame rate to estimate the amount of storage required for your content. With the parameters above, it is possible to store approximately twenty seconds of full-color content in a 2Gb flash device. It is possible to significantly increase the amount of content stored by carefully choosing the type of content and choosing the correct illumination (RGB or single color) to match the type of content being displayed.

5 Summary

To support placement throughout the vehicle, projectors for dynamic ground projection must be small, low-cost, and able to operate independent of a video input. The DLP3021-Q1 DMD and FPGA based controller solution provide a simplified architecture to support dynamic ground projection. When designing these systems, it's important to understand the differences between this architecture and other traditional projection system architectures. With careful planning and content selection it's possible to optimize the bill of materials and create smaller projectors with fewer components. For additional questions regarding dynamic ground projection or other DLP Automotive applications please visit the TI E2E™ support forums.

6 References

- Texas Instruments, DLP3021-Q1 Product Folder
- Texas Instruments, DLP3021-Q1 0.3-Inch WVGA DMD Data Sheet
- Texas Instruments, DLP3021-Q1 FPGA User's Guide
- Texas Instruments, DLP Composer for DGP Application Software
- Texas Instruments, DLPC120-Q1 Automotive DMD Controller Data Sheet
- Texas Instruments, DLPC230-Q1 Automotive DMD Controller for the DLP553x-Q1 Chipset Data Sheet

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