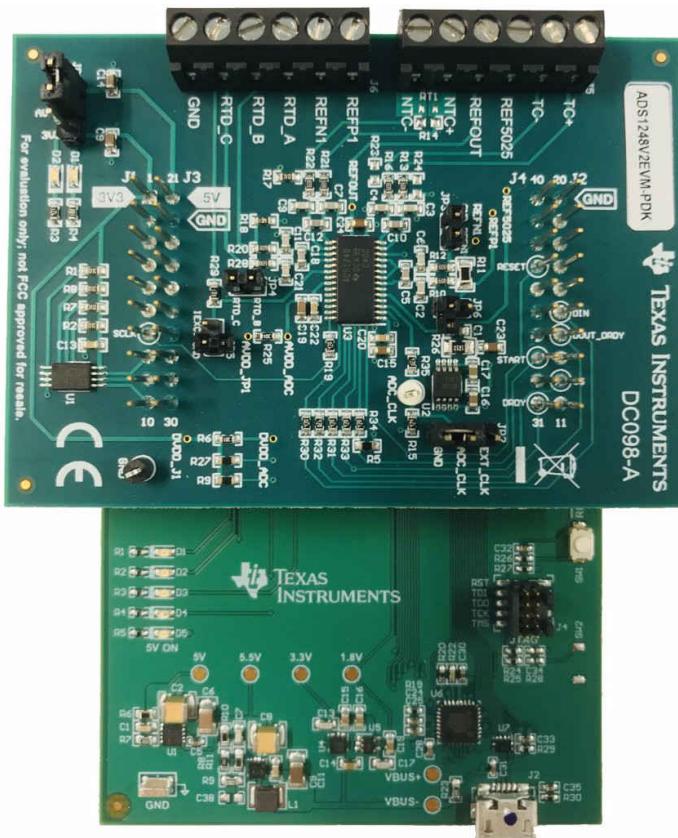


ABSTRACT

The ADS1x48 evaluation module (EVM) allows users to evaluate the functionality of the Texas Instruments' 16-bit ADS1148 or the 24-bit ADS1248. ADS1x48 refers to what is common to both devices and EVMs. Any differences in operation between the devices or EVMs are listed separately. The ADS1x48 devices are highly integrated delta-sigma ADCs that include a programmable gain amplifier, a 2.048-V voltage reference, an internal oscillator, dual current sources (IDACs), and several system-monitoring features. Each ADS1x48 device has inputs that can be configured as seven single-ended or four differential inputs. All of these features integrated into the ADS1x48 devices enable precision measurement for many types of analog temperature sensors including thermocouples, resistance temperature detectors (RTDs), and thermistors. This user's guide describes both the EVM hardware platform and the graphical user interface (GUI) software used to configure and operate the device. This user's guide also includes the EVM schematic diagram, board layout, and bill of materials. The EVM platform eases the evaluation of the ADS1x48 device with hardware, software, and computer connectivity through the universal serial bus (USB) interface.

Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the *ADS1x48EVM*.



ADS1x48 Evaluation Module (ADS1248EVM Shown)

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1 Introduction

The ADS1x48EVM is a fully assembled evaluation platform designed to highlight the ADS1x48 features and modes of operation that make this device suitable for measuring analog temperature sensors. The EVM sits on top of an accompanying precision ADC motherboard (PAMBoard) used as a USB-to-PC GUI communication bridge. This board combination also serves as an example implementation of connecting a microcontroller (MCU) to communicate with the ADS1x48 device through a serial-peripheral interface (SPI). [Figure 1-1](#) shows a functional block diagram for the ADS1x48EVM.

Note

The ADS1x48EVM requires an external controller to evaluate the ADS1x48 device.

The PAMBoard is controlled by commands received from the ADS1x48EVM GUI, and returns data to the GUI for display and analysis. If the PAMBoard is not used, the EVM plug-in module format allows for an alternative external host to communicate with the ADS1x48 through the pin headers J1 through J4. Header connections are identified in [Section 5.2](#) and listed in [Table 3-2](#).

The combined ADS1x48EVM and PAMBoard incorporate the following features:

- ADS1x48, a 16- or 24-bit delta-sigma ADC with eight input channels
- Input terminal block and jumper configurations that enable easy measurement of many types of analog temperature sensors
- Analog voltage (AVDD) selection of 3.3-V or 5-V operation for the ADS1x48
- Multiple voltage reference options: 2.048-V reference integrated into the ADS1x48, discrete REF5025, ratiometric reference for RTD measurements, or external reference supplied via the input terminal blocks
- Internal or external clock selection
- SPI for communication and configuration

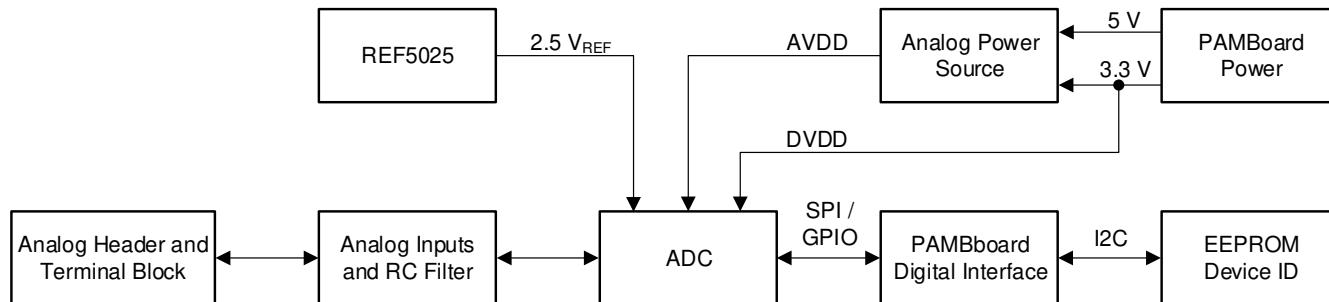


Figure 1-1. ADS1x48EVM Functional Block Diagram

[Table 1-1](#) lists documents related to the ADS1x48EVM.

Table 1-1. Related Documentation

Device	Literature Number
ADS1248	SBAS426
ADS1148	SBAS453
REF5025	SBOS410

2 Getting Started With the ADS1x48EVM

The following list of steps provides an overview to quickly get the ADS1x48EVM setup and operational. The subsequent sections in this document expand on each step in order to explain in detail the available features on the ADS1x48EVM and the corresponding GUI. Links are provided to navigate from this quick-start guide to the appropriate section at each step, where applicable.

1. Remove the ADS1x48EVM, PAMBoard, and USB cable from the ADS1x48EVM box.
2. If necessary, connect the ADS1x48EVM to the PAMBoard as shown in the left image in [Figure 2-1](#).
3. Set the ADS1x48EVM jumpers to the desired location:
 - a. [Power](#)
 - b. [Clock](#)
 - c. [RTD connections \(if applicable\)](#)
4. Connect the micro-USB-to-USB cable from the PAMBoard directly to a USB port on the computer. Do not connect the cable through a USB hub.
5. Open up the web-based GUI available on the EVM landing page ([ADS1148EVM-PDK](#) or [ADS1248EVM-PDK](#)).
 - a. First-time users may be [prompted to download and install](#) the browser extension for Firefox™ or Chrome™ and the TI Cloud Agent Application. Installing the TI Cloud Agent is a one-time download and installation.
6. Refresh the GUI such that a green signal displays and the *Hardware Connected* indicator shows in the bottom status ribbon (see [Figure 4-2](#)).
7. Select the desired [ADC reference voltage](#).
8. [Connect your sensors or signals](#) to the input terminal blocks (J5 and J6).
9. [Capture and analyze data](#) using the GUI.

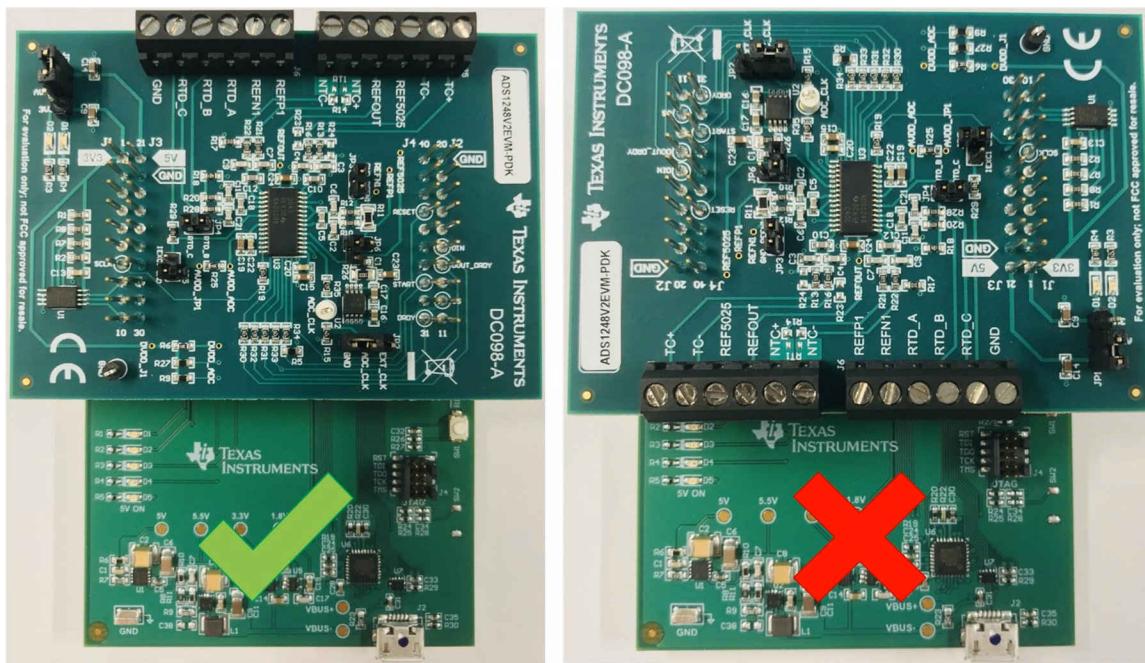


Figure 2-1. Connecting the ADS1x48EVM to the PAMBoard

3 ADS1x48EVM Overview

Various onboard components are used to provide power to, communicate with, and interface the analog input to the ADS1x48 device.

3.1 Analog and Digital Power Supplies

The ADS1x48 supports a wide unipolar analog supply voltage (AVDD) range from 2.7 V to 5.5 V and a bipolar AVDD of ± 2.5 V. The ADS1x48EVM AVDD can be set to either 3.3 V or 5 V. Power is supplied from the USB 5-V source to the PAMBoard. However, the USB power-supply voltage is not consistent from PC to PC. A DC/DC converter on the PAMBoard increases the USB output to 5.5 V. A linear low-dropout (LDO) regulator uses this 5.5-V output to provide clean and stable 5-V and 3.3-V supplies from the PAMBoard to the ADS1x48EVM.

Two LEDs light up on the PAMBoard, as shown in [Figure 3-1](#), when the USB cable is plugged into the computer. The top LED (D1) indicates that the ADS1x48EVM is ready to communicate with the GUI. The bottom LED (D5) indicates that the 5-V output is active.

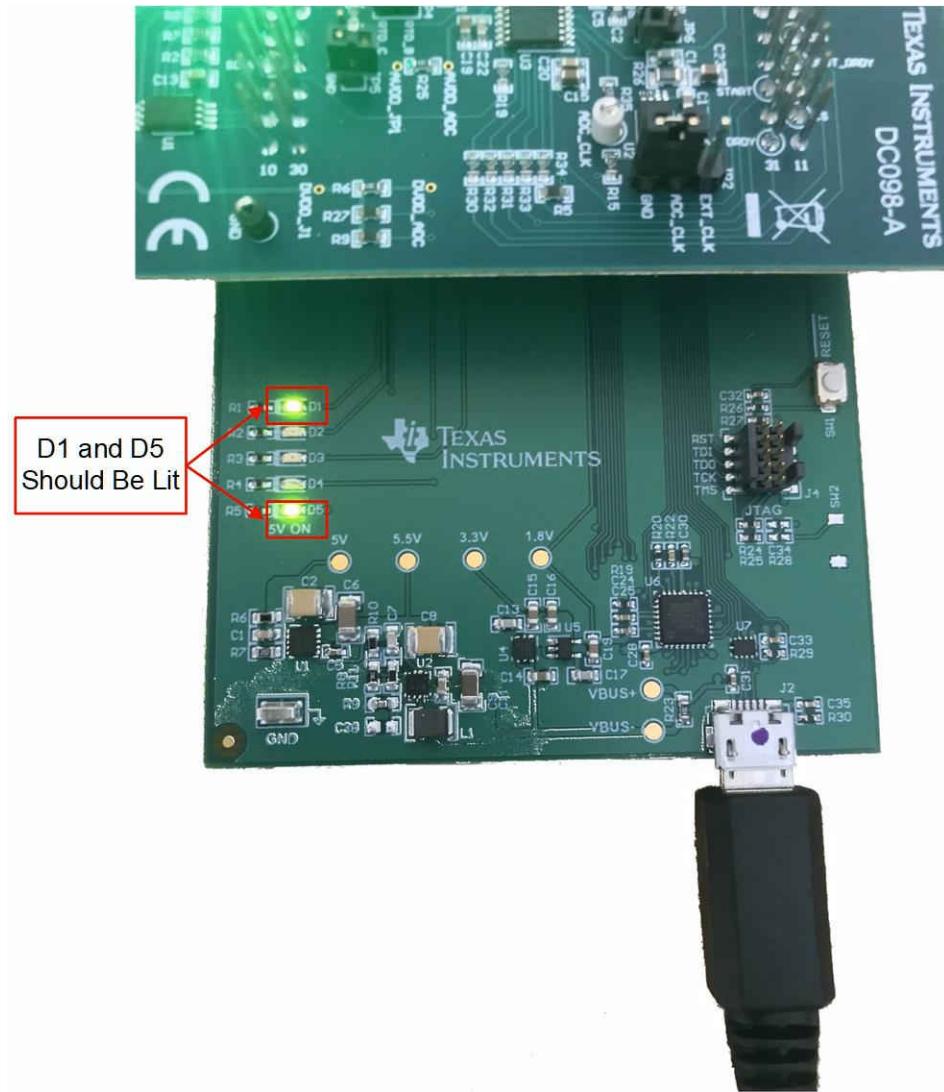


Figure 3-1. LED Indicators D1 and D5

Jumper JP1 selects the ADS1x48 AVDD voltage. When jumper JP1 is in the left position (see [Figure 3-2](#)), AVDD on the ADS1x48 is set to 5 V. When the jumper JP1 is set to the right position, AVDD is set to 3.3 V.

Figure 3-2 also shows two diodes on the ADS1x48EVM that help indicate when power is valid. The top diode (D1) denotes that the 3.3-V output is active. The bottom diode (D2) indicates that AVDD is active after the shunt selection on jumper JP1 is made.

The ADS1x48 devices accept a digital supply voltage (DVDD) range from 2.7 V to 5.25 V. On the ADS1x48EVM, the ADS1x48 DVDD is a fixed value of 3.3 V. As with AVDD, this 3.3-V DVDD is sourced from the USB power-supply voltage and is used as the PAMBoard DVDD.

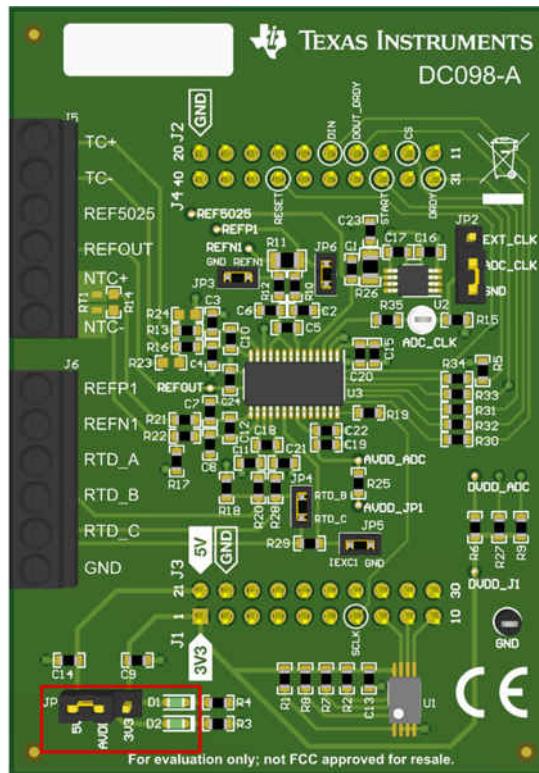


Figure 3-2. Jumper (JP1) Selects AVDD on the ADS1x48EVM

3.2 Voltage Reference Options

The ADS1x48 is a highly flexible ADC that can accept multiple voltage reference (VREF) options. First, the ADS1x48 integrates a low-noise, 2.048-V reference to help reduce overall component count. Moreover, this internal VREF voltage is supplied externally via the ADS1x48 REFOUT pin and is available on terminal block J5. The ADS1x48 also has two sets of differential VREF inputs defined as REFP0, REFN0 and REFP1, REFN1. All of these options are selected via the MUX1 register in the ADS1x48.

The ADS1x48EVM supports four different VREF options to offer maximum flexibility. [Table 3-1](#) details these four options. [Figure 3-3](#) shows the location of each VREF option (highlighted in yellow) as well as each VREF test point (highlighted in red).

Table 3-1. Summary of ADS1x48EVM VREF Options

VREF Mode	VREF Input Channel	Voltage	Location	Test Point	Comment
Internal	—	2.048 V	U3	Output on J5 (REFOUT)	—
External	REF5025	2.5 V	U2	Output on J5 (REF5025)	—
	Ratiometric	Variable	R11	REFP1, REFN1	Used for RTD measurements
	User-provided	Variable	J6 (REFP1, REFN1)	REFP1, REFN1	Remove R11

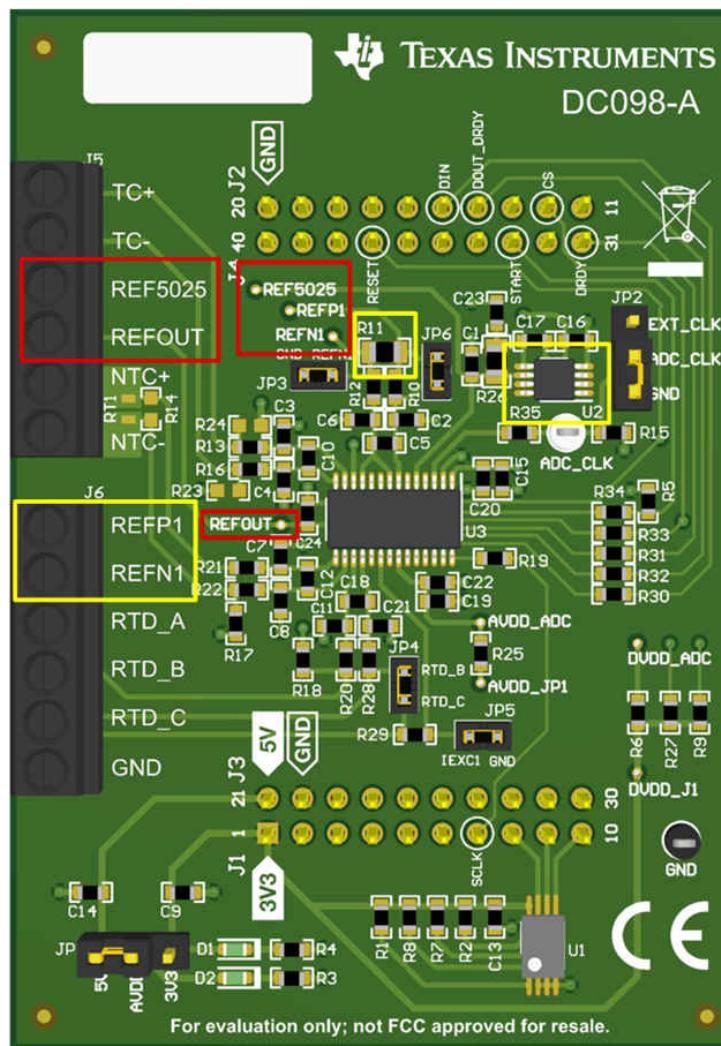


Figure 3-3. ADS1x48EVM VREF Options (Yellow) and Test Points (Red)

3.3 Clock Options

The ADS1x48 integrates a 4.096-MHz clock oscillator to provide the clock signal to the ADC. Additionally, the ADS1x48 offers an external CLK input pin if an external clock signal is required. Choose between these flexible clock options using the JP2 header on the ADS1x48EVM.

Enable the internal oscillator by connecting the shunt to the JP2-3 pin on the JP2 header. This pin is marked *GND* on the [ADS1x48EVM silkscreen](#). Enable an external clock by connecting the shunt to the JP2-1 pin on the JP2 header. This pin is marked *EXT_CLK* on the [ADS1x48EVM silkscreen](#). When the external clock option is chosen, provide the external clock signal via the J4-40 pin on the J4 header. This pin and jumper JP2 are highlighted in [Figure 3-4](#).

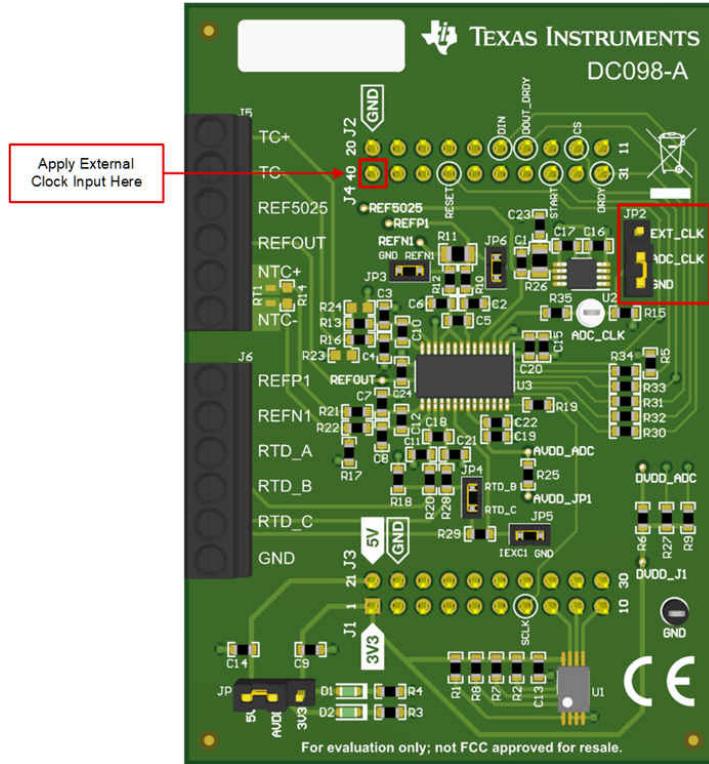


Figure 3-4. ADC Clock Options on the ADS1x48EVM

3.4 Digital Interface

The ADS1x48 devices support the digital SPI and functional modes as detailed in the [24-bit ADS1248 data sheet](#) or the [16-bit ADS1148 data sheet](#). As stated in [Section 3.1](#), the PAMBoard operates at a 3.3-V logic level provided by the host computer and the ADS1x48EVM board uses this same 3.3-V logic level for DVDD.

Digital interface connections from the ADS1x48EVM to the PAMBoard include power, I²C, SPI, and a GPIO connection used to trigger an interrupt at the end of conversion that signifies new data are available. The digital connections are highlighted in the silkscreen shown in [Figure 3-5](#) and are described in detail in [Table 3-2](#). Use these connection points for troubleshooting the SPI communication with a logic analyzer or to attach an external MCU to control the ADS1x48EVM without the PAMBoard.

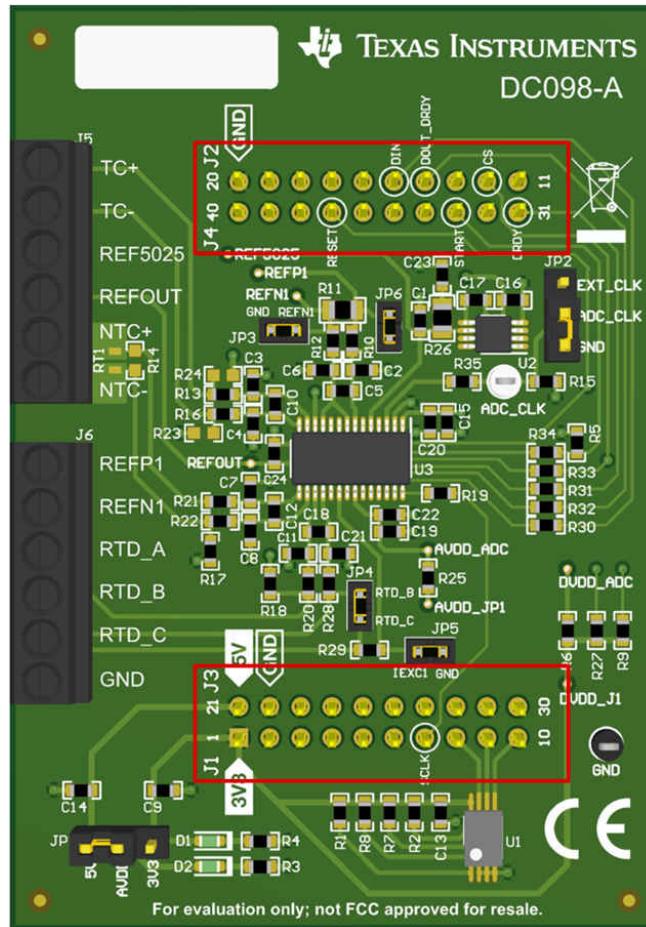


Figure 3-5. ADS1x48EVM-to-PAMBoard Connections

Table 3-2. ADS1x48EVM Header Pinout and Description

Description	Connector	Connector	Description	Description	Connector	Connector	Connector
3.3 V	J1:1	J3:21	5 V		J4:40	J2:20	GND
	J1:2	J3:22	GND		J4:39	J2:19	
	J1:3	J3:23			J4:38	J2:18	
	J1:4	J3:24		RESET	J4:37	J2:17	
	J1:5	J3:25			J4:36	J2:16	
	J1:6	J3:26			J4:35	J2:15	DIN
SPI SCLK	J1:7	J3:27			J4:34	J2:14	DOUT/DRDY
	J1:8	J3:28		START	J4:33	J2:13	
I ² C SCL	J1:9	J3:29			J4:32	J2:12	SPI CS
I ² C SDA	J1:10	J3:30		DRDY	J4:31	J2:11	SPI CS

3.5 Analog Input Connections

The ADS1x48EVM is designed for easy interface to external temperature sensors using the two screw terminal blocks (J5 and J6). Connector J5 provides connections for thermocouples and thermistors as well as the 2.048-V output voltage from the ADS1x48 integrated reference and the dedicated 2.5-V output from the REF5025.

Connector J6 includes a pair of differential reference inputs for connecting an external voltage reference source to the ADC as well as three dedicated terminals for connecting a 2-, 3-, or 4-wire RTD. [Table 3-3](#) summarizes the channel input connections for J5 and J6. Both connectors are clearly labeled on the [PCB silkscreen](#) for easy input connection identification. [Figure 3-6](#) shows the input layout.

Table 3-3. ADS1x48EVM Terminal Block Input Description (J5 and J6)

Terminal Block Input	Label	Description
J5:1	TC+	Positive thermocouple, general-purpose input
J5:2	TC-	Negative thermocouple, general-purpose input
J5:3	REF5025	2.5-V output from REF5025
J5:4	REFOUT	2.048-V output from ADS1x48 integrated VREF
J5:5	NTC+	Positive thermistor input
J5:6	NTC-	Negative thermistor input
J6:1	REFP1	Positive external VREF input to ADC
J6:2	REFN1	Negative external VREF input to ADC
J6:3	RTD_A	RTD connection point A
J6:4	RTD_B	RTD connection point B
J6:5	RTD_C	RTD connection point C
J6:6	GND	Analog ground

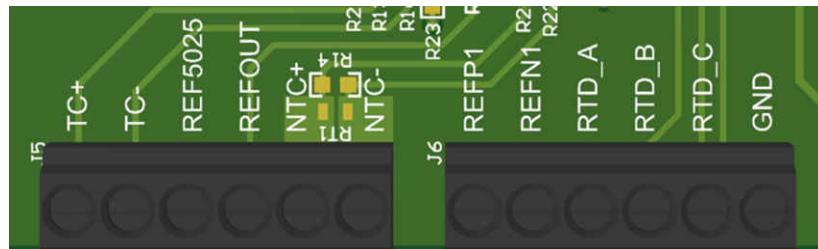


Figure 3-6. ADS1x48EVM Analog Input Terminal Blocks (J5, Left; J6, Right)

The following sections describe how to connect each different analog temperature sensor to its respective connector, beginning with terminal block J5.

3.5.1 Connecting a Thermocouple to J5 on the ADS1x48EVM

Connect an external thermocouple directly to the J5:1 and J5:2 inputs on the J5 terminal block, which represent the TC+ and TC- nets, respectively. The differential filter for this differential input pair has a cutoff frequency of 1.93 kHz. Additionally, each input has a common-mode filter with a cutoff frequency of 38.63 kHz. TC+ and TC- are connected through the filter resistors to two analog inputs (AIN4 and AIN5, respectively) on the ADS1x48. Figure 3-7 shows the portion of the ADS1x48EVM schematic with J5 and the thermocouple input structure.

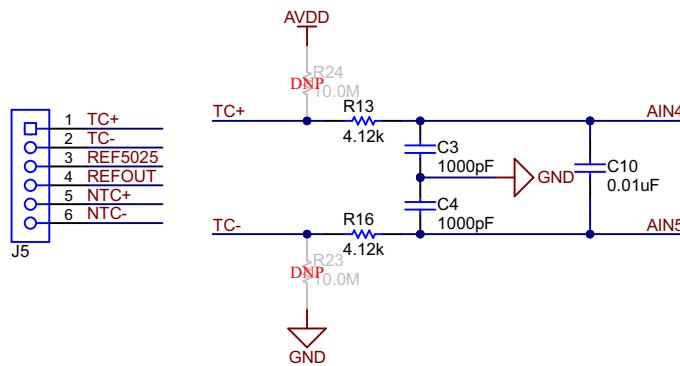


Figure 3-7. Thermocouple Input Structure on the ADS1x48EVM

Although thermocouples are self-powered, these components must be biased in order to avoid floating beyond the input range of the PGA integrated into the ADC. The ADS1x48EVM offers multiple ways to bias the thermocouple so that the output voltage can be successfully read by the ADC.

The first method uses pullup and pulldown resistors, which are labeled in Figure 3-7 as R24 and R23, respectively. These resistors are *do not place* (DNP) and therefore do not come installed on the EVM. To use the pullup and pulldown resistor method, install 1-MΩ to 10-MΩ resistors in the aforementioned locations. With these resistors installed, the thermocouple output voltage is centered at AVDD / 2, which puts the output voltage in the middle of the common-mode range of the PGA integrated into the ADS1x48. Additionally, using pullup and pulldown resistors enables continuous sensor break detection. If one of the thermocouple wires breaks, AIN4 is pulled to AVDD and AIN5 is pulled to GND, resulting in a full-scale input that can be detected in a separate firmware routine.

The second thermocouple-biasing method supported by the ADS1x48EVM uses one of the two reference voltage output pins to bias TC-. For example, Figure 3-8 shows that connecting an external jumper between the TC- input (J5:2) and the REF5025 output (J5:3) biases the thermocouple voltage to 2.5 V.

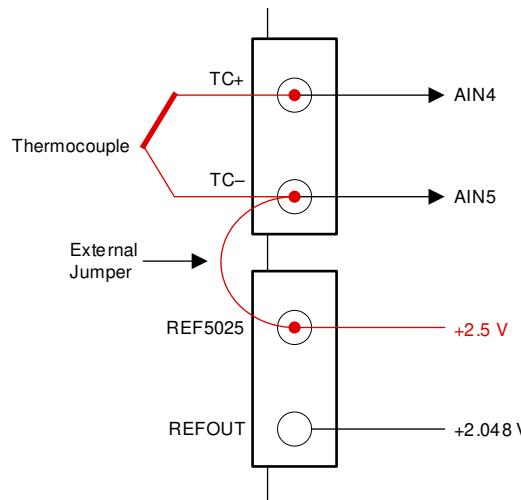


Figure 3-8. Using REF5025 (input J5:3) to Bias a Thermocouple

If AVDD = 5 V in the configuration shown in Figure 3-8, the thermocouple output voltage is now centered in the middle of common-mode range of the PGA integrated in the ADS1x48. If AVDD is instead chosen to be 3.3 V,

connect the external jumper between the REFOUT pin (J5:4) and the TC₋ input to bias the thermocouple output voltage to 2.048 V. Although this voltage is not equal to AVDD / 2 = 1.65 V, connecting TC₋ to REFOUT when AVDD = 3.3 V enables a wider PGA common-mode voltage swing compared to using the REF5025 output. An external bias voltage can also be directly connected to TC₋.

One challenge with the biasing scheme in [Figure 3-8](#) is that this configuration does not offer continuous wire-break detection. Instead, a separate diagnostic measurement can be made, or the pullup resistor (R24) in [Figure 3-7](#) can be populated to help perform this function. To learn more about different thermocouple biasing schemes as well as how to measure these sensors with precision ADCs, see the [A Basic Guide to Thermocouple Measurements application report](#). This document also discusses the need for cold junction compensation (CJC), which is used in conjunction with the thermocouple voltage to derive the measured temperature. The ADS1x48EVM includes provisions for a CJC measurement using a thermistor, which is discussed in more detail in the next section.

The steps for setting up a thermocouple measurement with the ADS1x48EVM are summarized below:

1. Connect the sensor to the TC_± terminals on J5
2. Select a biasing scheme:
 - a. For pullup and pulldown resistor biasing, populate R24 and R23, respectively
 - b. For constant voltage biasing:
 - i. Connect an external jumper between TC₋ and REF5025 or REFOUT
 - ii. Apply an external voltage to TC₋
3. Choose the ADC measurement channels to be MUX_SP[2:0] = AIN4 and MUX_SN[2:0] = AIN5
4. Select the ADC reference source (REF5025, internal VREF, or external VREF)

3.5.2 Connecting a Thermistor to J5 on the ADS1x48EVM

Unlike a thermocouple, thermistors are not self-powered and require a constant voltage or current source to operate. Typically, constant voltage is preferred because the thermistor impedance can vary from hundreds of ohms at low temperature to hundreds of thousands of ohms at high temperature (or vice versa for a thermistor with a negative temperature coefficient). A resistor is then added in series with the thermistor to create a resistor divider that can be measured by an ADC.

Connect an external thermistor directly to the J5:5 and J5:6 pins on the J5 terminal block, which represent the NTC+ and NTC- nets, respectively. The differential filter for this differential input pair has a cutoff frequency of 1.93 kHz. Additionally, each input has a common-mode filter with a cutoff frequency of 38.63 kHz. NTC+ and NTC- are connected through the filter resistors to two analog inputs (AIN6 and AIN7, respectively) on the ADS1x48. [Figure 3-9](#) shows the portion of the ADS1x48EVM schematic with J5 and the thermistor input structure.

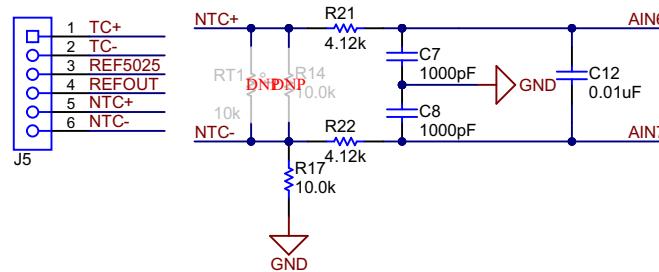


Figure 3-9. Thermistor Input Structure on the ADS1x48EVM

[Figure 3-9](#) shows two DNP components: a thermistor (RT1) and a 10-k Ω linearization resistor (R14). RT1 can be used for CJC for thermocouple measurements (see [Section 3.5.2.1](#)). R14 helps linearize the thermistor output voltage over a smaller temperature range. See section 2.8.2 in the [A Basic Guide to Thermocouple Measurements application report](#) to learn more about the benefits of using a linearization resistor when measuring a thermistor. Finally, resistor R17 in [Figure 3-9](#) is the bias resistor used in conjunction with the external resistor to form a resistor divider. Resistor R17 is chosen to be 10 k Ω because 10 k Ω is a commonly-used nominal thermistor impedance. Choosing both resistors to have the same nominal impedance balances the resistor divider at 25°C.

As stated earlier in this section, thermistors are not self-powered and require a bias source to operate. As [Figure 3-10](#) shows, connect the constant voltage output from REFOUT to NTC+ via an external jumper to bias the sensor. Alternatively, NTC+ can be connected to the REF5025 output instead. In either case, ensure that the reference output used to bias the resistor divider is the same reference selected for the ADC measurements.

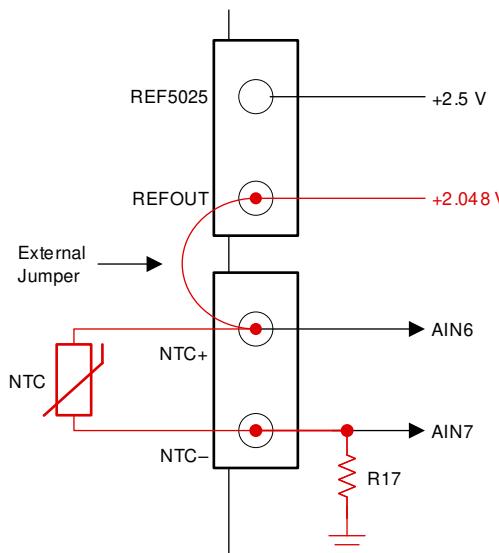


Figure 3-10. Connecting a Thermistor to the J5 Terminal Block on the ADS1x48EVM

The steps for setting up a thermistor measurement with the ADS1x48EVM are summarized below:

1. Connect the sensor to the NTC \pm terminals on J5
2. Connect an external jumper between NTC $+$ and REF5025 or REFOUT
3. Populate R14 with a 10-k Ω resistor if necessary
4. Choose the ADC measurement channels to be MUX_SP[2:0] = AIN6 and MUX_SN[2:0] = AIN7
5. Select the ADC reference source to be the same constant voltage output from step #2

3.5.2.1 Using Thermistor RT1 for Thermocouple Cold Junction Compensation

The ADS1x48EVM board includes provisions for using a PCB-mounted thermistor to measure the cold junction of a thermocouple connected to the TC $+$ and TC $-$ inputs on J5. As Figure 3-11 shows, top- and bottom-layer copper pours create an isothermal bridge between the NTC \pm and TC \pm inputs. This bridge helps ensure that thermistor RT1 measures the same temperature as the thermocouple cold junction at inputs J5:1 and J5:2, enabling a more accurate thermocouple measurement.

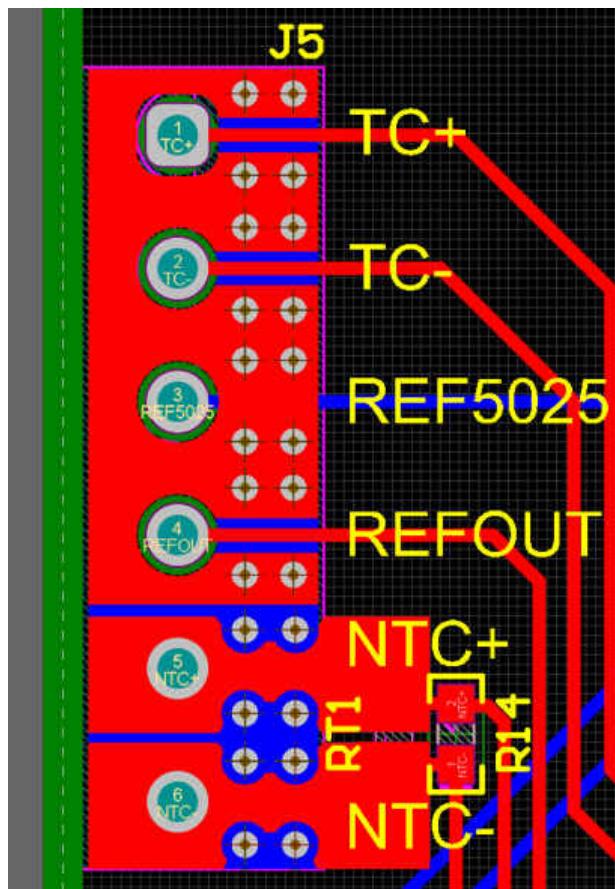


Figure 3-11. PCB Layout for J5 Terminal Block Showing Copper Pours for CJC Measurement

As discussed in Section 3.5.2 and in Figure 3-9, thermistor RT1 is not populated by default on the ADS1x48EVM. Choose a 10-k Ω NTC thermistor in a 0603 package for this component. To measure the thermistor voltage, follow the steps outlined at the end of Section 3.5.2, noting that step #1 (connect the sensor) is satisfied by soldering the thermistor (RT1) to the PCB. Also, the ADS1x48 is a multiplexed ADC and therefore can only measure one single-ended or differential input per conversion cycle. As a result, the thermocouple and CJC measurements must be taken separately and then manipulated in software to determine the resulting temperature. To learn more about CJC as well as how to use this value to determine the true measured temperature, see the [A Basic Guide to Thermocouple Measurements](#) application report.

3.5.3 Connecting an RTD to J6 on the ADS1x48EVM

The RTD input connections on J6 are J6:3, J6:4, and J6:5, which correspond to the RTD_A, RTD_B, and RTD_C nets, respectively. Additionally, terminal block J6 provides a pair of differential reference inputs, REFP1 and REFN1, which correspond to inputs J6:1 and J6:2, respectively. The RTD_A, RTD_B and REFP1, REFN1 input pairs have a differential filter with a cutoff frequency of 1.93 kHz. Additionally, each of these inputs has a common-mode filter with a cutoff frequency of 38.63 kHz. [Figure 3-12](#) shows the RTD input structure on the ADS1x48EVM, and [Table 3-4](#) describes the mapping between the terminal block connections, schematic net names, and the analog pins on the ADS1x48. Some nets may connect to multiple analog pins on the ADS1x48.

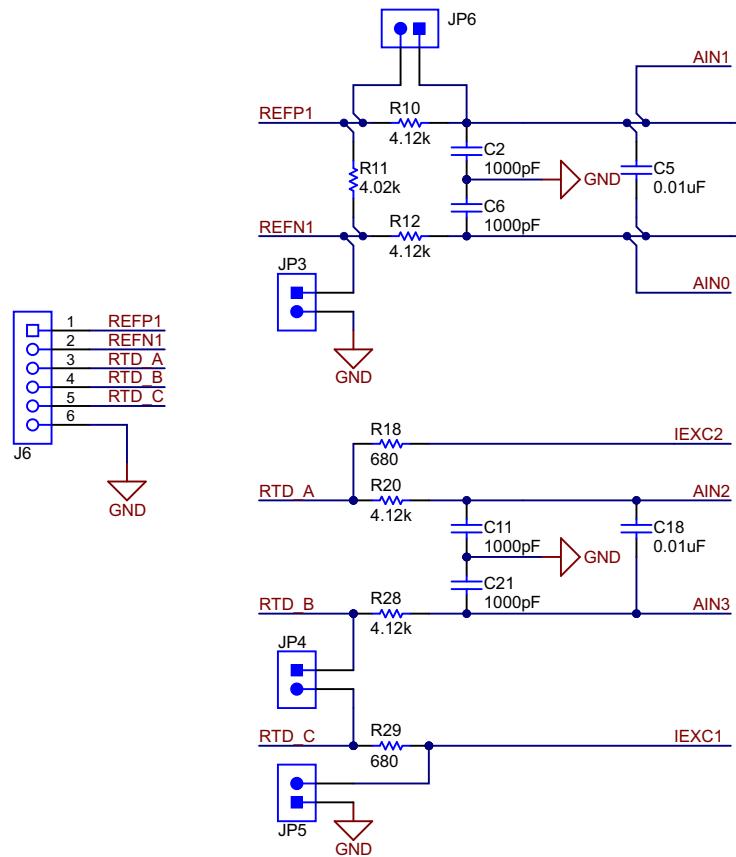


Figure 3-12. RTD Input Structure on the ADS1x48EVM

Table 3-4. ADS1x48EVM Terminal Block (J6) to ADC Connections

Connector	Net Name	ADS1x48 Input Connection	Description
J6:1	REFP1	REFP1	External reference input (positive)
		AIN1	Analog input 1
J6:2	REFN1	REFN1	External reference input (negative)
		AIN0	Analog input 0
J6:3	RTD_A	AIN2	Analog input 2
		IEXC2	Excitation current source #2
J6:4	RTD_B	AIN3	Analog input 3
		IEXC1	Excitation current source #1
J6:5	RTD_C	IEXC1	Excitation current source #1
J6:6	GND	n/a	Analog ground

In [Figure 3-12](#), resistor R11 is the reference resistor (R_{REF}) that is placed in series with the RTD and connected to the ADS1x48 external reference inputs, as described in [Table 3-4](#). An excitation current supplied by one of the two IDACs integrated into the ADS1x48 flows through R_{REF} and the RTD, creating a ratiometric relationship

between the analog input and reference voltages. As a result, the absolute IDAC accuracy is less critical and the system performance improves. However, choose the IDAC current magnitude and the total circuit impedance to ensure that the ADC IDAC compliance voltage is met. For additional information regarding ratiometric references, RTD measurement circuits using precision ADCs, and important specifications including compliance voltage, see the [A Basic Guide to RTD Measurements](#) application report.

R11 is chosen to be 4.02 k Ω in order to accommodate high-impedance RTDs at high temperature ranges. For example, a Pt1000 at 850°C has a typical impedance of approximately 3.9 k Ω . If a smaller measurement range is required, replace R11 with a different resistor in an 0805 package or remove R11 and use an external resistor connected between REFP1 and REFN1 on J6. Choose a high accuracy, low-drift resistor to ensure best system performance.

All common RTD configurations can be measured with the ADS1x48EVM, including:

- 2-wire RTD using a low-side R_{REF}
- 2-wire RTD using a high-side R_{REF}
- 3-wire RTD using one IDAC and a low-side R_{REF}
- 3-wire RTD using one IDAC and a high-side R_{REF}
- 3-wire RTD using two IDACs and a low-side R_{REF}
- 3-wire RTD using two IDACs and a high-side R_{REF}
- 4-wire RTD using a low-side R_{REF}
- 4-wire RTD using a high-side R_{REF}

The ADS1x48EVM accomplishes maximum flexibility using jumpers JP3, JP4, JP5, and JP6 (see [Figure 3-12](#)) in conjunction with different analog inputs and IDAC routing. The following subsections detail the appropriate connections and settings to enable each RTD configuration using the ADS1x48EVM. Each subsection contains a connection diagram where the red lines indicate how current flows in the circuit. Moreover, the red text indicates which jumpers are populated and which current sources are biasing the RTD, and the blue text indicates the measurement channels. This information is summarized in [Section 3.5.3.9](#).

3.5.3.1 Connecting a 2-Wire RTD Using a Low-Side R_{REF} to J6 on the ADS1x48EVM

Figure 3-13 shows how to connect a 2-wire RTD using a low-side R_{REF} configuration to J6.

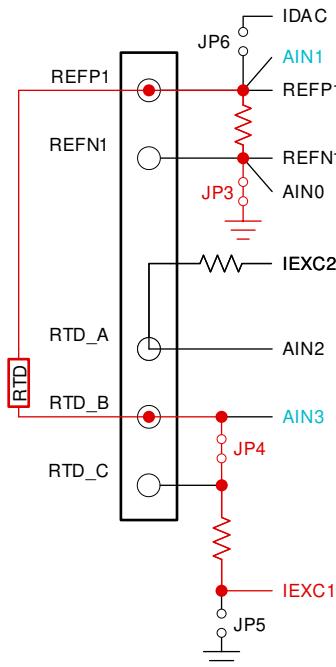


Figure 3-13. Connection Diagram for a 2-Wire RTD Using a Low-Side R_{REF}

Figure 3-13 also shows that for this RTD configuration, the RTD is connected to REFP1 and RTD_B. Additionally, jumpers JP3 and JP4 are connected whereas jumpers JP5 and JP6 are disconnected. Finally, the IEXC1 current source is enabled and the measurement is taken between AIN3 and AIN1. Table 3-5 summarizes the necessary connections and ADC configuration settings.

3.5.3.2 Connecting a 2-Wire RTD Using a High-Side R_{REF} to J6 on the ADS1x48EVM

Figure 3-14 shows how to connect a 2-wire RTD using a high-side R_{REF} configuration to J6.

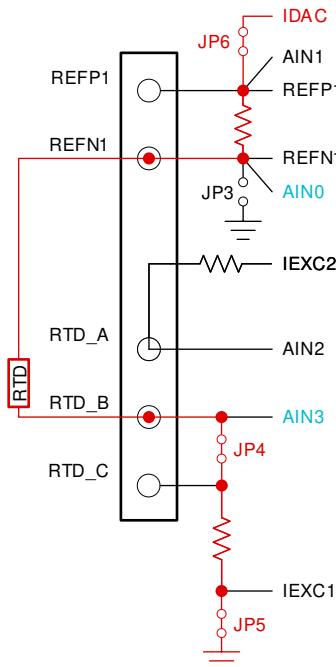


Figure 3-14. Connection Diagram for a 2-Wire RTD Using a High-Side R_{REF}

Figure 3-14 also shows that for this RTD configuration, the RTD is connected to REFN1 and RTD_B. Additionally, jumpers JP4, JP5, and JP6 are connected whereas jumper JP3 is disconnected. Finally, the AIN1 pin on the ADS1x48 is configured to be a current source and the measurement is taken between AIN0 and AIN3. Table 3-5 summarizes the necessary connections and ADC configuration settings.

3.5.3.3 Connecting a 3-Wire RTD Using One IDAC and a Low-Side R_{REF} to J6 on the ADS1x48EV

Figure 3-15 shows how to connect a 3-wire RTD using one IDAC and a low-side R_{REF} configuration to J6.

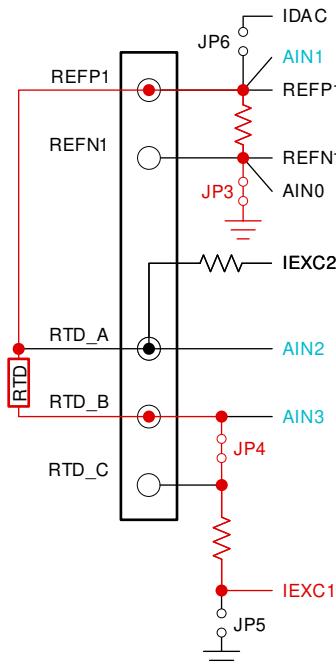


Figure 3-15. Connection Diagram for a 3-Wire RTD Using One IDAC and a Low-Side R_{REF}

Figure 3-15 also shows that for this RTD configuration, the RTD is connected to REFP1, RTD_A, and RTD_B. Additionally, jumpers JP3 and JP4 are connected whereas jumpers JP5 and JP6 are disconnected. Moreover, the IEXC1 current source is enabled. Finally, this specific configuration requires two measurements for lead-wire cancellation: the first is between AIN3 and AIN2, and the second is between AIN2 and AIN1. Table 3-5 summarizes the necessary connections and ADC configuration settings.

3.5.3.4 Connecting a 3-Wire RTD Using One IDAC and a High-Side R_{REF} to J6 on the ADS1x48EVM

Figure 3-16 shows how to connect a 3-wire RTD using one IDAC and a high-side R_{REF} configuration to J6.

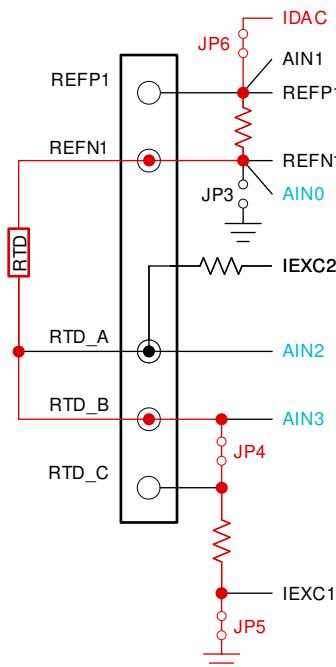


Figure 3-16. Connection Diagram for a 3-Wire RTD Using One IDAC and a High-Side R_{REF}

Figure 3-16 also shows that for this RTD configuration, the RTD is connected to REFN1, RTD_A, and RTD_B. Additionally, jumpers JP4, JP5, and JP6 are connected whereas jumper JP3 is disconnected. Moreover, the AIN1 pin on the ADS1x48 is configured to be a current source. Finally, this specific configuration requires two measurements for lead-wire cancellation: the first is between AIN0 and AIN2 and, the second is between AIN2 and AIN3. Table 3-5 summarizes the necessary connections and ADC configuration settings.

3.5.3.5 Connecting a 3-Wire RTD Using Two IDACs and a Low-Side R_{REF} to J6 on the ADS1x48EVM

Figure 3-17 shows how to connect a 3-wire RTD using two IDACs and a low-side R_{REF} configuration to J6 on the ADS1x48EVM.

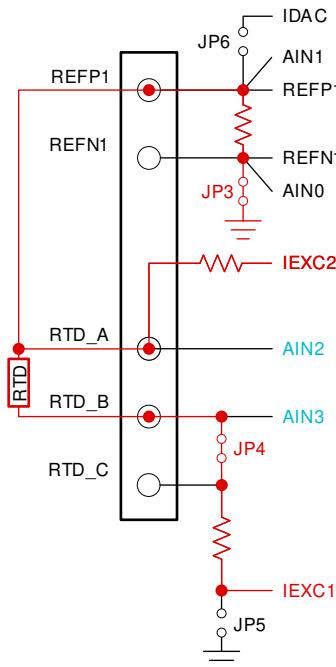


Figure 3-17. Connection Diagram for a 3-Wire RTD Using Two IDACs and a Low-Side R_{REF}

Figure 3-17 also shows that for this RTD configuration, the RTD is connected to REFP1, RTD_A, and RTD_B. Additionally, jumpers JP3 and JP4 are connected whereas jumpers JP5 and JP6 are disconnected. Finally, the IEXC1 and IEXC2 current sources are enabled and the measurement is taken between AIN3 and AIN2. Table 3-5 summarizes the necessary connections and ADC configuration settings.

3.5.3.6 Connecting a 3-Wire RTD Using Two IDACs and a High-Side R_{REF} to J6 on the ADS1x48EVM

Figure 3-18 shows how to connect a 3-wire RTD using two IDACs and a high-side R_{REF} configuration to J6.

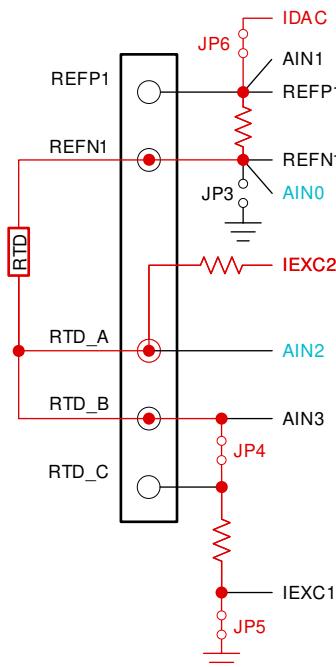


Figure 3-18. Connection Diagram for a 3-Wire RTD Using Two IDACs and a High-Side R_{REF}

Figure 3-18 also shows that for this RTD configuration, the RTD is connected to REFN1, RTD_A, and RTD_B. Additionally, jumpers JP4, JP5, and JP6 are connected whereas jumper JP3 is disconnected. Finally, the AIN1 pin on the ADS1x48 is configured to be a current source and is used in conjunction with the IEXC1 current source, while the measurement is taken between AIN0 and AIN2. Table 3-5 summarizes the necessary connections and ADC configuration settings.

3.5.3.7 Connecting a 4-Wire RTD Using a Low-Side R_{REF} to J6 on the ADS1x48EVM

Figure 3-19 shows how to connect a 4-wire RTD using a low-side R_{REF} configuration to J6.

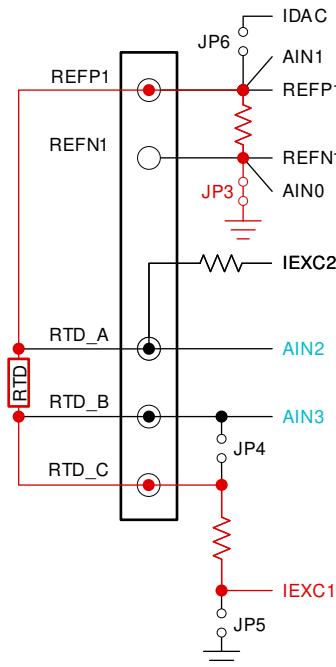


Figure 3-19. Connection Diagram for a 4-Wire RTD Using a Low-Side R_{REF}

Figure 3-19 also shows that for this RTD configuration, the RTD is connected to REFP1, RTD_A, RTD_B, and RTD_C. Additionally, jumper JP3 is connected whereas jumpers JP4, JP5, and JP6 are disconnected. Finally, the IEXC1 current source is enabled and the measurement is taken between AIN3 and AIN2. Table 3-5 summarizes the necessary connections and ADC configuration settings.

3.5.3.8 Connecting a 4-Wire RTD Using a High-Side R_{REF} to J6 on the ADS1x48EVM

Figure 3-20 shows how to connect a 4-wire RTD using a high-side R_{REF} configuration to J6.

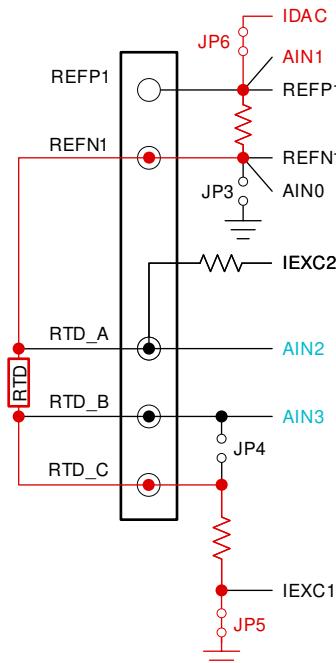


Figure 3-20. Connection Diagram for a 4-Wire RTD Using a High-Side R_{BEF}

Figure 3-20 also shows that for this RTD configuration, the RTD is connected to REFN1, RTD_A, RTD_B, and RTD_C. Additionally, jumpers JP5 and JP6 are connected whereas jumpers JP3 and JP4 are disconnected. Finally, the AIN1 pin on the ADS1x48 is configured to be a current source and the measurement is taken between AIN2 and AIN3. Table 3-5 summarizes the necessary connections and ADC configuration settings.

3.5.3.9 Summary of ADS1x48EVM RTD Configuration Settings

Table 3-5 summarizes the required IDAC, jumper, and analog input channel settings to measure each RTD configuration using the ADS1x48EVM.

Table 3-5. ADS1x48EVM Settings for Different RTD Types

RTD	No. of IDACs	R _{REF}	IDAC Channels	JP3	JP4	JP5	JP6	AINP	AINN
2-wire	1	Low-side	IEXC1	On	On	Off	Off	AIN3	AIN1
	1	High-side	AIN1	Off	On	On	On	AIN0	AIN3
3-wire	1	Low-side	IEXC1	On	On	Off	Off	AIN3 ⁽¹⁾	AIN2 ⁽¹⁾
	1	High-side	AIN1	Off	On	On	On	AIN2 ⁽²⁾	AIN1 ⁽²⁾
	2	Low-side	IEXC1, IEXC2	On	On	Off	Off	AIN0 ⁽¹⁾	AIN2 ⁽¹⁾
	2	High-side	AIN1, IEXC2	Off	On	On	On	AIN2 ⁽²⁾	AIN3 ⁽²⁾
4-wire	1	Low-side	IEXC1	On	Off	Off	Off	AIN3	AIN2
	1	High-side	AIN1	Off	Off	On	On	AIN2	AIN3

(1) First measurement.

(2) Second measurement.

3.5.4 Connecting a General-Purpose Input to J5 on the ADS1x48EVM

Although the ADS1x48EVM is designed for measuring all types of analog temperature sensors, general-purpose input signals can be applied to the ADS1x48 through the $TC\pm$ inputs on the J5 terminal block. [Figure 3-21](#) shows the input structure used for the $TC\pm$ inputs.

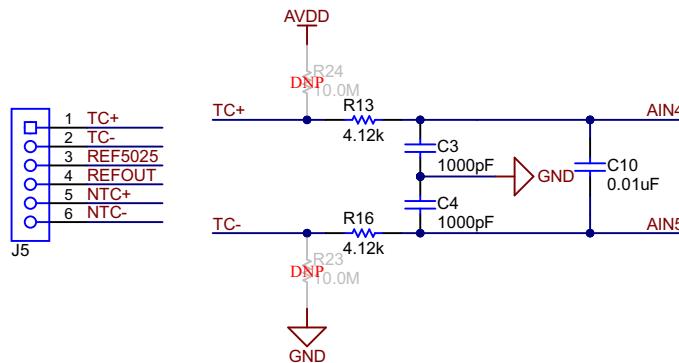


Figure 3-21. Using the $TC\pm$ Inputs on J5 as General-Purpose Signal Inputs

As [Figure 3-21](#) shows, resistors R24 and R23 are not populated by default, resulting in a set of analog inputs that are only subject to the differential filter cutoff frequency of 1.93 kHz and the common-mode filter cutoff frequency of 38.63 kHz. The $TC\pm$ inputs can therefore be used for any general input signal as long as the ADS1x48 absolute input and common-mode range requirements are satisfied. Select the AIN4 and AIN5 inputs on the ADS1x48 to measure a voltage connected to the $TC\pm$ inputs.

4 ADS1x48EVM GUI

The ADS1x48EVM requires a communication driver that is installed automatically. However, this [FAQ](#) can help troubleshoot driver-related issues if any arise.

The following steps describe the ADS1x48 GUI software installation:

1. Connect the micro-USB-to-USB cable from the PAMBoard directly to a USB port on the computer. Do not connect the cable through a USB hub.
2. Open up the web-based GUI available on the EVM landing page ([ADS1148EVM-PDK](#) or [ADS1248EVM-PDK](#)).
 - a. First-time users may be prompted to download and install the browser extension for Firefox™ or Chrome™ and the TI Cloud Agent Application as shown in [Figure 4-1](#). Installing the TI Cloud Agent is a one-time download and installation.
3. Refresh the GUI such that a green signal displays and the *Hardware Connected* indicator shows in the bottom status ribbon (see [Figure 4-2](#)).

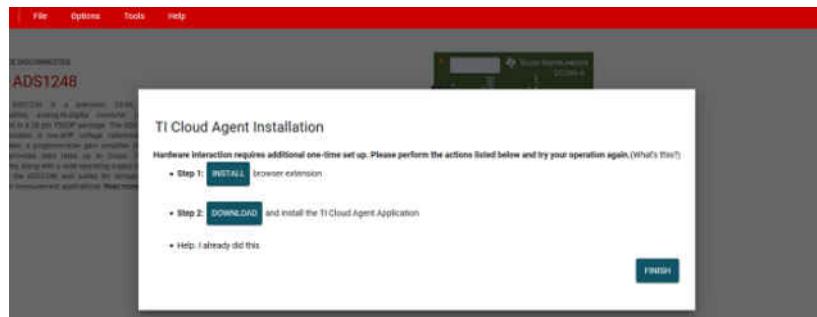


Figure 4-1. Browser Extension and TI Cloud Agent Installation

When connected, the ADS1x48EVM GUI has multiple pages to help navigate and control the ADS1x48EVM:

- [Home](#)
- [Data Capture](#)
- [Register Map](#)

The following sections step through each GUI page in more detail.

4.1 Home

The *Home* page is the GUI start-up landing page. The *Home* page provides a high-level overview of the ADS1x48 including a device description and a 3D view of the EVM PCB. Highlighted in orange in the upper-left corner of [Figure 4-2](#) is a vertical *Navigation* bar for the various GUI pages, including:

- [Home](#)
- [Data Capture](#)
- [Register Map](#)

The horizontal *Menu* bar at the top of the GUI shows the following menu options, which are highlighted in blue in [Figure 4-2](#) and are discussed in more detail in [Section 4.1.1](#):

- [File](#)
- [Options](#)
- [Tools](#)
- [Help](#)

Quick links to *Support Resources* are shown at the bottom of the *Home* page. These links are highlighted in purple in [Figure 4-2](#) and include the EVM user's guide, schematic, and ADC data sheet. Finally, a successfully connected EVM displays as *Device Connected* in the top left and as *Hardware Connected* in the status ribbon. Both of these indicators are highlighted in green in [Figure 4-2](#).

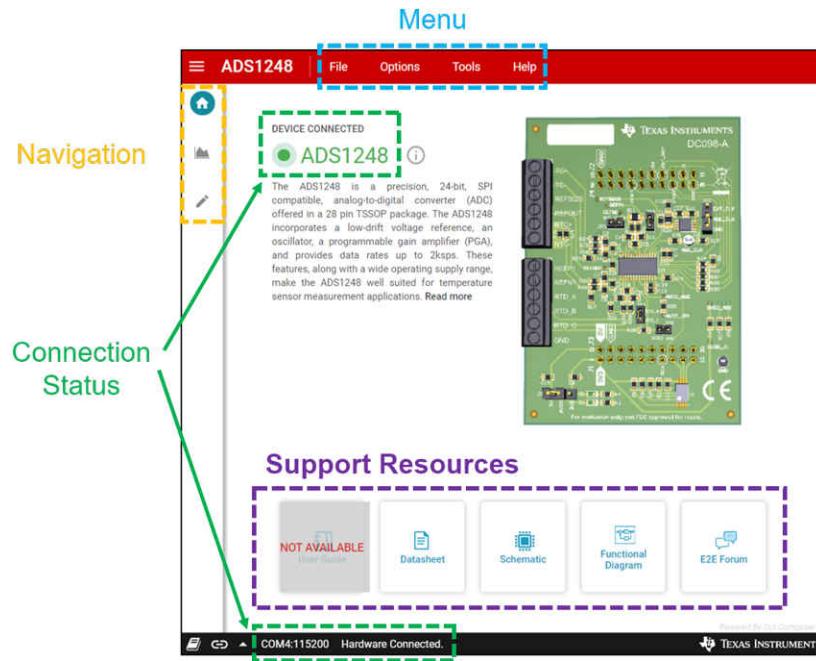


Figure 4-2. ADS1x48EVM GUI Home Page

One other important feature of the *Home* page is an information icon next to the device name. Clicking the icon, as shown in [Figure 4-3](#), displays specific information regarding the ADS1x48EVM.

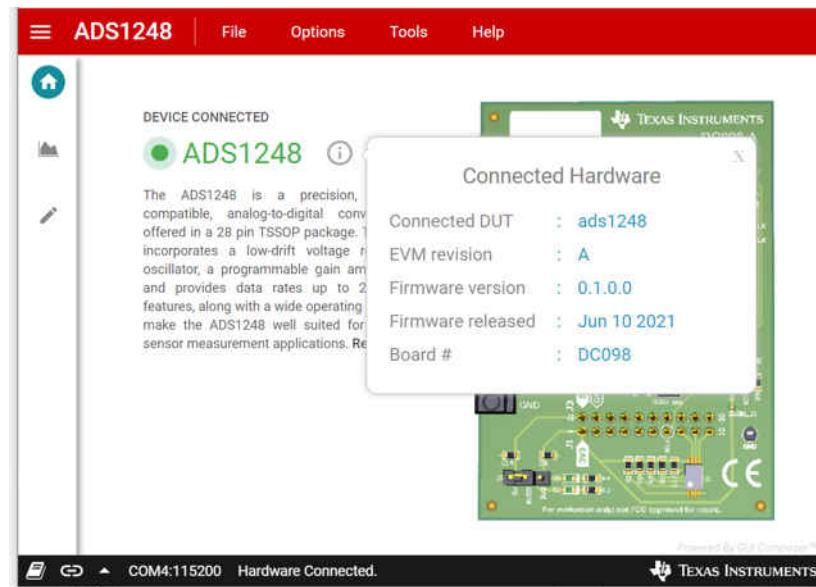


Figure 4-3. Connected Hardware Information

4.1.1 Menu Bar

The *Menu* bar across the top of the GUI displays the device name used on the EVM along with a number of drop-down menu options.

4.1.1.1 File Menu

The *File* drop-down menu displays the available options shown in [Figure 4-4](#). These options include:

- *Program Device*: Only necessary if an important firmware change is required
- *Analysis Data*:
 - *Save data*: Save the *Analysis Data* to a comma-separated values (CSV) formatted file for further analysis using external programs
 - *Load data*: Loads a saved data file back into the GUI for further review or analysis
- *Register Data*
 - *Save register*: Save the register data for a specific configuration
 - *Load register*: Load a previously saved register map configuration

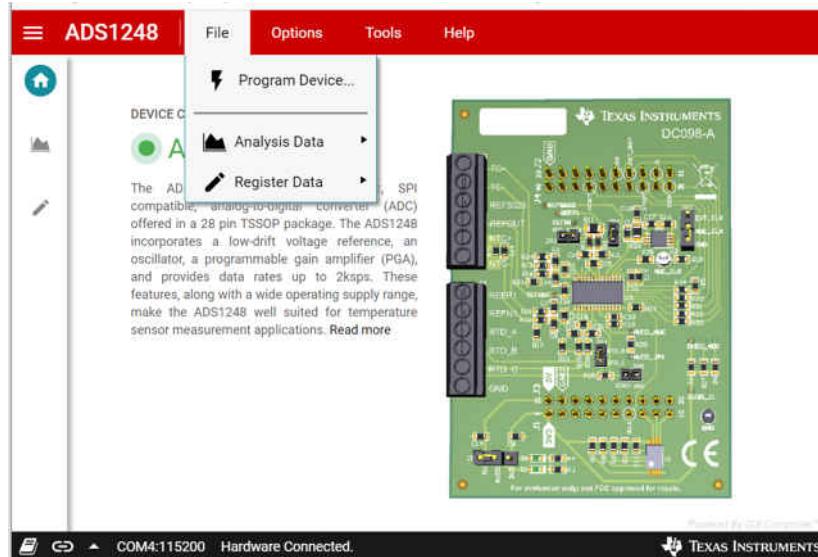


Figure 4-4. File Menu

4.1.1.2 Options Menu

The *Options* drop-down provides a way to display the current COM port settings in a pop-up dialog with options to change the COM port or reconfigure the settings as necessary.

4.1.1.3 Tools Menu

The *Tools* drop-down menu offers access to the *Log pane* that displays an activity log at the bottom of the GUI. Clicking the book icon in the status ribbon displays the same information as selecting *Log pane* in the *Tools* menu.

4.1.1.4 Help Menu

The *Help* drop-down menu displays the following options:

- *E2E Support Forum* links to the E2E forum in order to ask questions or search for answers
- *View README.md* displays pertinent start-up information not necessarily included in this guide
- *About* displays specific information regarding the GUI and EVM hardware to help confirm that the latest version of the GUI is being used

4.2 Data Capture

The *Data Capture* icon selects the available charting options for displaying conversion data. The data options, as shown in [Figure 4-5](#), include the *Time Domain*, *Histogram*, and *FFT* displays. However, the FFT plot and information may have little meaning because the ADS1x48 is primarily a dc measurement device.

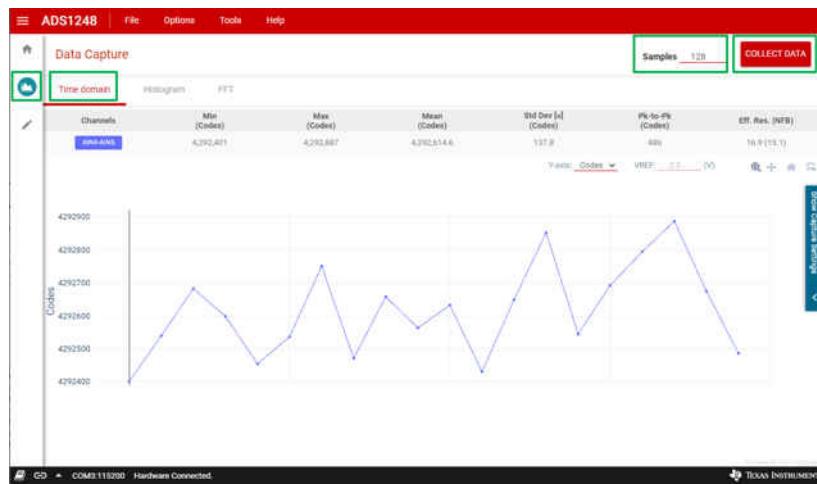


Figure 4-5. Data Capture Window

A slide-out menu (as shown in [Figure 4-6](#)) is viewable on the right side of the *Chart* window. By clicking the *Show Capture Settings* slide-out, various configurations and displays are selectable. The drop-down menus available in the *Capture Settings* slide-out are:

- *Select data rate* for the data output conversion rate
- *Select MUXP channels* and *Select MUXN channels* for choosing the desired input channels to be measured
- *Select PGA* for choosing the required input signal amplification
- *SEFOCAL* button for performing a device (ADC) offset calibration

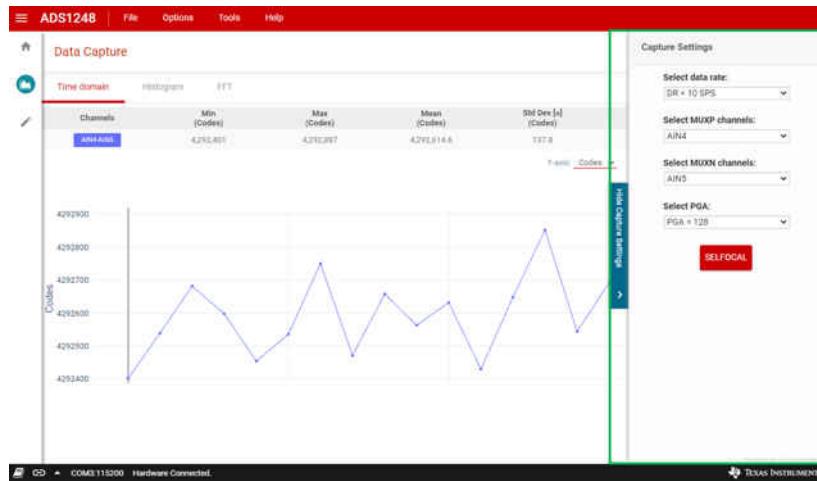


Figure 4-6. Capture Settings Slide-Out

To collect data, select the number of *Samples* to collect in the upper right corner of the capture window. To capture data, press the *Collect Data* button next to the *Samples* setting (shown in [Figure 4-5](#)).

Conversion data collects when the *Collect Data* button is pressed, after which the button changes to read *Stop Collect*. Pressing the *Stop Collect* button stops the collection of conversion data; otherwise the data are collected for the chosen number of *Samples*. The number of *Samples* can be changed prior to pressing *Collect Data* by directly entering the desired number of samples or by clicking on the up and down arrows. The number of samples cannot be changed while data are being collected.

When the *Collect Data* operation is complete, the data displays the calculated channel statistics and a plot of the data in the chart window. Various icons for viewing the data include zoom, pan, and home. The home icon restores the graph to show all data collected. The viewing icons are underneath the statistics information on the right side of the GUI.

4.2.1 Time Domain and Histogram Statistics

The *Time Domain* and *Histogram* plots share the same statistical information shown in [Figure 4-7](#):

- Input *Channels* selected
- *Min* code within the data set
- *Max* code within the data set
- *Mean* code value within the data set
- *Std Dev* representing the standard deviation within the data set
- *Pk-to-Pk* representing the total noise peak-to-peak within the data set
- *Eff. Res* representing the effective resolution as number of bits with the value in parenthesis showing the noise-free number of bits

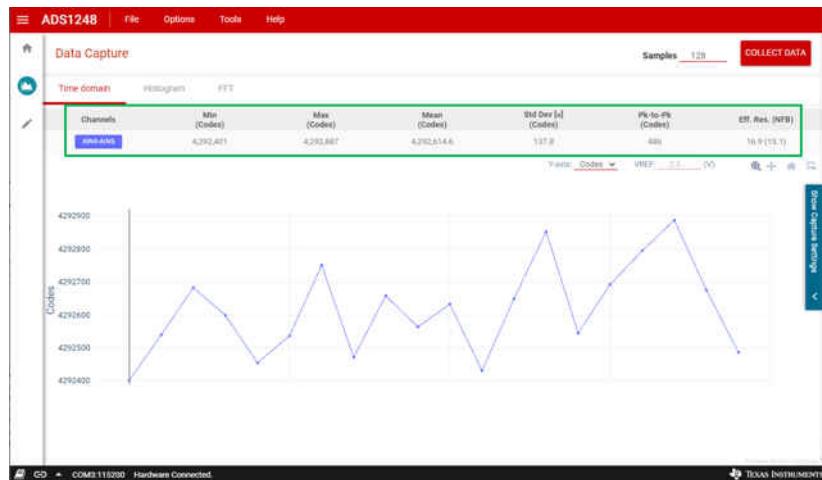


Figure 4-7. Capture Statistics

4.2.2 Time Domain Plot

The *Time Domain* plot displays the sample count number in the X-axis. The Y-axis is displayed as either codes or volts with the selection in a drop-down menu. The Y-axis drop-down menu displays next to the charting icons near the right side of the GUI below the statistics. [Figure 4-8](#) shows the *Time Domain* plot and its features.

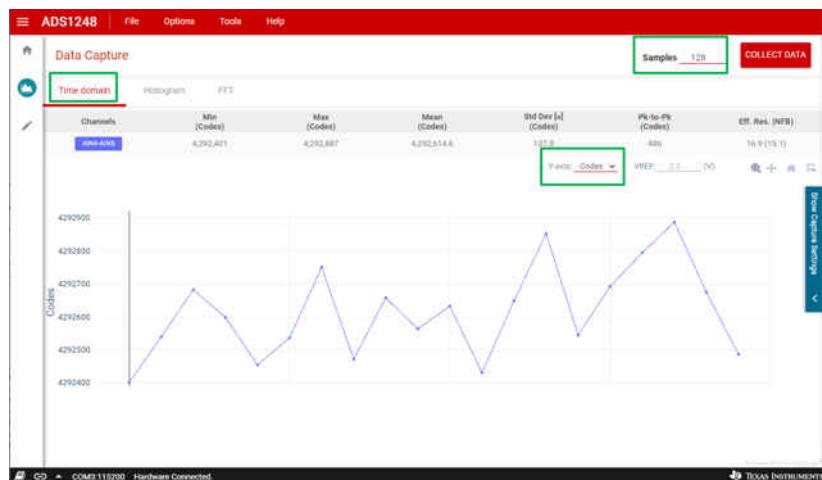


Figure 4-8. Time Domain Plot

4.2.3 Histogram Plot

The *Histogram* plot in [Figure 4-9](#) shows the number of occurrences that a code or group of codes appear. User selection includes a choice of:

- *# of Bins* selects the number of bins to include in the plot
- *Bin Size* selects the number of unique codes to include in each bin

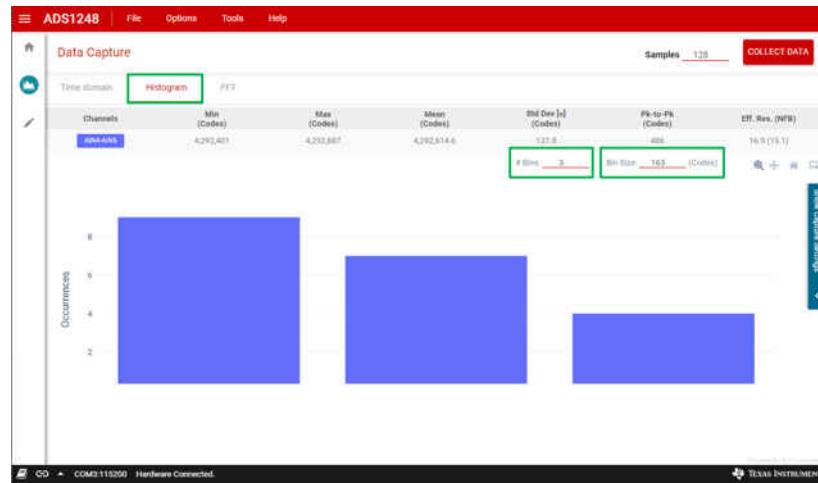


Figure 4-9. Histogram Plot

The *# Bins* and *Bin Size* are selectable options and display next to the charting icons near the right side of the GUI below the statistics.

4.2.4 FFT Statistics and Plot

The FFT plot displays the following statistics:

- Input *Channels* selected
- *Fundamental frequency*
- *Fundamental power*
- *Noise floor*
- *SNR* or signal-to-noise ratio
- *SFDR* or spurious-free dynamic range
- *THD* or total harmonic distortion
- *SINAD* or signal-to-noise and distortion
- *ENOB* or effective number of bits
- *Harmonics*

The *FFT* plot is rather meaningless for dc input voltages. However, a low-frequency ac signal can be analyzed and the *FFT* plot displayed.

4.3 Register Map

The *Register Map* window contains information about the how the ADS1x48 is configured. A number of control buttons and drop-down menus exist to configure the *Register Map* read and write operations.

Throughout the *Register Map* window question mark icons appear. Clicking on these icons provides details pertaining to the items in the locations where they appear. See [Figure 4-10](#) for more details.

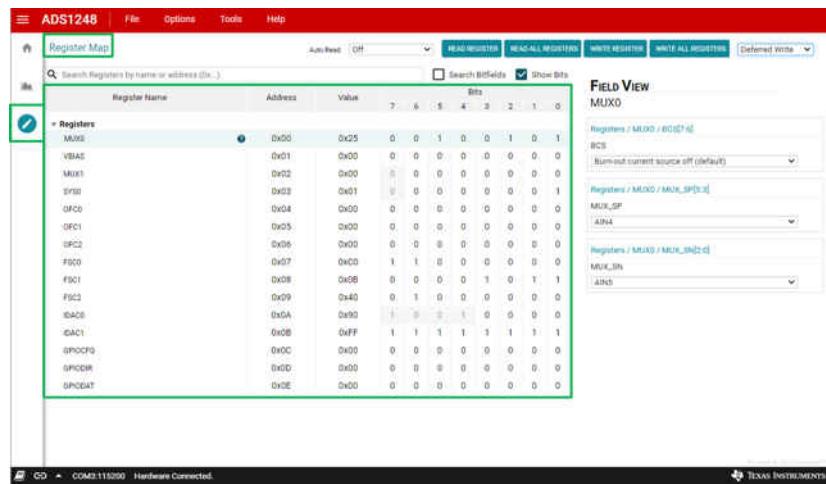


Figure 4-10. Register Map

As shown in [Figure 4-10](#), the ADS1x48 devices have many configurable registers. Configure these registers by using the drop-down menu and clickable options shown in the *Field View* menu on the right side of the GUI window. The *Field View* menu replicates the register setting information provided in the [ADS1x48 data sheets](#). Reference these documents for additional information about or questions related to the specific ADC register settings.

Instead of using the *Field View* menu, the 1's and 0's can also be double-clicked in the *Bits* menu to toggle the bit settings. As the bit settings change, the *Field View* options also change to the corresponding register setting.

4.3.1 Register Read and Write Options

[Figure 4-11](#) highlights the top of the *Register Map* window where reading from and writing to registers is controlled. The default behavior has the *Auto Read* register function turned off as well as performs an *Immediately Write* operation on the *Config* register when options change. All read and write options are discussed in more detail in the next sections.

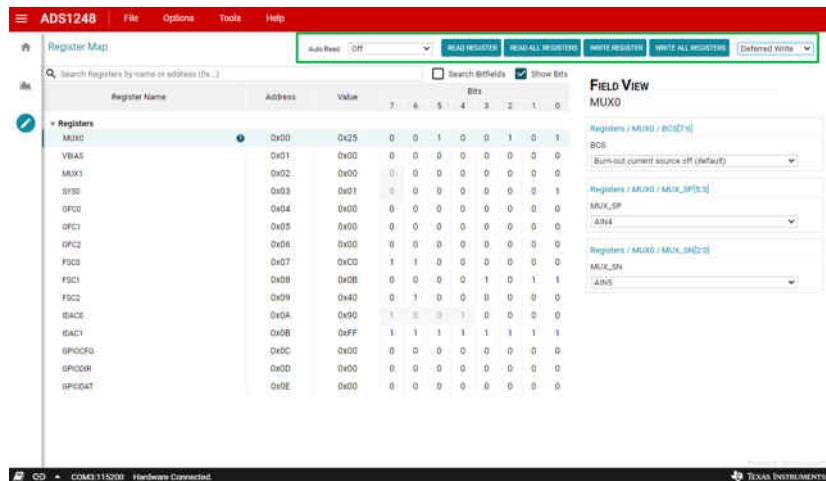


Figure 4-11. Register Read and Write Controls

4.3.1.1 Read Register Options

As stated in the previous section, the default GUI configuration has the *Auto Read* functionality turned off and instead manually reads the registers using the *READ REGISTER* and *READ ALL REGISTERS* buttons. The *READ REGISTER* button reads only the selected register. The *READ ALL REGISTERS* button reads all available ADS1x48 registers. The advantage of manually reading the register contents is reduced USB communication between the ADS1x48EVM and the GUI.

The registers can be read automatically from the ADS1x48 at a variety of intervals from once per second to as fast as possible. As shown in [Figure 4-12](#), the intervals can be reviewed and selected using the *Auto Read* drop-down menu. The *READ REGISTER* and *READ ALL REGISTERS* button options are only enabled when the *Auto Read* selection is turned off.

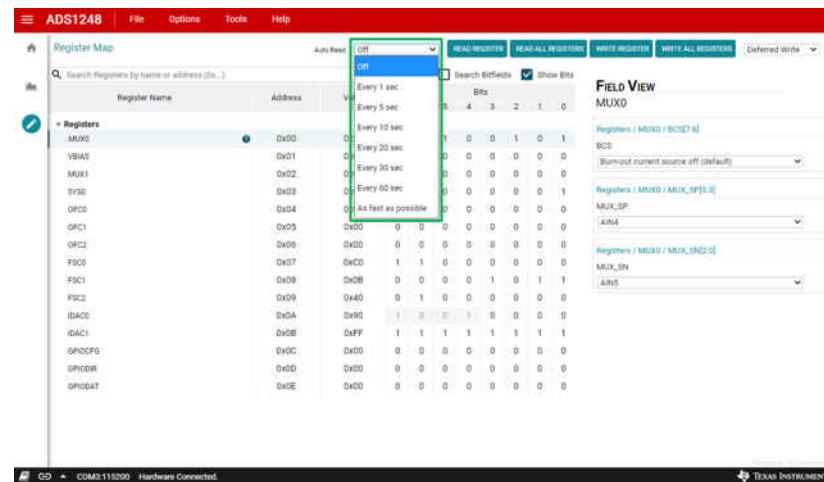


Figure 4-12. Auto Read Options

4.3.1.2 Write Register Options

The GUI default option for register writes is *Immediate Write*. When *Immediate Write* is selected, any register configuration changes are immediately written from the GUI to the ADS1x48 device. Using the *Immediate Write* option ensures that what is being displayed in the register map view is how the ADS1x48 is configured. If the write register drop-down menu selection is for a *Deferred Write* as shown in [Figure 4-13](#), then the write register buttons *WRITE REGISTER* and *WRITE ALL REGISTERS* are enabled. Similar to the functionality of the read register buttons, the *WRITE REGISTER* button writes the configuration for the currently selected register. Comparatively, selecting the *WRITE ALL REGISTERS* button writes to all configurable registers.

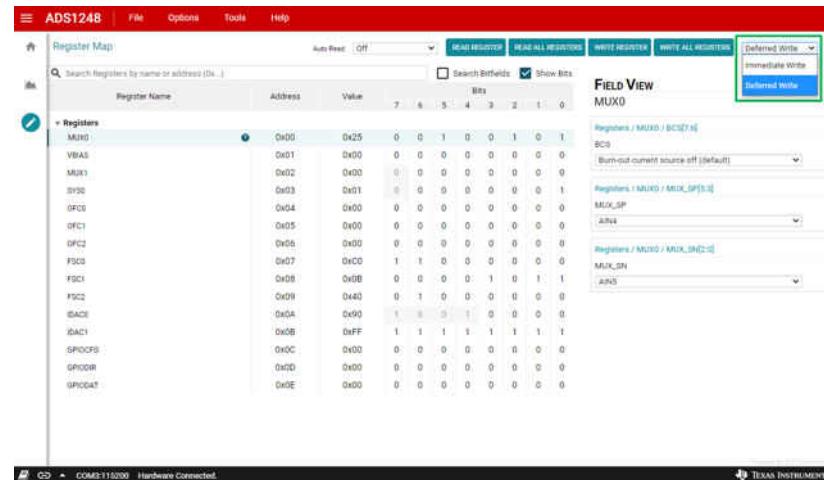


Figure 4-13. Register Write Options

5 Bill of Materials, Printed Circuit Board Layout, and Schematic

This section contains the ADS1x48EVM bill of materials (BOM), printed-circuit board (PCB) layout, and board schematic.

5.1 Bill of Materials

Table 5-1 lists the bill of materials (BOM) for the ADS1x48EVM.

Table 5-1. Bill of Materials

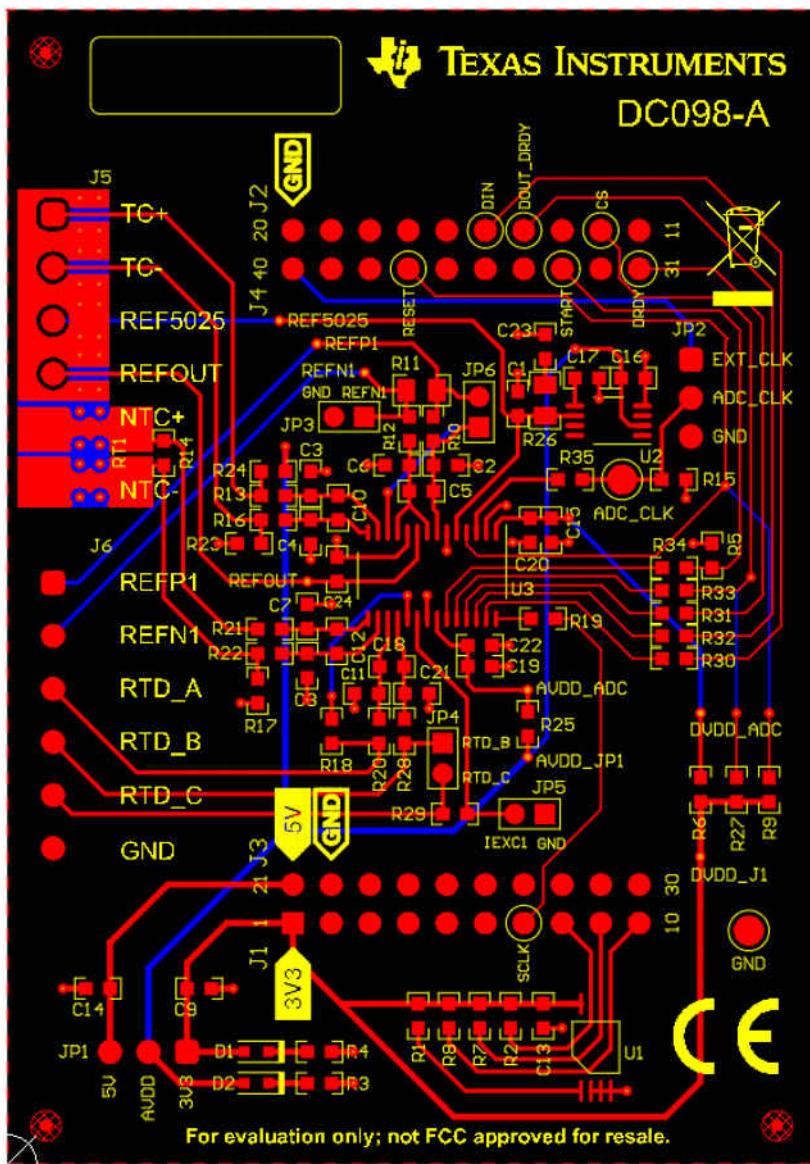
Designator	Quantity	Description	Part Number	Manufacturer
C1, C5, C10, C12, C18	5	CAP, CERM, 0.01 uF, 25 V, +/- 5%, C0G/NP0, 0603	C0603H103J3GACTU	Kemet
C2, C3, C4, C6, C7, C8, C11, C21	8	CAP, CERM, 1000 pF, 100 V, +/- 5%, C0G/NP0, 0603	GRM1885C2A102JA01D	MuRata
C9, C14, C15, C19, C23, C24	6	CAP, CERM, 10 uF, 25 V, +/- 20%, X5R, 0603	GRT188R61E106ME13D	MuRata
C13, C20, C22	3	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0603	C0603C104K3RACTU	Kemet
C16, C17	2	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603	C0603C105K3RACTU	Kemet
D1, D2	2	LED, Green, SMD	150060GS75000	Wurth Elektronik
J1/J3, J2/J4	2	Receptacle, 2.54mm, 10x2, Tin, TH	SSQ-110-03-T-D	Samtec
J5, J6	2	Terminal Block, 3.5mm, 6x1, Tin, TH	0393570006	Molex
JP1, JP2	2	Header, 100mil, 3x1, Gold, TH	TSW-103-07-G-S	Samtec
JP3, JP4, JP5, JP6	4	Header, 2mm, 2x1, Tin, TH	TMM-102-01-T-S	Samtec
R1, R2, R7, R8, R17	5	RES, 10.0 k, 1%, 0.1 W, 0603	RC0603FR-0710KL	Yageo
R3	1	RES, 470, 5%, 0.1 W, 0603	RC0603JR-07470RL	Yageo
R4	1	RES, 390, 1%, 0.1 W, 0603	RC0603FR-07390RL	Yageo
R5, R9, R27	3	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603100KFKEA	Vishay-Dale
R6, R25	2	RES, 0.1, 1%, 0.1 W, AEC-Q200 Grade 1, 0603	ERJ-L03KF10CV	Panasonic
R10, R12, R13, R16, R20, R21, R22, R28	8	RES, 4.12 k, 1%, 0.1 W, 0603	RC0603FR-074K12L	Yageo
R11	1	RES, 4.02 k, 0.1%, 0.125 W, 0805	RT0805BRD074K02L	Yageo America
R15	1	RES, 470 k, 1%, 0.1 W, 0603	RC0603FR-07470KL	Yageo
R18, R29	2	RES, 680, 1%, 0.1 W, 0603	RC0603FR-07680RL	Yageo
R19, R30, R31, R32, R33, R34, R35	7	RES, 47, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060347R0JNEA	Vishay-Dale
R26	1	RES, 1.1, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	ERJ-6GEYJ1R1V	Panasonic
SH-JP1, SH-JP2	2	Shunt, 100mil, Gold plated, Black	SNT-100-BK-G	Samtec
SH-JP3, SH-JP4, SH-JP5, SH-JP6	4	Shunt, 2mm, Gold plated, Black	2SN-BK-G	Samtec
TP1	1	Test Point, Miniature, Black, TH	5001	Keystone

Table 5-1. Bill of Materials (continued)

Designator	Quantity	Description	Part Number	Manufacturer
TP2	1	Test Point, Miniature, White, TH	5002	Keystone
U1	1	I2C BUS EEPROM (2-Wire), TSSOP-B8	BR24G32FVT-3AGE2	Rohm
U2	1	3 μ Vpp/V Noise, 3 ppm/ $^{\circ}$ C Drift Precision Series Voltage Reference, DGK0008A (VSSOP-8)	REF5025IDGKT	Texas Instruments
U3	1	24-Bit (or 16-bit), 2kSPS, 8-Ch, Delta-Sigma ADC for Precision Sensor Measurement, PW0028A (TSSOP-28)	ADS1248IPWR (or ADS1148IPWR)	Texas Instruments
R14	0	RES, 10.0 k, 1%, 0.1 W, 0603	RC0603FR-0710KL	Yageo
R23, R24	0	RES, 10.0 M, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060310M0FKEA	Vishay-Dale
RT1	0	Thermistor NTC, 10k ohm, 3%, 0603	ERT-J1VR103H	Panasonic

5.2 Printed Circuit Board Layout

Figure 5-1 to Figure 5-7 depict the ADS1x48EVM PCB layout.



Red = top layer; blue = bottom layer; yellow = top silkscreen; internal GND layers not shown

Figure 5-1. Composite PCB Layout

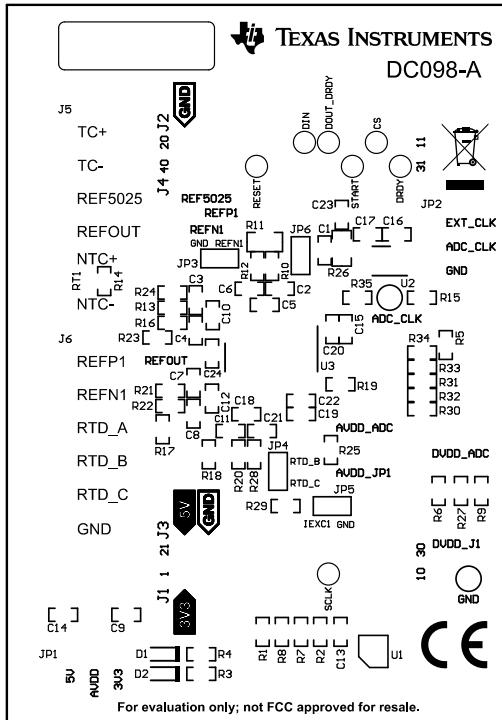


Figure 5-2. Top Silkscreen

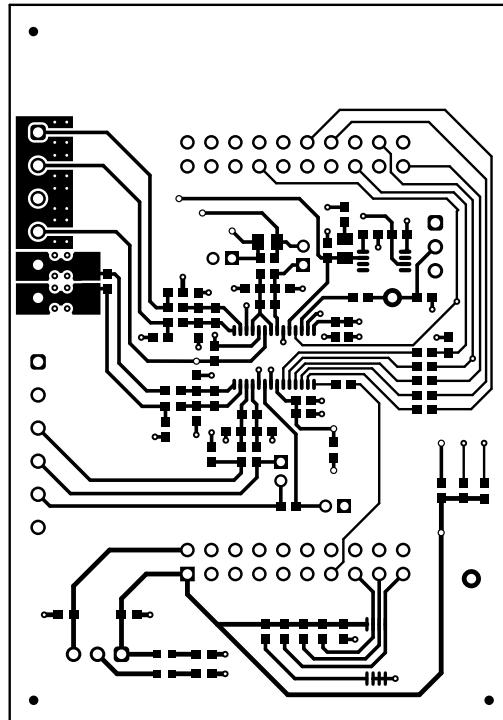


Figure 5-3. Top Layer

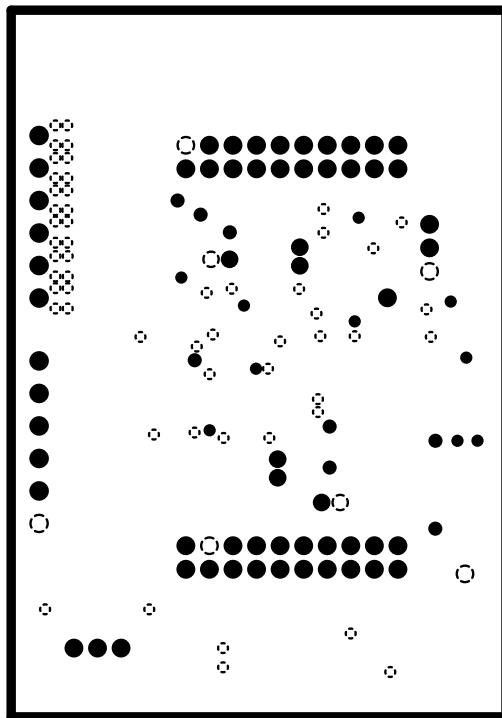


Figure 5-4. Internal Ground Layer 1

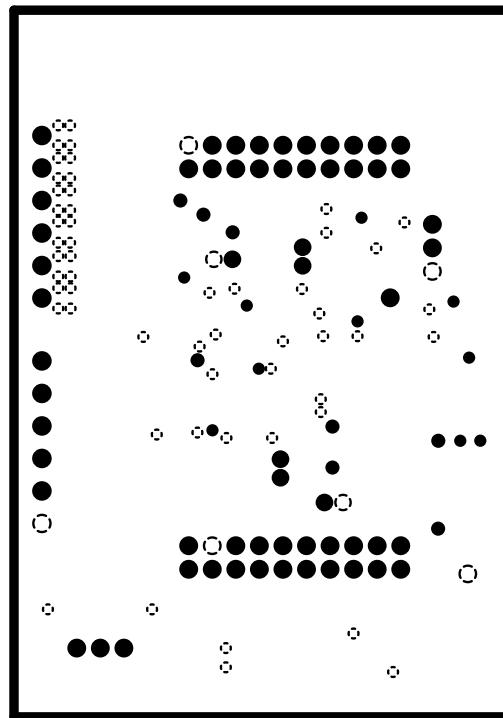


Figure 5-5. Internal Ground Layer 2

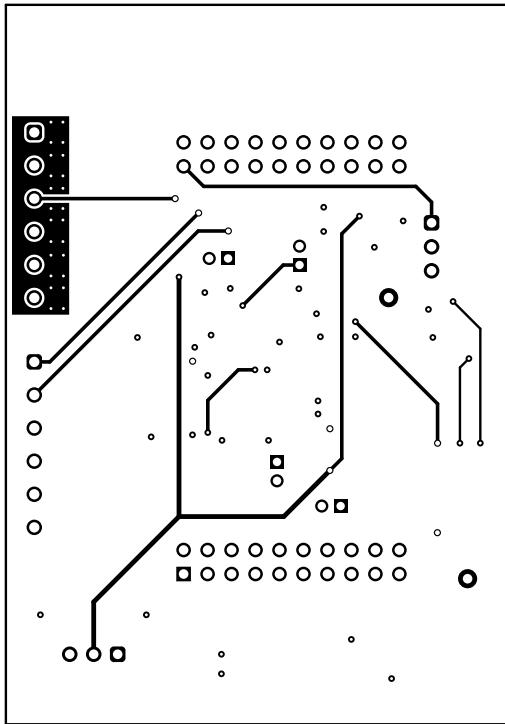


Figure 5-6. Bottom Layer

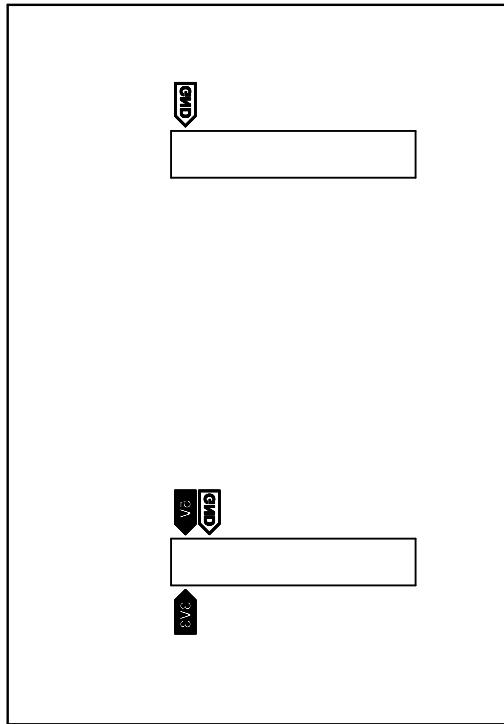


Figure 5-7. Bottom Silkscreen

5.3 Schematic

Figure 5-8 shows the ADS1x48EVM schematic.

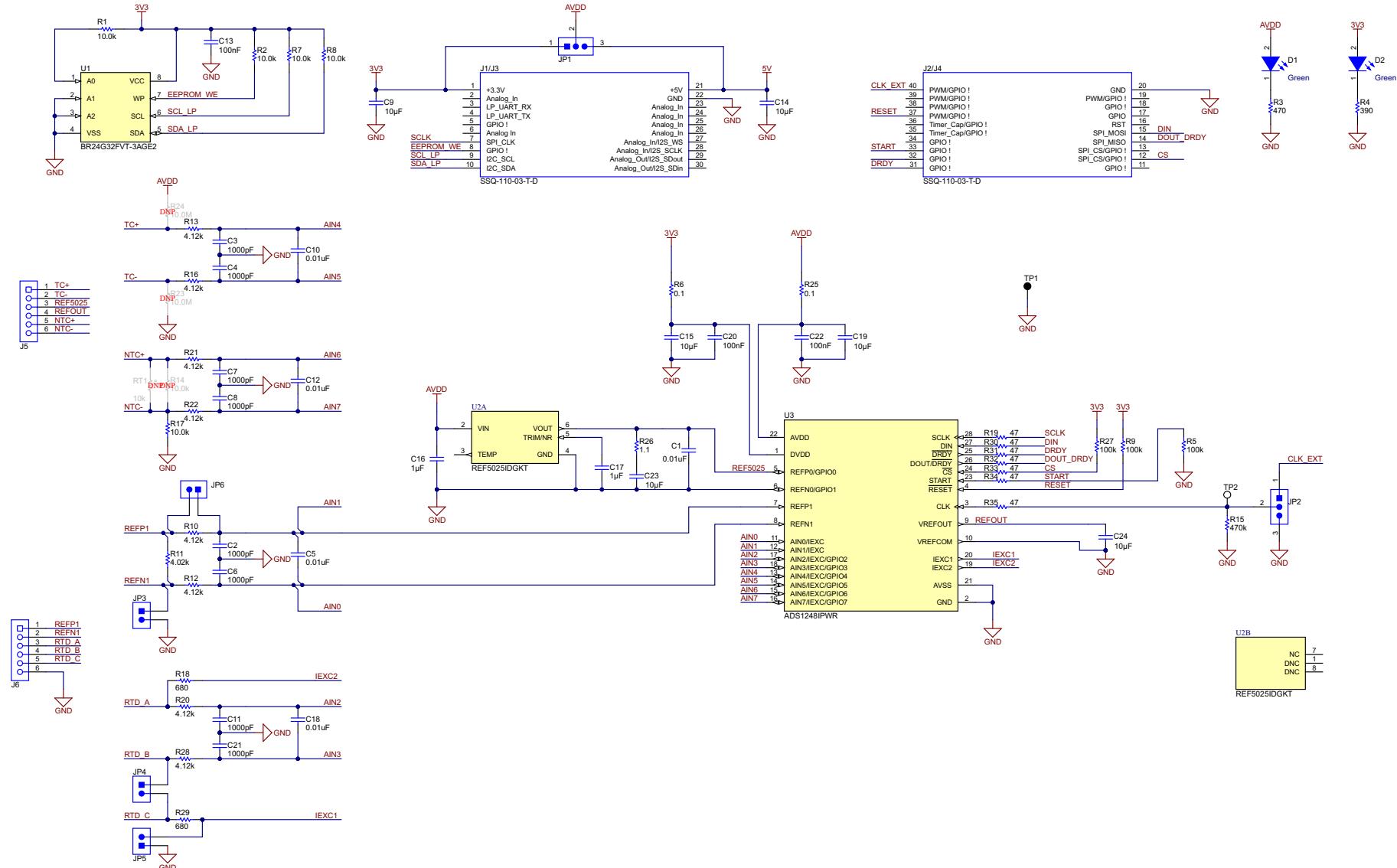


Figure 5-8. ADS1x48EVM Schematic

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from September 10, 2021 to January 11, 2022 (from Revision * (September 2021) to Revision A (January 2022))

	Page
• Deleted inclusive terminology from document.....	5
• Changed EVM landing page links to correct locations throughout document.....	6

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