Application Note

Designing EMC-Compliant, High-Accuracy Temperature Measurement (RTD/Thermocouple) Systems With ADS124S08

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ABSTRACT

This application note provides practical guidelines for designing electromagnetic compatibility (EMC)-optimized resistive temperature detector (RTD) and thermocouple (TC) measurement systems for industrial settings. This application note delves into important design aspects to help designers pass standard EMC tests, including effective circuit design and printed circuit board (PCB) layout techniques for both 2-layer and 4-layer boards. Additionally, this application note covers test setup considerations and the interpretation of IEC 61000-4-x standard EMC test results, aiding in the development of reliable industrial temperature measurement solutions.

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1 Circuit Design and Test System

This section discusses the input configurations, temperature error calculation and measurement, circuit and PCB layout design and optimization for designing a RTD and TC-based temperature measurement system.

1.1 Design Overview

Many industrial systems require precise temperature measurement, including temperature transmitters, temperature controllers, and temperature sensing input modules in programmable logic controllers (PLCs). Many industrial applications require high accuracy RTD and TC measurements that are also protected against electromagnetic interference (EMI), overvoltages, and other interference signals. This application note discusses two different types of EMC test boards that are designed for temperature measurement systems, one that supports all RTD wiring configurations, and another that can measure TCs using different bias techniques. Each type of circuit has a 4-layer and 2-layer circuit board. Table 1-1 shows the function and features supported by each circuit board:

Table 1-1. Circuit Board Design Summary

RTD	PCB Board Layers	Support PT100/PT1000?	Support 2/3/4-wire RTD?	Support low and high-side Reference?	Support 1 or 2 IDACs?
Board 1	4	Yes	Yes	Yes	Yes
Board 2	2	Yes	Yes	Yes	Yes
TC	PCB Board Layers	Pullup and pulldown resistor biasing?	Resistor biasing to the negative lead?	VBIAS for sensor biasing?	REFOUT biasing with a pullup resistor?
Board 3	4	Yes	Yes	Yes	Yes
Board 4	2	Yes	Yes	Yes	Yes

Each board in Table 1-1 uses the ADS124S08, a precision, 24-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC) offering low power consumption and many integrated features to reduce system cost and component count in applications measuring small-signal sensors. This ADC features a low-noise, programmable gain amplifier (PGA) to amplify low-level signals for resistive bridge, RTD or thermocouple applications. Additionally, two programmable current sources (IDACs) allow for easy and accurate current excitation in RTD applications. Finally, an input multiplexer supports up to 12 input signals that can be connected to the ADS124S08 in any combination for design flexibility.

All circuit boards in Table 1-1 also include external isolated power supplies and a digital isolator. The digital isolator provides galvanic isolation between the ADC serial peripheral interface (SPI) and the precision host interface (PHI) controller card that monitors conversion data from the ADS124S08. The PCB is designed to satisfy the IEC 61000-4-x standards for systems operating in a harsh electromagnetic environment.

Table 1-1 shows that all EMC test boards include the same circuit and characteristics other than 4-layer and 2-layer PCB design. RTD circuit board 1 and board 2 have the same schematic but use a different number of layers. TC circuit board 3 and board 4 have the same schematic but use a different number of layers. See Section 3 for the details.

For simplicity, the rest of this document uses two distinct design examples to illustrate the behavior and operation of a temperature measurement system:

- RTD temperature measurement: Circuit board 1 using a 3-wire RTD with a low-side and high-side voltage reference configuration.
- TC temperature measurement: Circuit board 3 with VBIAS and REFOUT biasing configuration.

If applicable, each section details any differences between circuit board 1 or circuit board 3 and the other circuit boards described in Table 1-1.

Figure 1-1 shows the ADS124S08 RTD EMC test board 1.

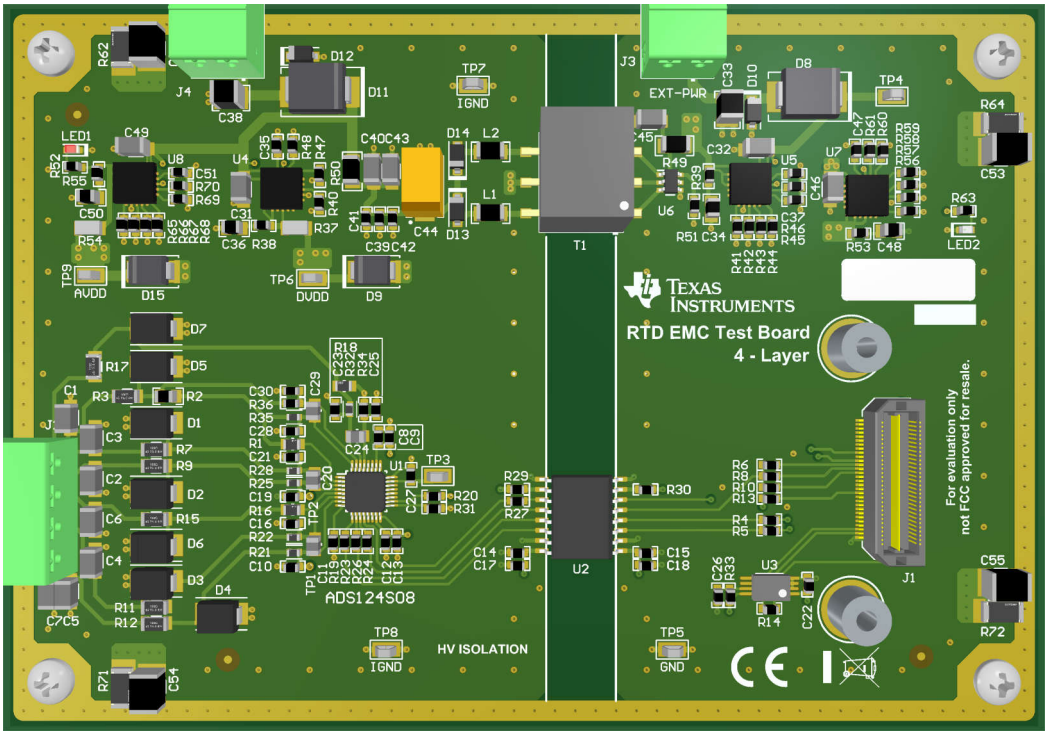


Figure 1-1. RTD EMC Test Board with ADS124S08 (4-Layer)

Figure 1-2 shows the ADS124S08 TC EMC test board 3.

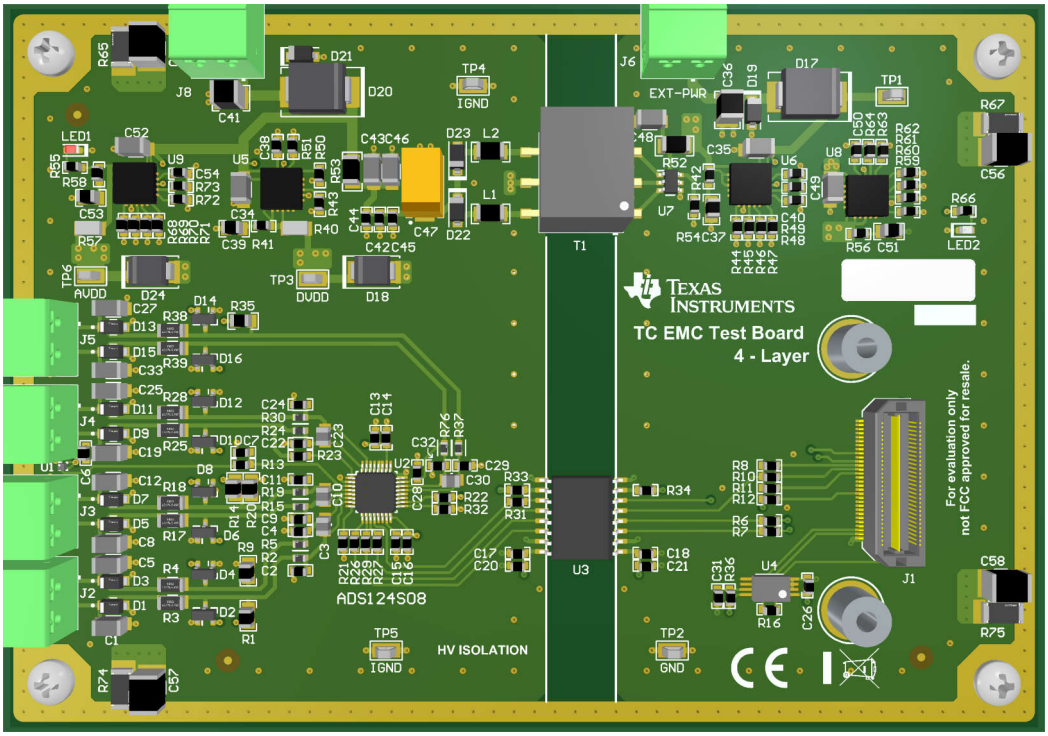


Figure 1-2. TC EMC Test Board with ADS124S08 (4-Layer)

1.2 Overview of EMC Test Board for RTD Measurements

This section describes the RTD EMC test board input configurations and provides the actual measured temperature error performance results.

- Input Configurations and ADC Settings
- Temperature Error - RTD Measurement

1.2.1 Input Configurations and ADC Settings

This section covers the RTD EMC test board input connections and configurations for 3-wire RTD measurements with a low-side and high-side reference configuration.

- Configuration and settings for a 3-wire RTD measurement with a low-side reference
- Configuration and settings for a 3-wire RTD measurement with a high-side reference

1.2.1.1 Configuration and settings for a 3-wire RTD measurement with a low-side reference

Figure 1-3 shows the 3-wire RTD measurement system with a low-side reference configuration used by the EMC test board. Two matched IDAC current sources are used for lead wire resistance cancellation. The ADS124S08 measures the RTD voltage using the AIN4 and AIN3 analog input channels on the EMC test board.

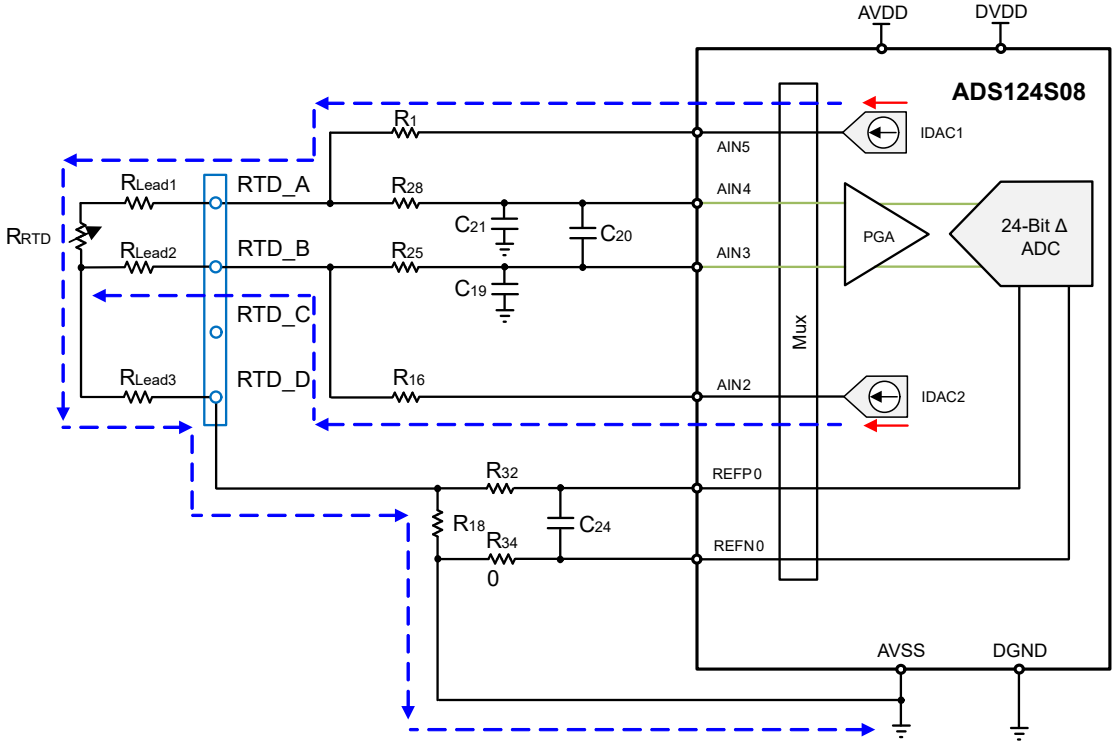


Figure 1-3. 3-Wire RTD, Low-Side Reference Measurement Circuit

The ADS124S08 was programmed with the following settings to measure the circuit shown in Figure 1-3:

- 4−kSPS data rate
- Sinc3 digital filter
- AIN4/AIN3 analog input
- IDAC1=IDAC2=250uA
- IDAC1 on AIN5, IDAC2 on AIN2
- External voltage reference on REFP0/REFN0
- Positive reference buffer is enabled

Equation 1 to Equation 7 calculate that a gain of 8 is required to maximize the ADS124S08 dynamic range for RTD measurements using a low-side reference:

$$R1=3.4k\Omega,\ R2=0\Omega \quad (1)$$

$$R_{RTD_{min}} \approx 18.5\Omega \text{ at } -200°C \text{ (PT100)} \quad (2)$$

$$V_{RTD\_max}=I_{IDAC}\times R_{RTD\_min}=250\mu A\times 18.5\Omega=0.004625V \quad (3)$$

$$V_{ADC\_min}=Gain\times V_{RTD\_min}=8\times 0.004625V=0.037V \quad (4)$$

$$R_{RTD_{max}} \approx 390\Omega \text{ at } +850°C \text{ (PT100)} \quad (5)$$

$$V_{RTD\_max}=I_{IDAC}\times R_{RTD\_max}=250\mu A\times 390\Omega=0.0975V \quad (6)$$

$$V_{ADC\_max}=Gain\times V_{RTD\_max}=8\times 0.0975V=0.78V \quad (7)$$

Equation 8 calculates the ADS124S08 reference voltage due to the specified IDAC current flowing through the precision 2.2kΩ reference resistor (R18):

$$V_{REF}=2\times I_{IDAC}\times R_{REF}=2\times 250\mu A\times 2.2k\Omega=1.1V \quad (8)$$

Equation 9 and Equation 10 show how to compute the RTD resistance (R_{RTD}) from the conversion code in decimal format:

$$CODE=\frac{V_{RTD}\times Gain\times 2^{N-1}}{V_{REF}}=\frac{I_{IDAC}\times R_{RTD}(\Omega)\times Gain\times 2^{N-1}}{2\times I_{IDAC}\times R_{REF}}=\frac{R_{RTD}(\Omega)\times Gain\times 2^{N-2}}{R_{REF}} \quad (9)$$

$$R_{RTD}=\frac{CODE\times R_{REF}}{Gain\times 2^{N-2}} \quad (10)$$

Where:

- CODE is the conversion code obtained from the ADS124S08.
- R_{REF} is the external reference resistor.
- N is the resolution of the ADC, where N = 24 for the ADS124S08.
- Gain is the value of the ADS124S08 PGA gain.

1.2.1.2 Configuration and settings for a 3-wire RTD measurement with a high-side reference

Figure 1-4 shows the 3-wire RTD measurement system with a high-side reference configuration used by the EMC test board. Two matched IDAC current sources are used for lead wire resistance cancellation. The ADS124S08 measures the RTD voltage using the AIN4 and AIN3 analog input channels on the EMC test board.

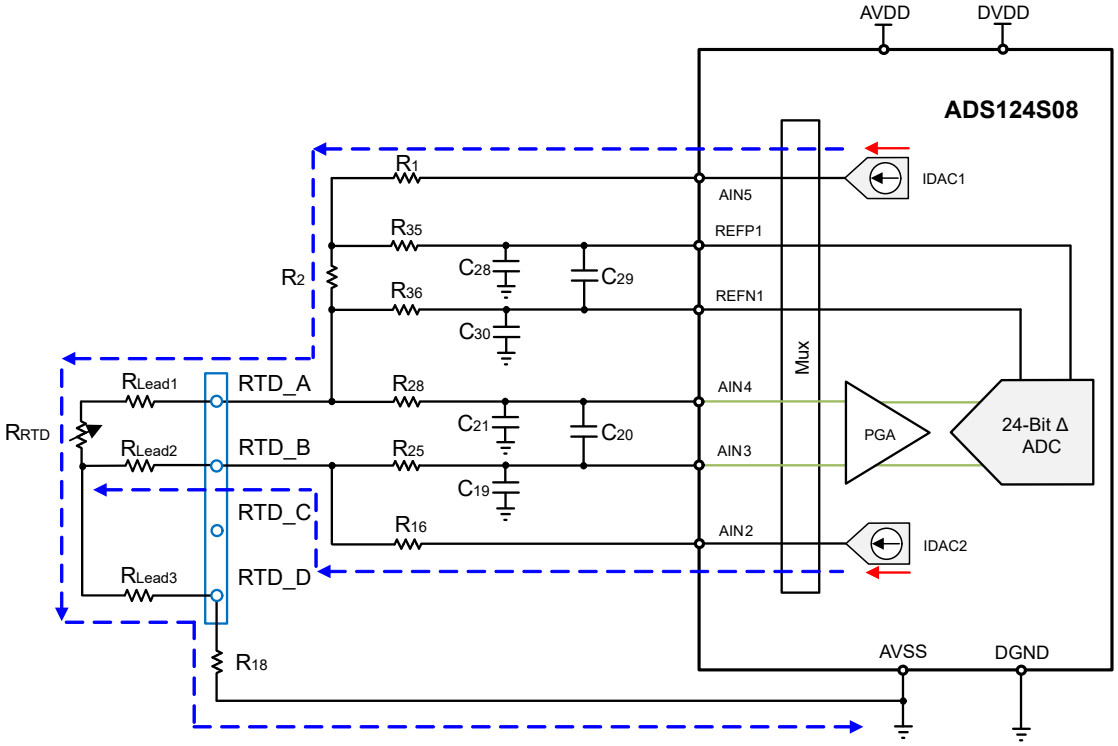


Figure 1-4. 3-Wire RTD, High-side Reference Measurement Circuit

The ADS124S08 was programmed with the following settings to measure the circuit shown in Figure 1-4:

- 4−kSPS data rate
- Sinc3 digital filter
- AIN4/AIN3 analog input
- IDAC1=IDAC2=250uA
- IDAC1 on AIN5, IDAC2 on AIN2
- External voltage reference on REFP1/REFN1
- Both positive and negative reference buffers are enabled

Equation 11 to Equation 17 calculate that a gain of 4 is required to maximize the ADS124S08 dynamic range for RTD measurements using a high-side reference:

$$R1=0\Omega,\ R18=400\Omega\ \text{(bias resistor)} \tag{11}$$

$$R_{RTD_{min}} \approx 18.5\Omega \text{ at } -200°C\ (PT100) \tag{12}$$

$$V_{RTD\_min}=I_{IDAC}\times R_{RTD\_min}=250\mu A\times 18.5\Omega=0.004625V \tag{13}$$

$$V_{ADC\_min}=Gain\times V_{RTD\_min}=4\times 0.004625V=0.00185V \tag{14}$$

$$R_{RTD_{max}} \approx 390\Omega \text{ at } +850°C\ (PT100) \tag{15}$$

$$V_{RTD\_max}=I_{IDAC}\times R_{RTD\_max}=250\mu A\times 390\Omega=0.0975V \tag{16}$$

$$V_{ADC\_max}=Gain\times V_{RTD\_max}=4\times 0.0975V=0.39V \tag{17}$$

Equation 18 calculates the ADS124S08 reference voltage due to the specified IDAC current flowing through the precision 2.2kΩ reference resistor (R2) :

$$V_{REF}=I_{IDAC}\times R_{REF}=250\mu A\times 2.2k\Omega=0.55V \quad (18)$$

Equation 19 and Equation 20 show how to compute the RTD resistance (R_{RTD}) from the conversion code (CODE):

$$CODE=\frac{V_{RTD}\times Gain\times 2^{N-1}}{V_{REF}}=\frac{I_{IDAC}\times R_{RTD}(\Omega)\times Gain\times 2^{N-1}}{I_{IDAC}\times R_{REF}}=\frac{R_{RTD}(\Omega)\times Gain\times 2^{N-1}}{R_{REF}} \quad (19)$$

$$R_{RTD}=\frac{CODE\times R_{REF}}{Gain\times 2^{N-1}} \quad (20)$$

Where:

- CODE is the conversion code obtained from the ADS124S08.
- R_{REF} is the external reference resistor.
- N is the resolution of the ADC, where N = 24 for the ADS124S08.
- Gain is the value of the ADS124S08 PGA gain.

Additionally, the resistor values, IDAC current and gain setting are selected to meet the ADS124S08 IDAC compliance voltage in both designs.

1.2.2 Temperature Error - RTD Measurement

This section describes how to calculate the ADS124S08 output data temperature error as well as provides the RTD EMC test board performance results.

- Calculating RTD temperature from RTD resistance
- Calculating the temperature error from RTD measurements
- Experimental setup and results

1.2.2.1 Calculating RTD temperature from RTD resistance

RTDs use the Callendar-Van Dusen equations to describe the relationship between the RTD resistance and measured temperature. Different equations are required across two different temperature ranges:

Equation 21 provides the relationship between RTD resistance and temperature in the range of 0˚C to 850˚C:

$$R_{RTD}(T)=R_0\times\left(1+A\times T+B\times T^2\right) \quad (21)$$

Calculate the temperature from the resistance by solving the quadratic equation in Equation 22:

$$T_{RTD}(°C)=\frac{-A\pm\sqrt{A^2-4\times B\times\left(1-\frac{R_{RTD}(T)}{R_0}\right)}}{2\times B} \quad (22)$$

Where:

- R_{RTD} (T)= Resistance at temperature (T).
- R_0 =Resistance at 0°C (R_0 = 100Ω for PT100 RTD).
- T = Temperature in degrees Celsius (°C).

A, B and C in Equation 22 are known as the Callendar-Van Dusen constants and are derived from experimentally determined parameters for platinum RTDs conforming to IEC 60751 and ASTME1137 standards:

$$A=3.908310^{-3} \quad (23)$$

$$B=-5.77510^{-7} \quad (24)$$

$$C=-4.18310^{-12} \quad (25)$$

Equation 26 provides the relationship between RTD resistance and temperature in the range of -200˚C to 0˚C:

$$R_{RTD}(T) = R_0 \times \left[1 + A \times T + B \times T^2 + C \times (T\text{-}100) \times T^3\right] \quad (26)$$

Calculating the temperature in terms of resistance requires determining the inverse of this quadratic equation, which involves complex math. Instead, use the best fit 5th-order polynomial shown in Equation 27 as a highly-accurate approximation:

$$T_{RTD}(°C) = -242.02 + 2.2228 \times R_{RTD} + \left(2.585910^{-3}\right) \times {R_{RTD}}^2 - \left(4.82610^{-6}\right) \times {R_{RTD}}^3 - \left(2.818310^{-8}\right) \times {R_{RTD}}^4 + \left(1.524310^{-10}\right) \times {R_{RTD}}^5 \quad (27)$$

1.2.2.2 Calculating the temperature error from RTD measurements

This section describes the steps to calculate the RTD temperature error from the ADS124S08 output data.

1. calculate the RTD resistance (R_{RTD}) from the conversion code using Equation 10 or Equation 20.
2. convert R_{RTD} to RTD temperature (T_{RTD}) using Equation 22 or Equation 27.
3. measure the RTD resistor value (R_{MEAS}) with a Keysight Technologies 3458A digital multimeter (or similar).
4. convert R_{MEAS} to temperature (T_{MEAS}) using Equation 22 or Equation 27. T_{MEAS} is the temperature corresponding to R_{MEAS}.
5. compute the temperature error measured using Equation 28:

$$T_{ERROR}(°C) = T_{MEAS} - T_{RTD} \quad (28)$$

1.2.2.3 Experimental setup and results

The RTD performance tests use precision resistors to simulate a temperature change instead of an actual PT100 sensor to maintain high accuracy measurements and simplify the tests. The input signal is calibrated with a Keysight Technologies 3458A digital multimeter to eliminate error from the resistors. Figure 1-5 shows the RTD EMC test board circuit that can be used with either a low-side or high-side reference configuration.

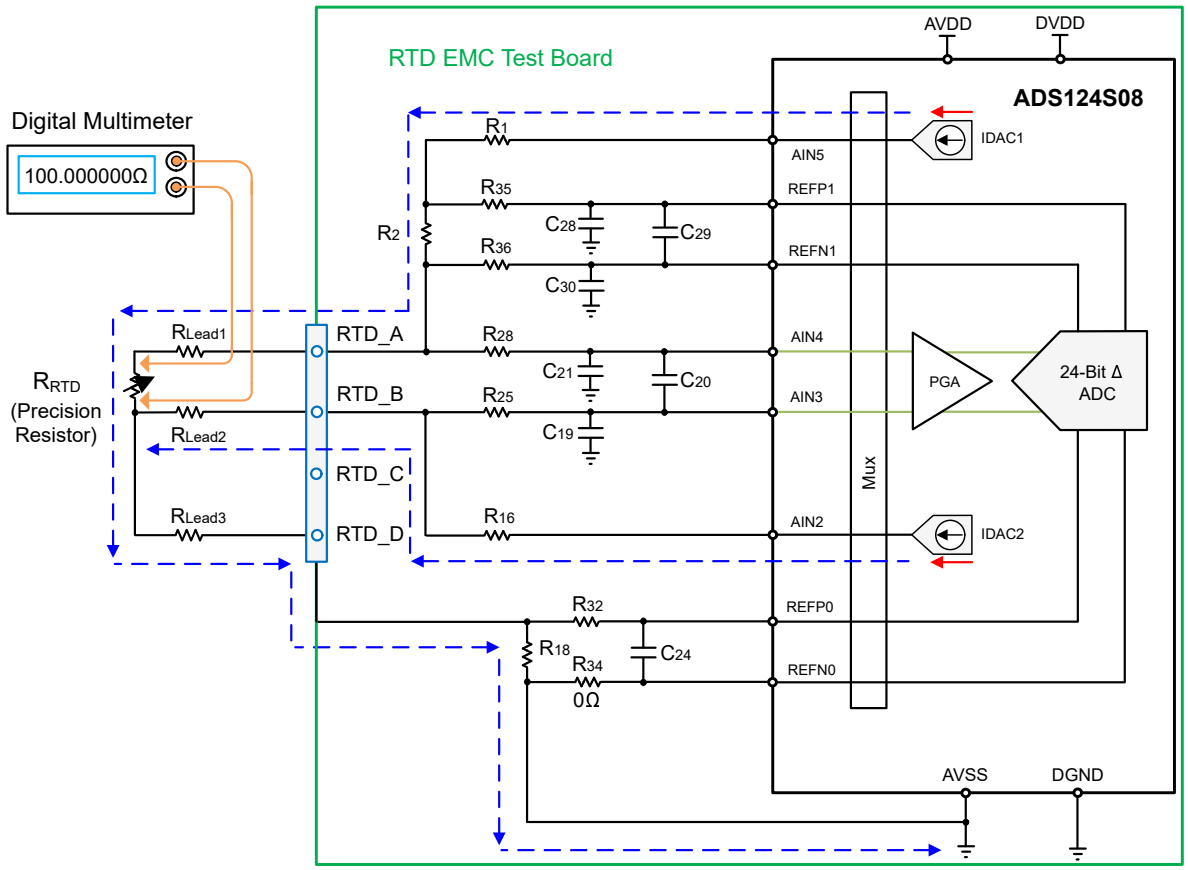


Figure 1-5. Low-Side and High-Side RTD Measurement Circuits on EMC Test Board

Figure 1-6 shows the measured, uncalibrated temperature error in blue and the measured, calibrated temperature error in red for the low-side reference configuration. This plot uses data collected from the 4-layer RTD EMC test board operating at room temperature and measuring a 3-wire RTD. The graph x-axis shows the RTD temperature converted from the measured resistance applied to the ADS124S08.

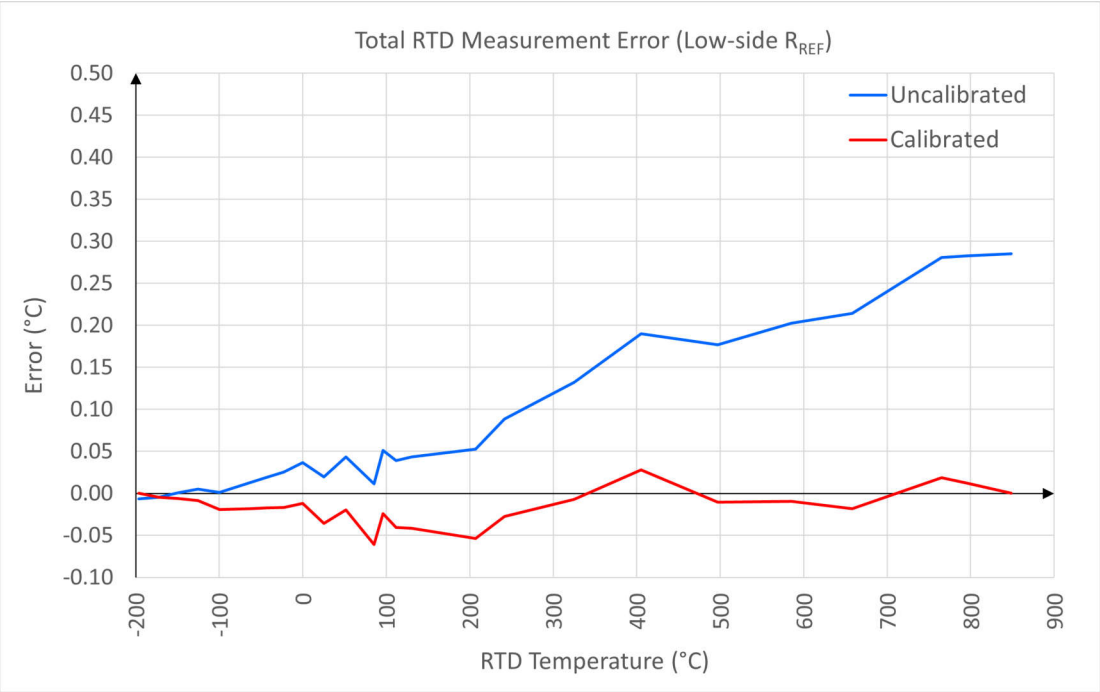


Figure 1-6. Uncalibrated VS. Calibrated Total RTD Measurement Error with Low-Side R_{REF}

Figure 1-7 shows the measured, uncalibrated temperature error in blue and the measured, calibrated temperature error in red for the high-side reference configuration. This plot uses data collected from the 2-layer RTD EMC test board operating at room temperature and measuring a 3-wire RTD. The graph x-axis shows the RTD temperature converted from the measured resistance applied to the ADS124S08.

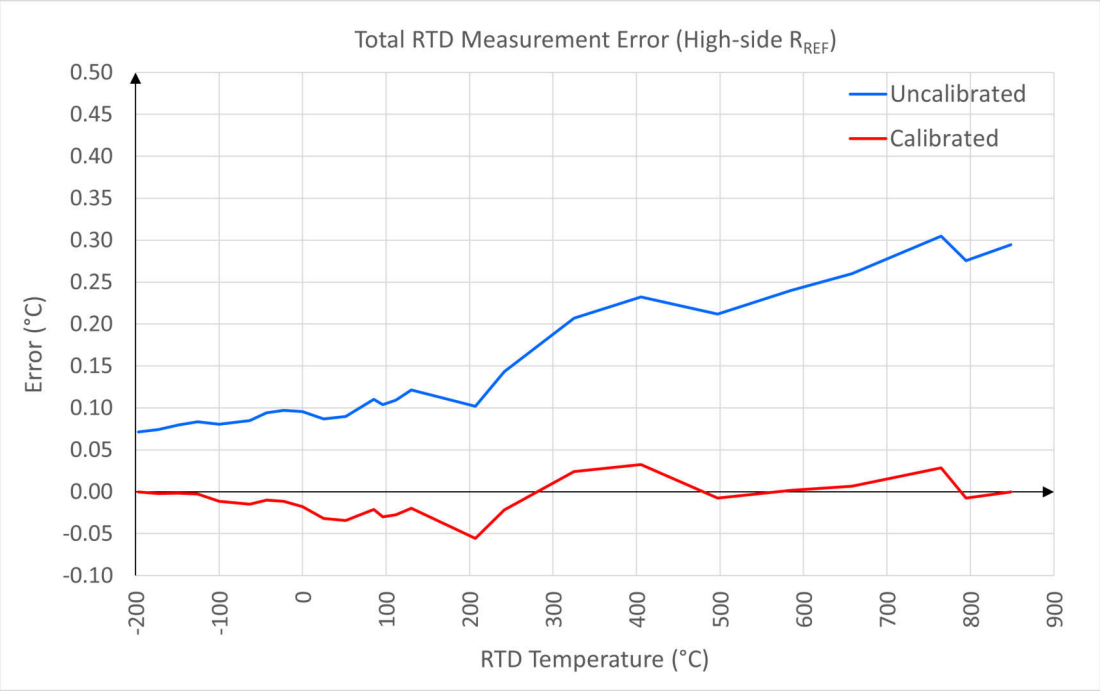


Figure 1-7. Uncalibrated VS. Calibrated Total RTD Measurement Error with High-Side R_{REF}

The resistor and IDAC settings can be adjusted to be compatible with a PT1000 or other type RTD sensor. Refer to the application note for more information regarding RTD measurements: A Basic Guide to RTD Measurements.

1.3 Overview of EMC Test Board for TC Measurements

This section describes the TC EMC test board input configurations and provides the actual measured temperature error performance results.

- Input Configurations and ADC Settings
- Temperature Error - TC Measurement

1.3.1 Input Configurations and ADC Settings

This section describes input configurations, thermocouple characteristics and ADC settings for TC measurements with VBIAS and REFOUT biasing.

- Input Configurations
- Thermocouple Characteristics and ADC Settings

1.3.1.1 Input Configurations

The TC EMC test boards support four different biasing circuits. Each biasing circuit uses a different analog input channel pair on the ADS124S08. This section describes two circuit topologies used to bias the thermocouple during the EMC compliance testing.

Figure 1-8 shows a thermocouple biasing circuit that uses the ADS124S08 VBIAS generator. The VBIAS generator is applied to the negative lead of the thermocouple through the AINCOM pin and sets the common-mode voltage to mid-supply.

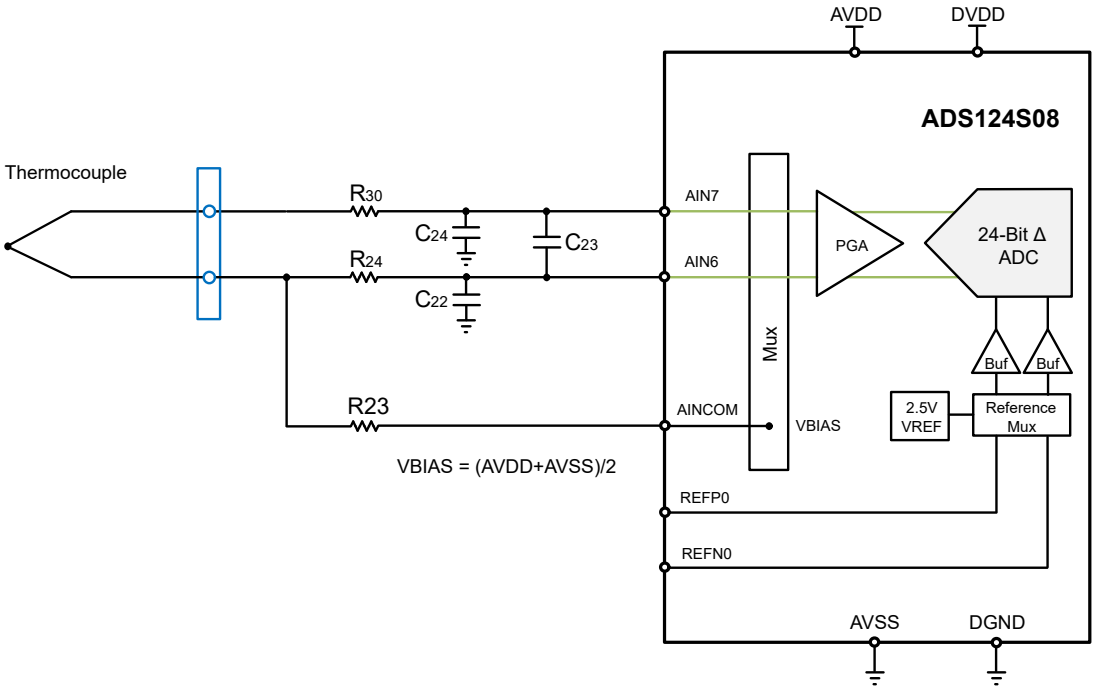


Figure 1-8. VBIAS Biasing, TC Measurement Circuit on EMC Test Board

Figure 1-9 shows a thermocouple biasing circuit that uses the ADS124S08 internal voltage reference (REFOUT). The circuit sets the common-mode voltage of the thermocouple signal to 2.5V, which is the mid-supply voltage when AVDD is +5V. Pull up resistor (R35) to AVDD allows for burn-out detection without a separate measurement.

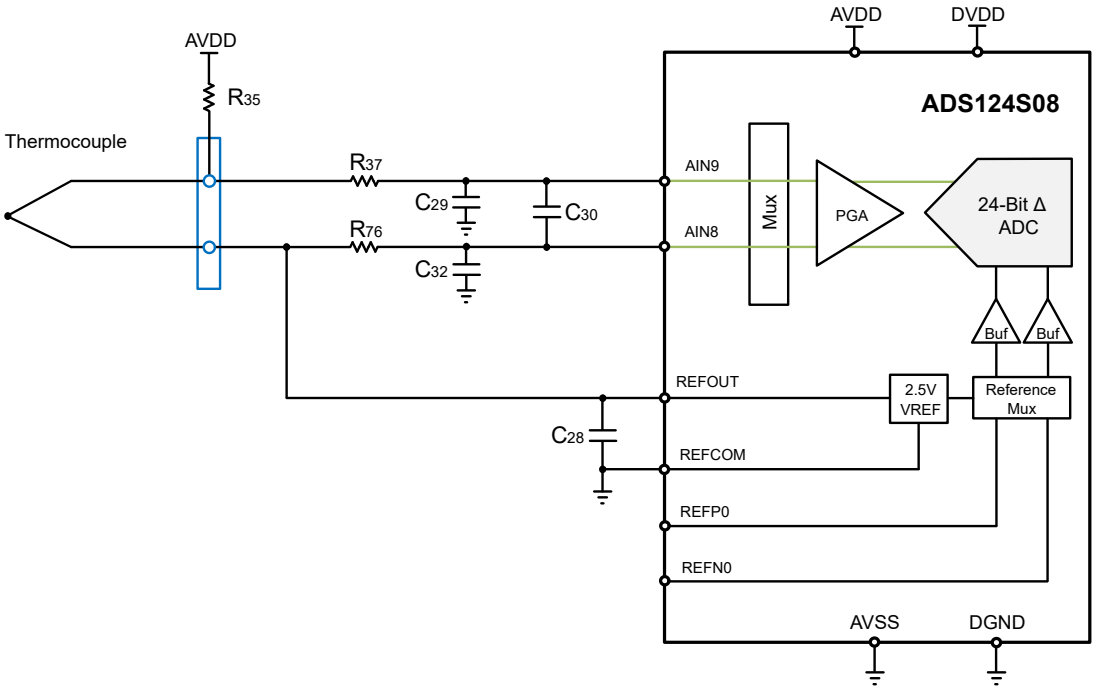


Figure 1-9. REFOUT Biasing, TC Measurement Circuit on EMC Test Board

Refer to the application note for more information regarding TC measurements: A Basic Guide to Thermocouple Measurements.

1.3.1.2 Thermocouple Characteristics and ADC Settings

There are a wide variety of thermocouple types that are suitable for different applications. Each type of thermocouple has different characteristics for temperature range, sensitivity, voltage range, and application capability depending on the physical properties of its metals. Table 1-2 lists several common thermocouple types and their characteristics.

Table 1-2. Temperature and Voltage Range of Common Thermocouples

Thermocouple type	Measurable temperature range (°C)	Voltage over temperature range (mV)
J	−210 to 1200	−8.095 to 69.553
K	−270 to 1370	−6.458 to 54.886
T	−200 to 400	−6.258 to 20.872
E	−270 to 1000	−9.385 to 76.373
S	−50 to 1768	−0.236 to 18.693

K-Type thermocouples are the most common thermocouples used in industrial applications. Therefore, this document uses the typical voltage range of a K-type thermocouple as the test input signal.

The ADS124S08 was programmed with the following settings to measure the circuit shown in Figure 1-8 and Figure 1-9:

- 4-kSPS data rate
- Sinc3 digital filter
- Internal 2.5V voltage reference (V_{REF})
- Gain=32 to maximize the dynamic range of ADS124S08 for K-Type thermocouple
- AIN7/AIN6 analog input, enable VBIAS on AINCOM pin for TC measurement with VBIAS biasing
- AIN9/AIN8 analog input, connect REFOUT to AIN8 for TC measurement with REFOUT biasing

Use Equation 29 to compute the thermoelectric voltage (V_{TC}) from the ADS124S08 conversion code (CODE):

$$V_{TC} = \frac{CODE \times V_{REF}}{Gain \times 2^{N-1}} \quad (29)$$

1.3.2 Temperature Error - TC Measurement

This section describes how to calculate the ADS124S08 output data temperature error as well as provides the TC EMC test board performance results.

- Calculating temperature from TC thermoelectric voltage
- Calculating the temperature error from TC measurements
- Experimental setup and results

1.3.2.1 Calculating temperature from TC thermoelectric voltage

The International Temperature Scale of 1990 (ITS−90) standard defines several polynomial equations that correlate the thermocouple measured voltage output to temperature. The equations are used to calculate the thermoelectric voltage from temperature or to calculate temperature from the thermoelectric voltage.

The TC EMC test boards support cold-junction compensation (CJC), which is required to accurately determine the absolute thermocouple junction temperature. However, the test results based in the application note do not include compensation. Refer to the application note for details on thermocouple measurement if CJC is needed: A Basic Guide to Thermocouple Measurements.

Equation 30 shows the general polynomial function used to calculate the temperature based on the thermocouple voltage.

$$T_{TC}(°C) = d_0 + d_1 \times E + d_2 \times E^2 + d_3 \times E^3 + d_4 \times E^4 + d_5 \times E^5 + d_6 \times E^6 + d_7 \times E^7 + d_8 \times E^8 + d_9 \times E^9 \quad (30)$$

Where:

- E is the voltage in microvolts measured by the ADS124S08
- T_{TC} is the temperature in degrees Celsius (°C)

Table 1-3 shows the coefficients of a K−type thermocouple as an example. Note that the polynomial coefficients are different depending on the measured temperature range.

Table 1-3. ITS-90 Temperature Coefficients for a K−Type Thermocouple

Temperature Range	−200°C to 0°C	0°C to 500°C	500°C to 1372°C
Voltage Range	**−5.891 mV to 0 mV**	**0 mV to 20.644 mV**	**20.644 mV to 54.886 mV**
d_0	0	0	-1.31805810^{2}
d_1	2.517346210^{1}	2.50835510^{1}	4.83022210^{1}
d_2	-1.1662878	7.86010610^{-2}	-1.646031
d_3	-1.0833638	-2.50313110^{-1}	5.46473110^{-2}
d_4	-8.97735410^{-1}	8.31527010^{-2}	-9.65071510^{-4}
d_5	-3.734237710^{-1}	-1.22803410^{-2}	8.80219310^{-6}
d_6	-8.663264310^{-2}	9.80403610^{-4}	-3.11081010^{-8}
d_7	-1.045059810^{-2}	-4.41303010^{-5}	0
d_8	-5.192057710^{-4}	1.05773410^{-6}	0
d_9	0	-1.05275510^{-8}	0
Error Range	0.04°C to -0.02°C	0.04°C to -0.05°C	0.06°C to -0.05°C

Using a lookup table is another efficient way to determine the temperature from the thermoelectric voltage.

1.3.2.2 Calculating the temperature error from TC measurements

This section describes the steps to calculate the TC temperature error from the ADS124S08 output data.

1. calculate the thermoelectric voltage (V_{TC}) from the conversion code using Equation 29.
2. convert V_{TC} to TC temperature (T_{TC}) using Equation 30 and Table 1-3 for a K−Type thermocouple.
3. measure the test signal (V_{MEAS}) on ADS124S08 input with a Keysight Technologies 3458A digital multimeter (or similar).
4. convert V_{MEAS} to temperature T_{MEAS} using Equation 30 and Table 1-3. T_{MEAS} is the temperature corresponding to V_{MEAS}.
5. compute the temperature error using Equation 31:

$$T_{ERROR}(°C) = T_{MEAS} - T_{TC} \quad (31)$$

1.3.2.3 Experimental setup and results

The TC performance tests use a precision signal generator (DP8200) to simulate a temperature change instead of an actual K-type TC to maintain high accuracy measurements and simplify the tests. The input signal is calibrated with a Keysight Technologies 3458A digital multimeter (or similar) to eliminate error from the signal generator. Figure 1-10 shows the TC EMC test board circuit that can be used with either a VBIAS or REFOUT thermocouple biasing circuit.

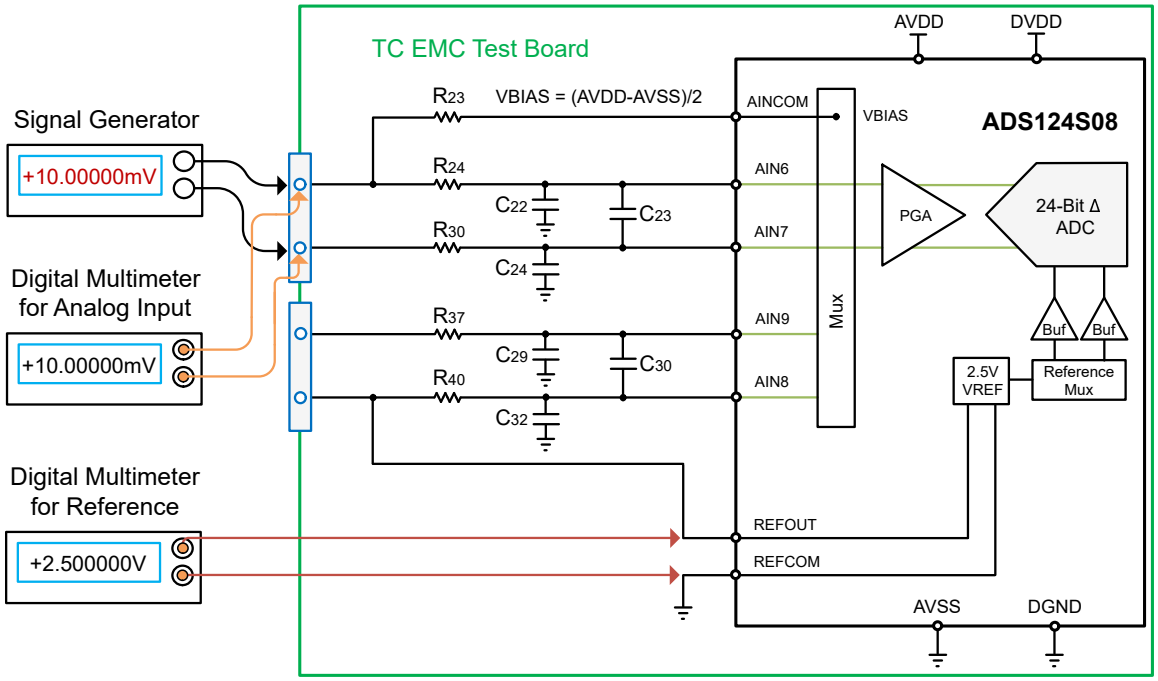


Figure 1-10. VBIAS and REFOUT Biasing TC Measurement Circuits on EMC Test Board

Figure 1-11 shows the measured, uncalibrated temperature error in blue and the measured, calibrated temperature error in red using VBIAS thermocouple biasing. This plot uses data collected from the 2-layer TC EMC test board operating at room temperature. The graph x−axis shows the TC temperature converted from the measured voltage applied to the ADS124S08 using the precision signal generator.

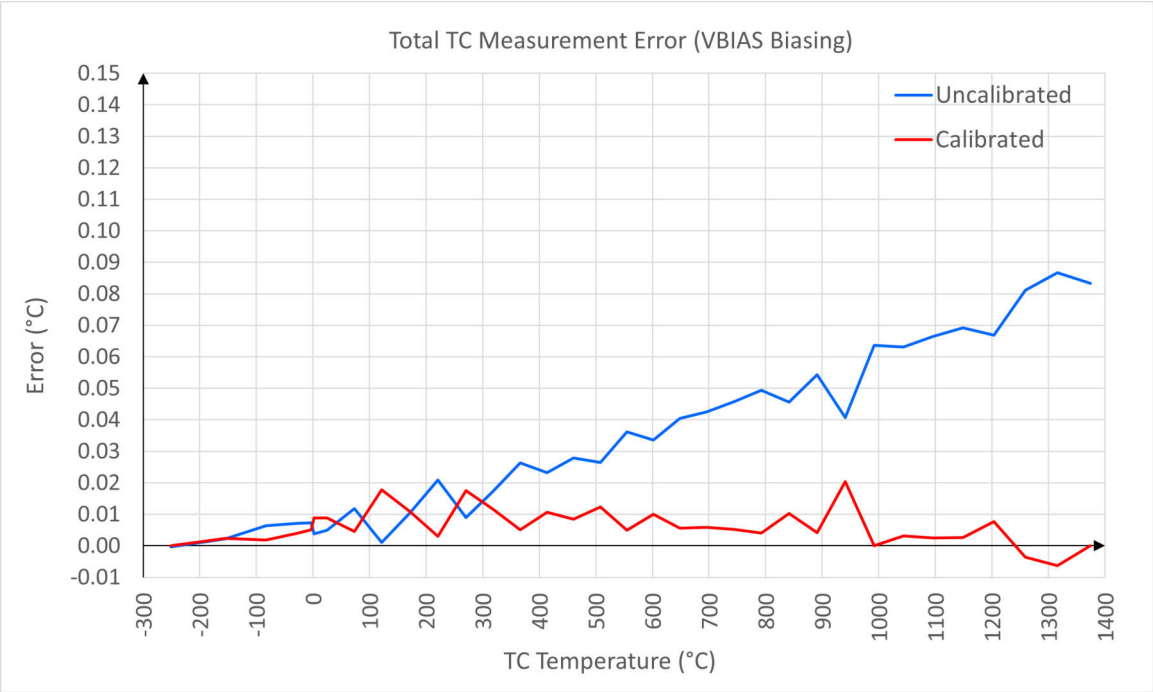


Figure 1-11. Uncalibrated VS. Calibrated Total TC Measurement Error with VBIAS Biasing

Figure 1-12 shows the measured, uncalibrated temperature error in blue and the measured, calibrated temperature error in red using REFOUT thermocouple biasing. This plot uses data collected from the 2-layer TC EMC test board operating at room temperature. The graph x−axis shows the TC temperature converted from the measured voltage applied to the ADS124S08 using the precision signal generator.

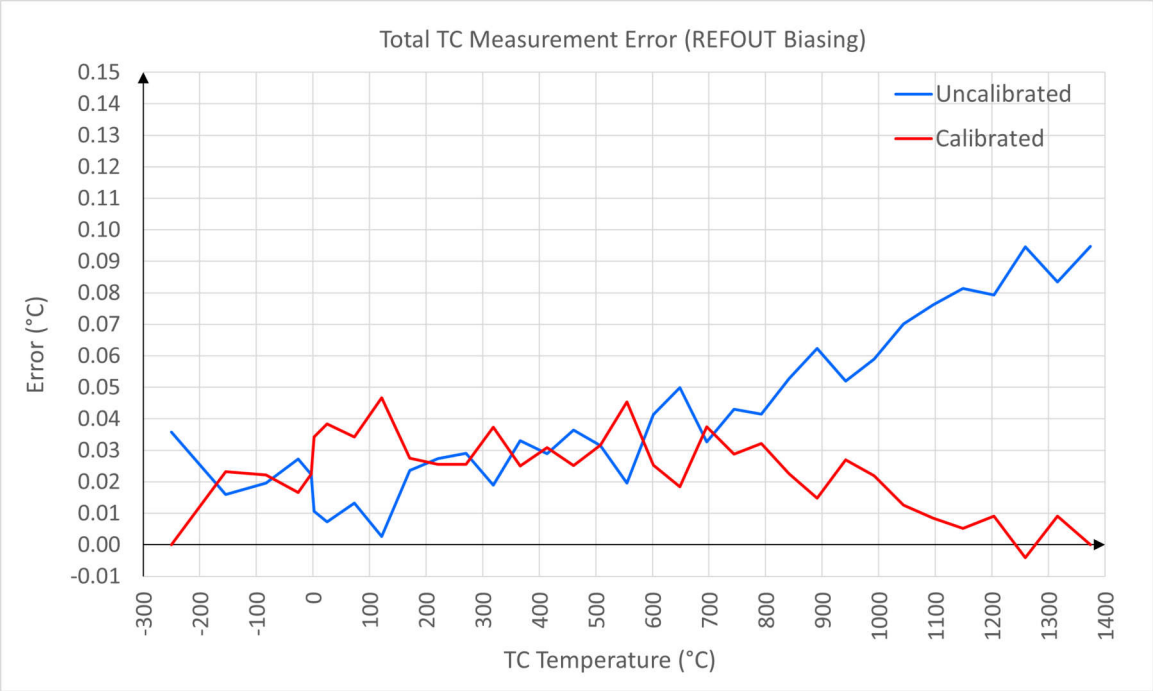


Figure 1-12. Uncalibrated VS. Calibrated Total TC Measurement Error with REFOUT Biasing

1.4 Circuit Design Considerations for EMC compliance

This section describes the EMC test board design that protects the ADS124S08, improves the system EMC performance, and maintains measurement accuracy.

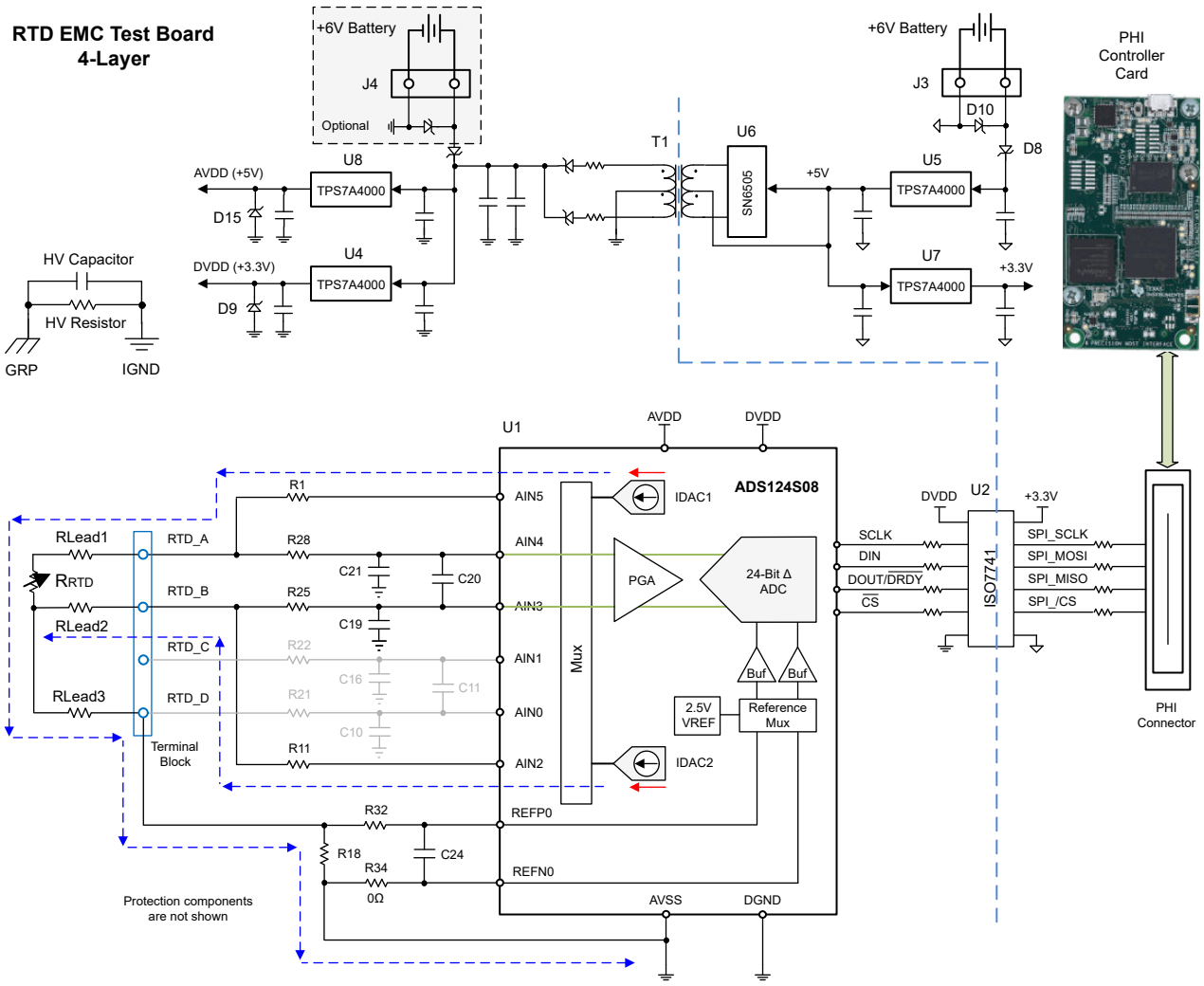


Figure 1-13. EMC Test Circuit Board (3-wire RTD, low-side reference) and PHI Connection

Figure 1-13 uses a 3-wire RTD with a low-side reference measurement circuit as an example to show the complete EMC test board block diagram. The TC EMC test boards use a design similar to the RTD test boards for the anti-aliasing filter, protection circuity, isolated power supply, isolated digital isolator and PCB layout. Only the input configurations are different. For simplicity, the rest of this section uses the 4-layer RTD EMC test board as an example of the circuit and the layout design, as well as the operation of all test boards.

Considerations for the EMC test board include:

- Analog Input Protection
- Anti-aliasing Filter
- High-voltage Capacitors on every Input Connector Pin
- High-voltage Capacitors and Resistors for Discharging Path
- Series Resistors on Digital Signals
- Digital Isolation
- Power Supply and Protection

1.4.1 Analog Input Protection

Each analog input includes an external protection circuitry to protect the ADS124S08 from electrical overstress (EOS). Additionally, each analog input includes properly-selected bidirectional transient voltage suppressor (TVS) diode to help shunt transient energy away from the signal path.

The general selection guidelines are as follows:

- TVS diode: Low leakage current, low temperature drift of leakage current, proper standoff voltage
- Current limiting resistor: power rating, temperature drift, tolerance, ADC IDAC compliance voltage

Refer to the application note for details about protection techniques and component selection: Circuit for Protecting ADS124S08 ADC from EOS for RTD Measurement.

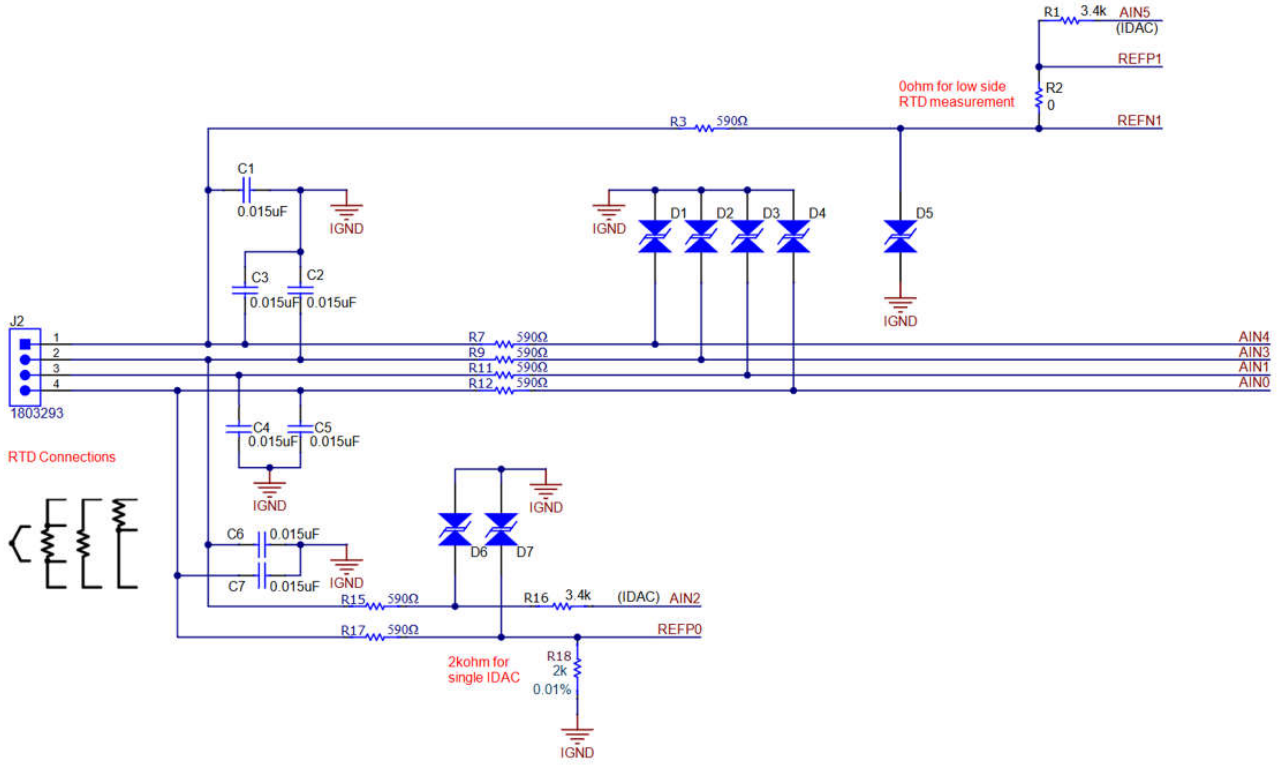


Figure 1-14. Analog Input Protection

1.4.2 Anti-aliasing Filter

An anti-aliasing filter is designed to keep frequency content at or near the delta-sigma ADC modulator frequency from aliasing back into the passband, since these frequencies are not natively rejected by the digital filter. As a result, start by choosing a differential filter 3dB cutoff frequency that is 10x to 100x lower compared to the modulator frequency. This results in 20dB to 40dB rejection of frequencies around the modulator frequency, respectively. The amount of rejection depends on the design goals.

A large filter resistance can introduce significant offset errors at the ADC inputs due to ADC input leakage current. It is typically acceptable to choose the resistor value in the anti-aliasing filter to be no larger than 10kΩ to help minimize these offset errors, though R_{FILTER}< 5kΩ is usually sufficient in most cases. Choose common-mode capacitors 10x to 20x smaller than the differential capacitor so any mismatch between these two capacitors does not cause common-mode noise to become differential noise.

The ADS124S08 EMC test boards use two 4.99kΩ resistors, two 4.7nF common-mode capacitors and a 47nF differential capacitor for the anti-aliasing filter at the ADC analog inputs.

The differential cutoff frequency of the anti-aliasing filter is given by Equation 32:

$$f_{DIFF} = \frac{1}{2\pi \times (2 \times R_{FILTER}) \times C_{DIFF}} = \frac{1}{2\pi \times (2 \times 4.99 \times 10^{3}) \times 47 \times 10^{-9}} = 339.5Hz \quad (32)$$

The common-mode cutoff frequency of the anti-aliasing filter is given by Equation 33:

$$f_{CM} = \frac{1}{2\pi \times R_{FILTER} \times C_{CM}} = \frac{1}{2\pi \times 4.99 \times 10^{3} \times 4.7 \times 10^{-9}} = 6.79kHz \quad (33)$$

Figure 1-15 shows a typical anti-aliasing filter circuit on the EMC test boards:

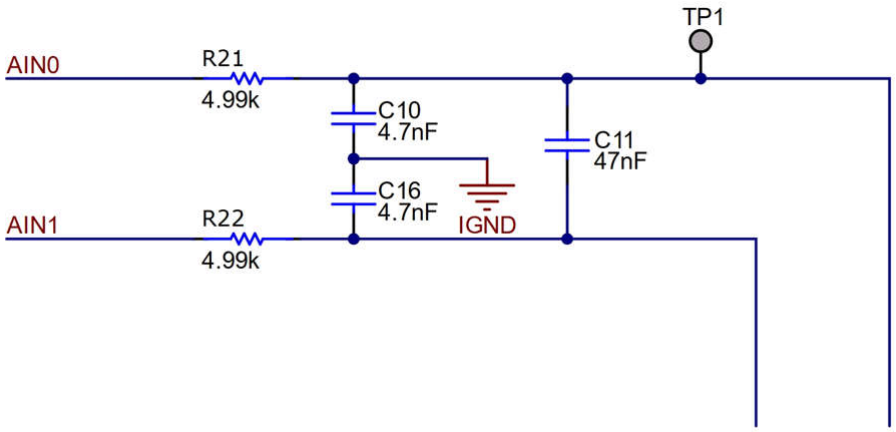


Figure 1-15. RC Components in Anti-aliasing Filter

1.4.3 High-voltage Capacitors on Every Input Connector Pin

Filtering signals directly at the input connector helps increase electrostatic discharge immunity, reduce radiated emissions, and increase immunity to coupled burst signals on the input. Every input signal that enters the PCB board needs a filter element such as a ceramic capacitor. Connect the capacitor between the input connector and the local ground plane with a wide trace. Place this capacitor as close as possible to the connector pin.

Use C0G/NPO type capacitors to minimize input signal distortion because C0G/NPO capacitors have minimal capacitance change with temperature, negligible capacitance drift with voltage and frequency changes, and no aging characteristics.

Use a high-voltage rated capacitor because this component is exposed to high energy transient signals including electrostatic discharge, electrical fast transients or surge signals during the EMC test.

The capacitance of the capacitor is determined by the frequency of the input signal. This design measures slow-moving temperature signals such that larger value capacitors can be used. Therefore, this design uses a 250V high voltage, C0G type, 0.015µF ceramic capacitor on each ADC channel as close as possible to the input terminal blocks so that the transient energy is discharged to ground through the shortest path.

Figure 1-16 shows high-voltage capacitor circuit on the EMC test boards:

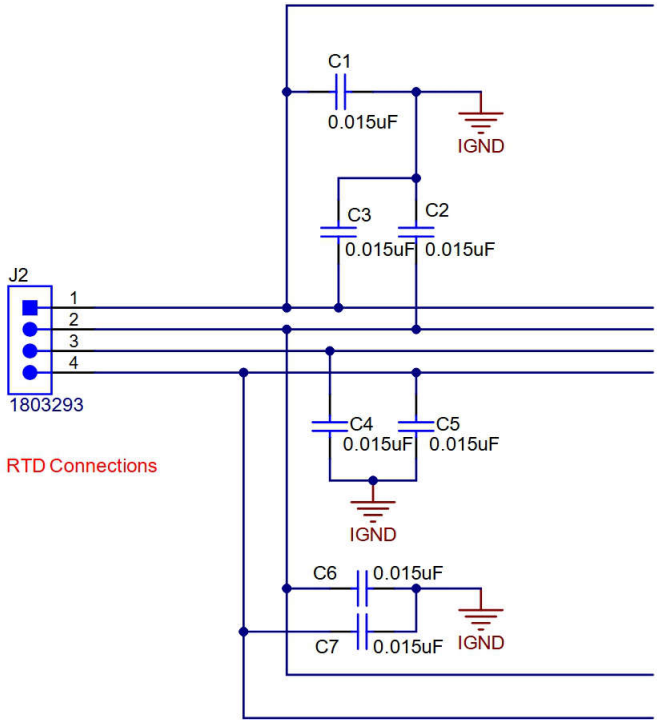


Figure 1-16. High-voltage Capacitors on Input Connector

1.4.4 High-voltage Capacitors and Resistors for Discharging Path

A high voltage 3kV, 2.2nF capacitor and a 2.2kV, 3.3MΩ resistor are placed in parallel between the protected local ground and the ground reference plane (GRP). These components provide a path to discharge transient energy to the GRP (E_GND) and protect the components on the circuit board. Two discharge paths including R62 || C52 and R71 || C54 are designed on the isolated side of the circuit board. The same components in parallel are used in the non-isolated side of the EMC test board, R64 || C53 and R72 || C55.

Figure 1-17 shows the high-voltage capacitor and resistor schematic and PCB layout example on the EMC test boards:

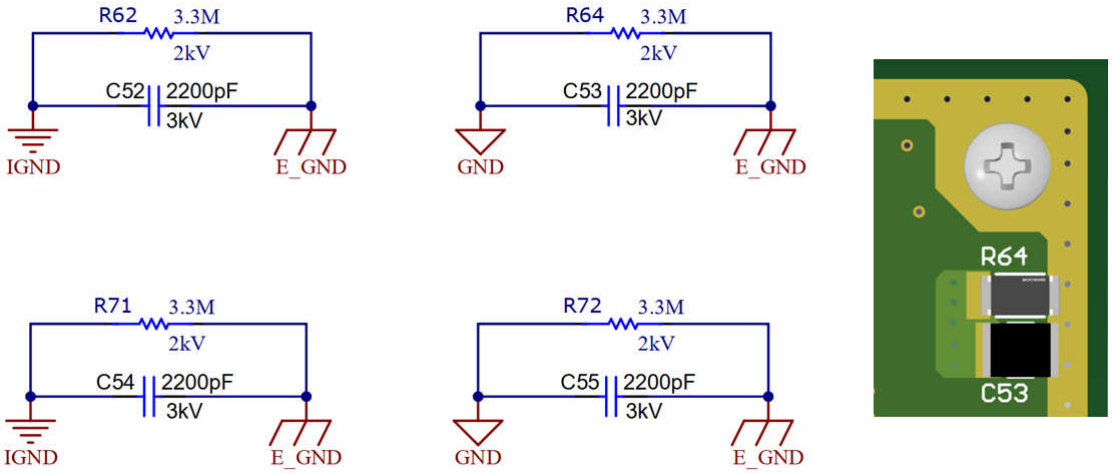


Figure 1-17. Adding High-voltage Capacitors and Resistors

1.4.5 Series Resistors on Digital Signals

The fast transitions on high-speed digital signals can lead to radiated emissions or reflections in the case of a long transmission line. Adding a series resistor can help increase the rise- and fall-time of any digital signal, especially high-speed clock signals, and impact EMC performance by:

- Slowing down transition edges:

  a series termination resistor effectively increases the time constant of the digital line by adding the resistance in series with the capacitance and inductance of the digital line.
- Reducing reflections and emissions:

  a series termination resistor can minimize the reflections that can cause ringing, overshot, and undershoot by matching the source impedance to the characteristic impedance of the transmission line.
- Reducing high-frequency harmonics:

  longer transition times can result in lower bandwidth and high-frequency harmonics that are often responsible for radiating emissions.
- Improving signal integrity:

  a series termination resistor helps improve the integrity of the digital signal, leading to more reliable data transmission.

Choose the value of the series resistor to match the characteristic impedance of the transmission line for optimal impedance matching and minimal reflections. The 49.9Ω resistors on the digital lines between the ADS124S08, digital isolator and the PHI controller board are chosen in this design as shown in Figure 1-18. Place the series resistor as close to the driver as possible for effective series termination.

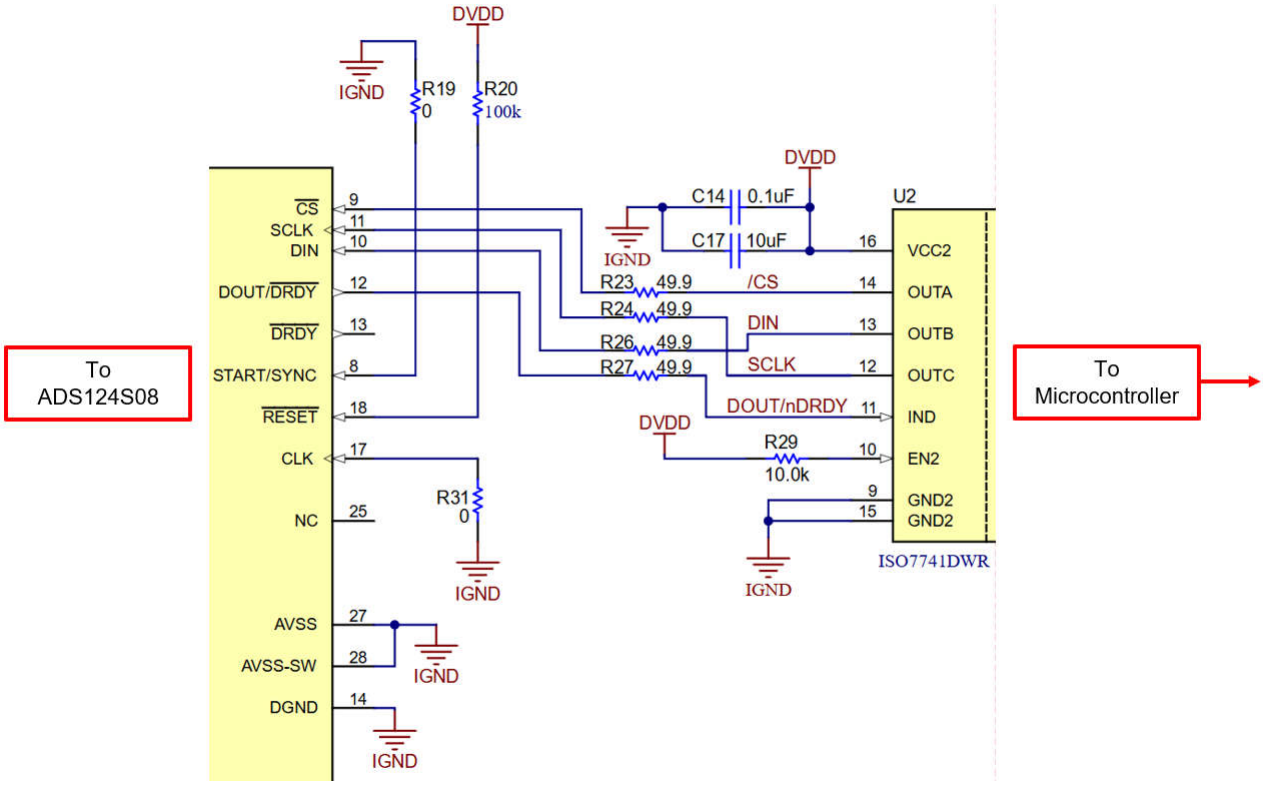


Figure 1-18. Inserting Series Resistors on Digital Signals

1.4.6 Digital Isolation

This EMC test board is designed with ISO7741 digital isolators to isolate data communication. The ISO7741 isolator is reinforced with high immunity, a 5kVrms (DW package) isolation rating per UL 1577, 8kVpk maximum

transient isolation voltage and 6 kVpk maximum surge isolation voltage. This isolator supports signal rates up to 100MSPS with a low propagation delay (10.7ns) and a wide supply range (2.35V to 5.5V).

Figure 1-19 shows the digital isolatation circuit on the EMC test boards:

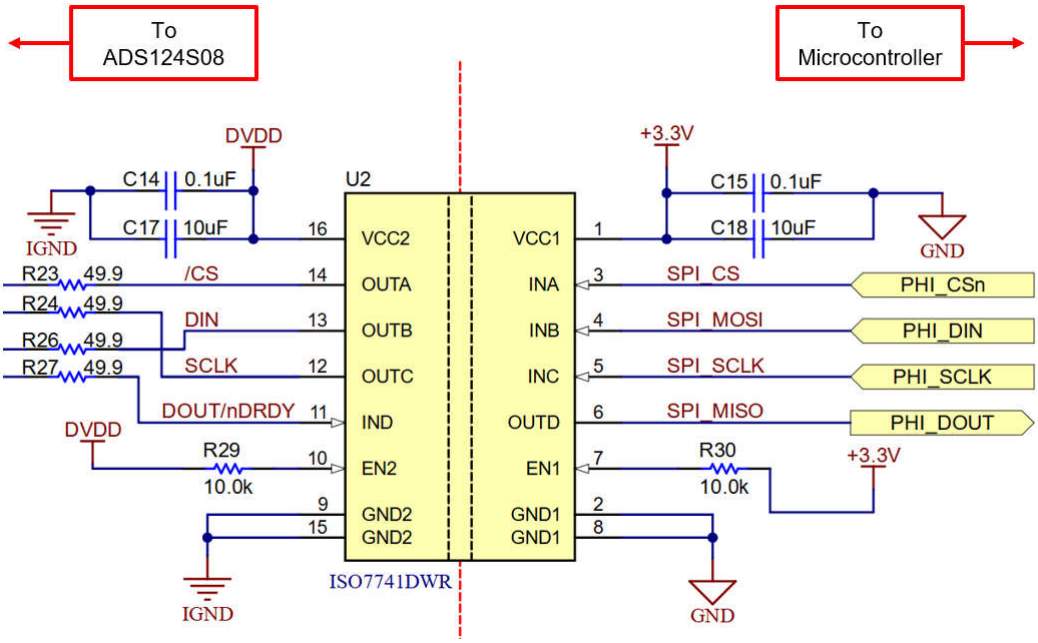


Figure 1-19. Digital Isolation

1.4.7 Power Supply and Protection

The EMC test board power supply circuits are intentionally designed to mimic typical industrial systems. The EMC test boards have an alternative solution powered by two DC power supplies through J3 and J4 to provide the necessary supplies separately on the isolated and non-isolated side of the EMC test boards. By default, only one power supply between +5V and +12V on J3 is required to power the entire circuit board.

Non-isolated side:

TPS7A4700 (U5) is a low-dropout regulator (LDO) that converts an external power supply (6V to 12V) to a steady +5V. This +5V output powers the components on the non-isolated side on the test board, which include a low noise, low EMI push-pull transformer driver, SN6505 (U6). A second TPS7A4700 (U7) regulates +5V to +3.3V for the ISO7741 digital isolators (U2) on the test board.

Isolated side:

TPS7A4700 (U4) regulates the output of the transformer (T1) and generates +3.3V for the ADS124S08 (U1) DVDD supply and the digital isolators (U2). A second TPS7A4700 (U8) generates +5V for the ADS124S08 (U1) AVDD supply on the isolated side of the circuit board. The +3.3V power supply is protected with a 3.3V TVS diode (D9) and the +5V power supply is protected with a TVS diode (D15).

1.5 PCB Layout Consideration for EMC compliance

Designing a PCB board for RTD and thermocouple applications requires special attention to pass EMC testing. These sensors generate low-amplitude, high-impedance signals that are highly susceptible to both radiated and conducted interference. The following layout practices help ensure the PCB design is robust against EMC phenomena while maintaining signal integrity and measurement accuracy:

- PCB Layer Stack-up and Ground Plane
- Avoiding a Long Return Path
- Avoiding 90-degree Bends in PCB Traces
- Using a Guard Ring to Isolate Interference Signals
- Decoupling Capacitors
- Differential Routing
- Stitching Vias
- Layout for Isolation Barrier
- Component Placement

1.5.1 PCB Layer Stack-up and Ground Plane

A continuous and uninterrupted ground plane is fundamental to achieve EMC compliance. An uninterrupted ground plane provides a low impedance return path for signal currents and acts as a shield against external interference.

Additionally, proper PCB layer stack-up is critical for EMC performance and signal integrity. Use a 4-layer PCB stack-up for precise RTD and TC temperature measurements. Place the high-speed and critical signals, such as SCLK of the SPI bus, on the layer that is adjacent to the ground plane, while non-critical signals can be placed near the power plane. Figure 1-20 shows the typical multi-layer circuit board stack-up. Power and ground planes are adjacent to each other as they provide additional interplane capacitance, which helps with high frequency decoupling of the power supply.

A good configuration is:

- Top layer: mixed analog/digital signal routing
- Layer 2 (inner layer): solid ground plane
- Layer 3 (inner layer): power plane with isolated analog and digital sections
- Bottom layer: additional signal routing or shielding if needed.

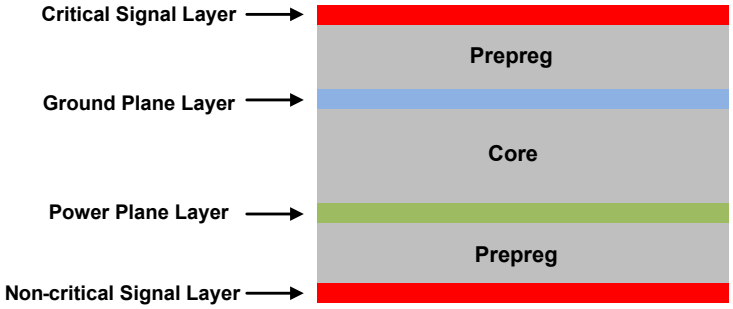


Figure 1-20. Stack-up of 4-layer PCB

A typical 4-layer PCB should have at least one dedicated layer as the ground plane to ensure a low impedance path for the return signals. The stack-up design places a solid ground layer directly adjacent to the signal layers providing consistent return paths and minimizing the loop area and electromagnetic radiation.

2-layer PCBs inherently offer fewer shielding options to dedicate one entire layer as a solid ground plane. Place copper ground pours as large as possible on both top and bottom layers of the PCB with stitching vias. The ground pours will ensure that every signal has a ground return nearby, which will help the design pass EMC testing. All signal traces should be routed on the top layer directly above this ground plane to ensure the return currents follow a short, direct path beneath the signal traces. This configuration provides the best compromise for low-cost boards while still offering acceptable EMC performance.

1.5.2 Avoiding a Long Return Path

A long or disrupted current return path can act as a radiating antenna, increasing susceptibility to EMI and violating EMC requirements. Every signal trace must be routed such that its return current flows directly beneath it through the ground plane. This is especially important for analog sensor signals like those from RTDs and thermocouples, which are extremely sensitive to noise.

1.5.3 Avoiding 90-degree Bends in PCB Traces

Trace geometry can significantly affect signal integrity and emissions. Sharp 90-degree bends in PCB traces should be avoided, as they create impedance discontinuities that may result in signal reflections and increase high frequency radiation. Instead, route traces with two 45-degree bends or smooth arcs when making turns to preserve controlled impedance and minimize emissions. Adhering to such guidance is a good practice for maintaining signal integrity in analog signal routing, while it is more critical in high-speed digital circuits.

Figure 1-21 shows an example for avoiding 90-degree Bends on the EMC test boards.

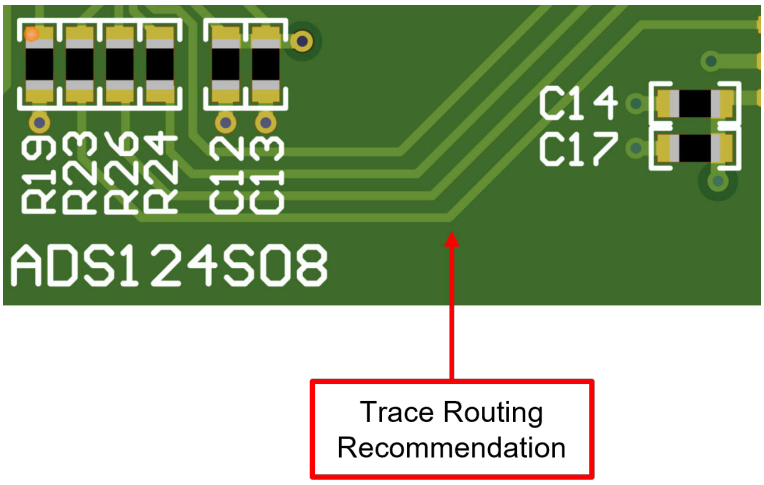


Figure 1-21. Avoiding 90-degree bends in PCB Traces

1.5.4 Using Guard Ring to Isolate Interference Signals

A guard ring is a continuous conductive trace that encircles the perimeter of a PCB or a specific circuit zone. Connecting the guard ring to the system chassis ground or earth ground acts as a Faraday cage on the PCB level, reducing electromagnetic interference signals both emitted from and received by the circuit board. Adding a guard ring is an effective technique for shielding highly sensitive analog signals or ADCs from nearby sources of noise or interference signals. Figure 1-22 shows the side view of the guard ring on a 4-layer circuit board.

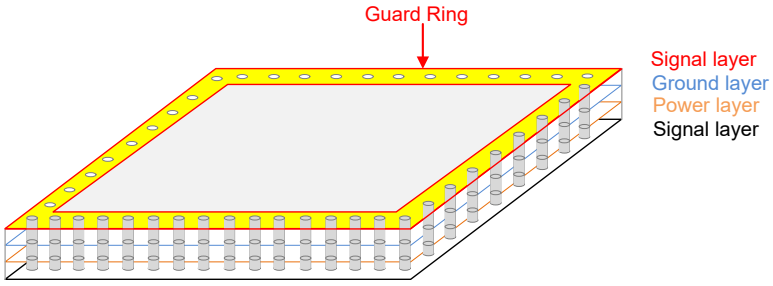


Figure 1-22. Side View of Guard Ring on 4-Layer Circuit Board

The purpose and benefits of using a guard ring include:

- Reducing radiated emissions:

  The guard ring provides a current return path and confines high-frequency signal currents, reducing unintentional radiation from the board edges.

- Improving immunity for electrostatic discharge, fast transients and surge:

  Transient signals can enter a circuit through both air and coupling (direct contact, conduction and electromagnetic fields) and affect the function of the circuit. A grounded guard ring helps dissipate the energy away from sensitive circuitry.

- Acting as a ground reference shield:

  The guard ring on the outer layer of a multi-layer board helps maintain signal integrity and reduce coupling between high-speed and analog sections.

The guidelines to implement a guard ring include:

- Layer placement:

  Place the guard ring on the top and bottom layer on a 2-layer board or on the outer layers of a 4-layer board. Ensure the ring forms a closed loop for maximum effectiveness.

- Hole-to-hole spacing between vias:

  Use vias to tie the guard rings on the top and bottom layer together. Determine the proper hole-to-hole spacing between vias to ensure high shielding effectiveness by following the wavelength limit as a rule of thumb:

  Wavelength (L) > (S/4)

  Where S is the spacing between the vias on the guard ring trace. All signal wavelengths longer than the above limit can be effectively shielded for high effectiveness.

- Trace width of guard ring:

  Determine the appropriate trace width of the guard ring. Wider traces enhance guarding effect but consume more space. As a general rule of thumb, the trace width of the guard ring should be equal to 2~3x width of the protected signal trace. Set the trace width of the guard ring to ~5x width of the protected signal trace for low impedance guarding. This guidance provides a robust shielding for critical high-speed or RF traces.

- Clearance of guard ring:

  The 3W rule specifies a space clearance between signal lines, guard traces, and solid ground planes. Maintain the clearance to reduce crosstalk and coupling by a distance equal to 3x width of a single signal trace.

- Chassis ground tie:

  For enhanced protection, tie the guard ring to chassis ground, protective earth or shield ground to isolate DC ground but still allow high-frequency discharge. This guidance is implemented by high voltage resistors and capacitors on the EMC test boards.

The second layer on 4-layer ADS124S08 EMC test boards is designed as the inner ground (GND and IGND) layer for good decoupling and ground returns. The ADS124S08 EMC test board guard ring is designed on all layers, and the edge guard on these layers are linked together with vias every 100mil to attenuate emissions of high frequency signals up to 472GHz. The 2-layer ADS124S08 EMC test boards have the same guard ring design as the 4-layer EMC test boards. Figure 1-23 shows the guard ring that is designed on the EMC test board:

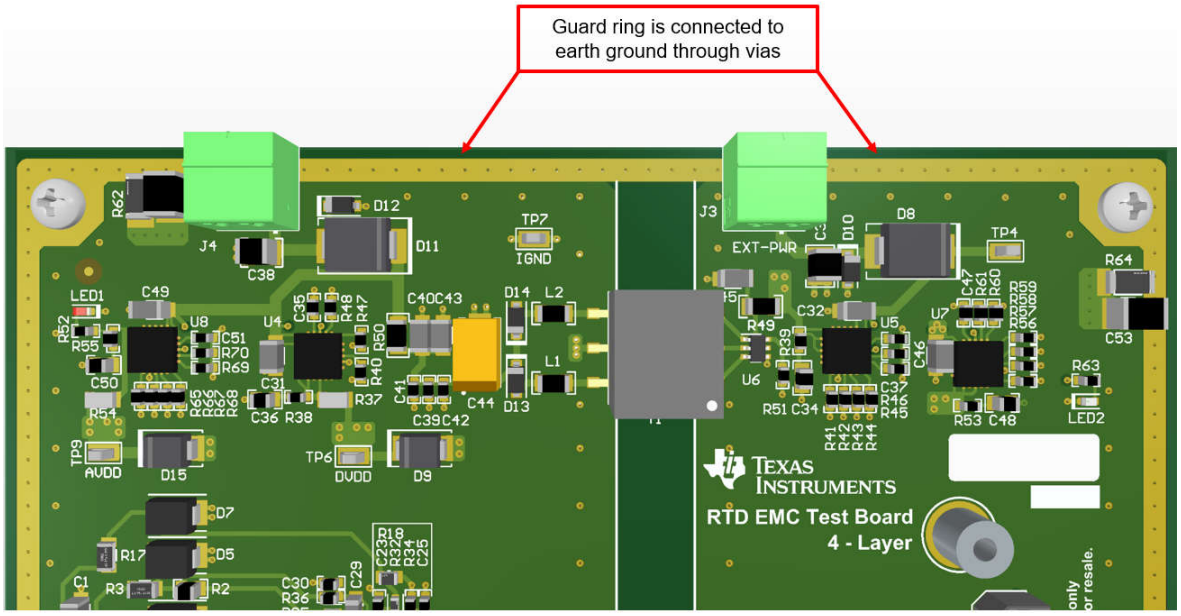


Figure 1-23. Guard Ring on EMC Test Boards

1.5.5 Decoupling Capacitors

Decoupling capacitors are essential for stabilizing power supplies and reducing high-frequency noise. Place a local decoupling capacitor, typically 0.1µF, as close as possible to each power pin with a short and direct return path to the ground plane. Larger bulk capacitors such as 1µF or 10µF can also be placed in parallel to reduce low-frequency power fluctuations. Place the decoupling capacitors between the power supply and the power pin of the device for the best decoupling effect. A power plane is recommended instead of individual traces to reduce inductance and provide better decoupling to the ground plane. Sensitive analog signals such as RTD or thermocouple sensors benefit greatly from clean, locally regulated analog supplies and careful decoupling. The circuit on the left in Figure 1-24 is an appropriate PCB layout example implemented on the EMC test board for decoupling capacitors on AVDD, and the circuit on the right is an inappropriate PCB layout example that is not designed on the EMC test boards.

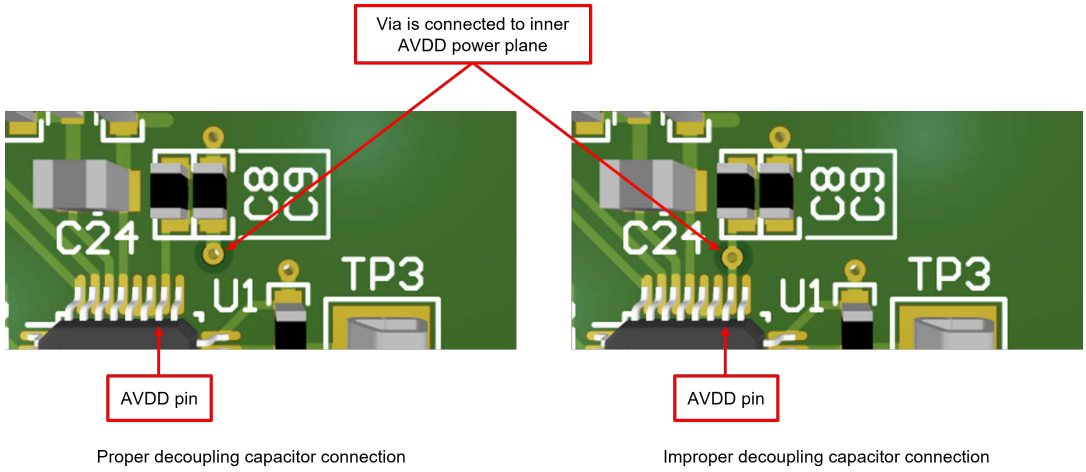


Figure 1-24. Decoupling Capacitor Connection

1.5.6 Differential Signal Routing

RTD or thermocouple signals are differential. The EMC test boards route the traces for each differential pair closely and symmetrically so that any external interference or noise couples equally into both traces. Therefore, the induced noise signal is a common-mode signal that the ADC will reject within the common-mode rejection

ratio (CMRR) specification limits. Avoid placing components and vias between differential traces. Placing components or vias between differential pairs could lead to EMC problems and impedance discontinuities.

Figure 1-25 shows a differential routing example on the EMC test boards:

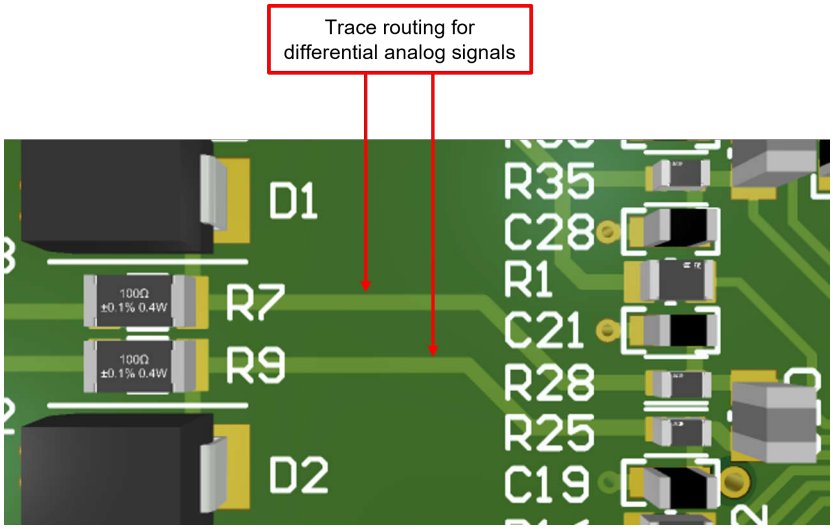


Figure 1-25. Differential Signal Routing

1.5.7 Stitching Vias

Stitching vias can improve signal integrity, reduce impedance and inductance, minimize noise and crosstalk, and also enhance EMI shielding. The EMC test boards employ stitching vias for several different purposes, including:

Enhancing high speed signal integrity and reliability:

The serial clock signal required by many ADCs can be as high as 50MHz. Stitching vias can significantly enhance signal integrity and reliability for high-speed signals by providing a low impedance ground return path, reducing ground ringing and crosstalk. Keep high-speed signals on the same layer as the ADC if possible. Use a single stitching via or stitching via array if a high-speed signal must be routed between different layers. Figure 1-26 shows the side view of a stitching via on a 4-layer circuit board.

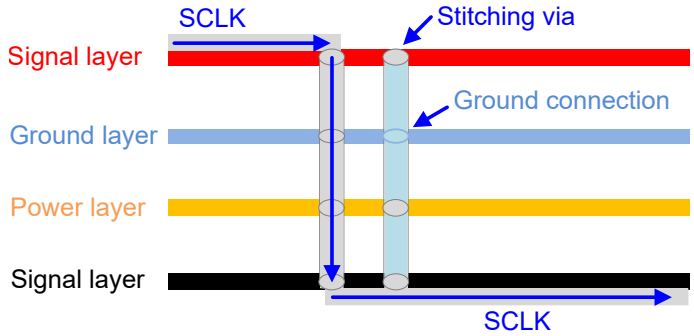


Figure 1-26. Side View of Stitching Via for High-Speed Signal

The EMC test boards route the SCLK trace on the top layer between the ADC and the digital isolator. The SCLK trace then continues from the digital isolator and connector J1 to the controller board on the top layer. Therefore, this design does not require stitching vias for the SCLK signal. Figure 1-27 shows stitching via examples for the DIN and DOUT signals on the RTD EMC test boards.

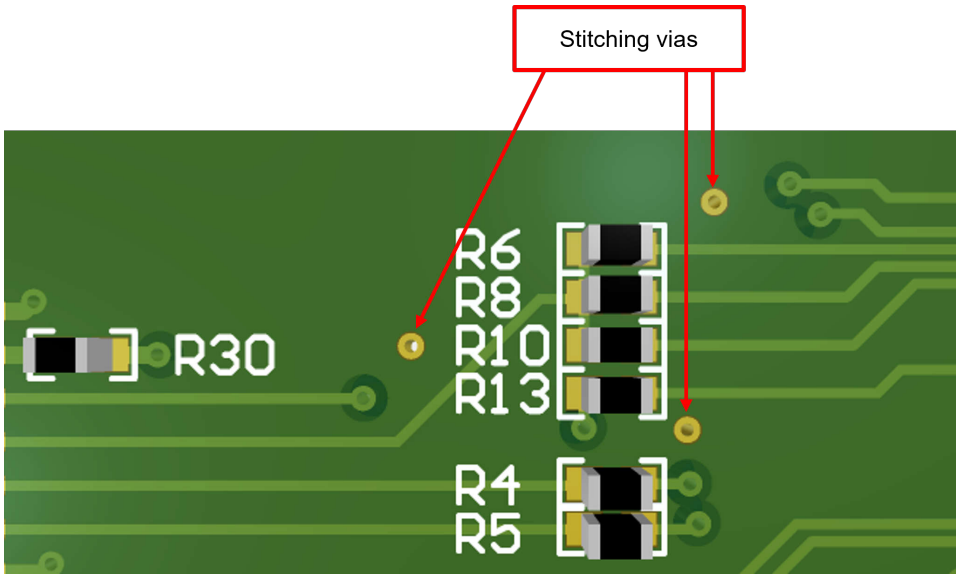


Figure 1-27. Stitching Vias for Signals

Layer transition and ground pour connection:

Use stitching vias transitioning between layers to improve signal integrity by providing a consistent reference plane and a low impedance return path for signals. Stitching vias are also used to connect ground pours across multiple layers and ensure minimum impedance for any return current propagating along the PCB reference plane. Figure 1-28 shows the layer transition and ground connection design example on the 2-layer RTD EMC test board.

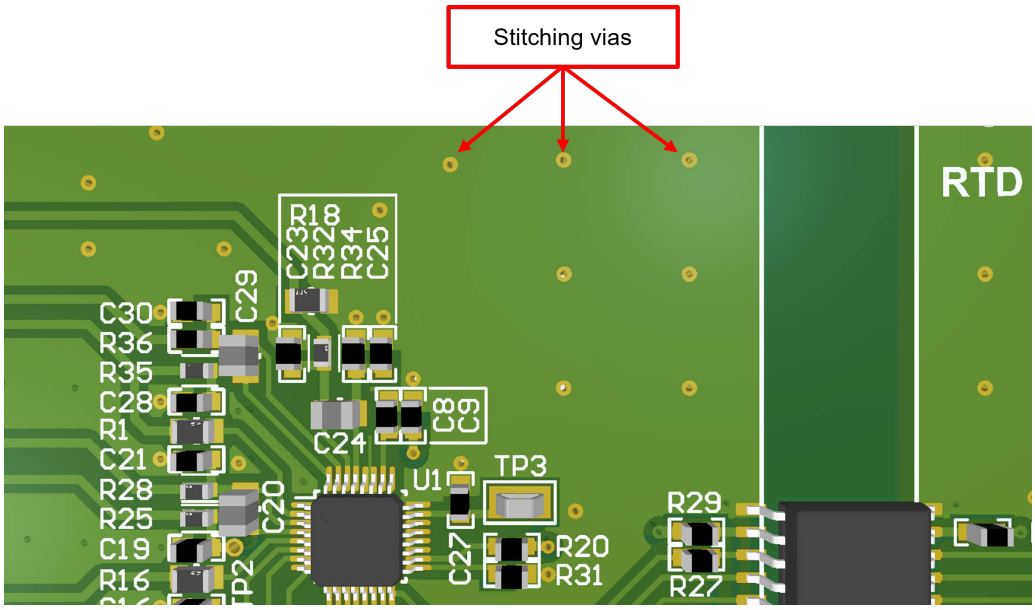


Figure 1-28. Stitching Vias for Layer Transition and Ground Connection

1.5.8 Layout for Isolation Barrier

Two important isolation barrier considerations in high voltage PCB design are clearance and creepage. Keep the space across the isolation barrier as wide as possible to meet the shortest clearance and creepage requirements and prevent electrical failure. Use rounded or smoothed corners at the edge of PCB board to avoid capacitive coupling between pours and electric charge accumulation. This guideline is important for passing high voltage and high frequency signal tests, such as electrical fast transients and radiated immunity test. Figure 1-29 shows

the isolation barrier design between ADS124S08 and the PHI controller card, as well as the PCB corner design on the EMC test boards.

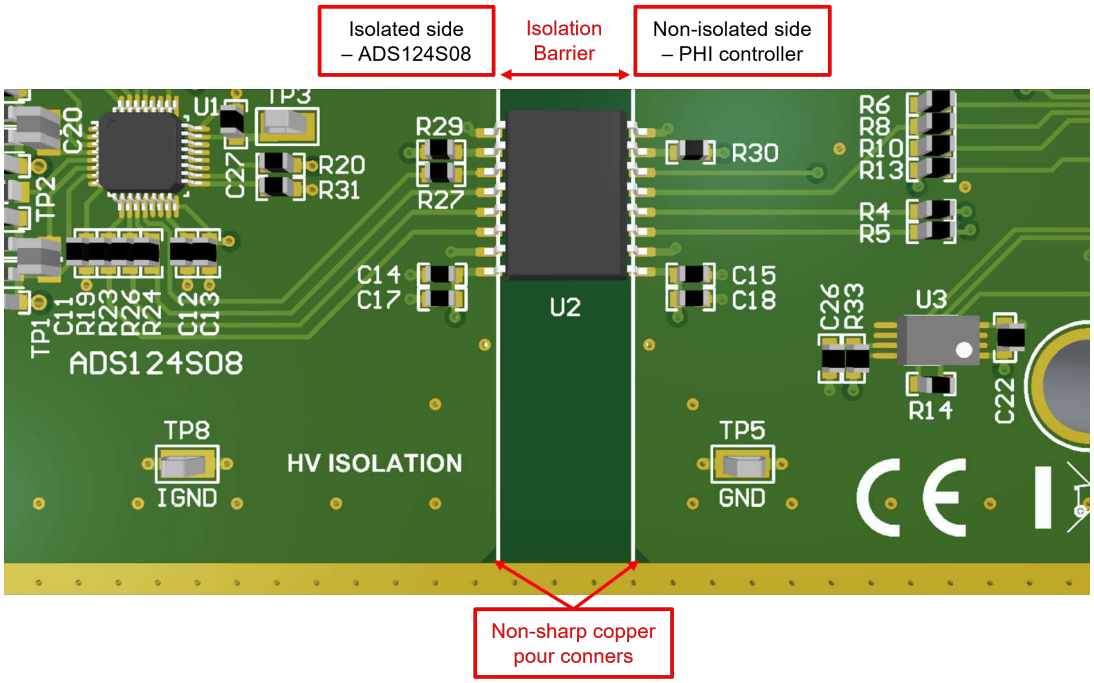


Figure 1-29. Layout for Isolation Barrier

1.5.9 Component Placement

Proper component placement is important for precision signal measurement and electromagnetic compatibility design in mixed-signal circuits. Designers must analyze function blocks, signal paths, and connections to optimize each component's location. For example, place connectors at the PCB edges, place decoupling capacitors close to the power supply and reference pin of the ADC, and place input differential capacitors as close as possible to the ADC. Separating analog and digital components can help minimize interference or noise from the shared return paths, ensuring signal integrity.

1.6 Test System

Figure 1-30 illustrates the general setup of the RTD/TC EMC test board with ADS124S08. A software script configures the system parameters including the SPI interface, clock frequency configuration, ADC mode selection, data capture and analysis, data monitoring, and exporting for post-processing. The software and the PHI controller verify the operation of the test system and the equipment under test (EUT) before the EMC test. The system continuously captures and monitors the data during the EMC event and also checks the EUT functionality after the EMC test.

The PHI controller card provides a communication interface between the ADS124S08 EMC test board and the laptop over a USB 2.0 (or higher) interface for digital input and output. The test system uses a battery powered optical transceiver pair between the laptop and the PHI controller card. The optical transceiver pair isolates harsh transient signals from the test environment and provides an additional layer of protection for the user equipment.

Test Hardware:

- RTD/TC EMC test boards with ADS124S08
- PHI controller card from Texas Instruments
- Optical transceivers with fiber optic cables
- Twisted-pair wire with a precision resistor for RTD or a precision signal for TC measurement
- Specific equipment for individual EMC test
- Laptop running Windows® 10 or 11, 64-bit version
- ZEUS® 6V battery

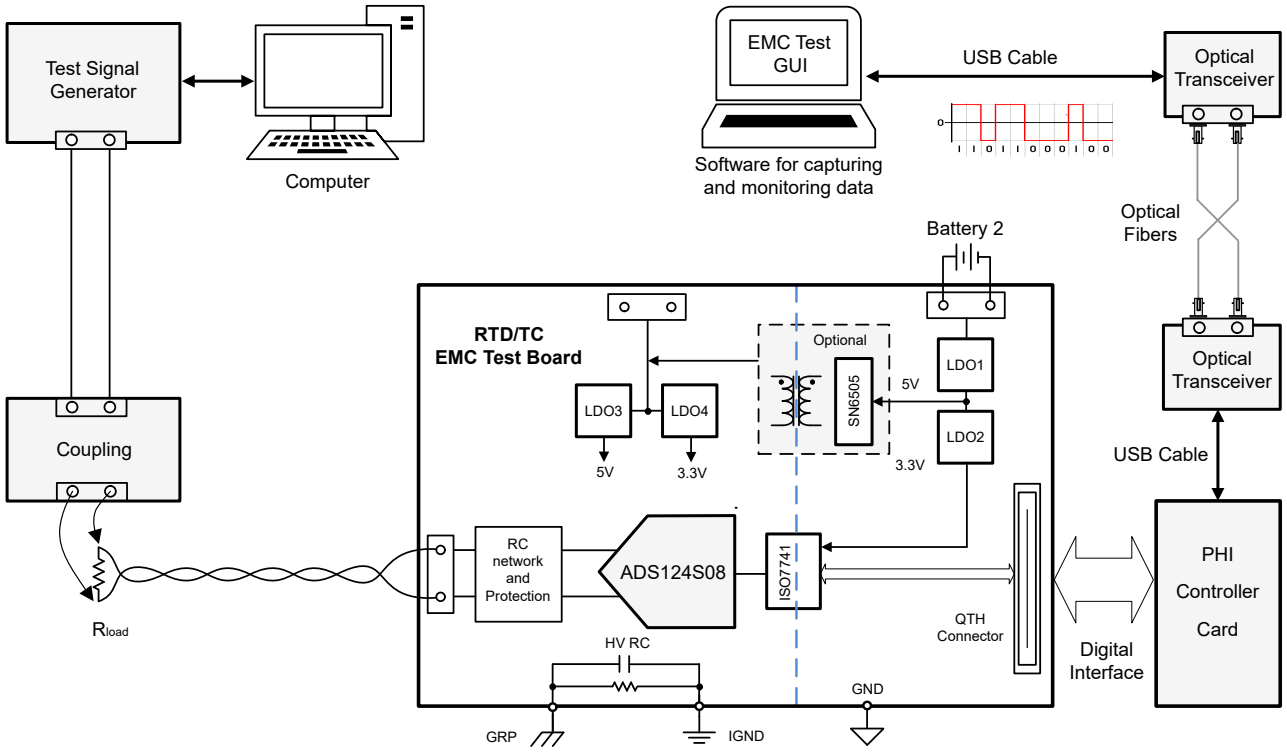


Figure 1-30. General EMC Test Setup

Test Software:

A specialized test graphical user interface (GUI) software is used for EMC testing. The GUI loads a pre-written register configuration file to ADS124S08 on the EMC test boards before each test starts. The GUI continuously monitors the data stream from the EMC test boards to ensure that no information is lost during the testing process after data capture starts.

Figure 1-31 illustrates the scope and functionality of the test GUI within the EMC testing environment.

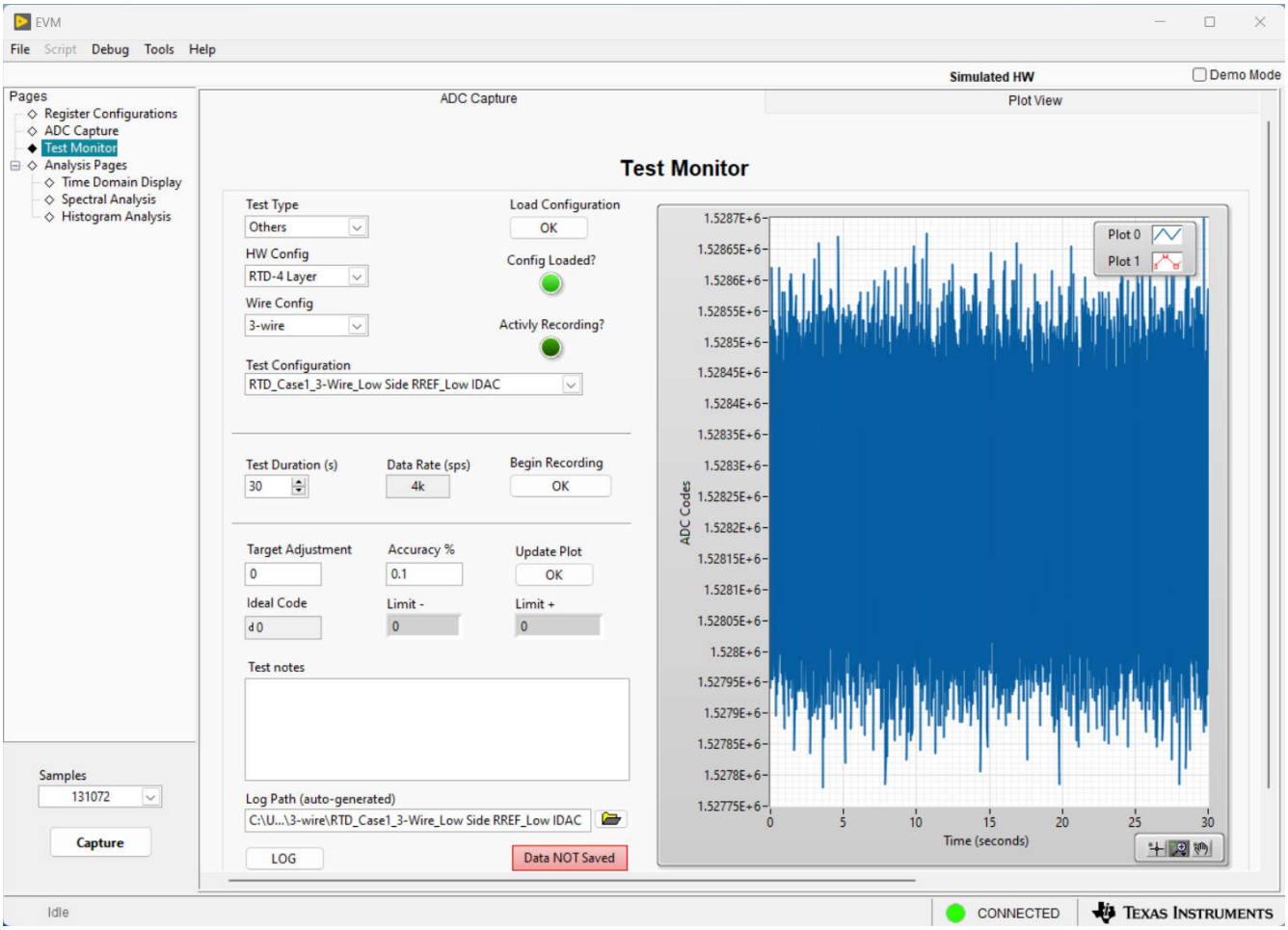


Figure 1-31. GUI Software for EMC testing

2 Test Details and Results

This section covers test standard and criteria, test setup and result for each test.

2.1 Standards and Test Criteria

The ADS124S08 EMC test boards are designed to meet EMC and EMI test standards and criteria for industrial applications. The following five tests are selected for the test:

- IEC 61000-4-2: Electrostatic Discharge (ESD)
- IEC 61000-4-3: Radiated Immunity (RI)
- IEC 61000-4-4: Electrical Fast Transients (EFT)
- IEC 61000-4-5: Surge Immunity (SI)
- IEC 61000-4-6: Conducted Immunity (CI)

Test Criteria

EMC test criteria define the limits and conditions under which an electronic device is tested to ensure it functions properly in its intended environment without causing or being affected by interferences. Table 2-1 shows the test criteria that are essential for product reliability and compliance with regulatory standards. Defining EMC test criteria involves specifying the types of tests (emissions and immunity), the test methods (radiated and conducted), the frequency ranges, and the acceptable performance levels.

Table 2-1. Test Criteria

Criteria	Description
A	Normal performance within specified limits
B	Temporary performance loss which can recover after disturbance ends
C	Temporary function or performance loss which can recover with user's intervention
D	Permanent function or performance loss due to damage or loss of data

2.2 Electrostatic Discharge (ESD)

The IEC 61000-4-2 standard specifies the details for the ESD test including the test criteria and setup requirements. The IEC 61000-4-2 test determines the EUT immunity to external ESD events during operation. Figure 2-1 shows a diagram of the setup and connection for the ESD test. A 0.8m high wood table stands on the GRP. A 1.6m × 0.8m horizontal coupling plane (HCP) is placed on the table. The EUT is tested and isolated on a 0.5mm thick insulating mat that is placed on top of the HCP. The EUT is placed on the insulating mat 0.1m away from a 0.5m × 0.5m vertical coupling plane (VCP).

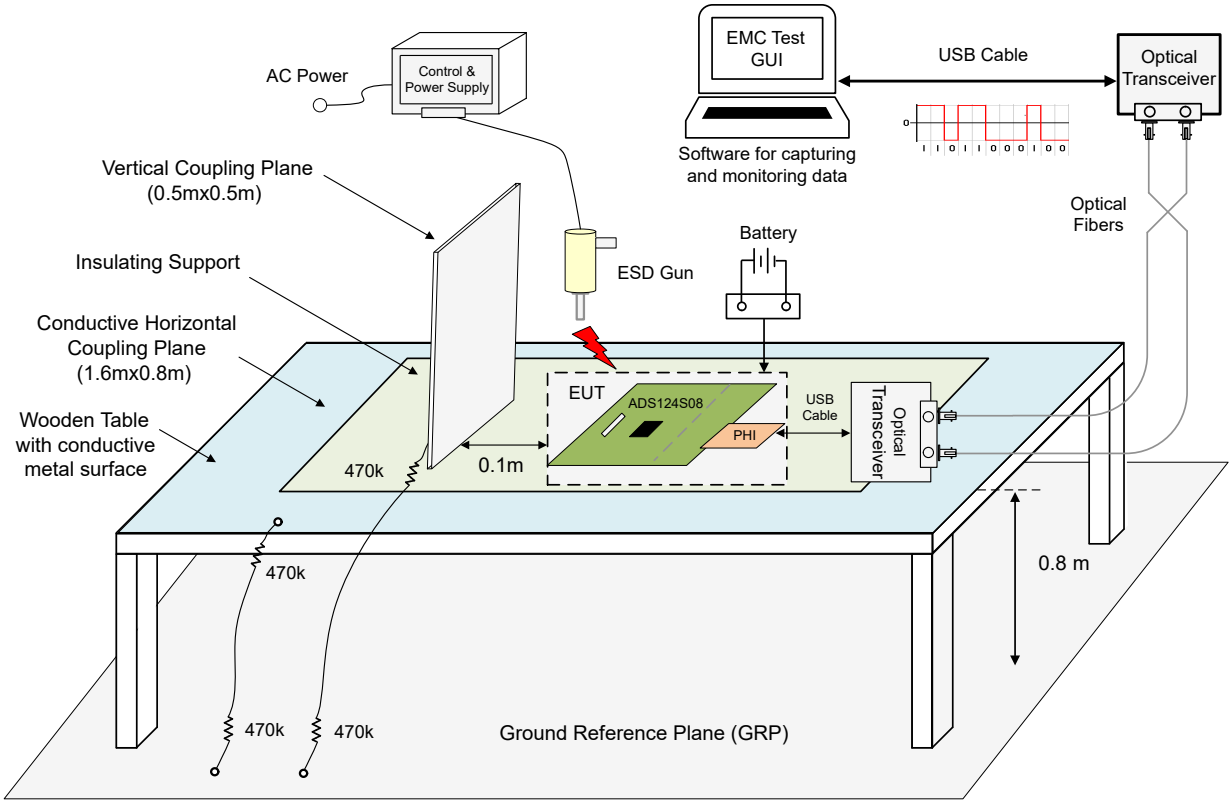


Figure 2-1. Diagram of Laboratory Setup for ESD Test

There are two types of ESD tests: contact discharge and air discharge. The contact discharge test is the most aggressive direct discharge test where the tip of the ESD gun directly contacts conductive screws of the input terminal block (J2) on the ADS124S08 RTD EMC test boards and the input terminal blocks (J2/J3/J4/J5) the ADS124S08 TC EMC test boards. Air discharge tests are executed three different ways: direct air gap discharge, indirect discharge to the horizontal coupling plane (HCP), and indirect discharge to the vertical coupling plane (VCP). The air gap discharge test places the tip of the ESD gun near the insulating surfaces of the input terminal blockd on the ADS124S08 EMC test boards. The indirect discharge tests applies the ESD signal into the HCP or VCP, which represents an ESD strike onto the equipment rack where the design is mounted.

Figure 2-2 shows a zoomed-in view where the ESD strikes are applied. The discharges to the HCP and the VCP are individually done with ESD gun 1 and ESD gun 2 in the contact discharge mode. The ESD gun is held perpendicular to the VCP edge, then the ESD strikes are discharged into the edge of the plane.

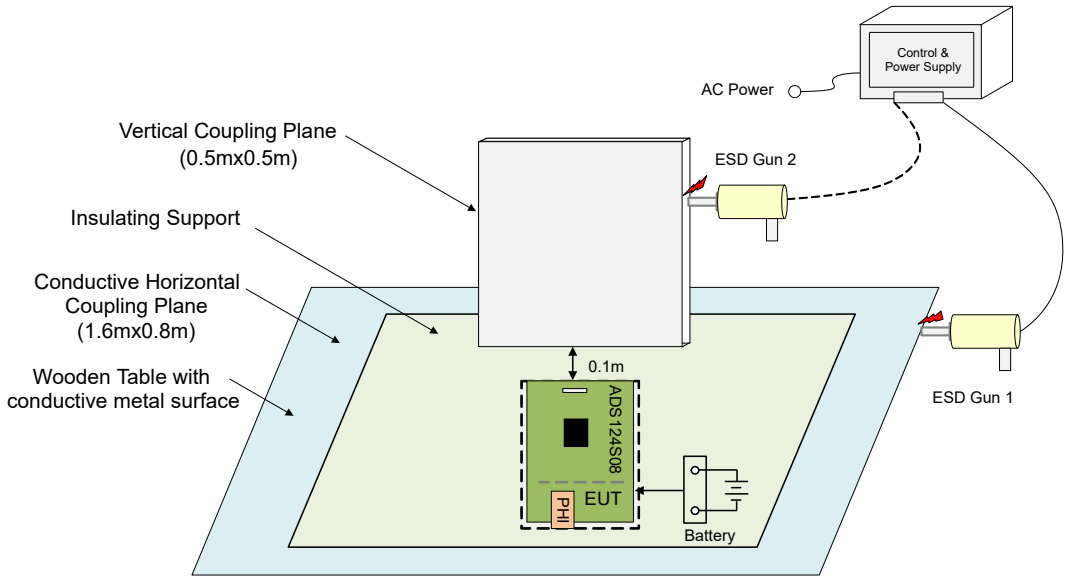


Figure 2-2. Discharges to the HCP and VCP with the ESD Gun 1 and Gun 2

Table 2-2 specifies the IEC 61000-4-2 test levels:

Table 2-2. : Test Level of ESD Test

Contact Discharge		Air Discharge	
Level	**Test Voltage (kV)**	**Level**	**Test Voltage (kV)**
1	2	1	2
2	4	2	4
3	6	3	8
4	8	4	15
x	Special	x	Special

Figure 2-3 shows a photograph of the actual setup for the ESD test on the ADS124S08 EMC test board.

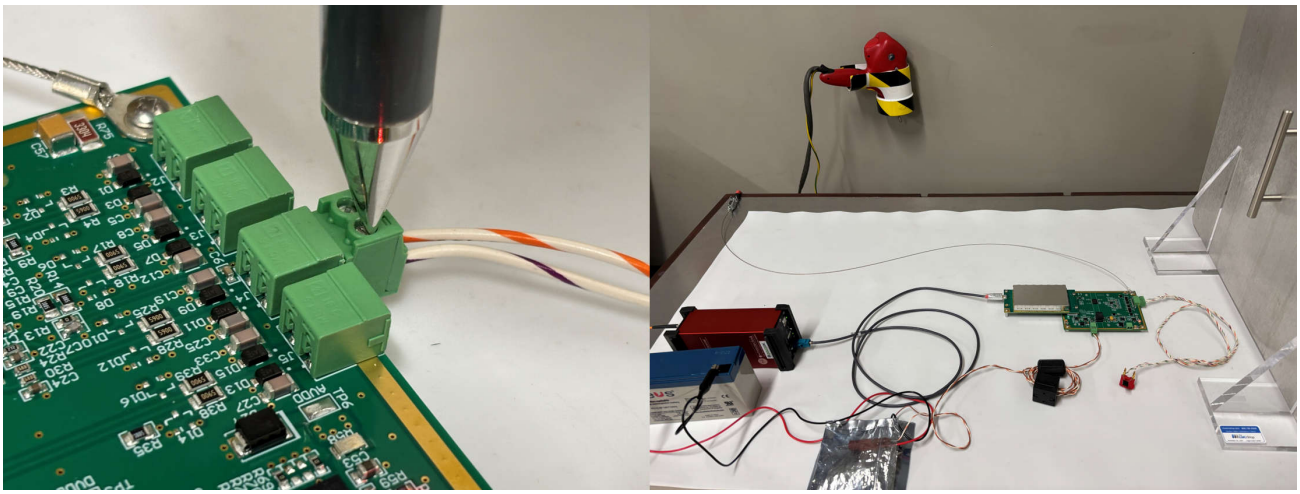


Figure 2-3. Laboratory Setup for ESD Test

Figure 2-4 shows the uncalibrated ADS124S08 output temperature data using the 2-layer TC EMC test board for the ESD test. The test board was configured to measure a thermocouple using the internal VBIAS voltage to bias the sensor. The graph on the left side in the figure shows the ADC conversion code when the positive ESD

discharges are applied to the input channel. The graph on the right side shows the ADC conversion code when the negative ESD discharges are applied to the input channel. Both graphs show that the ESD test affected the ADS124S08 and led to temporary performance loss. However, the device automatically recovered without any user intervention. Therefore, the ADS124S08 EMC test board passed the ESD test with criteria B.

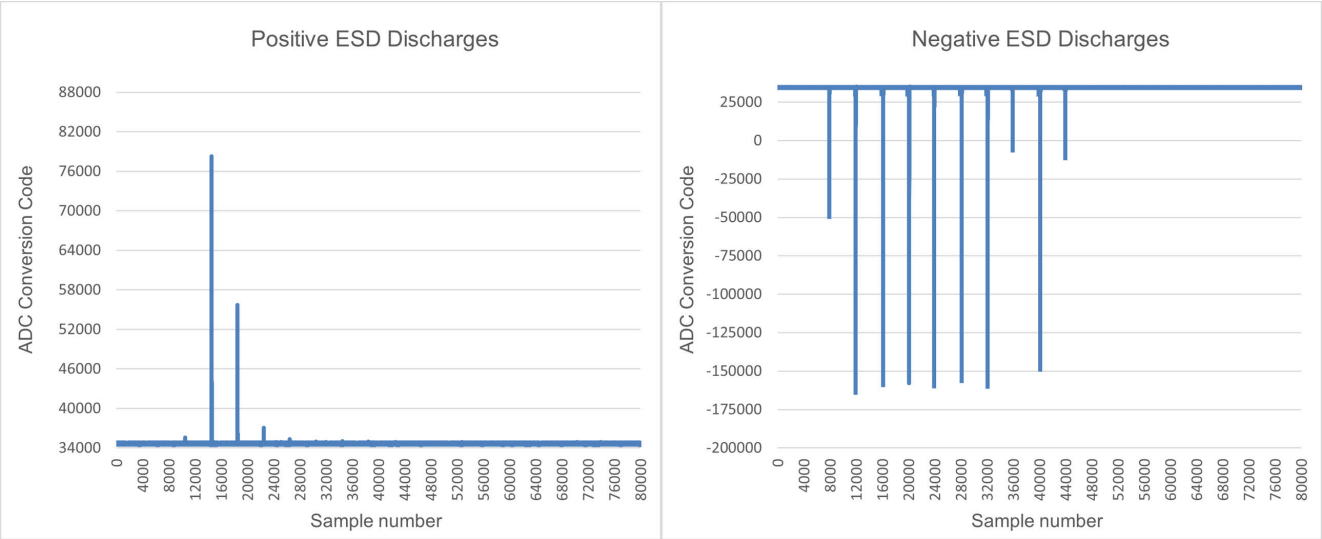


Figure 2-4. ADC Conversion Code Captured for ESD Test

Table 2-3 shows the results of the ESD test. The test result is the same for every configuration on all RTD and TC EMC test boards.

Table 2-3. Test Result of ESD Test

Test	IEC Standard	Configuration	Test Signal			Criterion	Test Result
			Test Type	Test Level	Test Voltage		
ESD	IEC 61000-4-2	RTD: 4-Layer, 3-Wire, Low-side R_{REF}	Contact Discharge	4	+8kV	B	Pass
					-8kV	B	Pass
			Air Discharge	4	+15kV	B	Pass
					-15kV	B	Pass
		RTD: 2-Layer, 3-Wire, High-side R_{REF}	Contact Discharge	4	+8kV	B	Pass
					-8kV	B	Pass
			Air Discharge	4	+15kV	B	Pass
					-15kV	B	Pass
		TC: 2-Layer, VBIAS for sensor biasing	Contact Discharge	4	+8kV	B	Pass
					-8kV	B	Pass
			Air Discharge	4	+15kV	B	Pass
					-15kV	B	Pass
		TC: 2-Layer, REFOUT Biasing Pullup Resistor	Contact Discharge	4	+8kV	B	Pass
					-8kV	B	Pass
			Air Discharge	4	+15kV	B	Pass
					-15kV	B	Pass

2.3 Radiated Immunity (RI)

The IEC 61000-4-3 standard specifies the details for the RI test including test criteria and setup requirements. The IEC61000-4-3 test determines the EUT immunity to external electromagnetic radiation during operation. The test is performed in an anechoic chamber and the EUT is placed on a nonconductive table that is 0.8m tall. The test distance between the EUT and the antenna is 3m. The EUT is exposed to both horizontal and vertical field polarities at each rating. The RF test signal is swept from 80MHz to 1GHz, and from 1GHz to 2.7GHz with a disturbance signal of 80% amplitude modulated with a 1kHz sinusoidal signal. The field strength is 10V/m and 18 V/m for each frequency range. The conversion data is captured from the EUT by the PHI controller card and sent to the laptop running the software script outside the chamber through the fully isolated optical fiber cables.

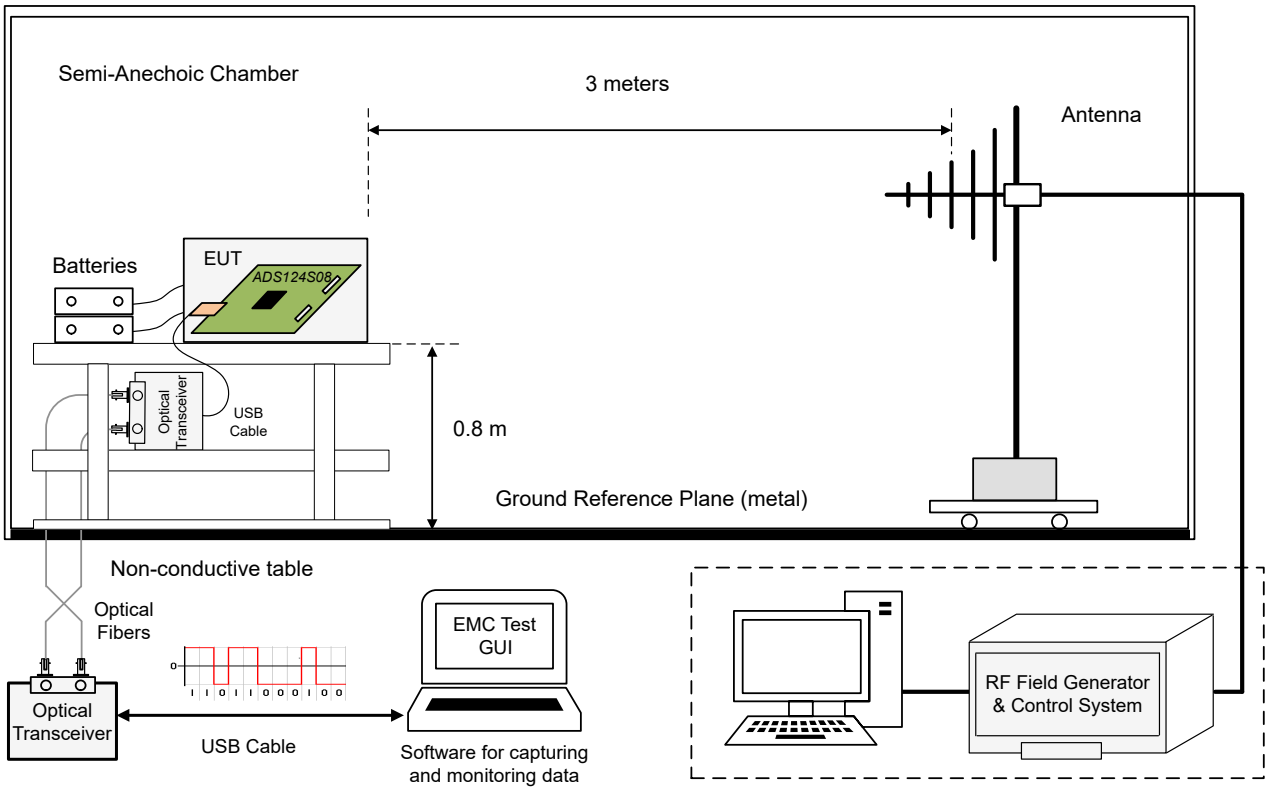


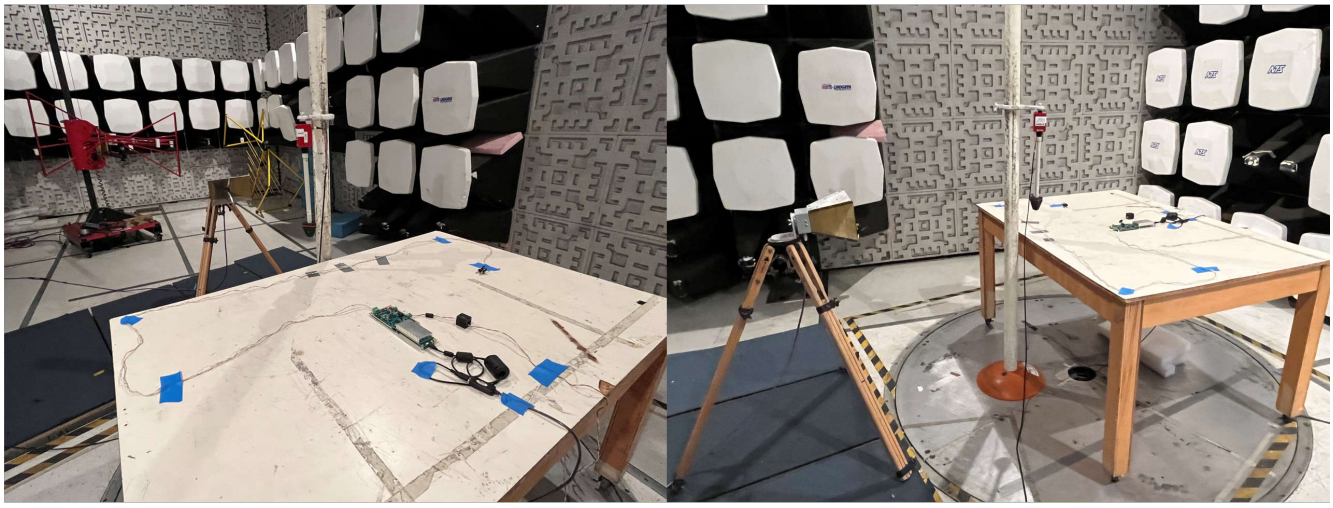
Figure 2-5. Diagram of Laboratory Setup for Radiated Immunity Test

Table 2-4 specifies the IEC 61000-4-3 test levels:

Table 2-4. Test Level of Radiated Immunity Test

Level	Field Strength of Test Signal (V/m)
1	1
2	3
3	10
4	30
x	This is an open test level, and the associated field strength can be any value. This level can be specified in product standard.

Figure 2-6 shows the actual setup for the radiated immunity test on the ADS124S08 EMC test board.



RF Immunity Test: 80 – 1000MHz RF Immunity Test: 1 - 2.7GHz

Figure 2-6. Laboratory Setup for Radiated Immunity Test

Figure 2-7 shows the uncalibrated ADS124S08 output temperature data using the 4-layer RTD EMC test board during and after the radiated immunity test. The test board was configured to measure a 3-wire RTD using a low-side voltage reference for these tests. The graph on the left side shows the captured temperature data from the ADC during the radiated immunity test when the test signal frequency sweeps from 80MHz to 1GHz. The graph in the middle shows the captured temperature data from the ADC when the test signal frequency sweeps from 1GHz to 2.7GHz. The graph on the right side shows the captured temperature data from the ADC when the radiated immunity test completes. As shown in the graphs, the ADS124S08 was not affected by the test signals. Therefore, the ADS124S08 EMC test board passed the radiated immunity test with criteria A.

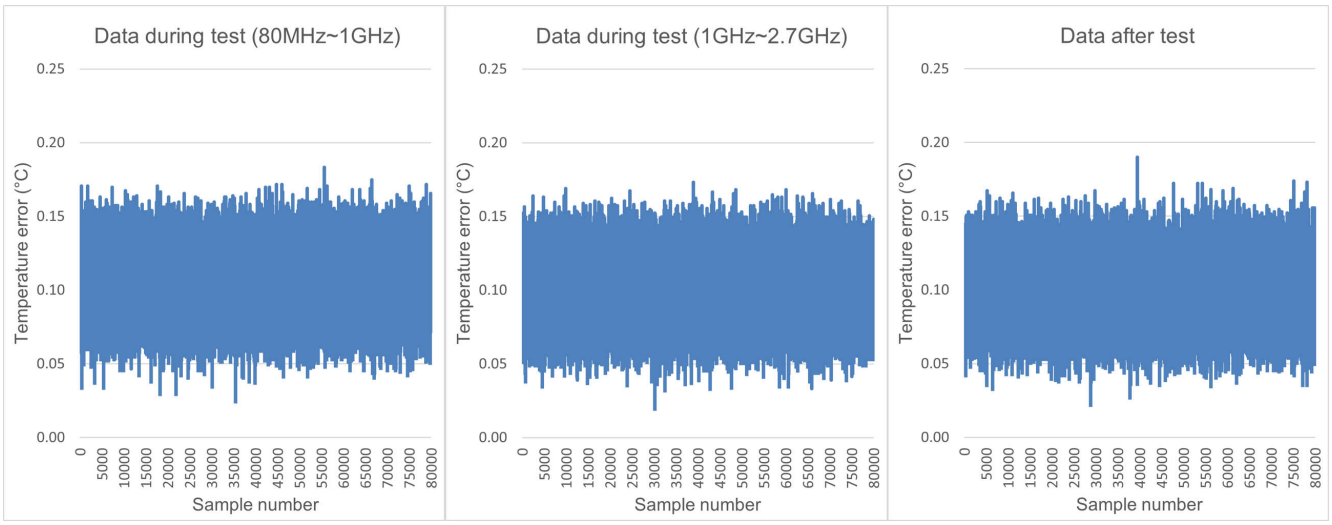


Figure 2-7. Temperature Data Captured for Radiated Immunity Test

Table 2-5 shows the results of the RI test. The test result is the same for every configuration on all RTD and TC EMC test boards.

Table 2-5. Test Result of Radiated Immunity Test

Test	IEC Standard	Configuration	Test Signal			Criterion	Test Result
			Field Strength	Frequency	Antenna Polarization		
Radiated Immunity (RI)	IEC 61000-4-3	RTD: 4-Layer, 3-Wire, Low R_{REF}	10V/m (Level 3)	80kHz -1GHz	Horizontal	A	Pass
					Vertical	A	Pass
				1GHz -2.7GHz	Horizontal	A	Pass
					Vertical	A	Pass
		RTD: 2-Layer, 3-Wire, High-side R_{REF}	10V/m (Level 3)	80kHz -1GHz	Horizontal	A	Pass
					Vertical	A	Pass
				1GHz -2.7GHz	Horizontal	A	Pass
					Vertical	A	Pass
		TC: 2-Layer, REFOUT Biasing Pullup Resistor	10V/m (Level 3)	150kHz -80MHz	Horizontal	A	Pass
					Vertical	A	Pass
				1GHz -2.7GHz	Horizontal	A	Pass
					Vertical	A	Pass

2.4 Electrical Fast Transients (EFT)

The IEC 61000-4-4 standard specifies the details for the EFT test including test criteria and setup requirements. The IEC61000-4-4 test determines EUT immunity to an external burst of transient signals with short duration and fast rise time during operation. The standard defines four test voltage levels with two repetition frequencies for signal and control ports: 0.25kV, 0.5kV, 1kV and 2kV at 5kHz and 100kHz repetition frequency. Each test also requires positive and negative polarity discharge. The ADS124S08 EMC test boards were tested at the standard 1kV and 2kV levels, as well as a more extreme 4kV level. The ADS124S08 EMC test boards were tested at both 5kHz and 100kHz frequencies. The EFT transient burst consists of 75 fast pulses followed by a break interval. One pulse occurs every 15ms for 5kHz and 0.75ms for 100 kHz, with bursts repeated every 300ms. Each individual burst pulse is a double exponential waveform with a rise time of 5ns and a total pulse duration of 50ns. The total test time for each test is approximately one minute.

Figure 2-8 shows a setup and connection diagram for the EFT immunity test. In this setup, the EFT signal is applied to the analog input of the ADS124S08 EMC test boards by running 2m of twisted pair input wires through a 1m length standard capacitive EFT clamp. All the cables in the test are placed on insulation support materials to keep them isolated from the GRP. The EUT is placed on top of the GRP and isolated from the GRP by a 0.1m insulated platform.

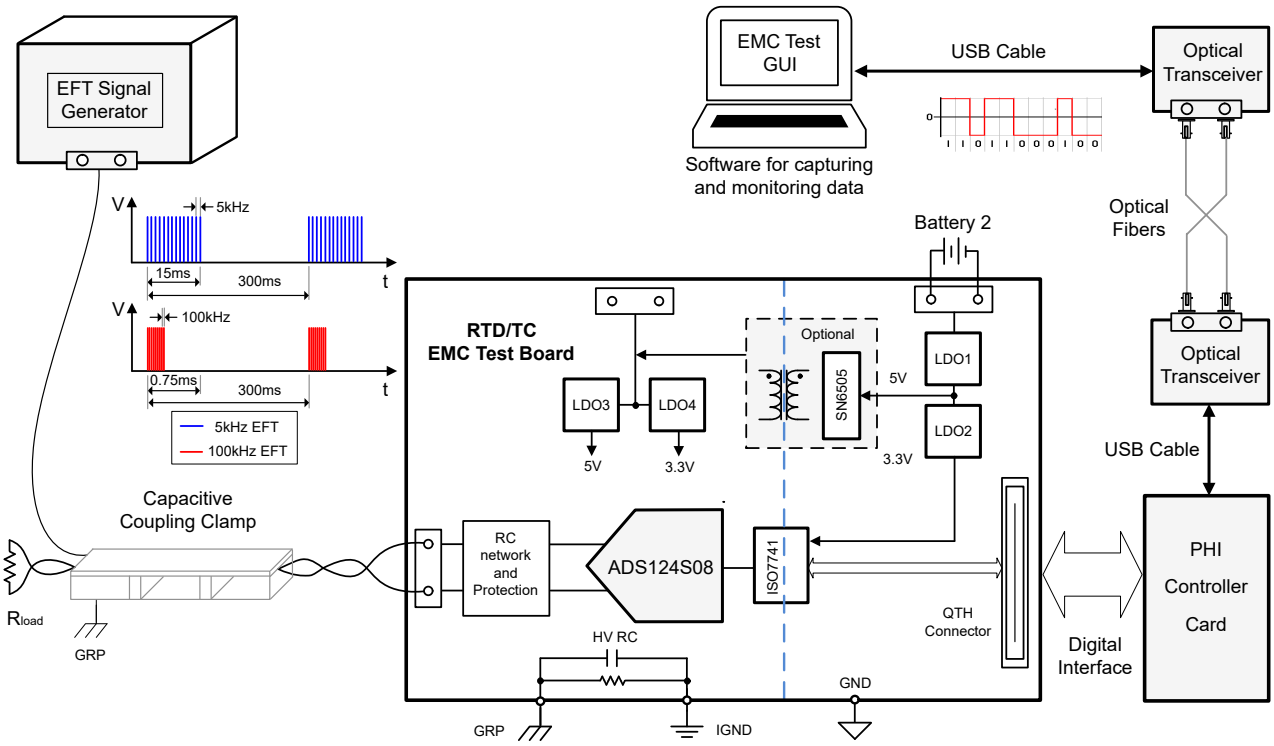


Figure 2-8. Diagram of Laboratory Setup for EFT Test

Table 2-6 specifies the IEC 61000-4-4 test levels:

Table 2-6. Test Level of EFT Test

Level	On Power Supply Port			On I/O, Signal, Data, and Control Lines		
	Open-Circuit Voltage (kV)	Short-Circuit Current (A)	Repetition Rate (kHz)	Open-Circuit Voltage (kV)	Short-Circuit Current (A)	Repetition Rate (kHz)
1	0.5	10	5 or 100	0.25	5	5 or 100
2	1	20	5 or 100	0.5	10	5 or 100
3	2	40	5 or 100	1	20	5 or 100
4	4	80	5 or 100	2	40	5 or 100
x	This is an open test level, and the test level can be any value. This level can be specified in product standard.					

Figure 2-9 shows the actual setup for the EFT test on the ADS124S08 EMC test board.

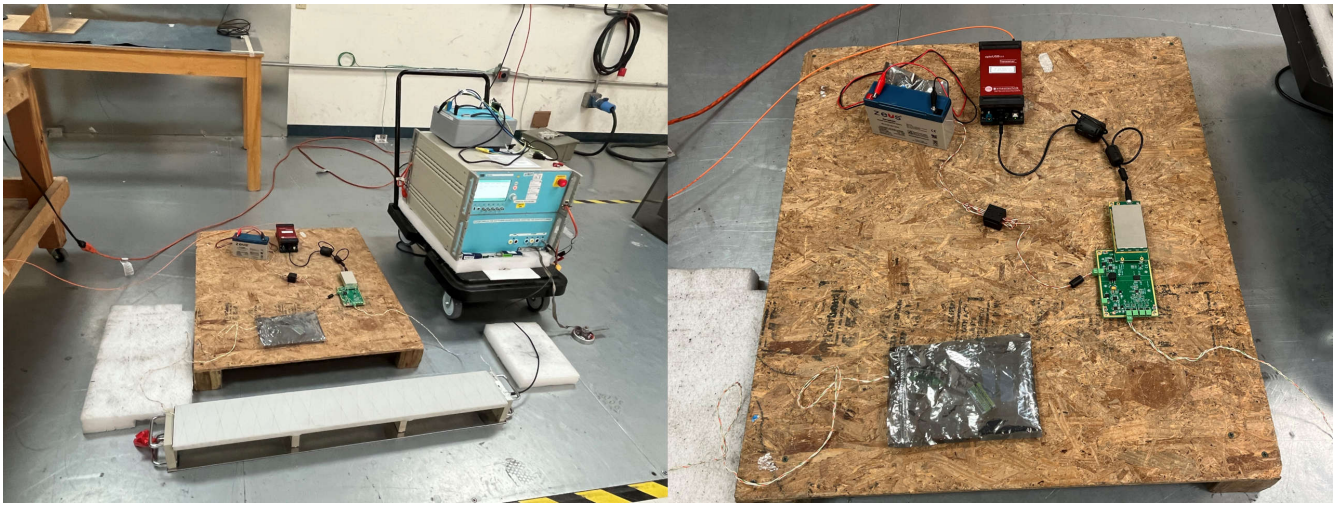


Figure 2-9. Laboratory Setup for EFT Test

Figure 2-10 shows the uncalibrated ADS124S08 output temperature data using the 2-layer TC EMC test board before, during and after the EFT test. The EFT test signal is coupled into the channel that uses the internal VBIAS voltage to bias the sensor. The graph on the left side shows the captured temperature data from the ADC just before and then during the EFT test. The graph on the right shows the captured temperature data from the ADC during and then after the EFT test completes. Both graphs show that the EFT test affected the ADS124S08 and led to temporary performance loss. However, the device automatically recovered without any user intervention. Therefore, the ADS124S08 EMC test board passed the EFT test with criteria B.

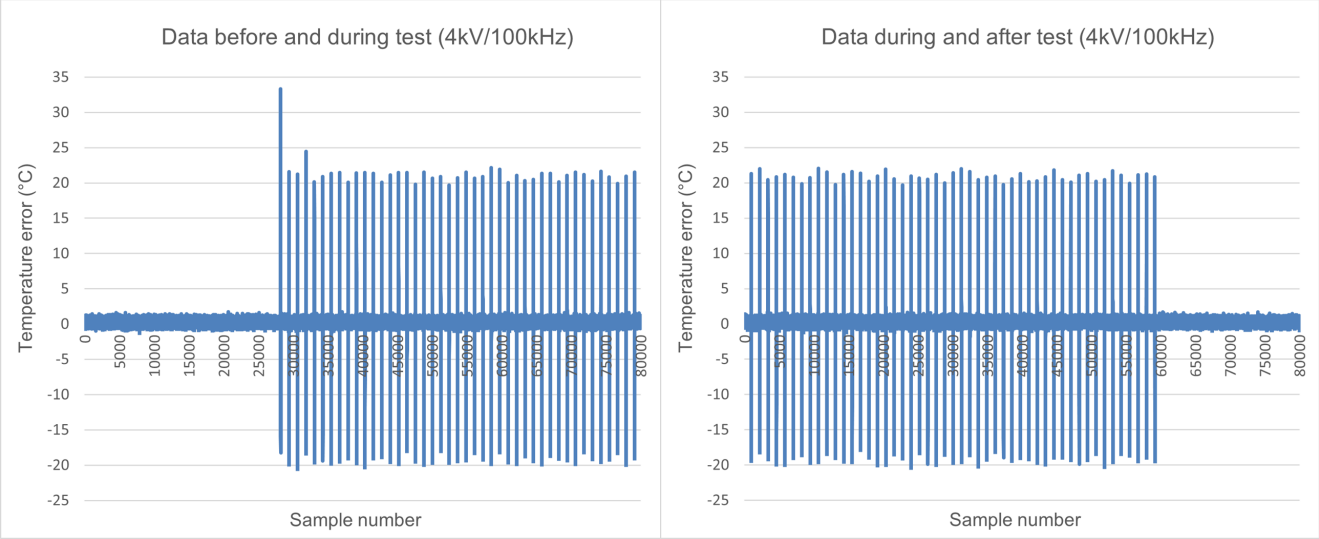


Figure 2-10. Temperature Data Captured for EFT Test

Table 2-7 shows the results of the EFT test. The test result is the same for every configuration on all RTD and TC EMC test boards.

Table 2-7. Test Result of EFT Test

Test	IEC Standard	Configuration	Test Signal		Test Level	Criterion	Test Result
			Voltage	Frequency			
EFT	IEC 61000-4-4	RTD: 4-Layer, 3-Wire, Low-side R_{REF}	±4kV	5kHz	4	B	Pass
			±4kV	100kHz	4	B	Pass
		RTD:2-Layer, 3-Wire, High-side R_{REF}	±4kV	5kHz	4	B	Pass
			±4kV	100kHz	4	B	Pass
		TC:2-Layer, VBIAS for sensor biasing	±4kV	5kHz	4	B	Pass
			±4kV	100kHz	4	B	Pass
		TC: 2-Layer, REFOUT Biasing Pullup Resistor	±4kV	5kHz	4	B	Pass
			±4kV	100kHz	4	B	Pass

2.5 Surge Immunity (SI)

The IEC 61000-4-5 standard specifies the details for the SI test including test criteria and setup requirements. The setup includes the test equipment and procedures for performing surge testing at a specific source impedance and coupling mode (line-to-line or line-to-ground). The IEC61000-4-5 test determines the EUT immunity to external high energy surges on both power and data lines. These energy surges can be caused by power system switching, load changes and short circuit faults, or direct or indirect lighting strikes. The IEC 61000-4-5 specifies two types of combination wave generators (CWGs). The 10µs / 700µs CWG is specifically used to test the ports of symmetrical telecommunication lines. The 1.2µs / 50µs CWG is used for all other cases. The surge for all other cases combines a 1.2µs / 50µs (1.2µs rising time with 50µs pulse width) open-circuit voltage waveform and 8µs / 20µs (8µs rising time with 20µs pulse width) short-circuit current waveform. The EUT is subject to 2 positive and 2 negative surges at each rating. The surge is repeated at least once per minute. A coupling/decoupling network (CDN) is required by the surge test. The IEC 61000-4-5 defines the impedance and capacitance used in the coupling network in different cases. The EUT is tested with the surge through a CDN with a 0.5µF capacitor and a twisted cable.

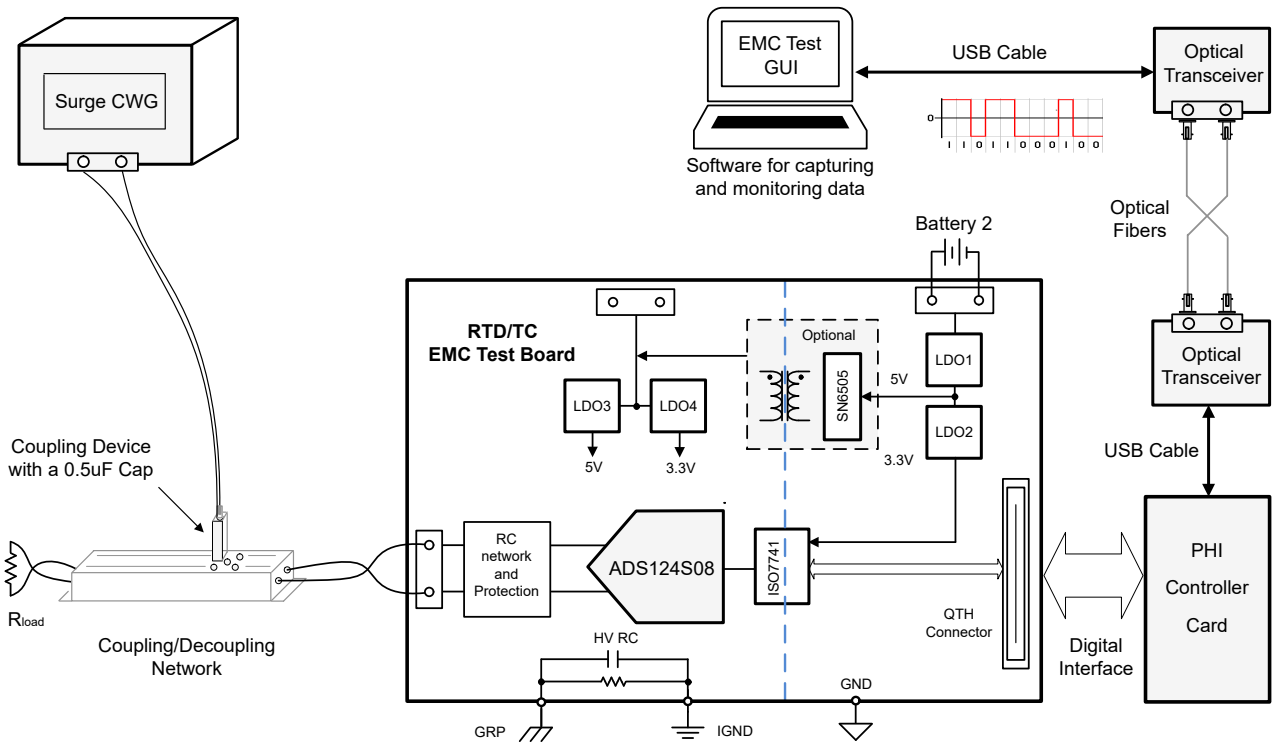


Figure 2-11. Diagram of Laboratory Setup for Surge Test

Table 2-8 specifies the IEC 61000-4-5 test levels:

Table 2-8. Test Level of Surge Test

Level	Open-circuit Test Voltage ±10% (kV)
1	0.5
2	1.0
3	2.0
4	4.0
X	Special for any level, above, below or between the other levels. This level can be specified in product standard.

The surge generator uses a 2Ω output impedance to model the source impedance of a low voltage power supply and the inherent source impedance of the waveform generator. An additional series resistance may be needed between the EUT and the surge generator based on the power and data line test requirements. The surge current is determined by the level of surge voltage and the total impedance (Req), where Req is the combination

of the surge generator output impedance and the additional series resistance. The selection of the impedance depends on the equipment type and test requirements.

Table 2-9 shows a reference matrix of the surge current levels for different surge voltages and impedances:

Table 2-9. Current Levels of Surge Test Voltage and Impedance

	Level 1	Level 2	Level 3	Level 4
	500V	1 kV	2 kV	4 kV
Req = 42 Ω	12 A	24A	48 A	96 A
Req = 12 Ω	42 A	84 A	167 A	334 A
Req = 2 Ω	250 A	500 A	1000 A	2000 A

Figure 2-12 shows the actual setup for the surge test on the ADS124S08 EMC test board.

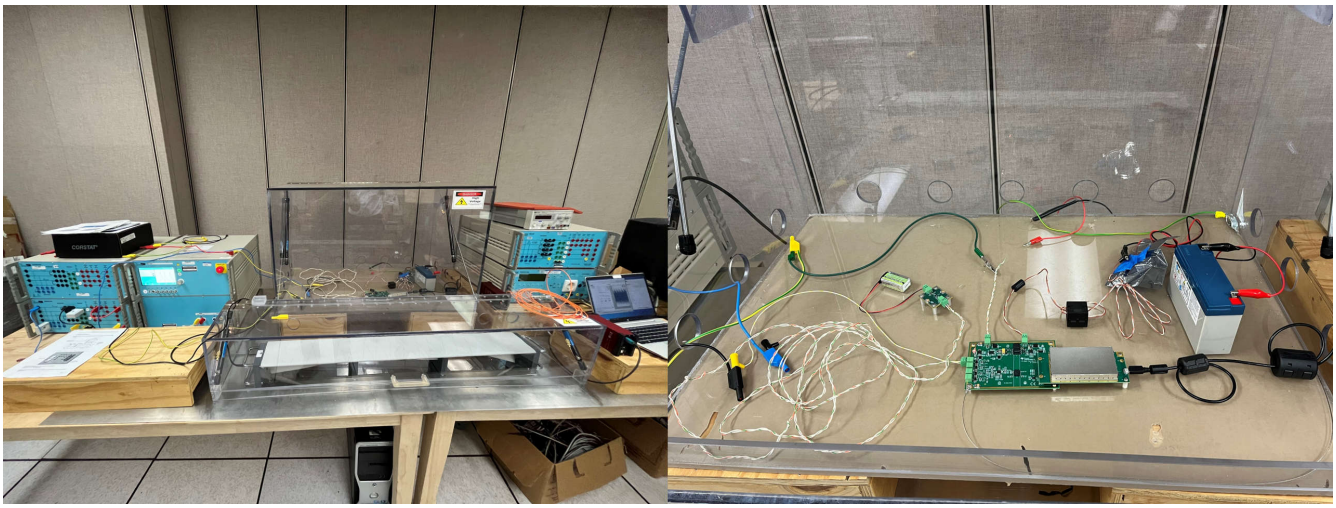


Figure 2-12. Laboratory Setup for Surge Test

Figure 2-13 shows the uncalibrated ADS124S08 output data using the 2-layer TC EMC test board during the surge test (±1.5kV and Line-to-GND). The surge test signal was coupled into the measurement channel that was configured to use the REFOUT bias with a pullup resistor. The graph on the left shows the ADC conversion code when the positive surge signal is applied. The graph on the right shows the ADC conversion code when the negative surge signal is applied to the input channel. Both graphs show that the surge test affected the ADS124S08 and led to temporary performance loss. However, the device automatically recovered without any user intervention. Therefore, the ADS124S08 EMC test board passed the surge test with criteria B.

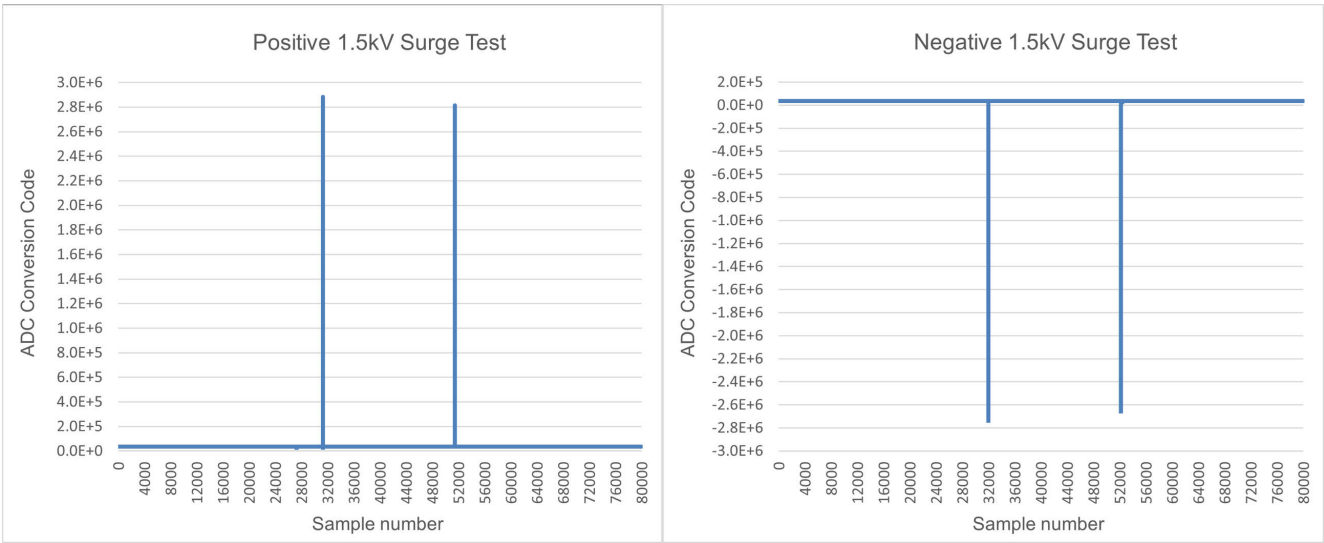


Figure 2-13. ADC Conversion Code Captured for Surge Test

Table 2-10 shows the results of the surge test. The test result is the same for every configuration on all RTD and TC EMC test boards.

Table 2-10. Test Result of Surge Test

Test	Standard	Type and Impedance	Configuration	Test Voltage	Test Level	Criterion	Test Result
Surge	IEC 61000-4-5	Line-to-Ground (2Ω source impedance + 40Ω from coupling network)	RTD: 4-Layer, 3-Wire, Low-side R_{REF}	500 V	1	B	Pass
				1 kV	2	B	Pass
			RTD: 2-Layer, 3-Wire, High-side R_{REF}	500 V	1	B	Pass
				1 kV	2	B	Pass
			TC: 2-Layer, VBIAS for sensor biasing	1 kV	2	B	Pass
				1.5 kV	> 2	B	Pass
			TC: 2-Layer, REFOUT Biasing Pullup Resistor	1 kV	2	B	Pass
				1.5 kV	> 2	B	Pass

2.6 Conducted Immunity (CI)

The IEC 61000-4-6 standard specifies the details for the CI test including test criteria and setup requirements. The IEC61000-4-6 test determines the EUT immunity to external conducted electromagnetic disturbances during operation. Figure 2-14 shows that the test signal is generated from an RF signal generator and an RF power amplifier that is used to amplify the test signal to a specified level. The test signal is injected to the EMC test board input with an injection probe. Spectrum analyzer 1 is used to monitor the output of the power amplifier, while spectrum analyzer 2 is used to monitor and verify the injected signal. The signal frequency is swept from 150kHz to 80MHz with a disturbance signal of 80% amplitude that is modulated with a 1kHz sinusoidal signal. The EUT should be placed at a specified height (10cm) above the ground plane.

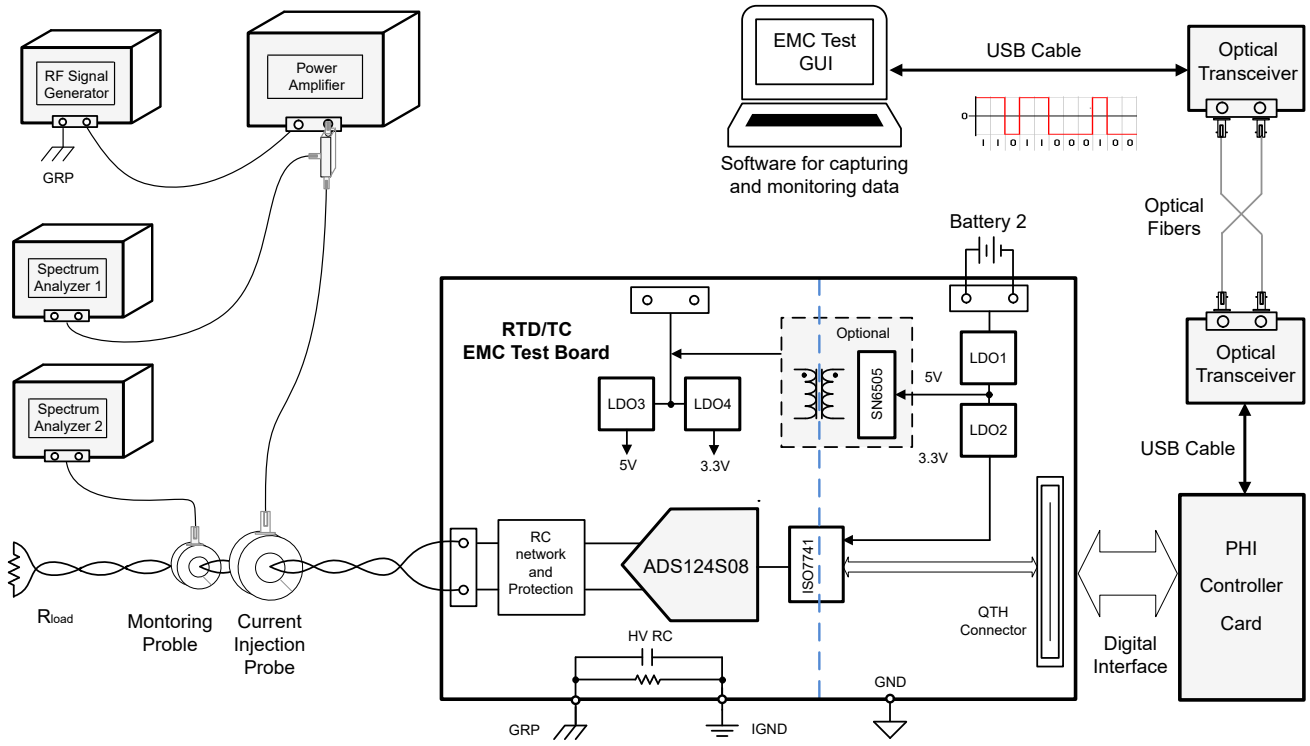


Figure 2-14. Diagram of Laboratory Setup for Conducted Immunity Test

Table 2-11 specifies the IEC 61000-4-6 test levels:

Table 2-11. Test Level of Conducted Immunity Test

Level	Field Strength of Test Signal	
	V0 (10V/m)	V0 (dBuV)
1	1	120
2	3	129.5
3	10	140
x	Special for any level, above, below or between the other levels. This level can be specified in product standard.	

Figure 2-15 shows the actual setup for the conducted immunity test on the ADS124S08 EMC test board.

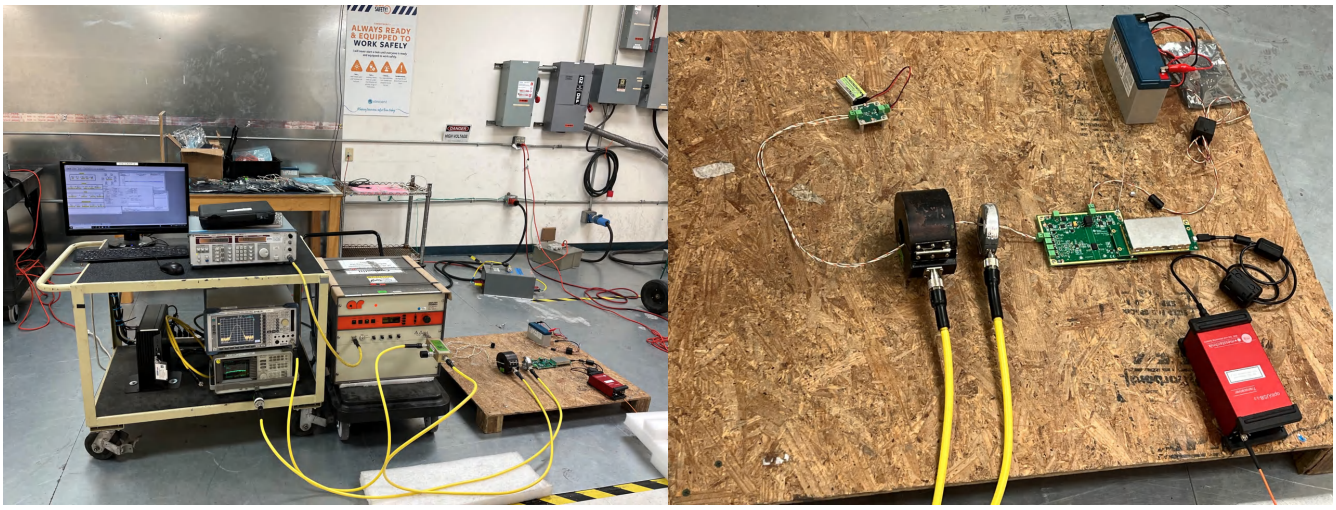


Figure 2-15. Laboratory Setup for Conducted Immunity Test

Figure 2-16 shows the calibrated ADS124S08 output temperature data using the 2-layer TC EMC test board during and after the CI test. The CI test signal was coupled into the measurement channel that was configured to use the REFOUT bias with a pullup resistor. The graph on the left shows the captured temperature data from the ADC during the conducted immunity test. The graph on the right shows the captured temperature data from the ADC when the conducted immunity test completes. Both graphs show that the CI test did not affect the ADS124S08 when the test signal frequency was swept from 150kHz to 80MHz. Therefore, the ADS124S08 EMC test board passed the conducted immunity test with criteria A.

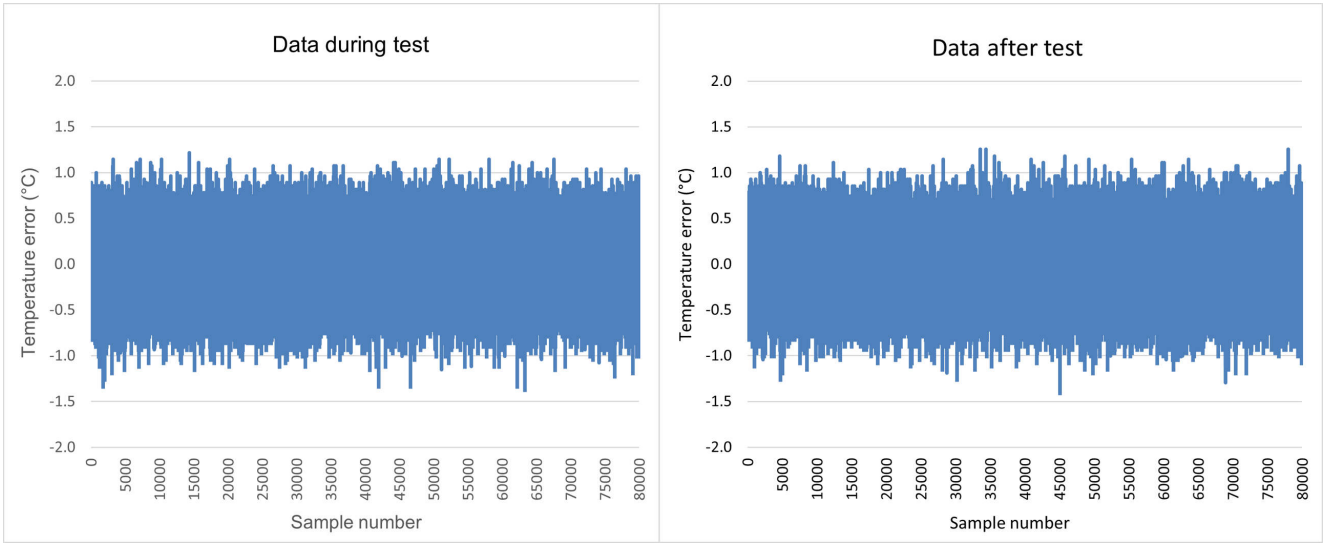


Figure 2-16. Temperature Data Captured for Conducted Immunity Test

Table 2-12 shows the results of the CI test. The test result is the same for every configuration on all RTD and TC EMC test boards.

Table 2-12. Test Result of Conducted Immunity Test

Test	IEC Standard	Configuration	Test Signal		Criterion	Test Result
			Field Strength	Frequency		
Conducted Immunity (CI)	IEC 61000-4-6	RTD: 4-Layer, 3-Wire, Low/High-side R_{REF}	10V/m (Level 3)	150kHz-80MHz	A	Pass
		RTD: 2-Layer, 3-Wire, High-side R_{REF}	10V/m (Level 3)	150kHz-80MHz	A	Pass
		TC: 2-Layer, REFOUT Biasing Pullup Resistor	10V/m (Level 3)	150kHz-80MHz	A	Pass

3 Schematic, PCB Layout and Bill of Materials

3.1 Schematic - RTD EMC Test Board

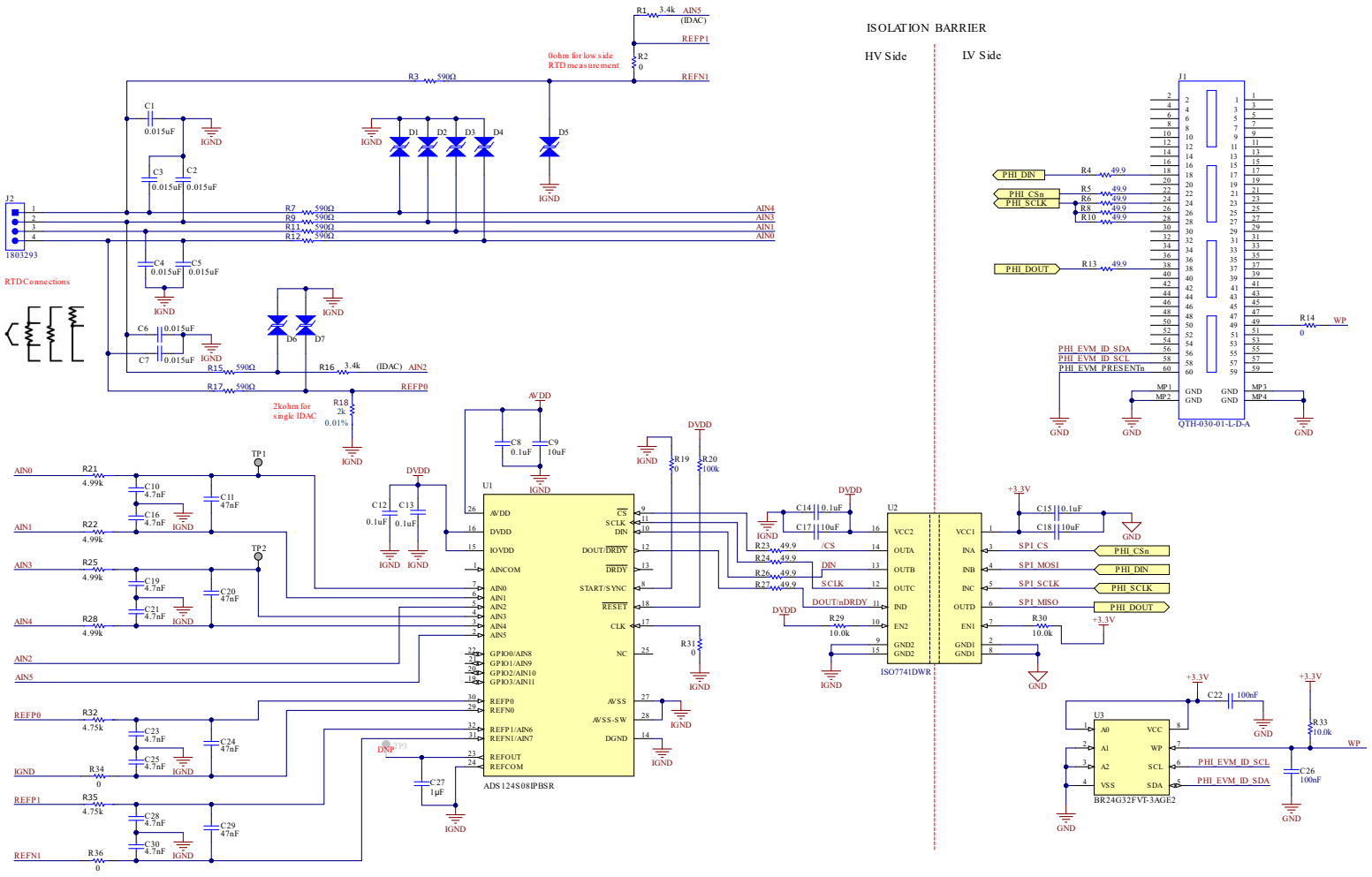


Figure 3-1. Schematic - ADC

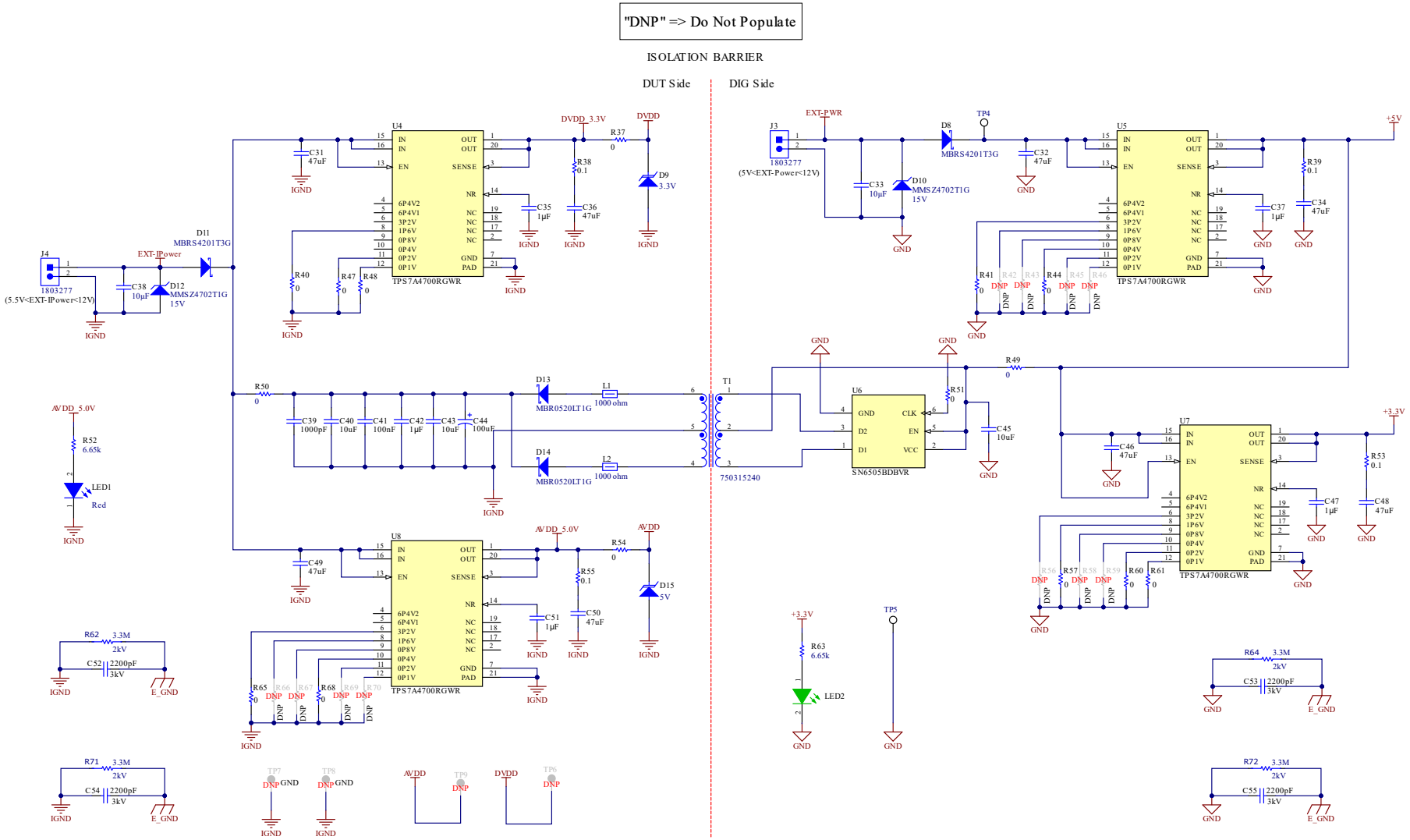


Figure 3-2. Schematic - Power Supply

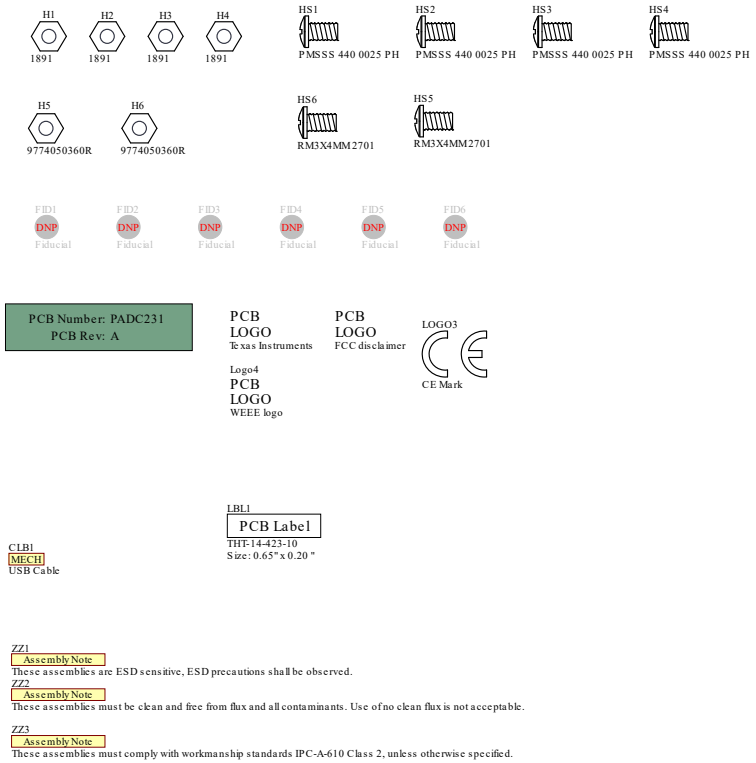


Figure 3-3. Schematic - Hardware

3.2 Schematic - TC EMC Test Board

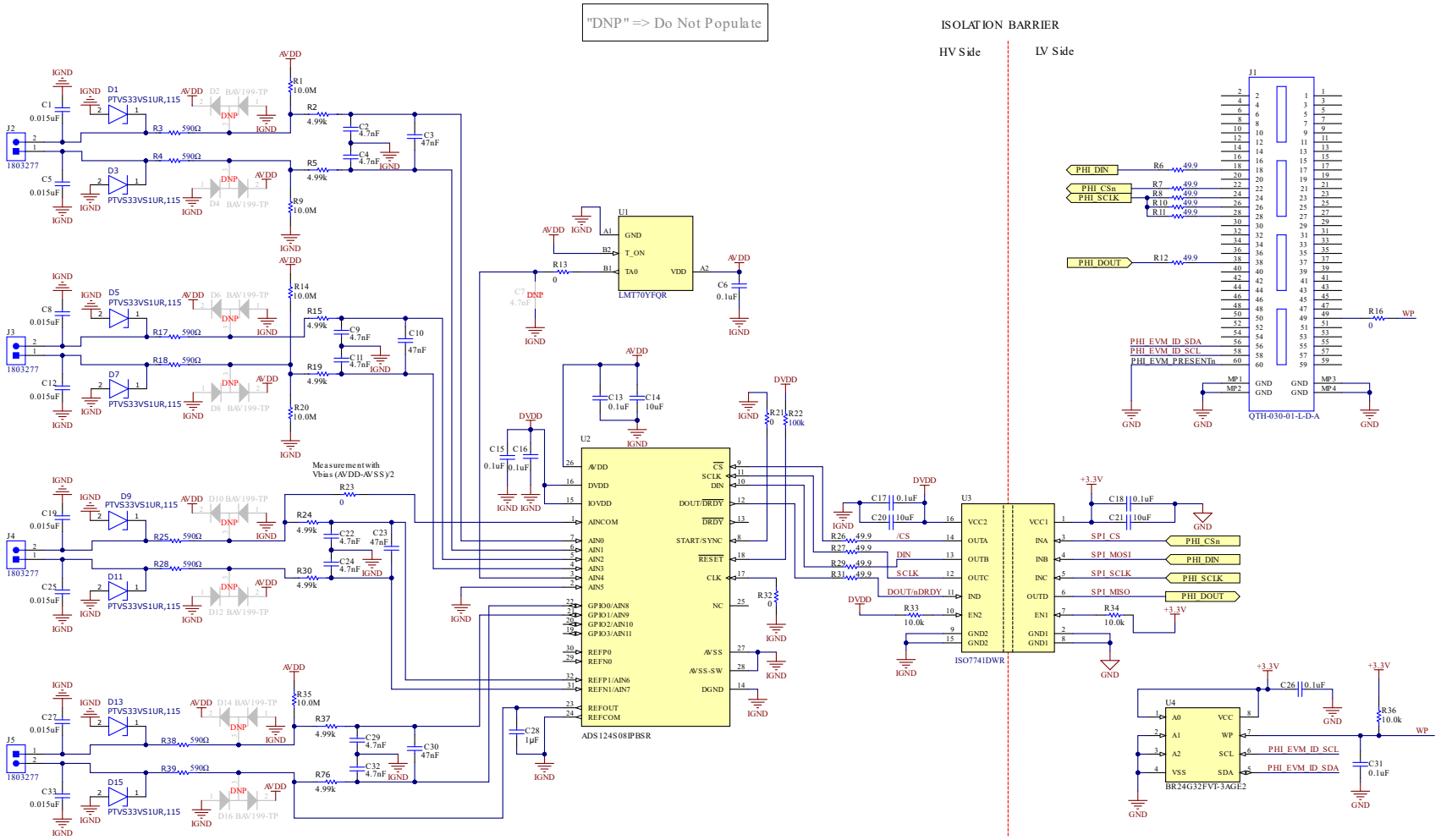


Figure 3-4. Schematic - ADC

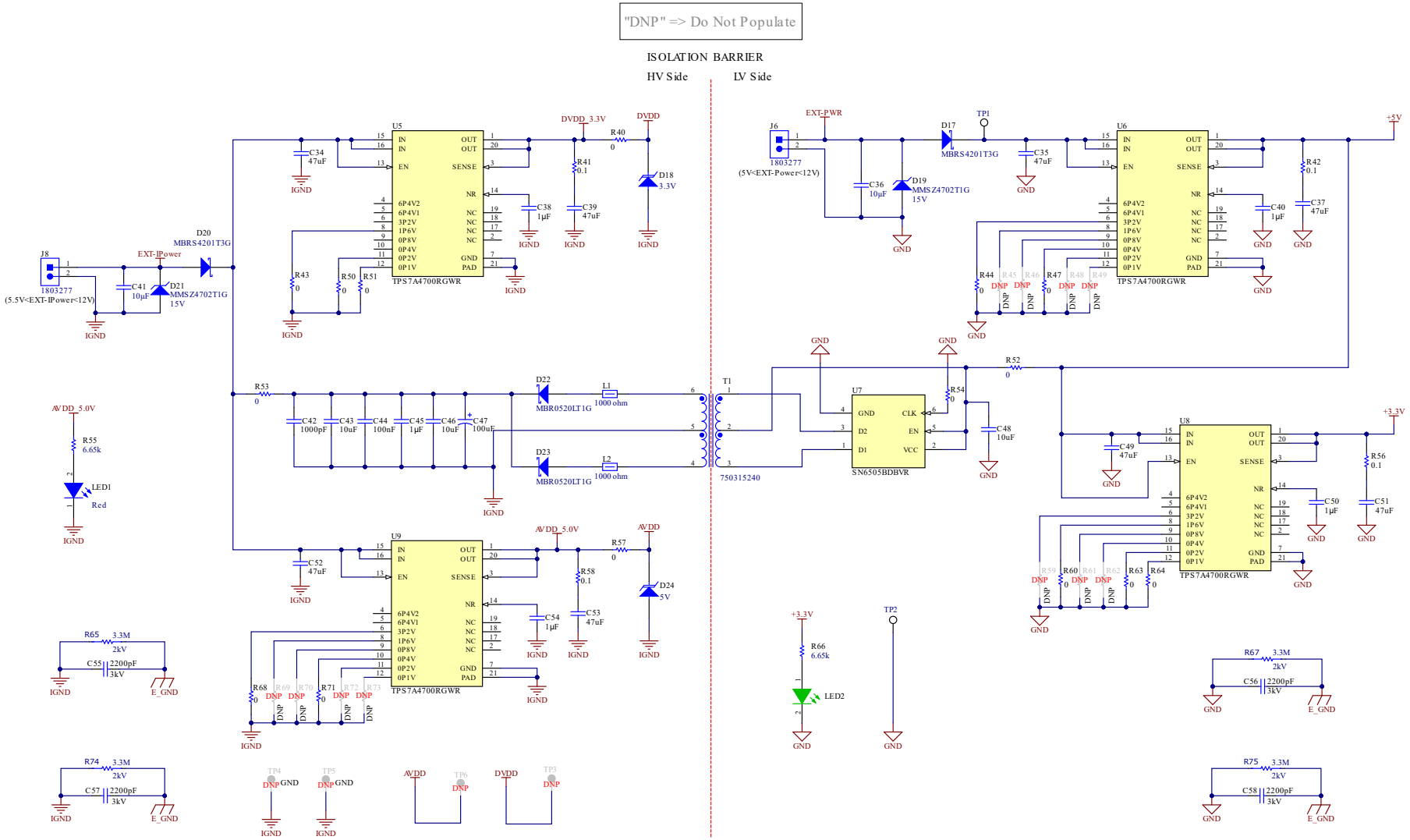


Figure 3-5. Schematic - Power Supply

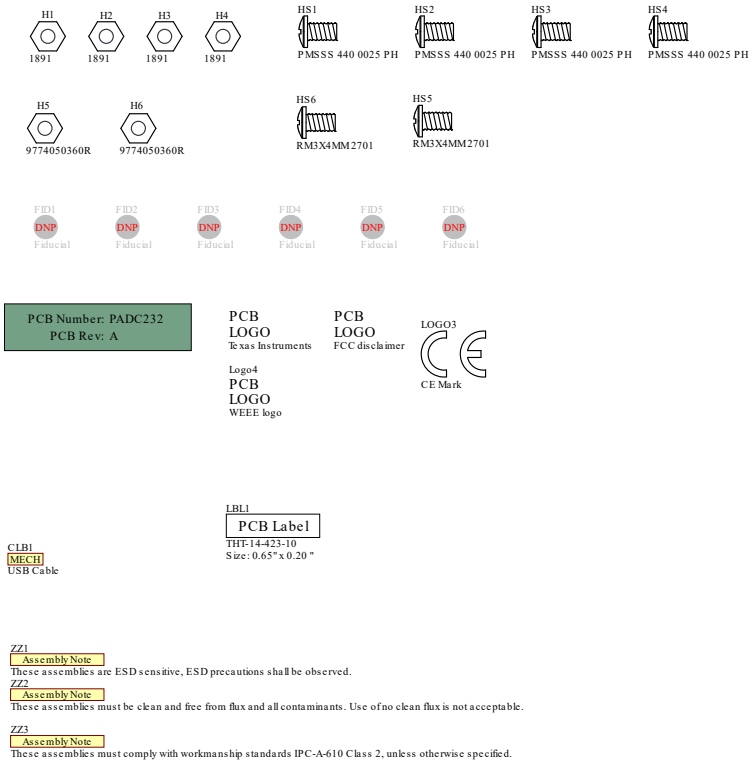


Figure 3-6. Schematic - Hardware

3.3 PCB Layout - RTD EMC Test Board (4-Layer)

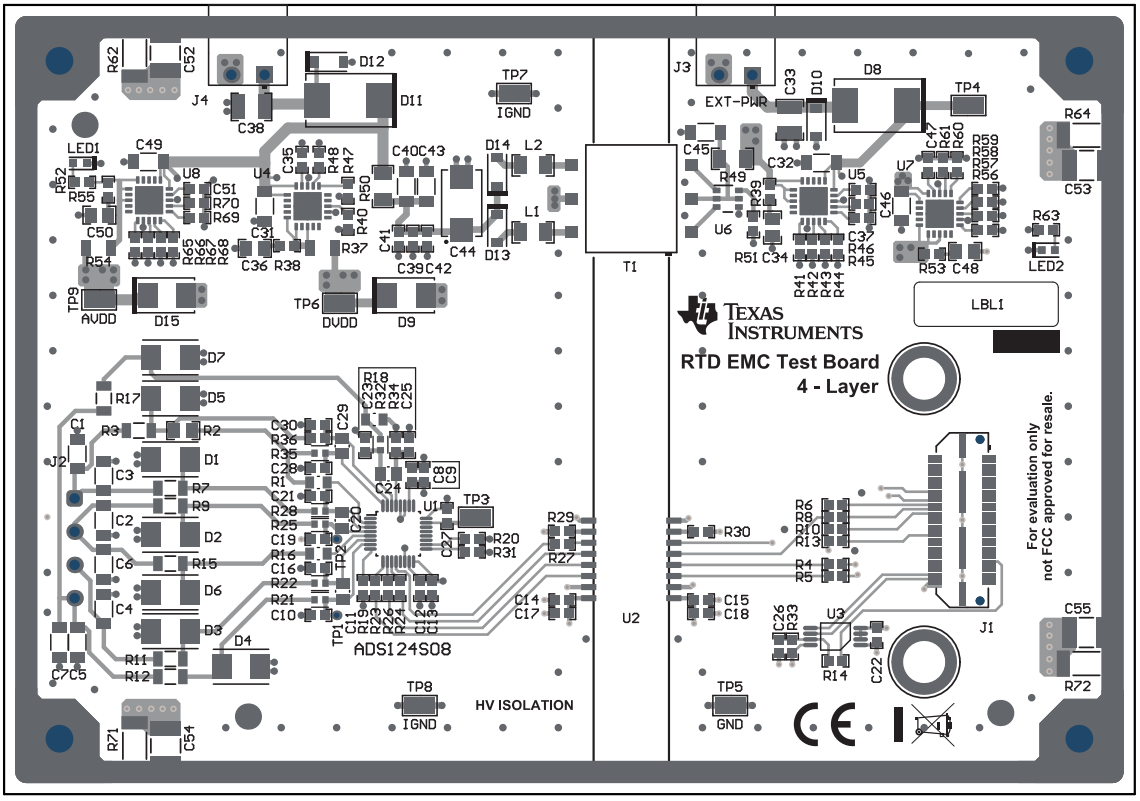


Figure 3-7. Top Layer with Silkscreen

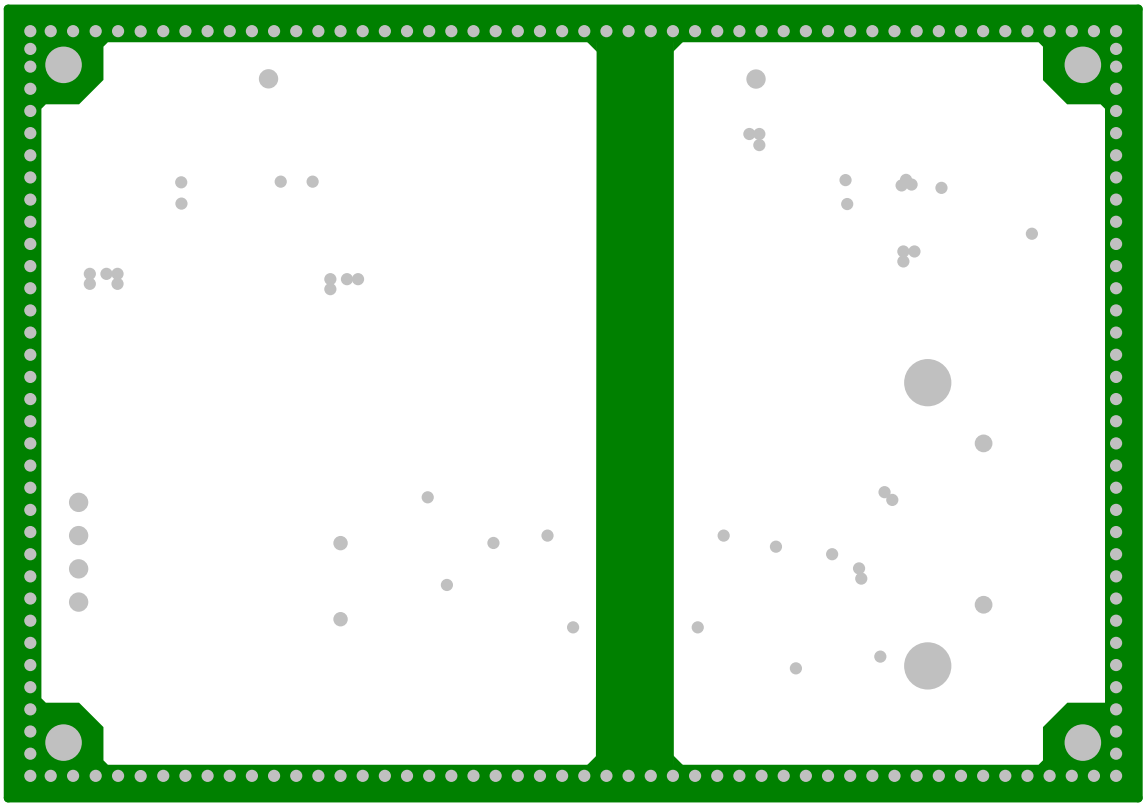


Figure 3-8. Inner Ground Layer

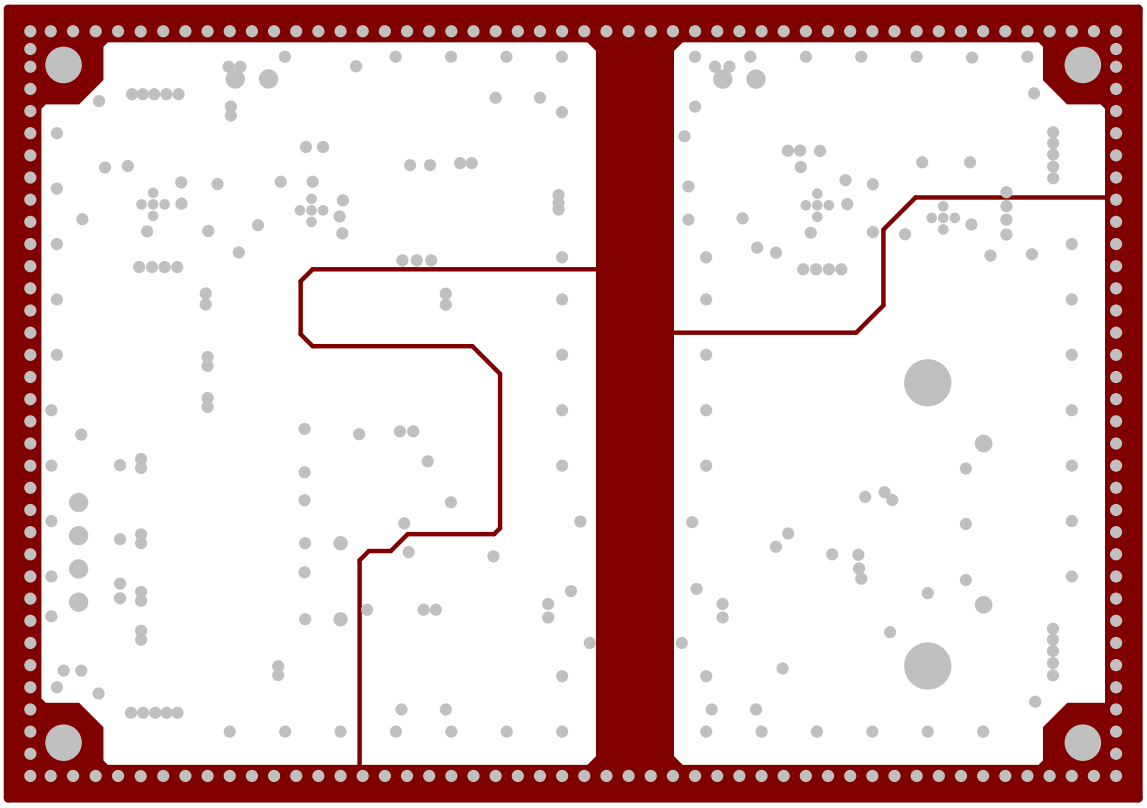


Figure 3-9. Inner Power Layer

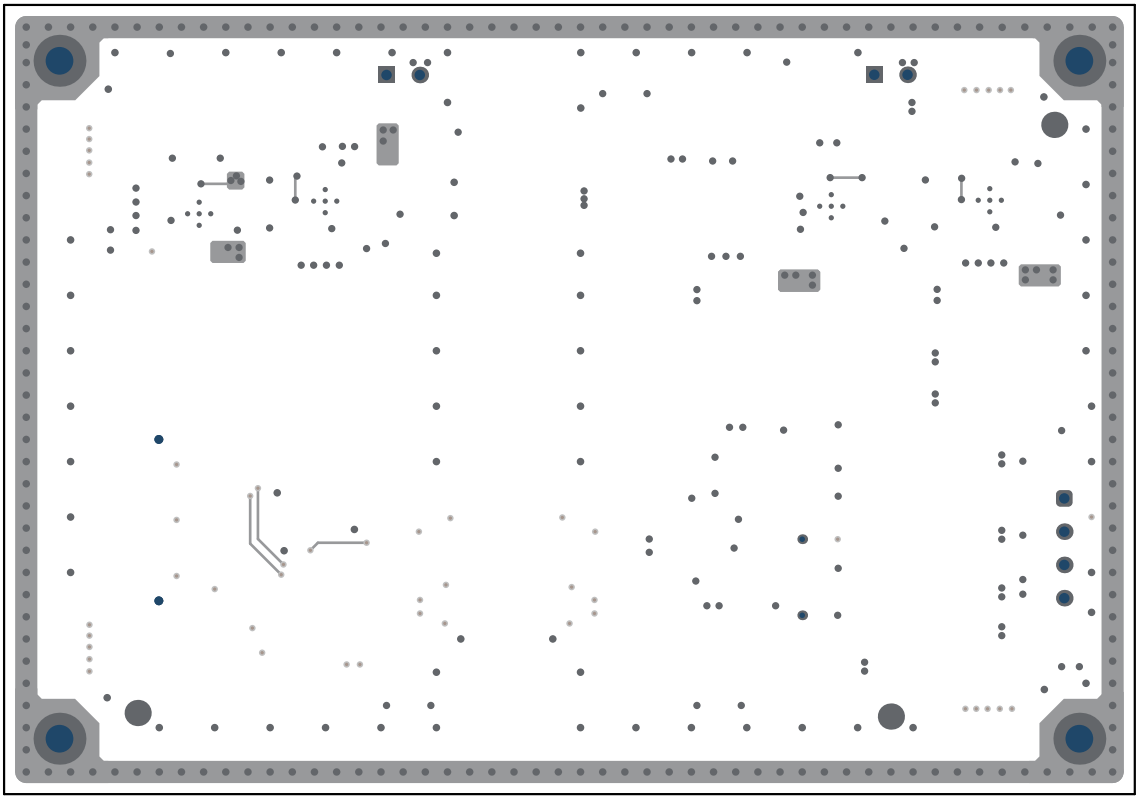


Figure 3-10. Bottom Layer with Silkscreen

3.4 PCB Layout - RTD EMC Test Board (2-Layer)

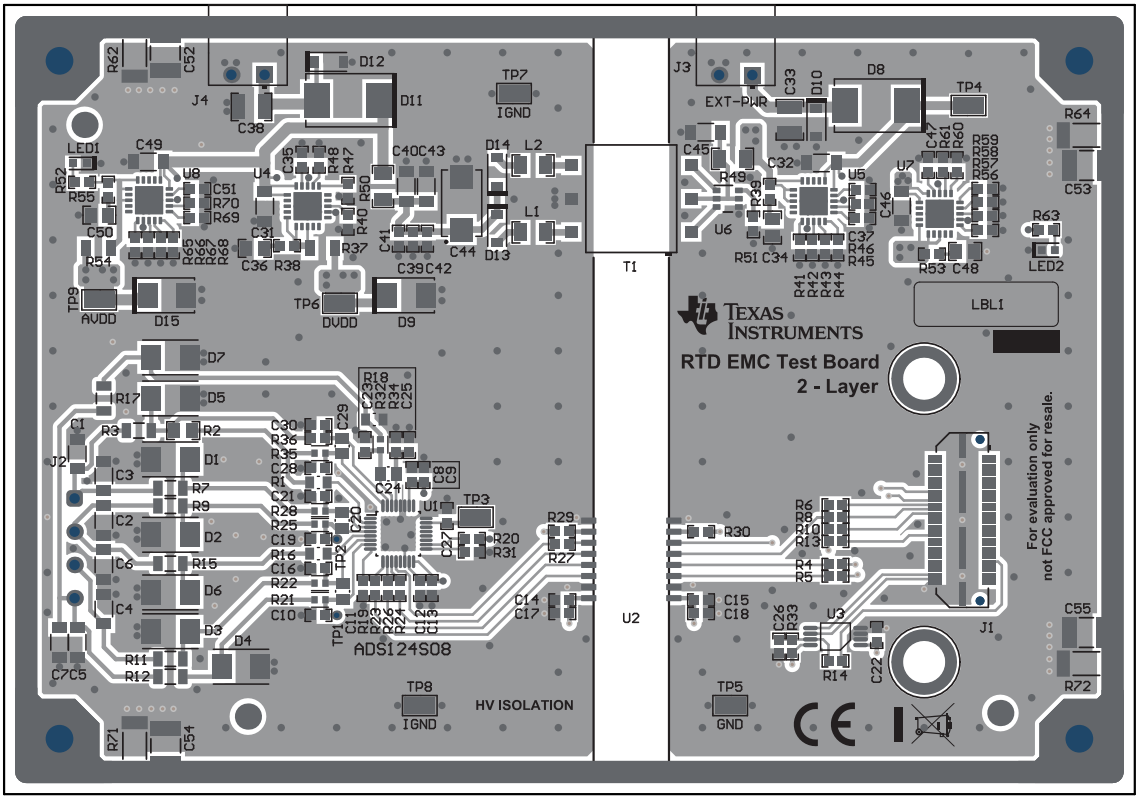


Figure 3-11. Top Layer with Silkscreen

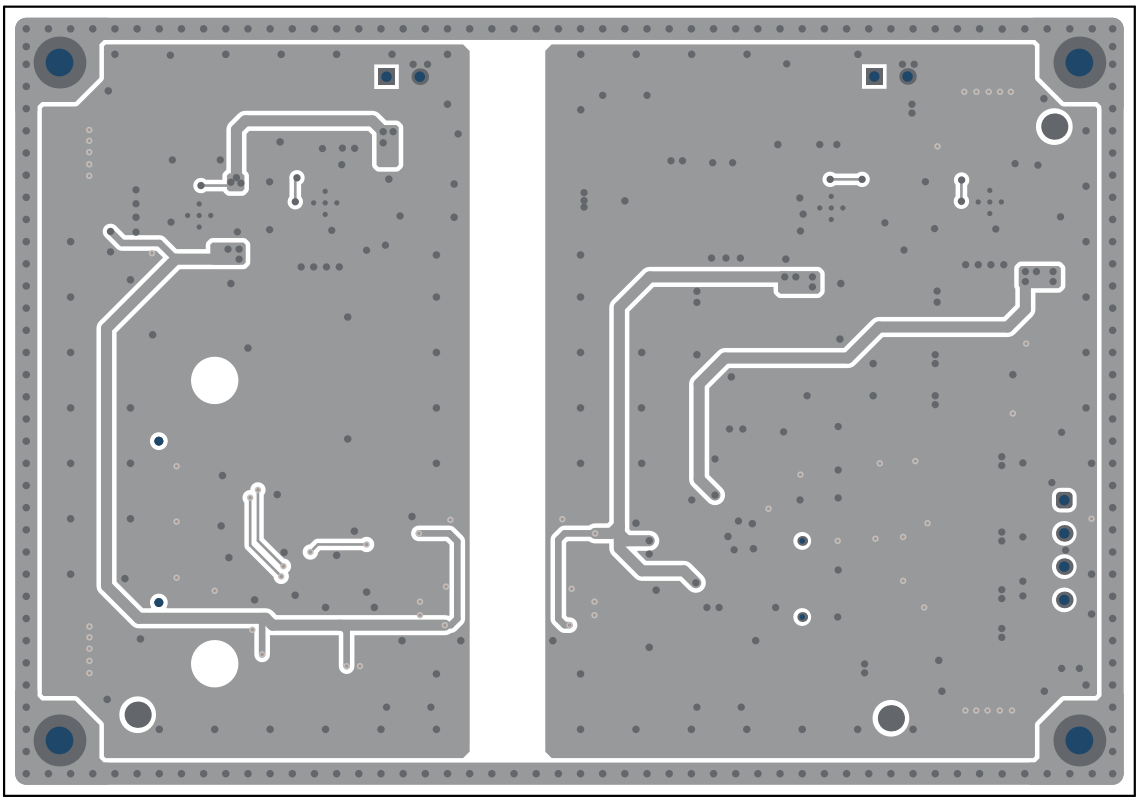


Figure 3-12. Bottom Layer with Silkscreen

3.5 PCB Layout - TC EMC Test Board (4-Layer)

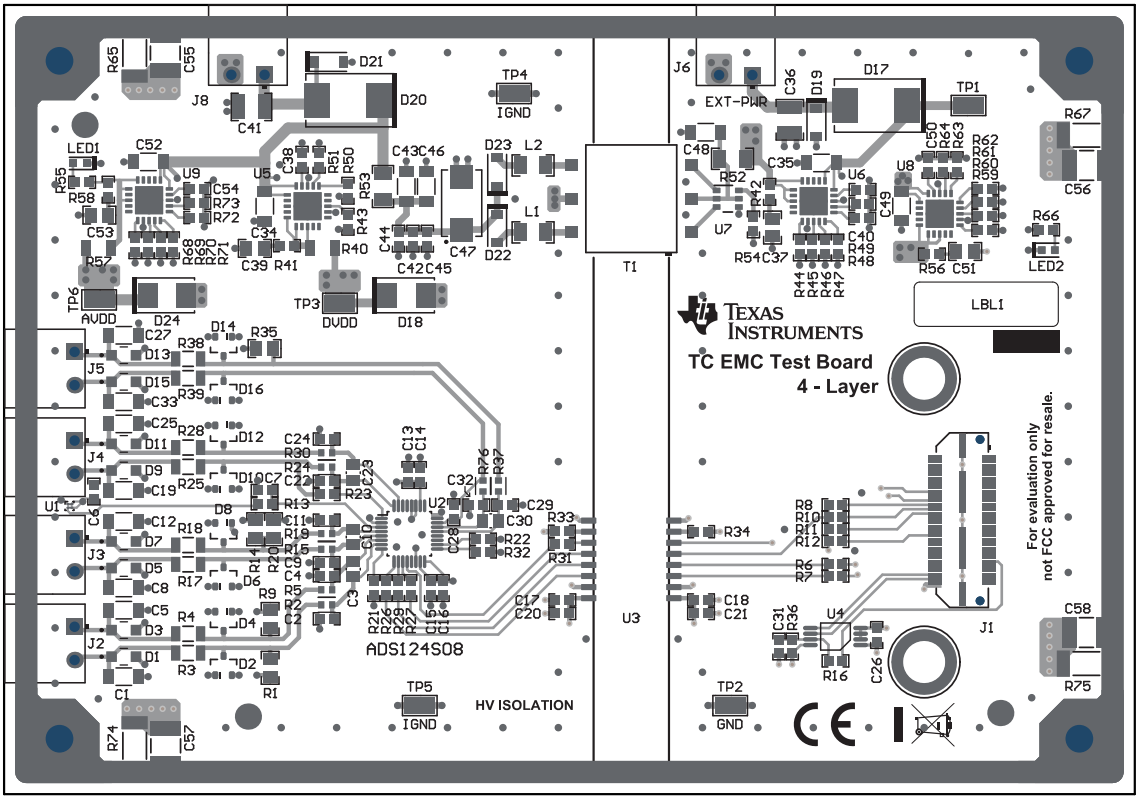


Figure 3-13. Top Layer with Silkscreen

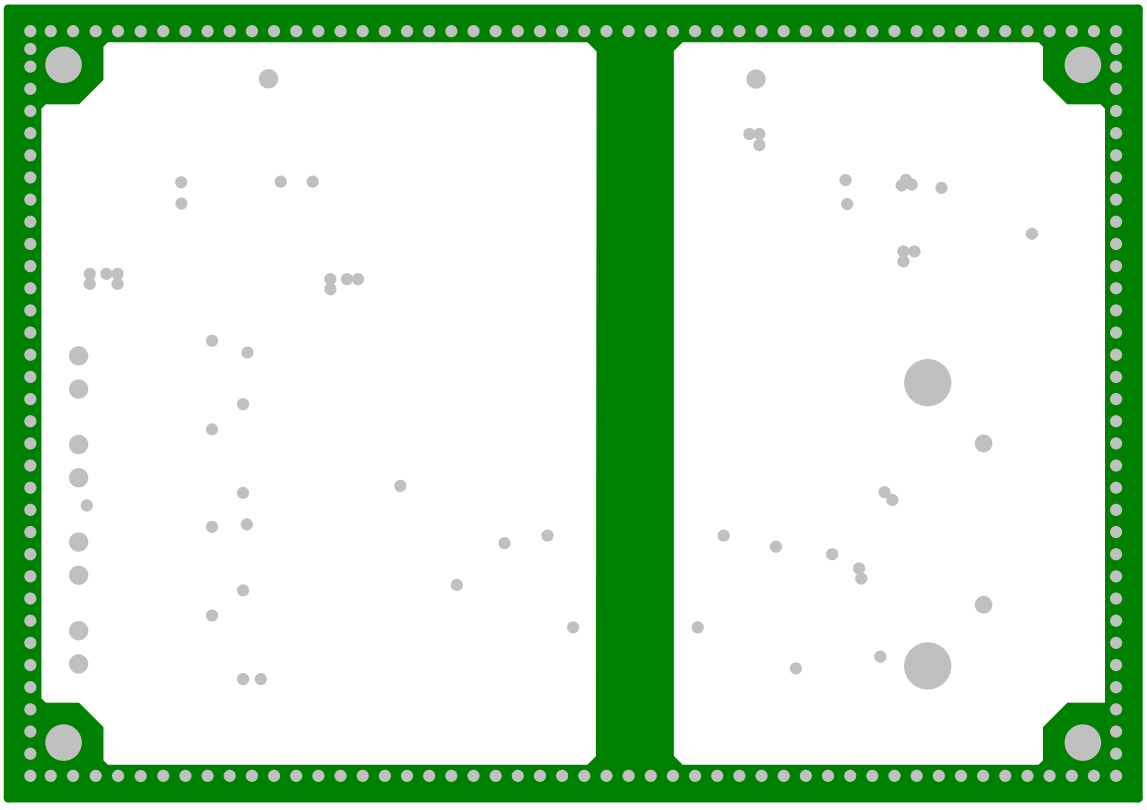


Figure 3-14. Inner Ground Layer

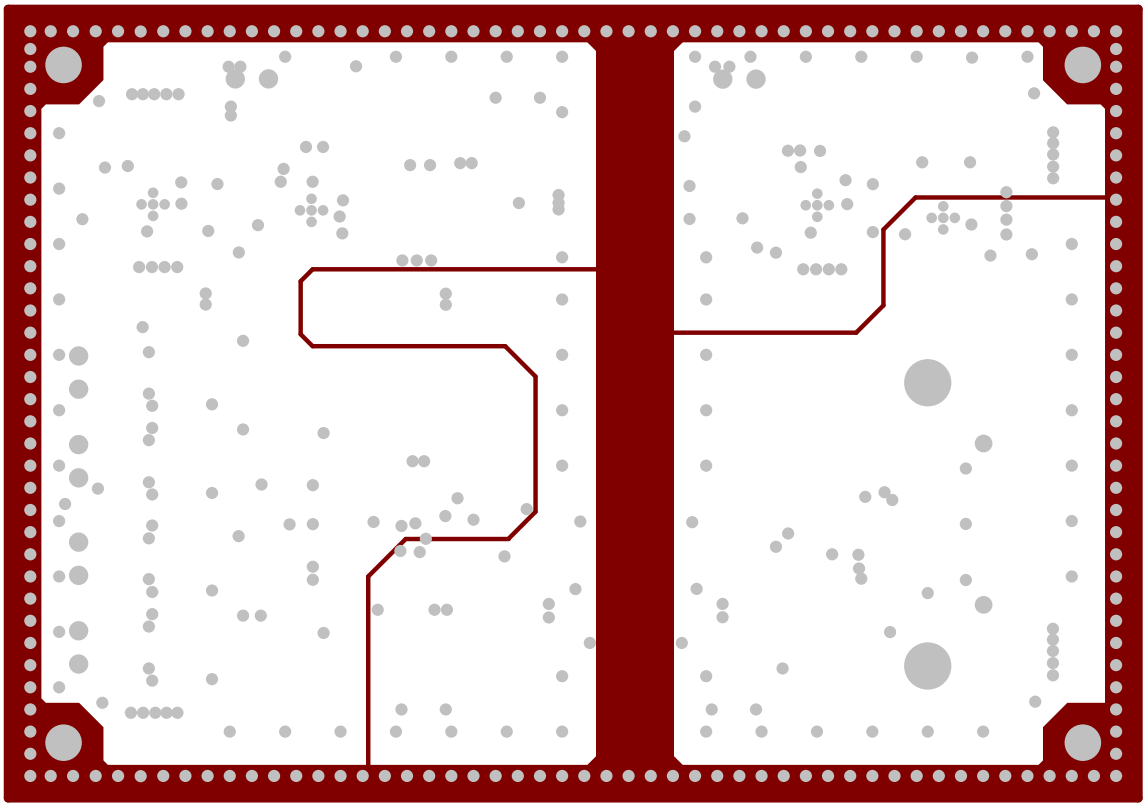


Figure 3-15. Inner Power Layer

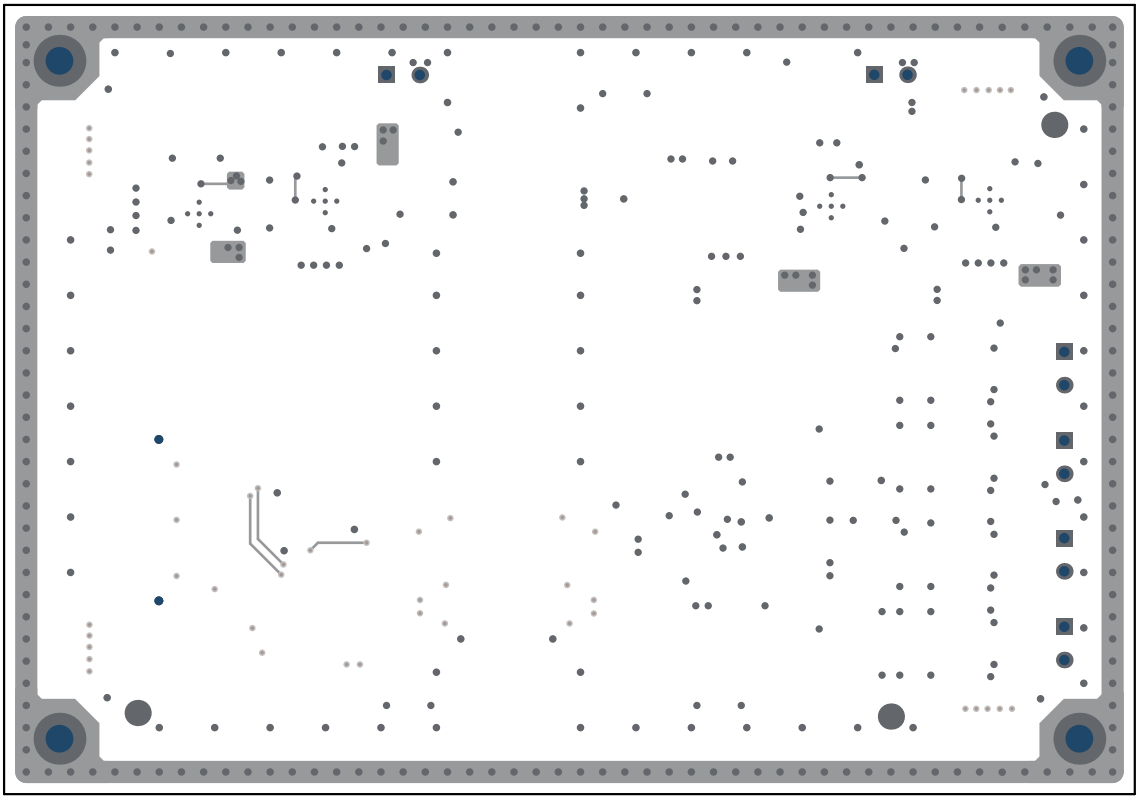


Figure 3-16. Bottom Layer with Silkscreen

3.6 PCB Layout - TC EMC Test Board (2-Layer)

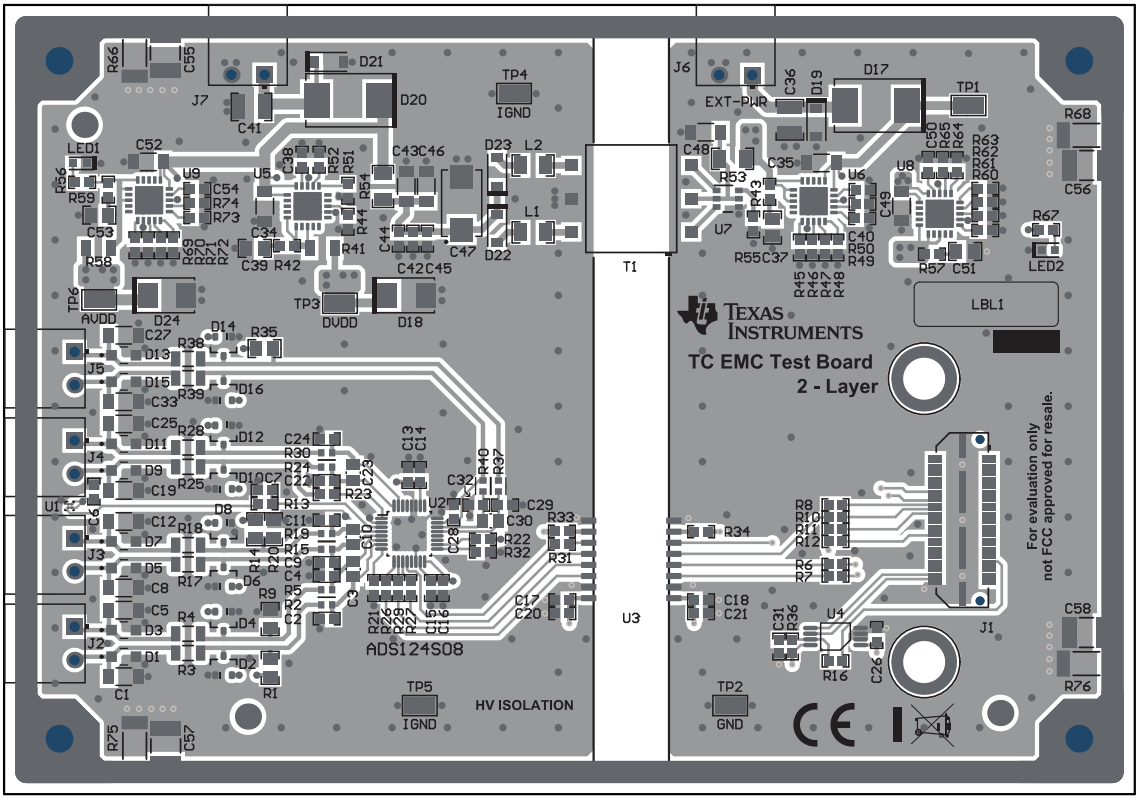


Figure 3-17. Top Layer with Silkscreen

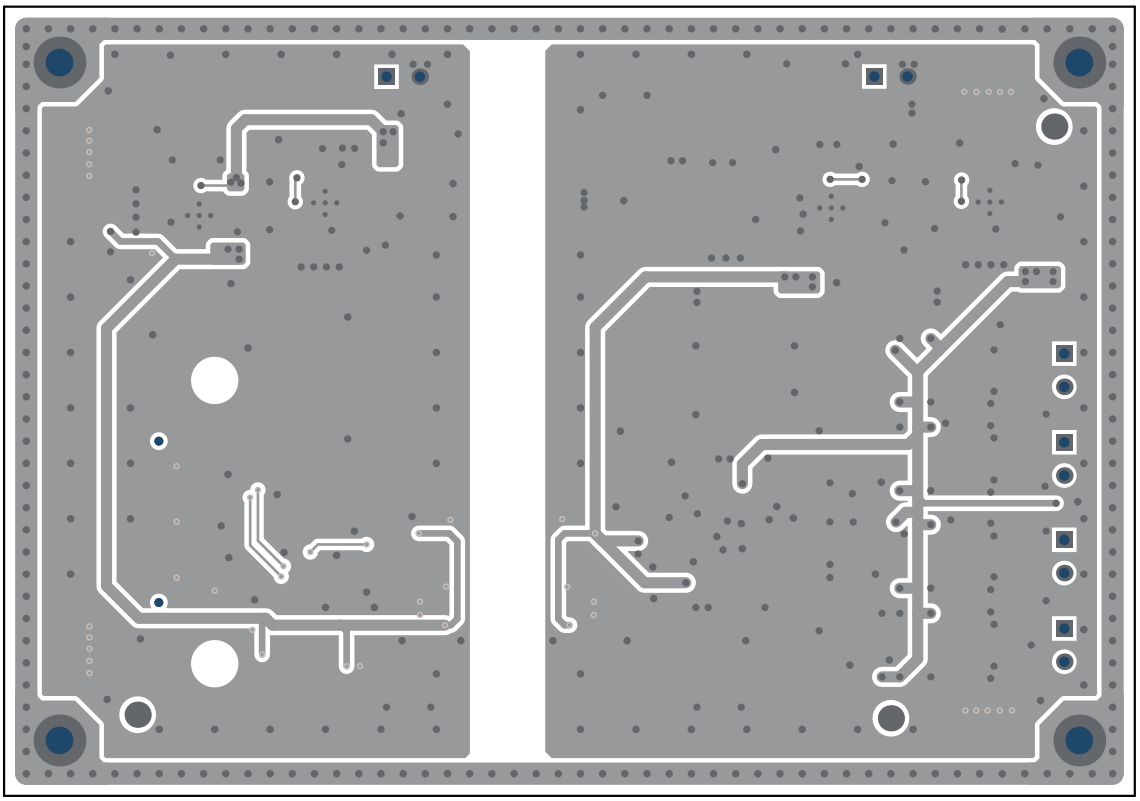


Figure 3-18. Bottom Layer with Silkscreen

3.7 Bill of Materials - RTD EMC Test Board

C1, C2, C3, C4, C5, C6, C7	C3216C0G2E153J160AA	TDK	CAP, CERM, 0.015 uF, 250 V, +/- 5%, C0G/NP0, 1206
C8, C12, C13, C14, C15, C22, C26, C41	C0603C104K5RACTU	Kemet	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603
C9, C17, C18	GRM188R61E106MA73D	MuRata	CAP, CERM, 10 uF, 25 V, +/- 20%, X5R, 0603
C10, C16, C19, C21, C23, C25, C28, C30	C0603C472J1GAC7867	Kemet	CAP, CERM, 4700 pF, 100 V, +/- 5%, C0G/NP0, 0603
C11, C20, C24, C29	C0805C473J3GACTU	Kemet	CAP, CERM, 0.047 µF, 25 V,+/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0805
C27, C35, C37, C42, C47, C51	06033C105KAT2A	AVX	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603
C31, C32, C46, C49	C3216X5R1E476M160AC	TDK	CAP, CERM, 47 uF, 25 V, +/- 20%, X5R, 1206_190
C33, C38	CL32B106KBJNNWE	Samsung Electro-Mechanics	CAP, CERM, 10 µF, 50 V,+/- 10%, X7R, 1210
C34, C36, C48, C50	C2012X5R1A476M125AC	TDK	CAP, CERM, 47 uF, 10 V, +/- 20%, X5R, 0805
C39	GRM1885C1H102FA01J	MuRata	CAP, CERM, 1000 pF, 50 V, +/- 1%, C0G/NP0, 0603
C40, C43, C45	CL31A106KBHNNNE	Samsung Electro-Mechanics	CAP, CERM, 10 uF, 50 V, +/- 10%, X5R, 1206_190
C44	293D107X9020E2TE3	Vishay-Sprague	CAP, TA, 100 uF, 20 V, +/- 10%, 0.5 ohm, SMD
C52, C53, C54, C55	1812HC222KAT1A	AVX	CAP, CERM, 2200 pF, 3000 V, +/- 10%, X7R, 1812
CLB1	6607652	CNC Teck	102-1092-BL-00100; Cable, USB, A Male - B Micro Male, 1M; 6607652 Kitting Item
D1, D2, D3, D4, D5, D6, D7	SMBJ14CA	Littelfuse	Diode, TVS, Bi, 14 V, SMB
D8, D11	MBRS4201T3G	ON Semiconductor	Diode, Schottky, 200 V, 4 A, SMC
D9	SMBJ3V3-E3/52	Vishay-Semiconductor	Diode, TVS, Uni, 3.3 V, 7.3 Vc, AEC-Q101, SMB
D10, D12	MMSZ4702T1G	ON Semiconductor	Diode, Zener, 15 V, 500 mW, SOD-123
D13, D14	MBR0520LT1G	ON Semiconductor	Diode, Schottky, 20 V, 0.5 A, SOD-123
D15	SMBJ5.0A-13-F	Diodes Inc.	Diode, TVS, Uni, 5 V, 9.2 Vc, SMB
H1, H2, H3, H4	1891	Keystone	Hex Standoff, #4-40, Aluminum, 1/4"
H5, H6	9774050360R	Wurth Elektronik	ROUND STANDOFF M3 STEEL 5MM
HS1, HS2, HS3, HS4	PMSSS 440 0025 PH	B&F Fastener Supply	MACHINE SCREW PAN PHILLIPS 4-40
HS5, HS6	RM3X4MM 2701	APM HEXSEAL	Machine Screw Pan PHILLIPS M3
J1	QTH-030-01-L-D-A	Samtec	Header (Shrouded), 19.7mil, 30x2, Gold, SMT
J2	1803293	Phoenix Contact	Terminal Block, 4 Position, 3.81mm, Tin, R/A, TH
J3, J4	1803277	Phoenix Contact	Terminal Block, 2x1, 3.81mm, R/A, TH
L1, L2	HZ1206D102R-10	Laird-Signal Integrity Products	Ferrite Bead, 1000 ohm @ 100 MHz, 0.4 A, 1206
LBL1	THT-14-423-10	Brady	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll
LED1	150060RS75000	Wurth Elektronik	LED, Red, SMD
LED2	LTST-C193TGKT-5A	Lite-On	LED, Green, SMD
R1, R16	RN73C2A3K4BTDF	TE Connectivity	3.4 kOhms ±0.1% 0.1W, 1/10W Chip Resistor 0805 (2012 Metric) Thin Film
R2	CRCW08050000Z0EAHP	Vishay-Dale	RES, 0, 5%, 0.333 W, AEC-Q200 Grade 0, 0805
R3, R7, R9, R11, R12, R15, R17	RQ73C2B590RBTD	TE	RQ732B 1206 590Ω 0.4W 10ppm/°C 0.1% 200V
R4, R5, R6, R8, R10, R13	RC0603FR-0749R9L	Yageo	RES, 49.9, 1%, 0.1 W, 0603
R14	CRCW06030000Z0EA	Vishay-Dale	RES, 0, 5%, 0.1 W, 0603
R18	RNCF0805TKY2K00	Stackpole Electronics	2 kOhms ±0.01% 0.125W, 1/8W Chip Resistor 0805 (2012 Metric) Automotive AEC-Q200 Thin Film

R19, R31, R34, R36, R40, R41, R44, R47, R48, R51, R57, R60, R61, R65, R68	CRCW06030000Z0EA	Vishay-Dale	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603
R20	RC0603FR-07100KL	Yageo	RES, 100 k, 1%, 0.1 W, 0603
R21, R22, R25, R28	RQ73C1J4K99BTD	TE Connectivity	4.99 kOhms ±0.1% 0.15W Chip Resistor 0603 (1608 Metric) Anti-Sulfur, Automotive AEC-Q200 Thin Film
R23, R24, R26, R27	CRCW060349R9FKEA	Vishay-Dale	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R29, R30	CRCW060310K0FKEA	Vishay-Dale	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R32, R35	RQ73C1J4K75BTD	TE	4.75 kOhms ±0.1% 0.15W Chip Resistor 0603 (1608 Metric) Anti-Sulfur, Automotive AEC-Q200 Thin Film
R33	RC0603FR-0710KL	Yageo	RES, 10.0 k, 1%, 0.1 W, 0603
R37, R54	5108	Keystone	RES, 0, 1%, 0.5 W, 1206
R38, R39, R53, R55	ERJ-3RSFR10V	Panasonic	RES, 0.1, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R49, R50	CRCW12060000Z0EAHP	Vishay-Dale	RES, 0, 0.75 W, AEC-Q200 Grade 0, 1206
R52, R63	RC0603FR-076K65L	Yageo	RES, 6.65 k, 1%, 0.1 W, 0603
R62, R64, R71, R72	CHV2010-FX-3304ELF	Bourns	RES SMD 3.3M OHM 1% 1/2W 2010
T1	750315240	Wurth Elektronik	Transformer, 110 uH, SMT
TP4, TP5	5015	Keystone	Test Point, Miniature, SMT
U1	ADS124S08IPBSR	Texas Instruments	24-Bit, 4kSPS, 12-Ch Delta-Sigma ADC With PGA and Voltage Reference for Precision Sensor Measurement, PBS0032A (TQFP-32)
U2	ISO7741DWR	Texas Instruments	High-Speed, Low-Power, Robust EMC Quad-Channel Digital Isolator, DW0016B (SOIC-16)
U3	BR24G32FVT-3AGE2	Rohm	I2C BUS EEPROM (2-Wire), TSSOP-B8
U4, U5, U7, U8	TPS7A4700RGWR	Texas Instruments	36V, 1A, 4.17μVRMS, RF Low-Dropout (LDO) Voltage Regulator, RGW0020A (VQFN-20)
U6	SN6505BDBVR	Texas Instruments	Low-Noise 1 A, 420 kHz Transformer Driver, DBV0006A (SOT-23-6)
R42, R43, R45, R46, R56, R58, R59, R66, R67, R69, R70	CRCW06030000Z0EA (Not Fitted)	Vishay-Dale	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603
TP3, TP6, TP7, TP8, TP9	5015 (Not Fitted)	Keystone	Test Point, Miniature, SMT

3.8 Bill of Materials - TC EMC Test Board

C1, C5, C8, C12, C19, C25, C27, C33	C3216C0G2E153J160AA	TDK	CAP, CERM, 0.015 uF, 250 V, +/- 5%, C0G/NP0, 1206_190
C2, C4, C9, C11, C22, C24, C29, C32	C0603C472J1GAC7867	Kemet	CAP, CERM, 4700 pF, 100 V, +/- 5%, C0G/NP0, 0603
C3, C10, C23, C30	C0805C473J3GACTU	Kemet	CAP, CERM, 0.047 μF, 25 V,+/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0805
C6, C13, C15, C16, C17, C18, C26, C31, C44	C0603C104K5RACTU	Kemet	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603
C14, C20, C21	GRM188R61E106MA73D	MuRata	CAP, CERM, 10 uF, 25 V, +/- 20%, X5R, 0603
C28, C38, C40, C45, C50, C54	06033C105KAT2A	AVX	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603
C34, C35, C49, C52	C3216X5R1E476M160AC	TDK	CAP, CERM, 47 uF, 25 V, +/- 20%, X5R, 1206
C36, C41	CL32B106KBJNNWE	Samsung Electro-Mechanics	CAP, CERM, 10 μF, 50 V,+/- 10%, X7R, 1210
C37, C39, C51, C53	C2012X5R1A476M125AC	TDK	CAP, CERM, 47 uF, 10 V, +/- 20%, X5R, 0805
C42	GRM1885C1H102FA01J	MuRata	CAP, CERM, 1000 pF, 50 V, +/- 1%, C0G/NP0, 0603

C43, C46, C48	CL31A106KBHNNNE	Samsung Electro-Mechanics	CAP, CERM, 10 uF, 50 V, +/- 10%, X5R, 1206_190
C47	293D107X9020E2TE3	Vishay-Sprague	CAP, TA, 100 uF, 20 V, +/- 10%, 0.5 ohm, SMD
C55, C56, C57, C58	1812HC222KAT1A	AVX	CAP, CERM, 2200 pF, 3000 V, +/- 10%, X7R, 1812
CLB1	6607652	CNC Teck	102-1092-BL-00100; Cable, USB, A Male - B Micro Male, 1M; 6607652 Kitting Item
D1, D3, D5, D7, D9, D11, D13, D15	PTVS33VS1UR,115	Nexperia	PTVS Series 400 W 53.3 V Uni-Directional Surface Mount TVS Diode - SOD-123W
D17, D20	MBRS4201T3G	ON Semiconductor	Diode, Schottky, 200 V, 4 A, SMC
D18	SMBJ3V3-E3/52	Vishay-Semiconductor	Diode, TVS, Uni, 3.3 V, 7.3 Vc, AEC-Q101, SMB
D19, D21	MMSZ4702T1G	ON Semiconductor	Diode, Zener, 15 V, 500 mW, SOD-123
D22, D23	MBR0520LT1G	ON Semiconductor	Diode, Schottky, 20 V, 0.5 A, SOD-123
D24	SMBJ5.0A-13-F	Diodes Inc.	Diode, TVS, Uni, 5 V, 9.2 Vc, SMB
H1, H2, H3, H4	1891	Keystone	Hex Standoff, #4-40, Aluminum, 1/4"
H5, H6	9774050360R	Wurth Elektronik	ROUND STANDOFF M3 STEEL 5MM
HS1, HS2, HS3, HS4	PMSSS 440 0025 PH	B&F Fastener Supply	MACHINE SCREW PAN PHILLIPS 4-40
HS5, HS6	RM3X4MM 2701	APM HEXSEAL	Machine Screw Pan PHILLIPS M3
J1	QTH-030-01-L-D-A	Samtec	Header(Shrouded), 19.7mil, 30x2, Gold, SMT
J2, J3, J4, J5, J6, J8	1803277	Phoenix Contact	Terminal Block, 2x1, 3.81mm, R/A, TH
L1, L2	HZ1206D102R-10	Laird-Signal Integrity Products	Ferrite Bead, 1000 ohm @ 100 MHz, 0.4 A, 1206
LBL1	THT-14-423-10	Brady	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll
LED1	150060RS75000	Wurth Elektronik	LED, Red, SMD
LED2	LTST-C193TGKT-5A	Lite-On	LED, Green, SMD
R1, R9, R14, R20, R35	CRCW080510M0FKEA	Vishay-Dale	RES, 10.0 M, 1%, 0.125 W, AEC-Q200 Grade 0, 0805
R2, R5, R15, R19, R24, R30, R37, R76	RQ73C1J4K99BTD	TE Connectivity	4.99 kOhms ±0.1% 0.15W Chip Resistor 0603 (1608 Metric) Anti-Sulfur, Automotive AEC-Q200 Thin Film
R3, R4, R17, R18, R25, R28, R38, R39	RQ73C2B590RBTD	TE	RQ732B 1206 590Ω 0.4W 10ppm/°C 0.1% 200V
R6, R7, R8, R10, R11, R12	RC0603FR-0749R9L	Yageo	RES, 49.9, 1%, 0.1 W, 0603
R13, R21, R32, R43, R44, R47, R50, R51, R54, R60, R63, R64, R68, R71	CRCW06030000Z0EA	Vishay-Dale	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603
R16, R23	CRCW06030000Z0EA	Vishay-Dale	RES, 0, 5%, 0.1 W, 0603
R22	RC0603FR-07100KL	Yageo	RES, 100 k, 1%, 0.1 W, 0603
R26, R27, R29, R31	CRCW060349R9FKEA	Vishay-Dale	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R33, R34, R36	CRCW060310K0FKEA	Vishay-Dale	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R40, R57	5108	Keystone	RES, 0, 1%, 0.5 W, 1206
R41, R42, R56, R58	ERJ-3RSFR10V	Panasonic	RES, 0.1, 1%, 0.1 W, AEC-Q200 Grade 0, 0603
R52, R53	CRCW12060000Z0EAHP	Vishay-Dale	RES, 0, 0.75 W, AEC-Q200 Grade 0, 1206
R55, R66	RC0603FR-076K65L	Yageo	RES, 6.65 k, 1%, 0.1 W, 0603
R65, R67, R74, R75	CHV2010-FX-3304ELF	Bourns	RES SMD 3.3M OHM 1% 1/2W 2010
T1	750315240	Wurth Elektronik	Transformer, 110 uH, SMT
TP1, TP2	5015	Keystone	Test Point, Miniature, SMT
U1	LMT70YFQR	Texas Instruments	+/-0.1degC Precision Analog Temperature Sensor, YFQ0004ACAC (DSBGA-4)

U2	ADS124S08IPBSR	Texas Instruments	24-Bit, 4kSPS, 12-Ch Delta-Sigma ADC With PGA and Voltage Reference for Precision Sensor Measurement, PBS0032A (TQFP-32)
U3	ISO7741DWR	Texas Instruments	High-Speed, Low-Power, Robust EMC Quad-Channel Digital Isolator, DW0016B (SOIC-16)
U4	BR24G32FVT-3AGE2	Rohm	I2C BUS EEPROM (2-Wire), TSSOP-B8
U5, U6, U8, U9	TPS7A4700RGWR	Texas Instruments	36V, 1A, 4.17μVRMS, RF Low-Dropout (LDO) Voltage Regulator, RGW0020A (VQFN-20)
U7	SN6505BDBVR	Texas Instruments	Low-Noise 1 A, 420 kHz Transformer Driver, DBV0006A (SOT-23-6)
C7	C0603C472J1GAC7867	Kemet	CAP, CERM, 4700 pF, 100 V, +/- 5%, C0G/NP0, 0603
D2, D4, D6, D8, D10, D12, D14, D16	BAV199-TP	Micro Commercial Components	Diode, Switching, 70 V, 0.215 A, SOT-23
FID1, FID2, FID3, FID4, FID5, FID6	N/A	N/A	Fiducial mark. There is nothing to buy or mount.
R45, R46, R48, R49, R59, R61, R62, R69, R70, R72, R73	CRCW06030000Z0EA	Vishay-Dale	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603
sTP3, TP4, TP5, TP6	5015	Keystone	Test Point, Miniature, SMT

4 Summary

Designing a high performance temperature measurement system that can also pass rigorous EMC testing presents a significant challenge for many designers. This application note provides practical, in-depth guidance for developing high-accuracy temperature measurement systems while ensuring robust EMC performance. Key topics covered in the application note include:

1. **Design for EMC Compliance:** Practical guidelines for protective circuit design and optimized PCB layout for both 2-layer and 4-layer boards that meet EMC standards.
2. **Measurement Fundamentals:** Detailed explanations of input connections, sensor configurations, code conversion, and error calculation methods for various RTD and TC systems.
3. **Achieved Precision:** Specific configurations using an EMC-compliant measurement system result in exceptionally high accuracy at room temperature:

   a. RTD Systems: A total calibrated system error of <±0.06°C over the full range of –200°C to +850°C.

   b. TC Systems: A total calibrated system error of <±0.05°C over the full range of –250°C to +1372°C.
4. **Validated Performance:** Test setups and measured results confirm that each design successfully passes all relevant IEC-61000-4 testing requirements.

Follow the practical guidelines and use the validated designs presented in this application note to achieve high-accuracy, reliable, and EMC-compliant temperature measurement systems. Additionally, this information can be generally applied to any measurement system that must also be EMC compliant.

5 References

Texas Instruments, *A Basic Guide to RTD Measurements*, application note.

Texas Instruments, *A Basic Guide to Thermocouple Measurements*, application note.

Texas Instruments, *Circuit for Protecting ADS124S08 ADC from EOS for RTD Measurement*, application note.

Texas Instruments, *ADS124S08: 24-bit, 4-kSPS, 12-ch Delta-Sigma ADC with PGA and Voltage Reference for Sensor mMasurement*, data sheet.

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