Application Note

Asynchronous Operation of LM5125x Boost Controller

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ABSTRACT

The LM5125x is a dual-phase synchronous controller that provides a regulated output voltage for lower up to equal input voltages, also supporting V_{IN} to V_{OUT} bypass mode. The LM5125x can support applications like high-end audio power supplies, voltage stabilizer modules and start-stop applications. Dual-phase, asynchronous operation of the device is also possible, which allows for lower BOM cost and complexity at a reasonable decrease in overall converter performance. This application note shows the evaluation of the LM5125x in asynchronous mode and gives design guidelines to help engineers to design properly for practical applications.

Table of Contents

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1 Introduction

The LM5125x operates over a wide input voltage range (up to 42V) and provides a regulated output that can be changed dynamically via the ATRK/DTRK pin. The LM5125x offers a number of different features such as: selectable switching frequency (100kHz to 2.2MHz), selectable dead time (18ns to 200ns), average inductor current monitoring, dynamically selectable switching modes (diode emulation mode (DEM) and forced pulse width modulation (FPWM)), programmable current limit and power good indicator.

[LM5125-Q1 data sheet, product information and support | TI.com]

[LM5125A-Q1 data sheet, product information and support | TI.com]

The boost controller is designed for synchronous operation, driving a high-side switch replacing the diode of the standard boost controller topology. Synchronous operation allows for lower power losses, by avoiding the forward voltage drop of the diode, hence an overall increase in efficiency. However, synchronous operation increases the BoM cost and the complexity of the design. In some applications, an asynchronous boost converter can still be a good fit, making use of a cheaper, smaller diode instead of the high-side switch.

This application note shows how to use the LM5125x in asynchronous mode while still having all the features the device offers. Test results show a decrease of only 2-3% in the overall efficiency of the converter.

2 Application Implementation

To demonstrate the feasibility of asynchronous operation for the LM5125x, the tests were performed on the LM5125EVM-BST evaluation module. The evaluation module showcases the features and performance of the LM5125 while being designed for ease of configuration, enabling the user to evaluate different conditions of the module. The standard configuration is intended to provide a 24V/300W output. The output voltage can be dynamically adjusted via ATRK/DTRK pin.

The DIP switches on the evaluation module allow to set up the three configuration registers CFG0, CFG1 and CFG2. As mentioned in the LM5125EVM-BST's user guide [https://www.ti.com/lit/snvu874], these three registers control most of the features of the device, including the overvoltage protection (OVP) and input current limit protection. Please refer to [https://www.ti.com/lit/snvu874] for further details about the device configuration using the DIP switches.

For a complete evaluation of asynchronous operation, the following tests are performed:

- Efficiency measurements with load current up to 5A.
- Device features such as soft-start (SS), OVP, phase 2 enable (EN2) and bypass mode.
- Load transients from 0.5A to 4.5A.
- Line transients from 14V to 20V.
- Temperature measurements including efficiency measurements at +85ºC and -35ºC, and thermal images with 5A load running for 10 minutes.
- Compensation loop stability measurement with Bode plot.

The above-mentioned tests are run with the following parameters.

Table 2-1. EVM Specification for Asynchronous Mode

Parameter	Condition	MIN	TYP	MAX	UNIT
Input Voltage	Operation		14.4		V
Output Voltage	R_{ATRK} = 40.2kΩ		24		V
	V_{ATRK} = 1.6V		48		V
	V_{ATRK} = 1.2V (OVP)		36		V
Output Power	R_{ATRK} = 40.2kΩ			120	W
	V_{ATRK} = 1.6V			240	W
	V_{ATRK} = 1.2V (OVP)			180	W
Switching Frequency	Operation		400		kHz
Efficiency	V_{IN} = 14.4V, V_{OUT} = 24V, P_{OUT} = 120W		95.1		W
	V_{IN} = 14.4V, V_{OUT} = 48V, P_{OUT} = 240W		92.9		W

The default connection is used (as described in Table 2-2 of (https://www.ti.com/lit/snvu874) for the evaluation module jumpers, with few exceptions for the phase 2 enable test (JP2 is removed) and the compensation loop stability measurement (JP6 is removed). The output voltage can be dynamically set with a voltage source connected to the J8 connector. The device is tested in DEM mode with three different configurations. These configurations are mentioned in [Table 2-2].

Table 2-2. Configuration used for Asynchronous Mode Testing

Configuration	CFG0	CFG1	CFG2	V_{OUT} set via	V_{ATRK}	V_{OUT}	OVP
Resistor	3	10	1	Resistor	n.a.	24V	50V
Analog	11	10	1	ATRK/DTRK	2.0V	48V	50V
OVP test	11	12	2	ATRK/DTRK	1.5V	36V	28.5V

The following test equipment is needed to perform the LM5125 asynchronous mode evaluation [Table 2-3]:

Table 2-3. Equipment Used

Equipment Type	Description
Power supply	Power supply needs to support 20V/20A at least, and generate line transients.
Electronic load	Electronic load needs to sink 250W at 48V at least, and generate load transients.
Digital multimeters	• Voltmeter 1 (V_{IN}): capable of measuring input voltage of 30V. • Voltmeter 2 (V_{OUT}): capable of measuring output voltage of 50V. • Ammeter 1 (I_{IN}): capable of 30A DC measurement. • Ammeter 2 (I_{OUT}): capable of 10A DC measurement.
Oscilloscope	Minimum 200MHz bandwidth.
Temperature cycling system	To simulate +85ºC and -35ºC ambient temperature.
Infra-Red camera	To take IR pictures of the device and check the heat being produced.
Network analyzer	For stability measurements

3 Design Considerations

Typically, in a DC/DC synchronous converter the SWx pin (device pin) and the SW node (inductor terminal) are connected. Also, a 100nF capacitor is connected between HBx pin and SWx pin for bootstrap functionality, i.e. providing a supply for the high-side gate driver which is 5V higher with respect to the SWx pin. In asynchronous mode the 100nF bootstrap capacitor is useless, since there is no high-side FET; therefore, it must be removed. However, in the absence of a bootstrap capacitor, the HBx pin does not have the capability to build 5V with respect to the SWx pin, hence a fault will be triggered inside the device; this fault in turn causes the unnecessary gate driver switching activity.

To avoid this, the HBx pin must be pulled to VCC and SWx pin must be grounded on the evaluation board (Figure 3-1). This verifies that the HBx pin with respect to the SWx pin is always 5V, hence bypassing the fault detector. Since SWx pin being grounded does not allow required voltage switching activity across inductor, the connection between the SWx pin and the switch node must be removed. See Figure 3-1 for the changes on the EVM.

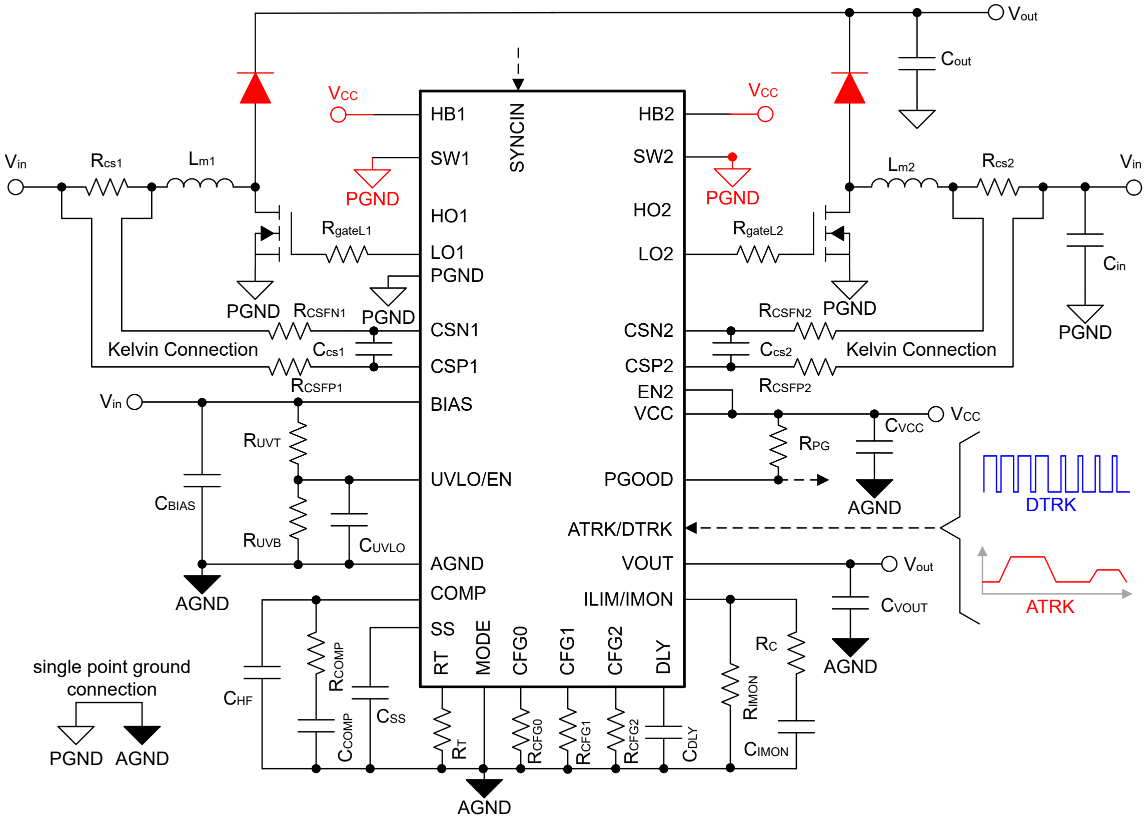


Figure 3-1. Block Diagram of the LM5125 in Asynchronous Mode

4 Test Results

4.1 Efficiency Measurements

Voltage and current measurements at input/output of the device are taken, to measure input/output power respectively and calculate the efficiency of the boost converter. The device is operated in configurations 'Resistor' and 'Analog', with an input voltage of 14.4V and a load ranging from 0.1A to 5A. Figure 4-1 shows the efficiency plot of the two configurations.

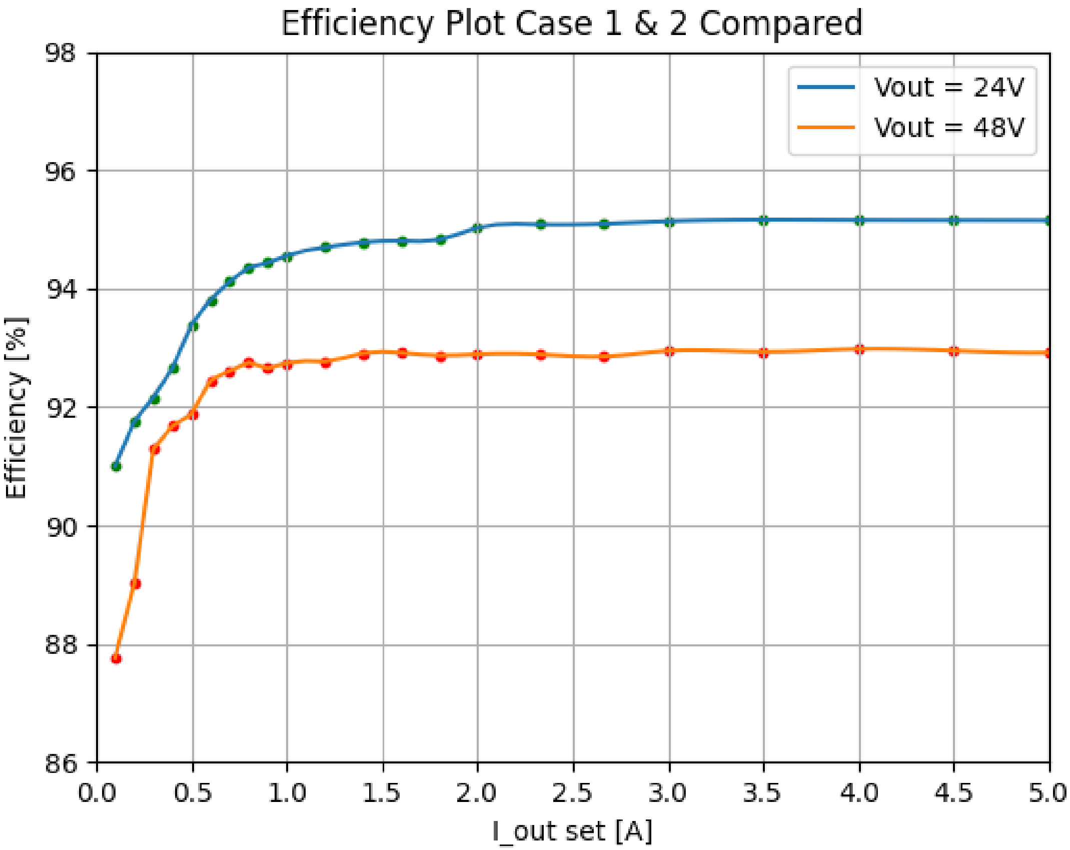


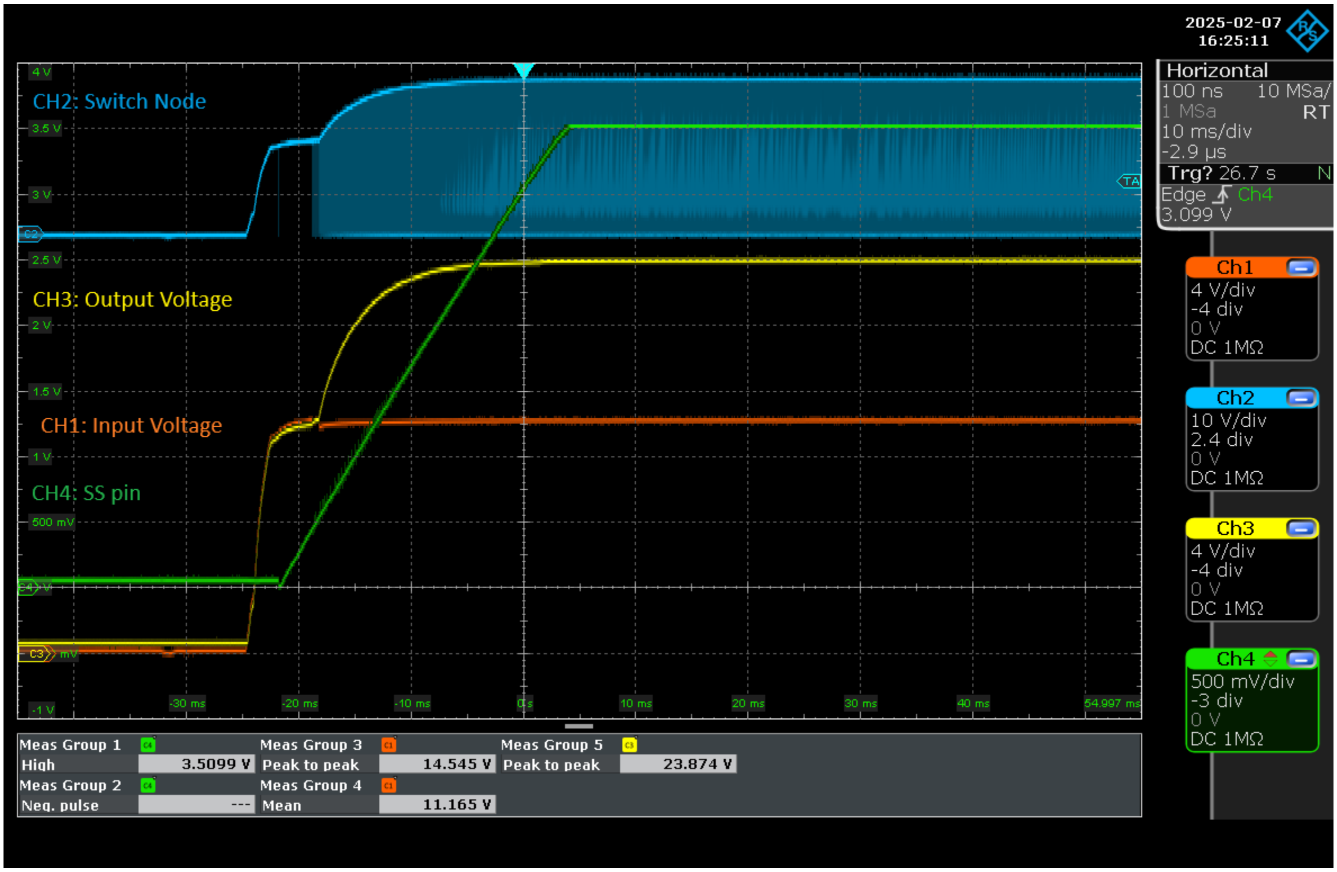
Figure 4-1. Efficiency Plot for V_{OUT} = 24V and V_{OUT} = 48V

In configuration resistors, the efficiency gets up to 95.16% at 5A load current, while in configuration analog, the efficiency goes up to 92.95% at 5A load current. As expected, the converter loses between 2% and 3% in efficiency with respect to synchronous operation (according to the EVM specification mentioned in Table 1-1 of LM5125EVM-BST Evaluation Module), due to the diode having higher conduction losses than the transistor. Higher output voltage means higher duty cycle for the low-side FET, which adds more switching loss to the total converter losses, and as a result, the efficiency is lower for configuration *analog* (V_{OUT} = 48V).

4.2 Device Features

4.2.1 Soft-Start (SS)

Even if the SS behavior is, in theory, not affected by the asynchronous operation, it is still good practice to check whether the device is starting up properly. Start-Up Behavior and Soft-Start Pin shows a snapshot of the signal on the SS pin. As is visible, the output voltage (in yellow) first follows the input (in orange), and then ramps up to the desired output (24V in this case). On the top of the picture (in blue), the switch node of the converter is visible.



Horizontal
100 ns 10 MSa/
1 MSa RT
10 ms/div
-2.9 µs
Trg? 26.7 s N
Edge Ch4
3.099 V

Ch1
4 V/div
-4 div
0 V
DC 1MΩ

Ch2
10 V/div
2.4 div
0 V
DC 1MΩ

Ch3
4 V/div
-4 div
0 V
DC 1MΩ

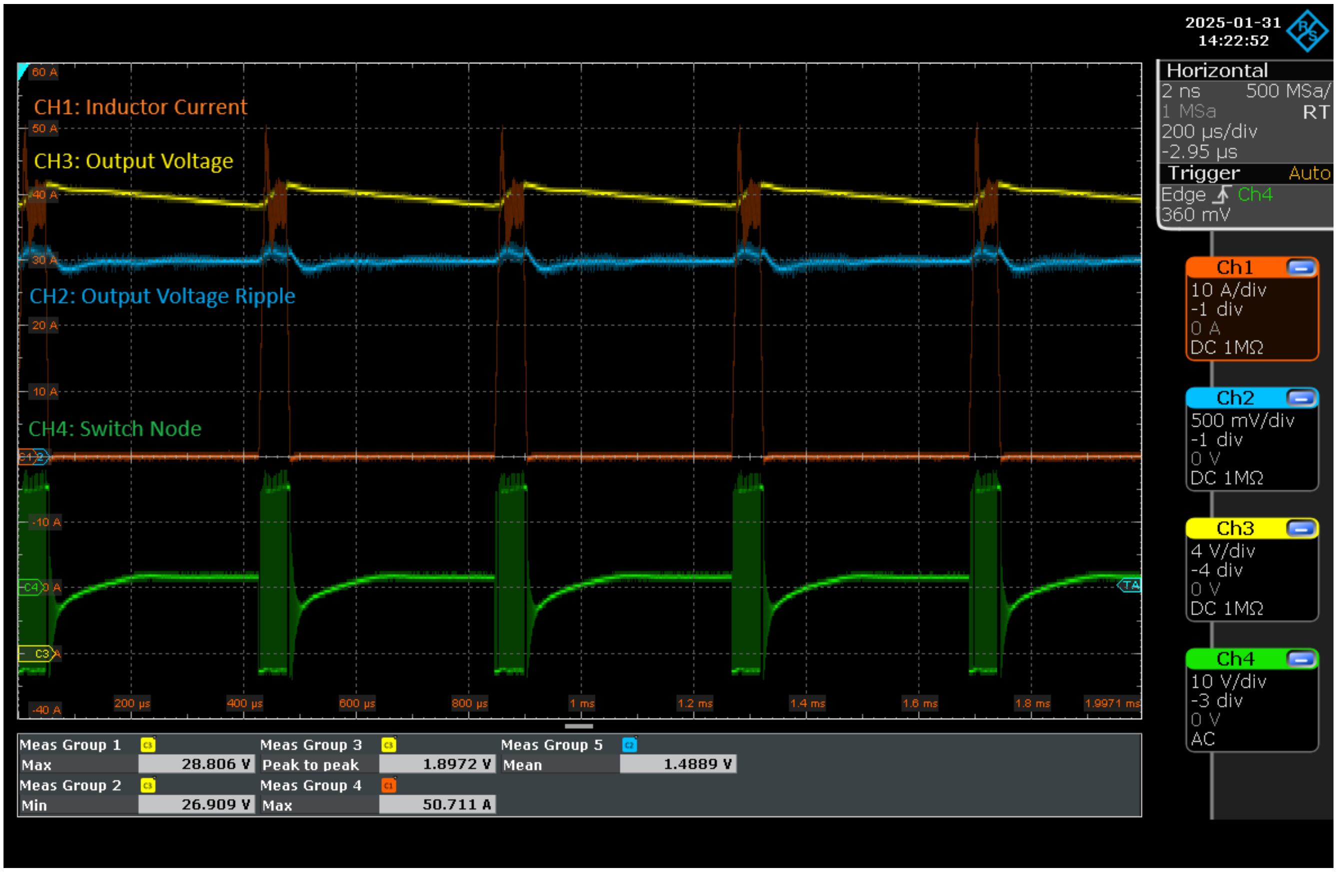
Ch4
500 mV/div
-3 div
0 V
DC 1MΩ

Meas Group 1	C4	Meas Group 3	C1	Meas Group 5	C3
High	3.5099 V	Peak to peak	14.545 V	Peak to peak	23.874 V
Meas Group 2	C4	Meas Group 4	C1		
Neg. pulse	---	Mean	11.165 V		

Figure 4-2. Start-Up Behavior and Soft-Start Pin

4.2.2 Over-Voltage Protection (OVP)

To test OVP, the device is operated in Config 'OVP test' (CFG0 = 11, CFG1 = 12, CFG2 = 2), changing the OVP level to 28.5V (OVP bits equal to [11]) and setting the target output voltage beyond that threshold (36V in this case). The result is visible in Figure 4-3. The device starts switching (green waveform), trying to reach the intended output voltage (waveform in yellow), but as soon as the device hits the OVP threshold, the device stops switching; the output voltage then starts to decrease until the device falls below the OVP level, and the same cycle repeats. How fast the output voltage decreases below OVP level depends on the load current. Here, a 3A load was used for the test.



Horizontal
2 ns 500 MSa/
1 MSa RT
200 µs/div
-2.95 µs
Trigger Auto
Edge Ch4
360 mV

Ch1
10 A/div
-1 div
0 A
DC 1MΩ

Ch2
500 mV/div
-1 div
0 V
DC 1MΩ

Ch3
4 V/div
-4 div
0 V
DC 1MΩ

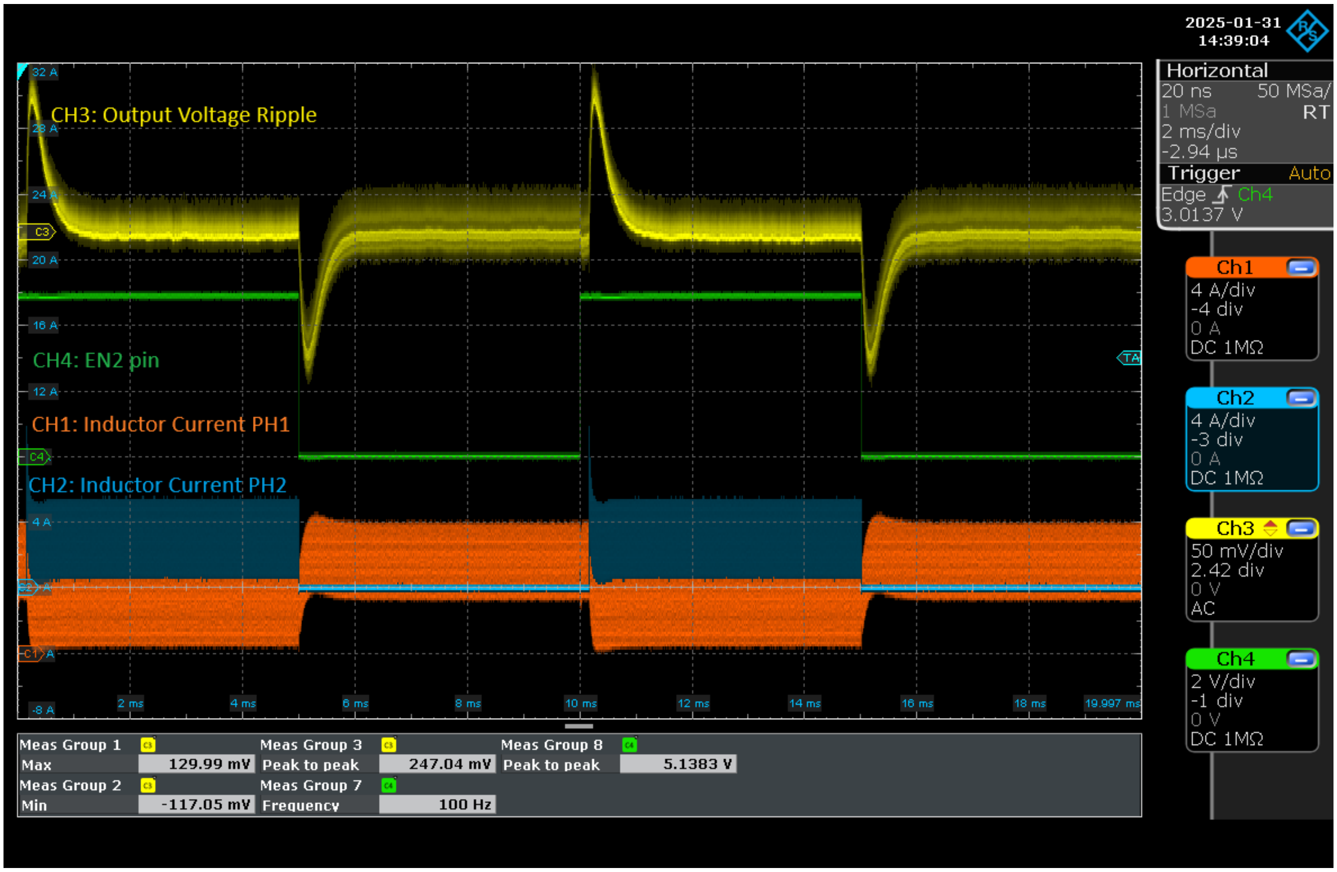
Ch4
10 V/div
-3 div
0 V
AC

Meas Group 1		Meas Group 3		Meas Group 5	
Max	28.806 V	Peak to peak	1.8972 V	Mean	1.4889 V
Meas Group 2		Meas Group 4			
Min	26.909 V	Max	50.711 A		

Figure 4-3. Over-voltage Protection Behavior

4.2.3 Second phase enable (EN2)

A square wave with 100Hz frequency was applied to the EN2 pin, to repeatedly turn on and off the second phase and see how the device behaves. As shown in Figure 4-4, the inductor currents (in orange and blue, respectively) flow according to the EN2 signal (in green). The output voltage (in yellow) shows over/undershoot of acceptable magnitude (hundreds of millivolt) with a fast recovery. The load current used for this test is 3A.



Meas Group 1	C3	Meas Group 3	C3	Meas Group 8	C4
Max	129.99 mV	Peak to peak	247.04 mV	Peak to peak	5.1383 V
Meas Group 2	C3	Meas Group 7	C4		
Min	-117.05 mV	Frequency	100 Hz		

Figure 4-4. Turning on and Off of Phase 2

4.2.4 Bypass mode

Bypass mode is triggered whenever the input voltage rises above the output voltage. Interesting to note here, as shown in Figure 4-5, is that as soon as this happens the device stops switching (waveform in blue). The output follows the input voltage (yellow and green, respectively), minus the diode voltage drop.

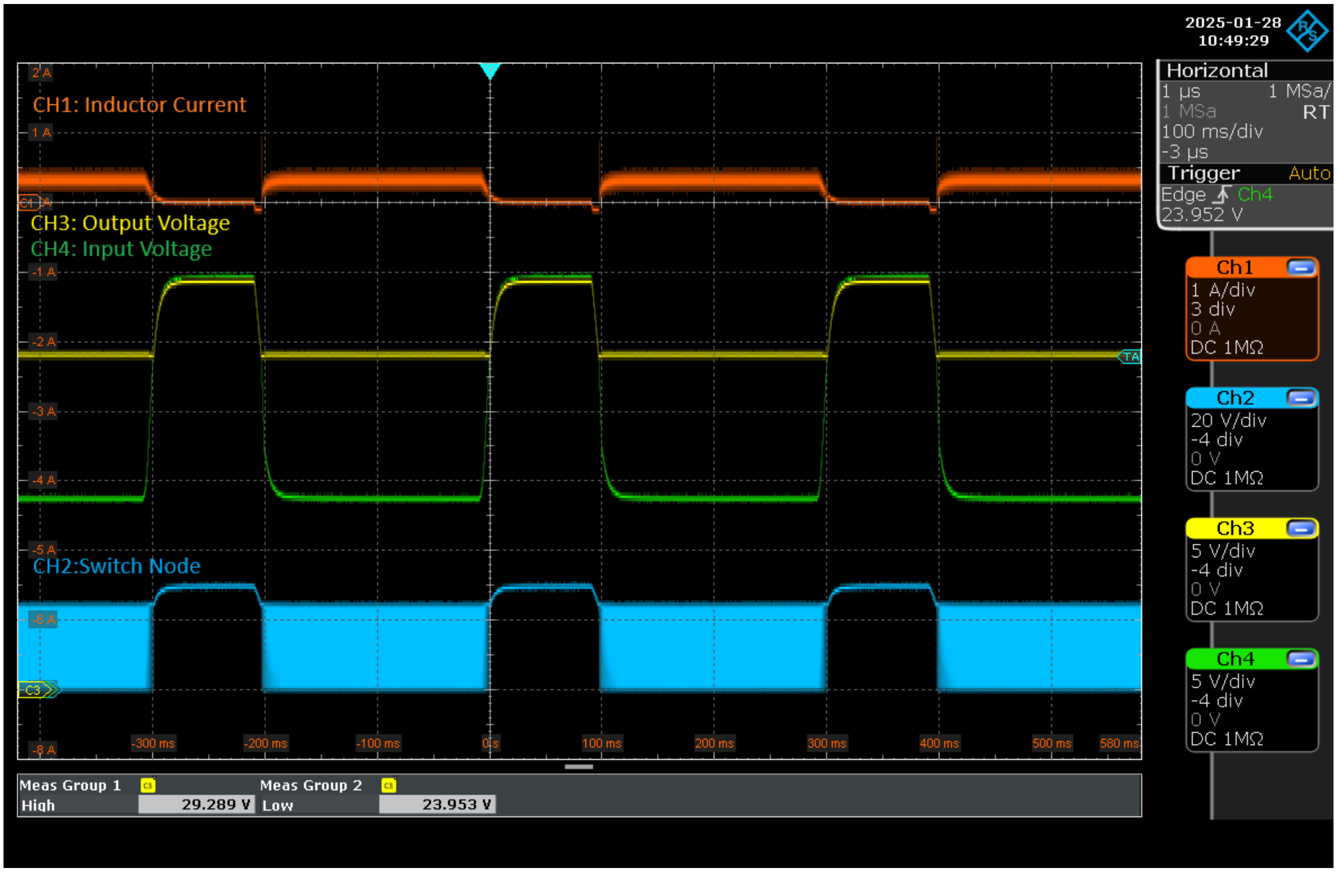
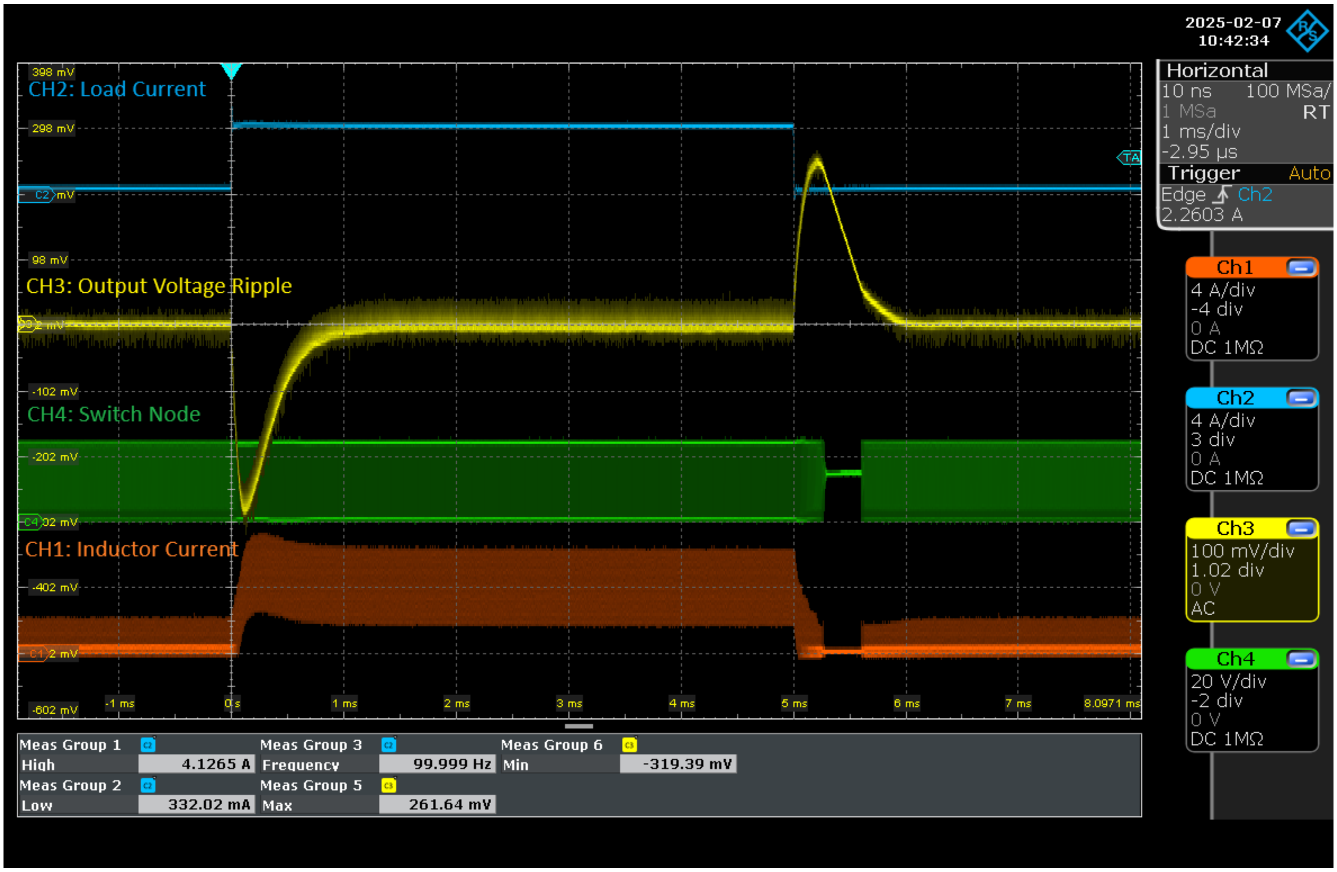


Figure 4-5. Bypass mode behavior

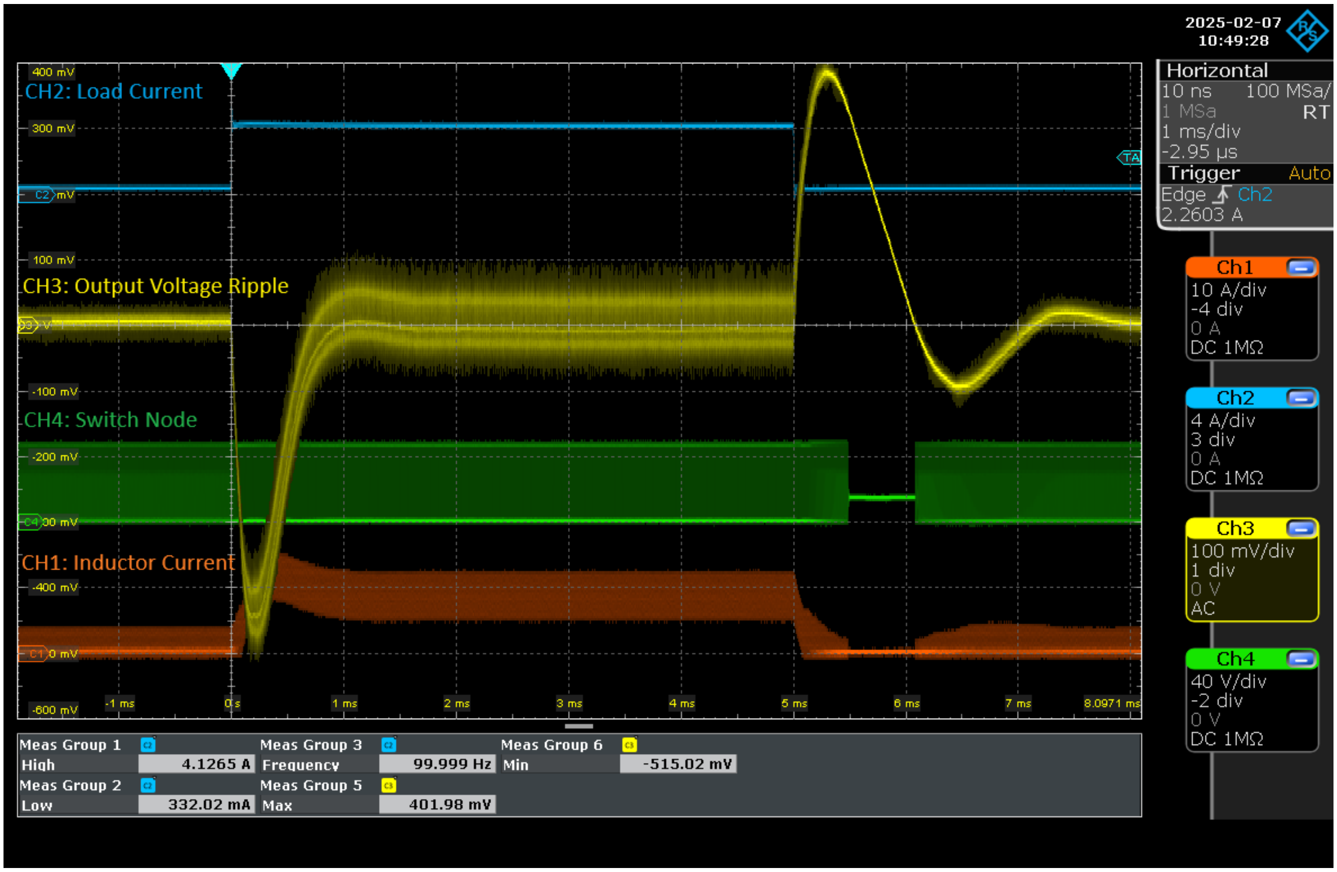
4.3 Load Transient

To check the robustness of the device with respect to changes on the load, a load step between 0.5A and 4.5A is applied at the output, with 100Hz frequency, both in configurations *Resistor* and *Analog*. From Figure 4-6 and Figure 4-7, the device takes just 1ms to recover, with overshoot and undershoot of maximum 1.4% in *Resistor* and 1.1% in *Analog* configuration. One interesting thing to note on both images is that the device stops switching (and inductor current goes to zero) as soon as the output voltage increases beyond the set value because of the overshoot. When the output value falls again below this threshold, the device resumes normal operation.



Meas Group 1
High 4.1265 A
Meas Group 2
Low 332.02 mA
Meas Group 3
Frequency 99.999 Hz
Meas Group 5
Max 261.64 mV
Meas Group 6
Min -319.39 mV

Figure 4-6. Load Transient for Configuration Resistor (24Vout)



Horizontal
10 ns 100 MSa/
1 MSa RT
1 ms/div
-2.95 µs
Trigger Auto
Edge Ch2
2.2603 A

Ch1
10 A/div
-4 div
0 A
DC 1MΩ

Ch2
4 A/div
3 div
0 A
DC 1MΩ

Ch3
100 mV/div
1 div
0 V
AC

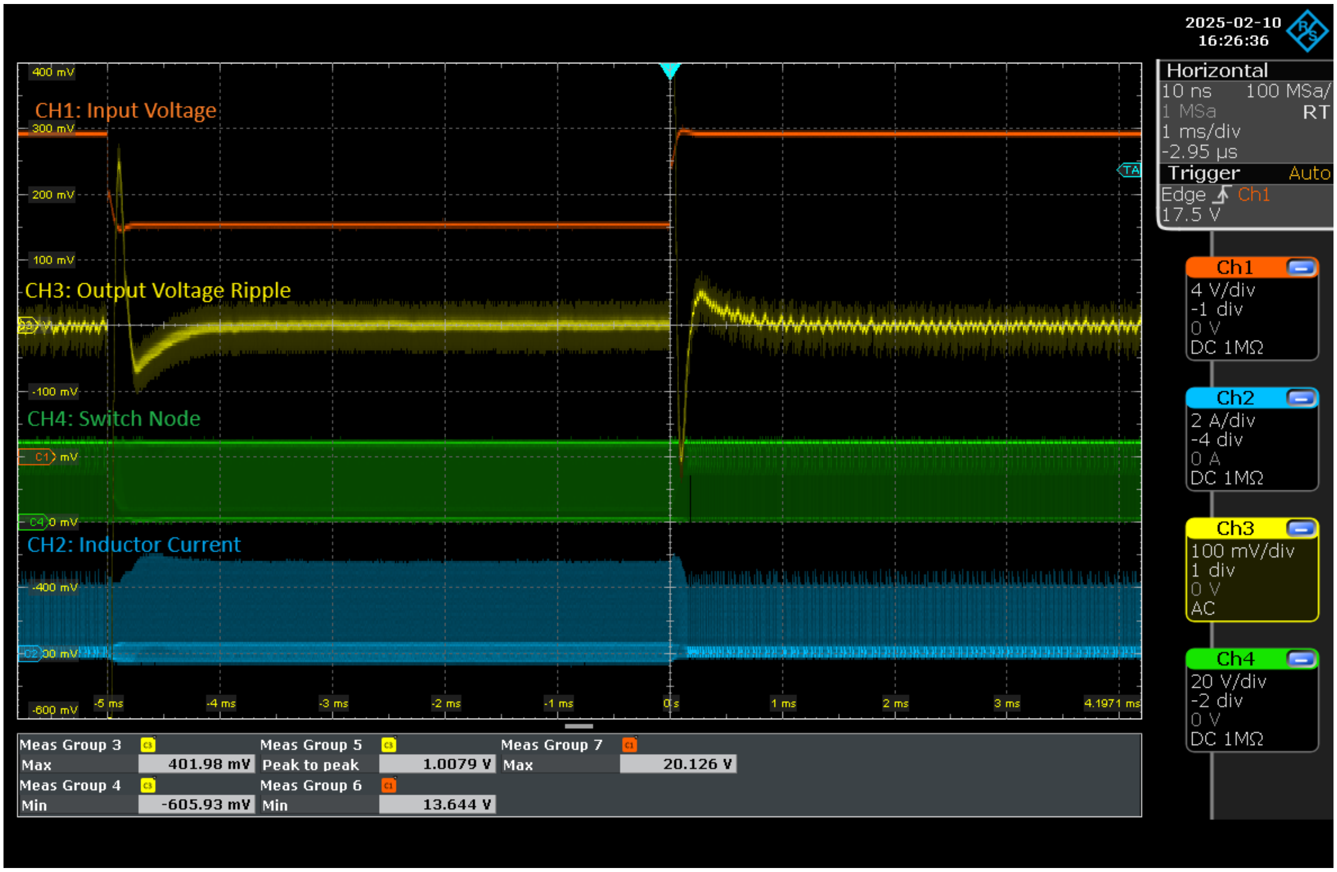
Ch4
40 V/div
-2 div
0 V
DC 1MΩ

Meas Group 1
High 4.1265 A
Meas Group 2
Low 332.02 mA
Meas Group 3
Frequency 99.999 Hz
Meas Group 5
Max 401.98 mV
Meas Group 6
Min -515.02 mV

Figure 4-7. Load Transient for Configuration Analog (48Vout)

4.4 Line Transient

Voltage transients were applied to input as well to check the robustness of the converter with respect to line disturbances: a line step between 14V and 20V is applied, and the output voltage ripple is observed. Results are shown in Figure 4-8 and Figure 4-9 for configurations 'Resistor' and 'Analog', respectively. The compensation loop used leads to a phase margin of 68º, which makes the device stable. Compared to the load transient analysis, the overshoot is causing the device to stop switching for a shorter time interval here (tens of µs), while the overshoot magnitude is comparable if not greater: this is because of how fast the device is in regulating the output voltage, this time interval is shorter than the propagation along the signal path that senses the output voltage and goes through the FB pin.



Meas Group 3		Meas Group 5		Meas Group 7	
Max	401.98 mV	Peak to peak	1.0079 V	Max	20.126 V
Meas Group 4		**Meas Group 6**			
Min	-605.93 mV	Min	13.644 V		

Figure 4-8. Line Transient for Configuration Resistor (24Vout)

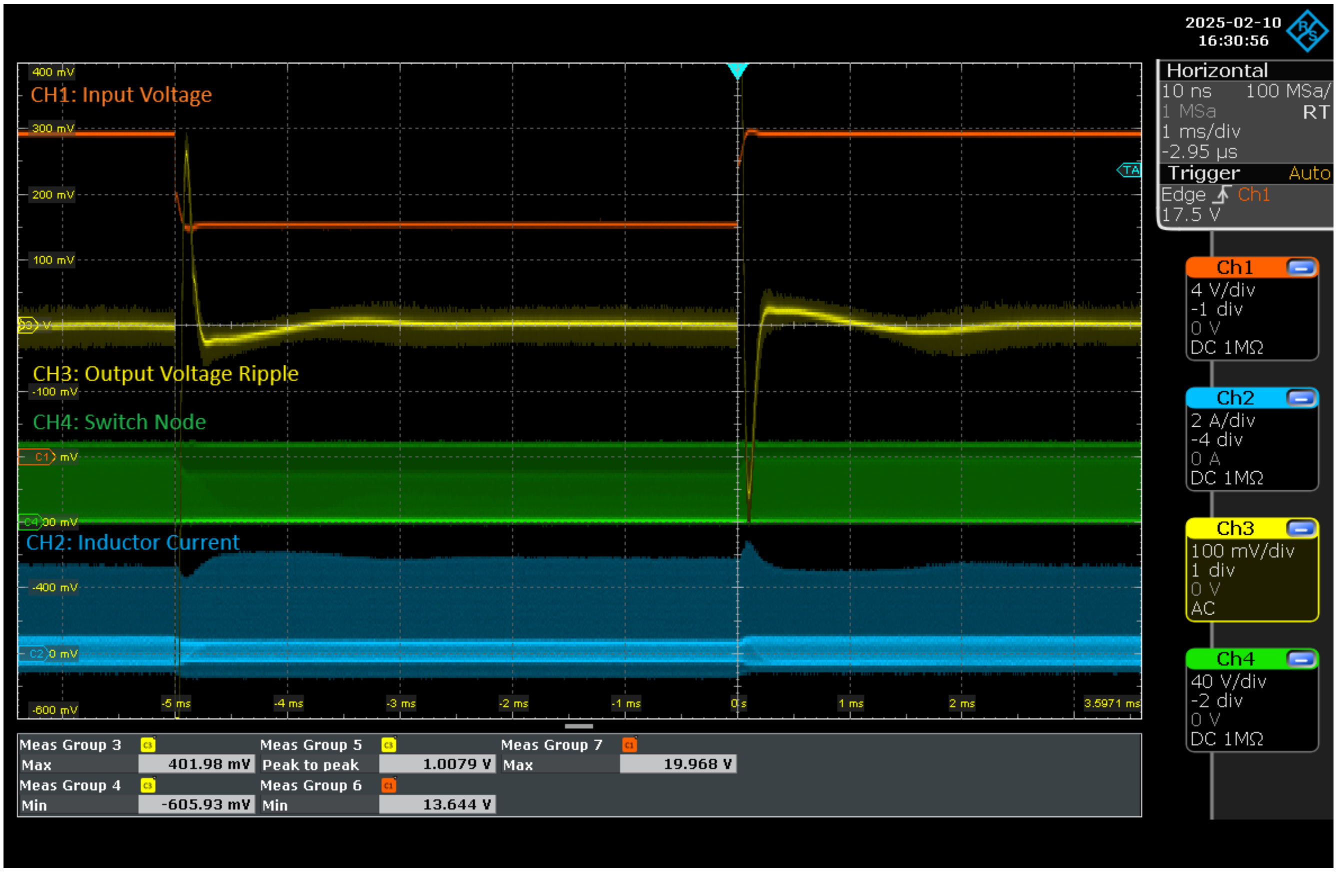


Figure 4-9. Line Transient for Configuration Analog (48Vout)

4.5 Temperature Measurements

Efficiency measurements are repeated at different temperatures than +25ºC ambient temperature, namely +85ºC and -35ºC. Results for configurations 'Resistor' and 'Analog' are shown in Figure 4-10 and Figure 4-11, respectively. As expected, the overall efficiency at higher temperatures gets worse, while the efficiency at lower temperatures is comparable to the efficiency at ambient temperature.

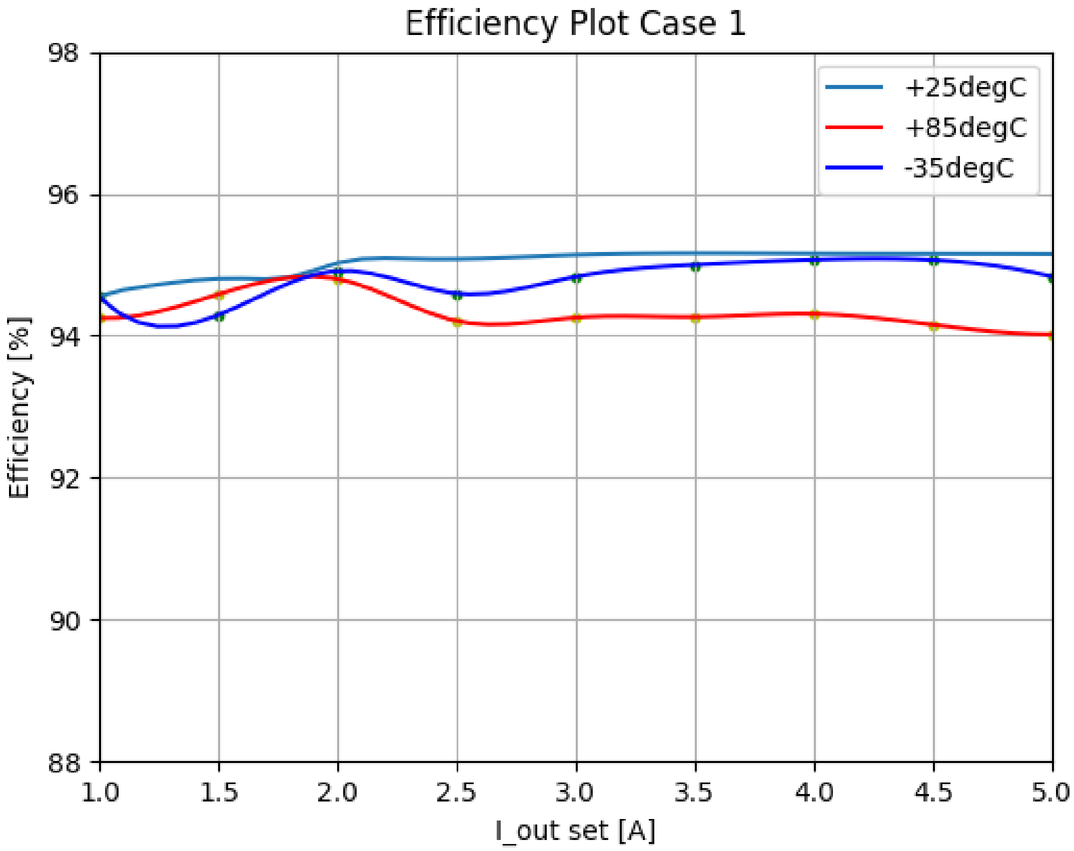


Figure 4-10. Efficiency Plot Configuration Resistor at Different Temperatures than Ambient

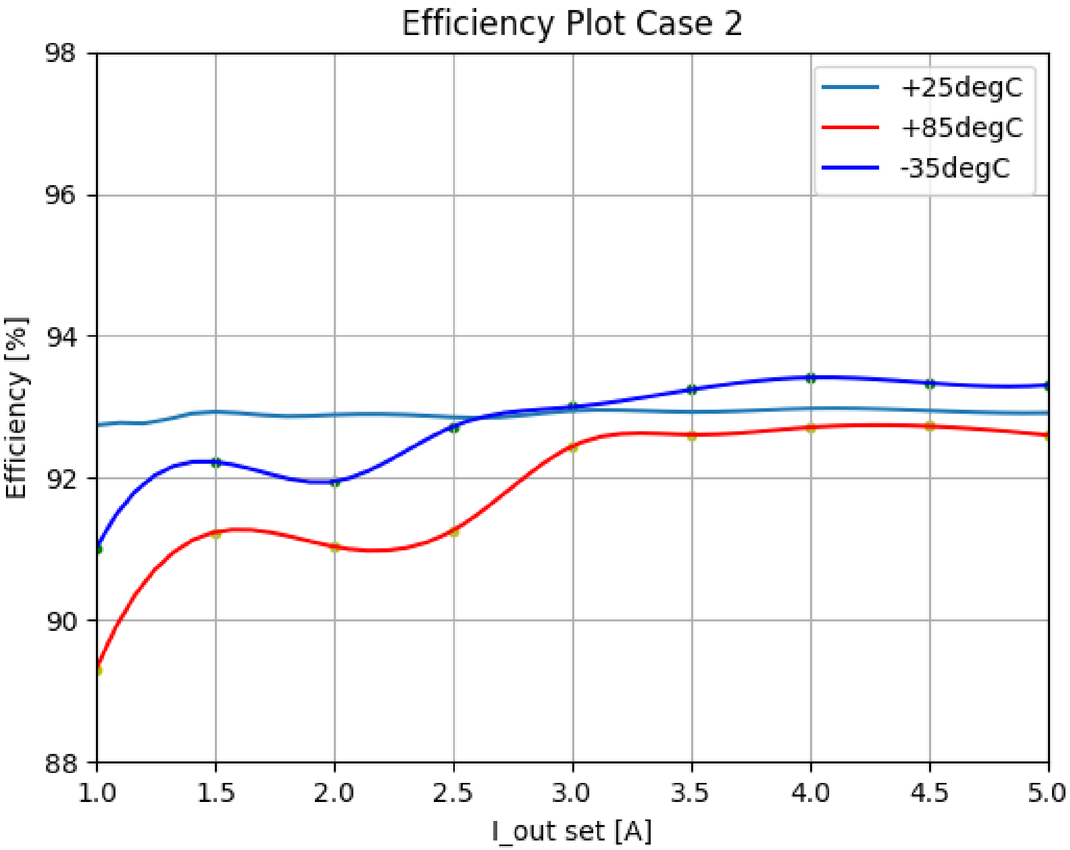


Figure 4-11. Efficiency Plot Configuration Analog at Different Temperatures than Ambient

In order to check heat dissipation of the board, the device is left running with 5A load for 10 minutes, and infra-red pictures of the evaluation board are taken, in both configurations 'Resistor' and 'Analog'. The infra-red shots are shown in Figure 4-12 and Figure 4-13. Note how at lower output power (configuration 'Resistor') the diodes are getting hotter than the low-side FETs (because of higher conduction losses), while it is the other way around in the second case (when the output voltage is higher), as the duty cycle increases and the low-side FETs stay on for longer (hence having higher conduction losses than the diodes). Overall, as you can see from the images, the heat production is mostly coming from the diodes and the low-side FETs, while the IC is always in the yellow to orange area.

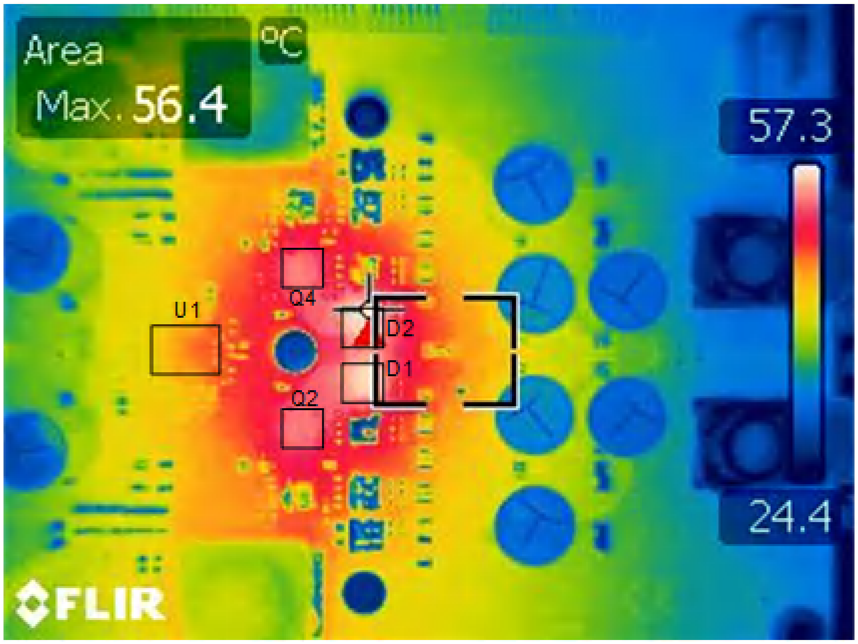


Figure 4-12. EVM Heat Dissipation in Configuration Resistor

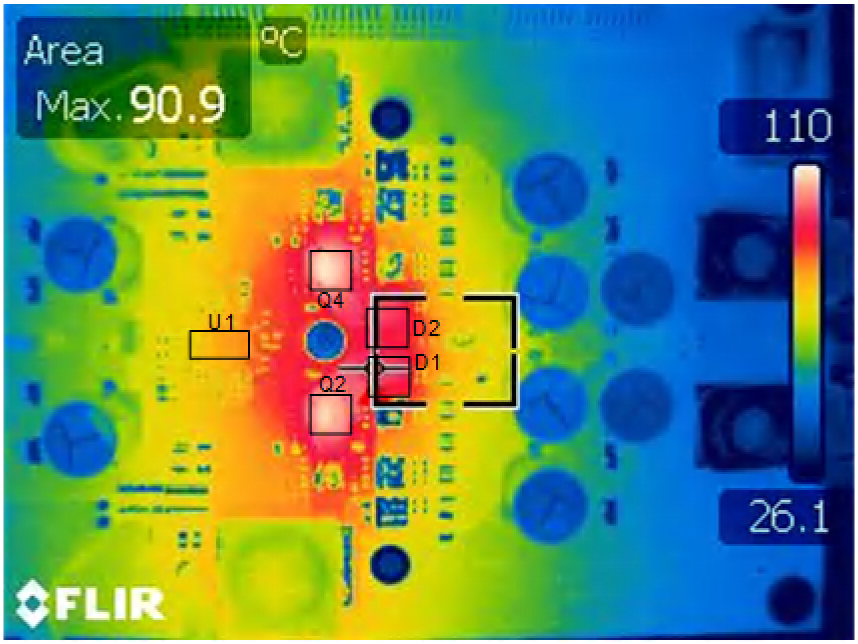
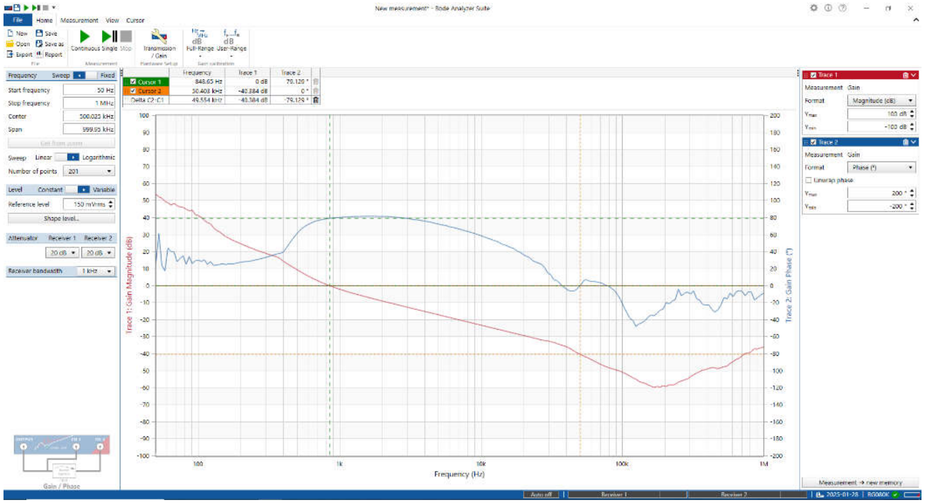


Figure 4-13. EVM Heat Dissipation in Configuration Analog

4.6 Bode Plot

Even if stability is indirectly checked with the load and line transients, another look at the stability of the compensation loop can be given with the Bode plot shown in Figure 4-14. This clearly shows how the device phase is roughly 80º above zero at the cutoff frequency (almost 1kHz), which confirms that the device is stable (the phase margin is higher than the mostly recommended value of 60º).



	Frequency	Trace 1	Trace 2
☑ Cursor 1	848.65 Hz	0 dB	79.129 °
☑ Cursor 2	50.403 kHz	-40.384 dB	0 °
Delta C2-C1	49.554 kHz	-40.384 dB	-79.129 °

Frequency: Sweep
Start frequency: 50 Hz
Stop frequency: 1 MHz
Center: 500.025 kHz
Span: 999.95 kHz
Sweep: Logarithmic
Number of points: 201
Level: Variable
Reference level: 150 mVrms
Attenuator: Receiver 1: 20 dB; Receiver 2: 20 dB
Receiver bandwidth: 1 kHz

Trace 1
Measurement: Gain
Format: Magnitude (dB)
Ymax: 100 dB
Ymin: -100 dB

Trace 2
Measurement: Gain
Format: Phase (°)
☐ Unwrap phase
Ymax: 200 °
Ymin: -200 °

Figure 4-14. Bode Plot in Asynchronous Mode in Configuration Resistor

5 Summary

As shown in the above images and scope plots, the LM5125x works properly in asynchronous mode. Nevertheless, some drawbacks have to be considered: even if overall BOM will be lower by replacing the high-side FET with a diode and removing the bootstrap capacitor, but the converter have a 2 to 3% lower efficiency (because of higher conduction losses of the diodes with respect to a transistors) and will therefore have higher heat dissipation at the same output voltage. With that being said, in order to make the LM5125x working in asynchronous mode, the evaluation module can be reworked to build the 5V step required between HBx and SWx pins to correctly operate the high-side driver (even if the HO1/HO2 pins are left floating).

6 References

1. https://www.ti.com/lit/ds/symlink/lm5125-q1.pdf
2. https://www.ti.com/lit/snvu874
3. https://www.ti.com/lit/ds/symlink/lm5125a-q1.pdf

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