Application Note

Comparative Waveform Study of TXB0604 and Competing Level Shifters

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ABSTRACT

High-throughput is essential for data-center communications, especially in serial interfaces such as Quad-SPI (single-ended, half-duplex, six channel bus). To verify good signal integrity and maximum bandwidth support, system designers must keep host/ target devices in proximity, though it is not always feasible to do so. If such systems require driving these signals over long traces/ connector lengths, it is recommended to use the TXB0604 or TXB0606 to compensate for the bandwidth loss from the added line capacitance, allowing swift QSPI flash updates. This application note evaluates the performance of leading design TXB0604 in the market today in a typical bench setup across three common setups.

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1 Introduction

This app note is an extension of Overcoming TXB-Type Translators Design Challenges, and addresses design challenges specific to the TXB-type translators (TXB010x, TXB030x, TXB060x). While all three devices resolve mismatched operating voltages for bidirectional data signals, the TXB0604/ TXB0606 is unique in that the device also helps designers mitigate noise and bandwidth limitations caused by transmission-line effects. In this application note, the capabilities of the TXB0604 and TXB0606 is demonstrated through a bench setup of the 4-channel equivalent, accompanied by waveforms from the leading devices of today. This industry-leading design enables designers to achieve higher throughput even when faced with moderate to severe capacitive-load buses, conditions that were previously thought not preferred for legacy or competitive designs. For the background use case of the TXB0604/ TXB0606 and examples of where it can be applied, see From Bottleneck to Breakthrough: QSPI Optimization in Data Centers with TXB0604/TXB0606.

For a list of recommended level-translation devices for common interface types, visit TI's Voltage Translators and Level Shifters page.

2 How Does the TXB0604 Compare to Legacy and Existing Market Solutions?

Both device architectures share similar push-pull buffer based output structures with dampening resistors to weakly drive the logic state to the appropriate DC level. During a transition of logic signal (AC state), the one-shots circuitry are activated momentarily providing a fast slew rate to achieve higher data rates. Table 2-1 depicts the characteristics of the differences in the TXB010x and TXB060x against competition.

Table 2-1. Specs Overview of TXB-Type Translators

	Device		
Spec	**TXB060x**	**TXB010x**	**Competitor**
V_{CCA}	0.9V- 2V	1.2V- 3.6V	0.9V- 2V
V_{CCB}	1.65V- 3.6V	1.65V- 5.5V	1.65V- 3.6V
Max Data Rate (Output Cload =15pF)	180Mbps	100Mbps	140Mbps
Max Data Rate (Output Cload =100pF)	132Mbps	Not Characterized	60Mbps
Max Data Rate (Output Cload =50pF + 20 in. trace)	128Mbps	Not Characterized	Not Specified
Input Architecture	Schmitt-Trigger Based	CMOS	CMOS
Power Supply Restrictions	-	$V_{CCA} \leq V_{CCB}$	-
I_{OFF} (Partial Power Down Leakage)	4uA	2uA	30uA
$I_{CCA} + I_{CCB}$	18uA	10uA	36uA
Internal Series Resistors	1kΩ	4kΩ	1kΩ
One-Shot Impedance (Typ.)	22Ω (V_{CCO}= 0.9V-3.6V)	• 70Ω (V_{CCO}= 1.2V- 1.8V) • 50Ω (V_{CCO}= 1.8V- 3.3V) • 40Ω (V_{CCO}= 3.3V-5V)	-
Input Driver Requirements	Drive Strength: ±3mA	Drive Strength: ±2mA	Drive Strength: ±3mA
Operating Temperature	-40C to 125°C	-40C to 85C	-40C to 85C
Pin to Pin?	Y	Y	Y
Supported Channel Variations	4,6	1,2,4,6,8	-

- For more information regarding TXB translators, see *A Guide to Voltage Translation With TXB-Type Translators* and the devices' respective datasheets.

2.1 Recommended Device Selection

While both TXB0104 and TXB0604 can be used for push-pull auto-bidirectional signal applications, the following are specific cases where one can be recommended over the other:

The TXB0604 is designed for applications with the following:

- Symmetrical power supplies (V_{CCA} ≤ or ≥ V_{CCB})
- I/Os operating between 0.9V and 3.6V
- High data bandwidth desired up to 100pF output load
- Moderate to heavy lumped, and distributed capacitive loads at the outputs, <20in. of connector lengths
- Slow or noisy input signals

The TXB0104 is recommended for applications with the following:

- I/Os operating between 1.2V and 5.5V
- Data rates up to 100Mbps
- Short trace lengths/ minimum capacitive loading

3 Case Study

A typical bench setup is emulated to cover three different loading scenarios:

- Light Capacitance; 15pF is added to the output of the Device Under Test (DUT)
- Heavy Capacitance; 100pF is added to the output of the DUT
- Distriubted Capacitance; 20in. Of Cabling length + 50pF is added to the output of the DUT

For each configuration, a block diagram of the setup is provided as a reference, and the corresponding performance compared with competitors and legacy counterparts is presented. The three situations are tested at room temperature (25°C) over two voltage ranges: 1.2V → 1.8V and 1.8V → 3.3V.

3.1 Performance with Light Capacitive Loads

The first test assesses each device's peak performance with a minimal capacitive load. By limiting the output load to only 15 pF, the user can measure the typical maximum capability of each translator. See Figure 3-1 for the test setup.

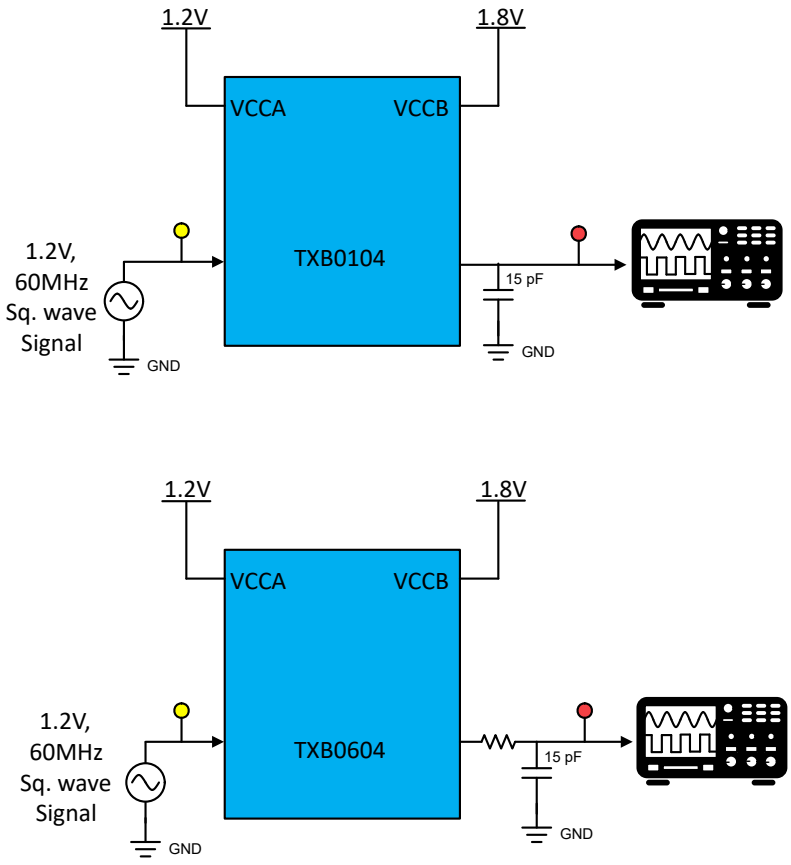

Figure 3-1. Light Capacitive Load Bench Setup, 1.2V to 1.8V

Figure 3-2. TXB0104, 1.2V to 1.8V, Output Cload = 15pF, 60MHz

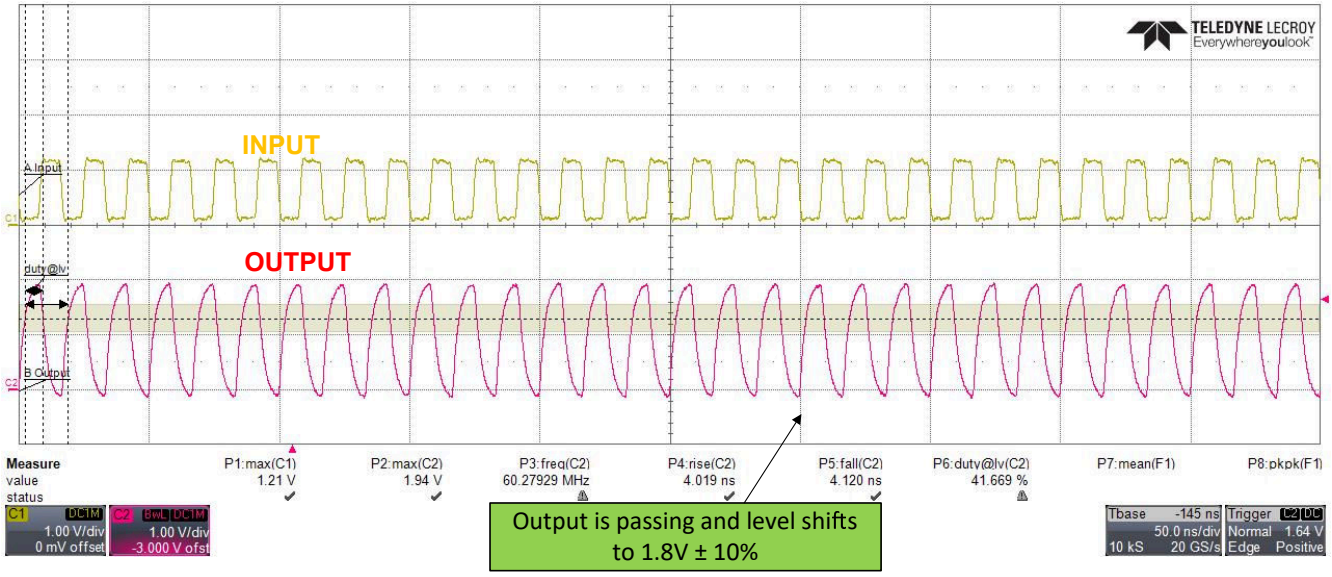

Figure 3-3. TXB0604, 1.2V to 1.8V, Output Cload = 15pF, 60MHz

With both devices provided the same input signal, the TXB0104 (Figure 3-2) is unable to support the 60MHz / 120Mbps signal—data bits are skipped because the signal exceeds the maximum supported data rate of the device. The TXB0604, however, can handle the 60MHz signal without issue. At higher VCC, the TXB0604 is able to achieve 80MHz+ as shown in the setup and waveform.

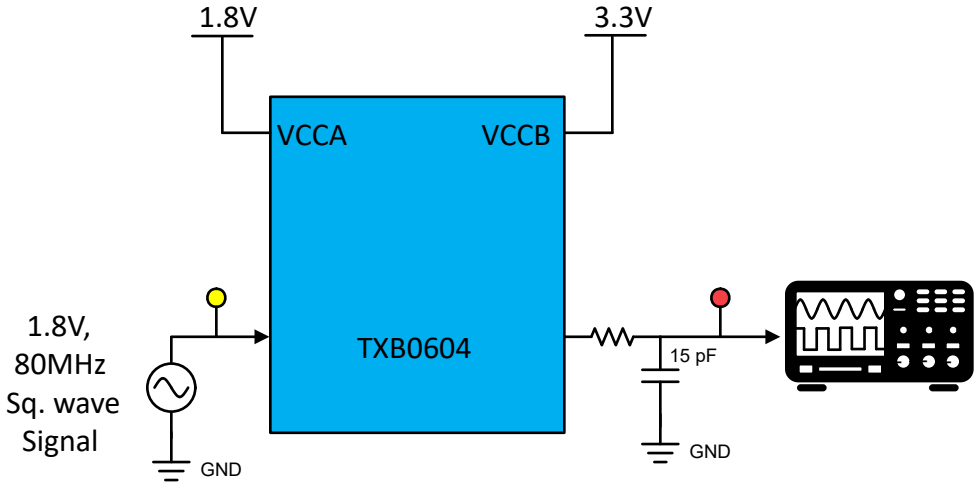

Figure 3-4. Light Capacitive Load Bench Setup, 1.8V to 3.3V

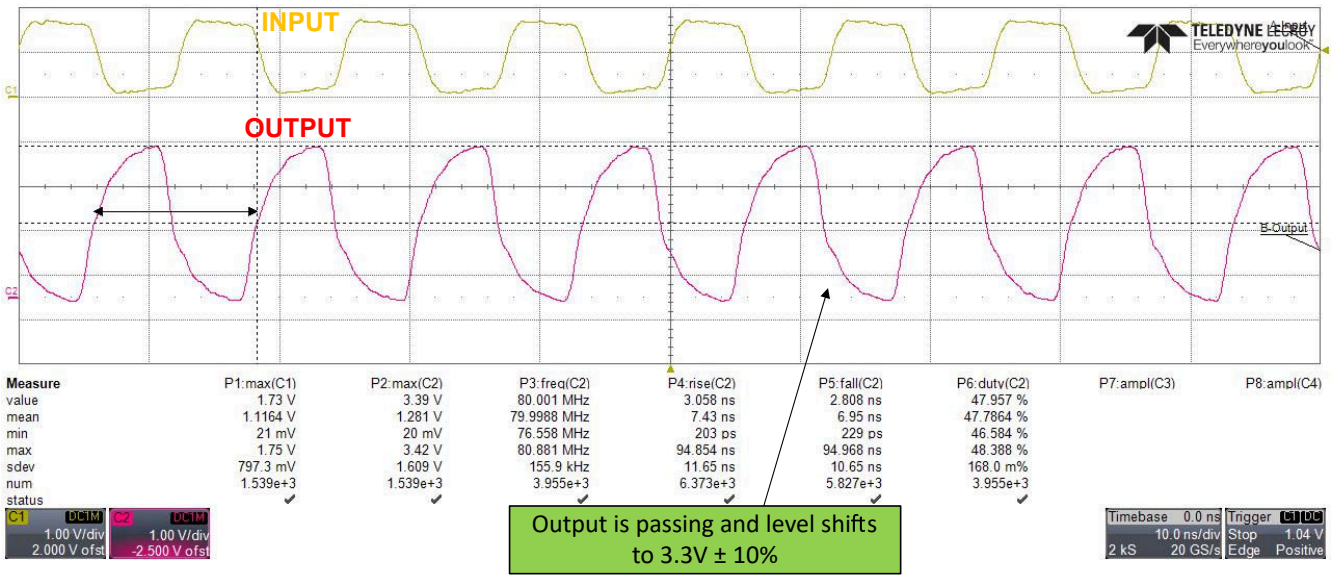

Figure 3-5. TXB0604, 1.8V to 3.3V, Output Cload = 15pF, 80MHz

The waveform above captures the signal integrity of the TXB0604 operating at a high data rate under a small capacitive loading condition.

3.2 Performance with Heavy Capacitive Loads

In the second set of tests, the signal integrity is analyzed with the DUTs operating under a heavy capacitive load. Both the 1.2V-> 1.8V and 1.8V to 3.3V voltage corners are evaluated.

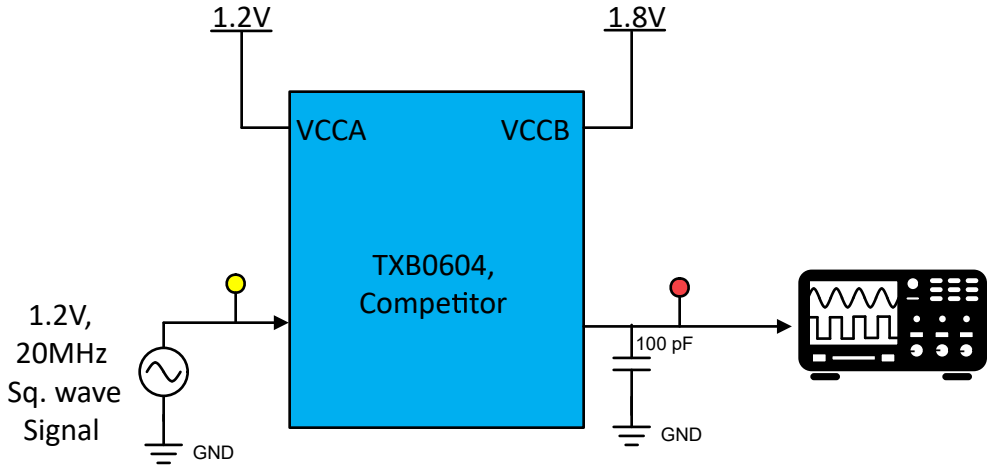

Figure 3-6. Heavy Capacitive Load Bench Setup, 1.2V to 1.8V

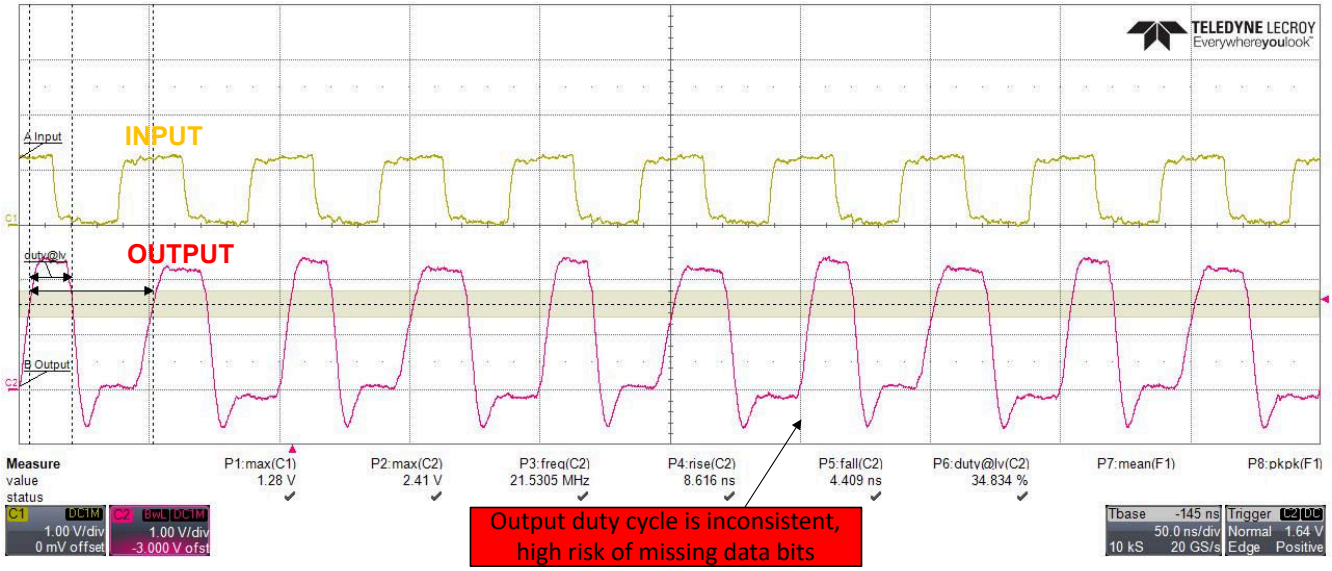

Figure 3-7. Competitor, 1.2V to 1.8V, Output Cload = 100pF, 20MHz

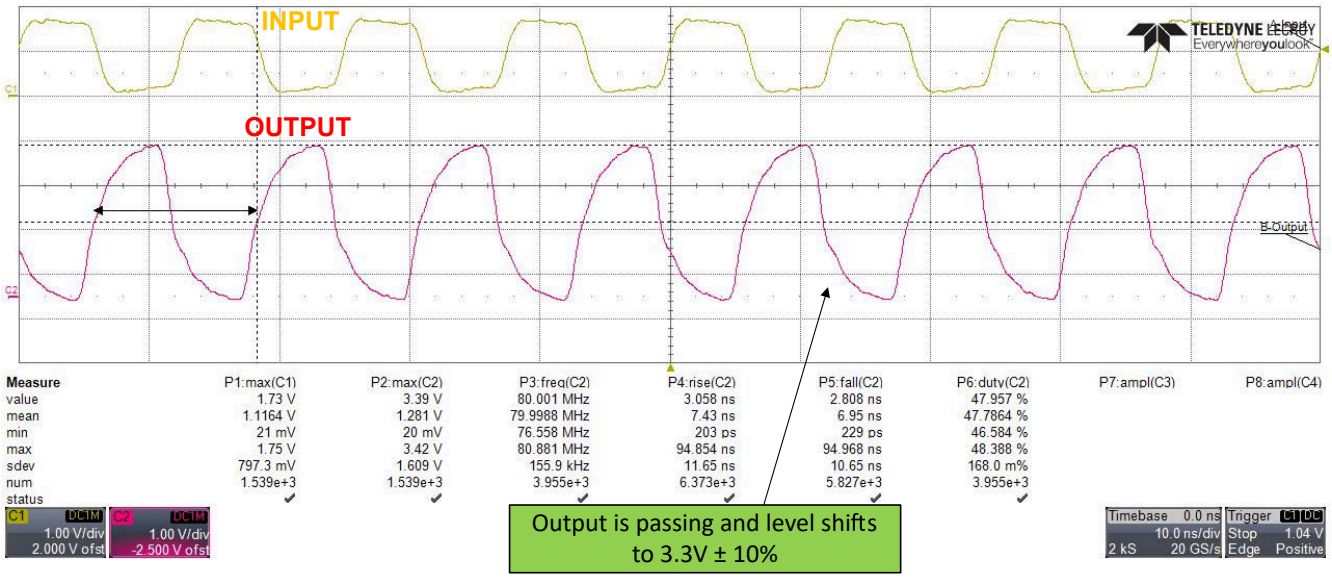

Figure 3-8. TXB0604, 1.2V to 1.8V, Output Cload = 100pF, 20MHz

Observe that the output signal of the competitor (Figure 3-7) is inconsistent with the logic hold times during an input high state (the output duty cycle time varies and drops to 35%). This increases the risk of a missed data bit leading to failed communication. The TXB0604 however, is able to pass 20MHz with cleaner signal integrity.

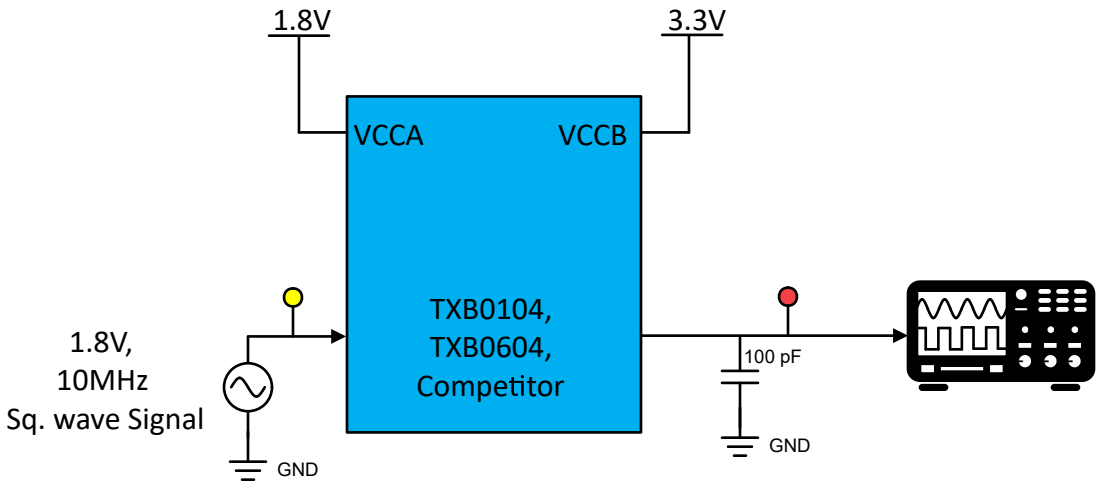

Figure 3-9. Heavy Lumped Capacitive Load Bench Setup, 1.8V to 3.3V

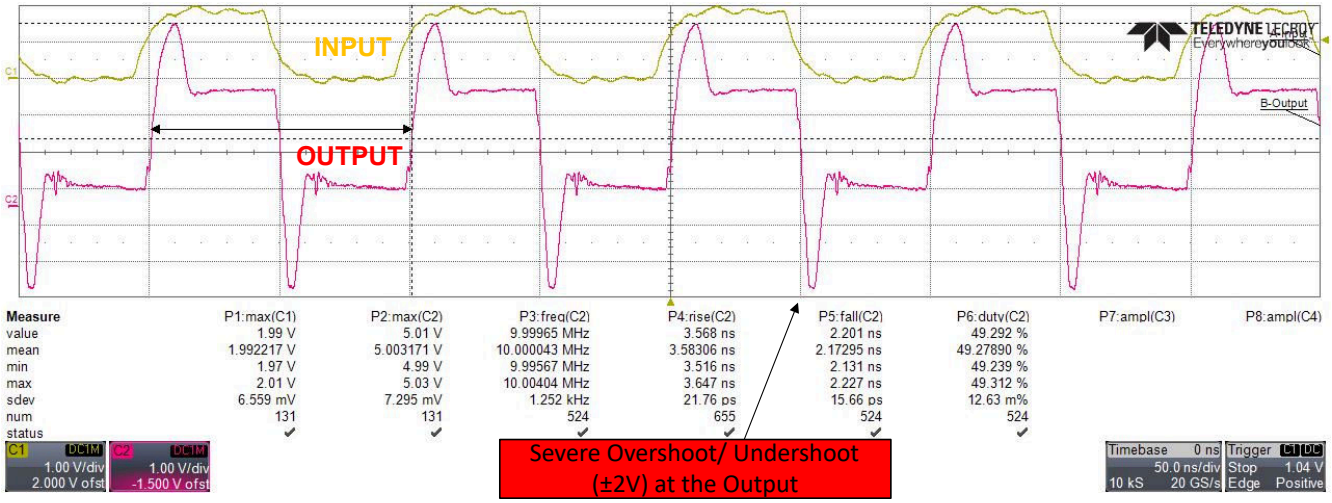

Figure 3-10. Competitor, 1.8V to 3.3V, Output Cload = 100pF , 10MHz

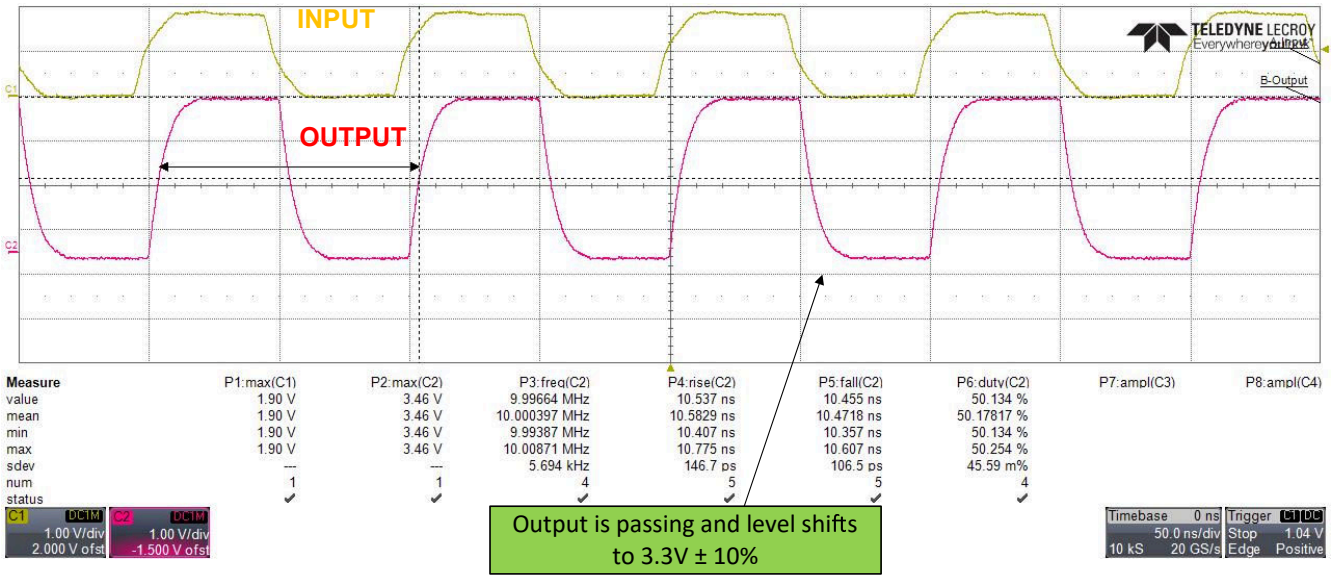

Figure 3-11. TXB0604, 1.8V to 3.3V, Output Cload = 100pF , 10MHz

The TXB0604 is able to level shift to the expected level of 3.3V at the output with no undershoot/ overshoot. The waveform of the competitor however, observes a logic high output at 4.4V (Figure 3-11), and can lead to damage of host/ target devices if this input voltage exceeds the supported absolute-maximum limits.

3.3 Performance with Distributed Capacitive Loads

The third bench test condition covers the distributed capacitance as a result of lengthy PCB traces and connectors used in between the processor to level shifter, or level shifter to flash device. The bench setup is evaluated for both 1.2V to 1.8V and 1.8V to 3.3V translation.

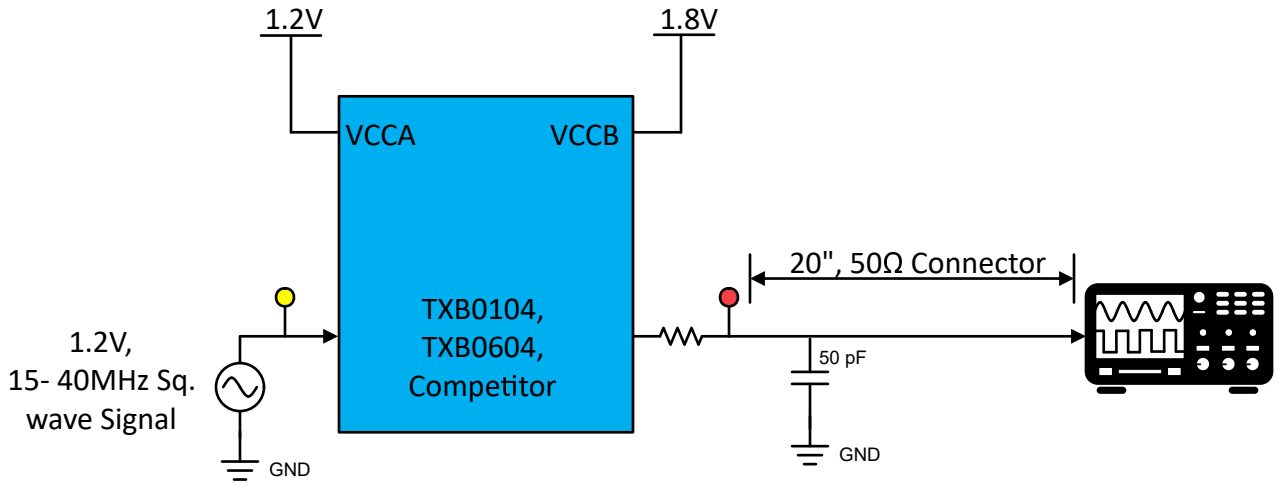

Figure 3-12. Heavy Distributed Capacitive Load Bench Setup, 1.2V to 1.8V

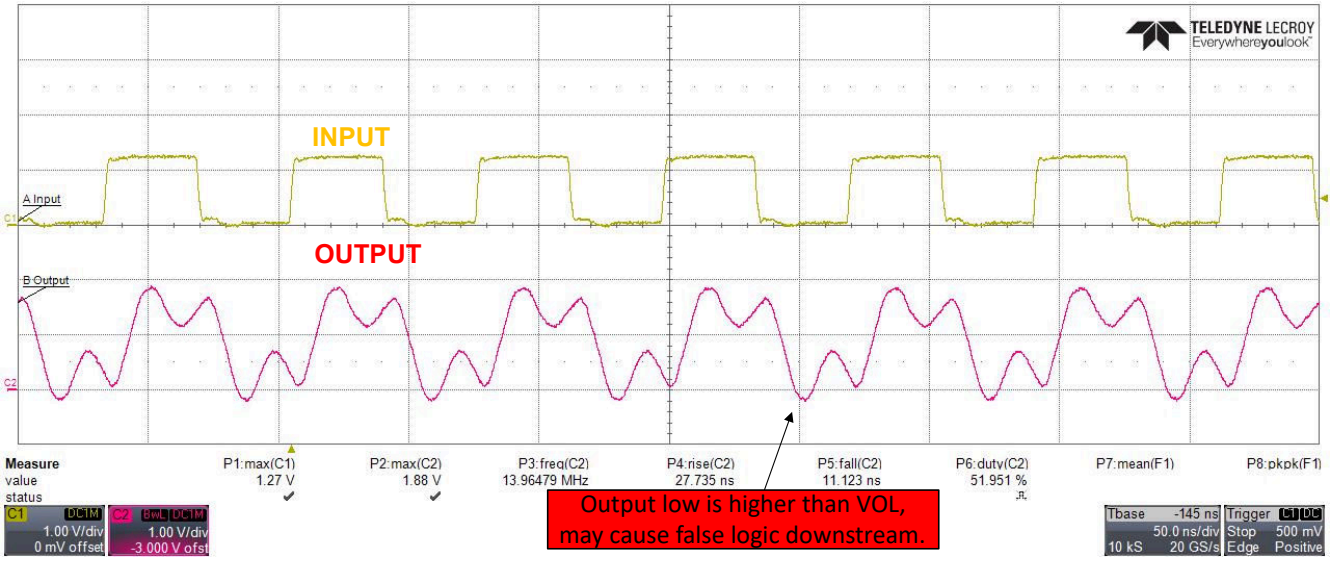

Figure 3-13. TXB0104, 1.2V to 1.8V, Output Cload = 20in. Trace + 50pF, 15MHz

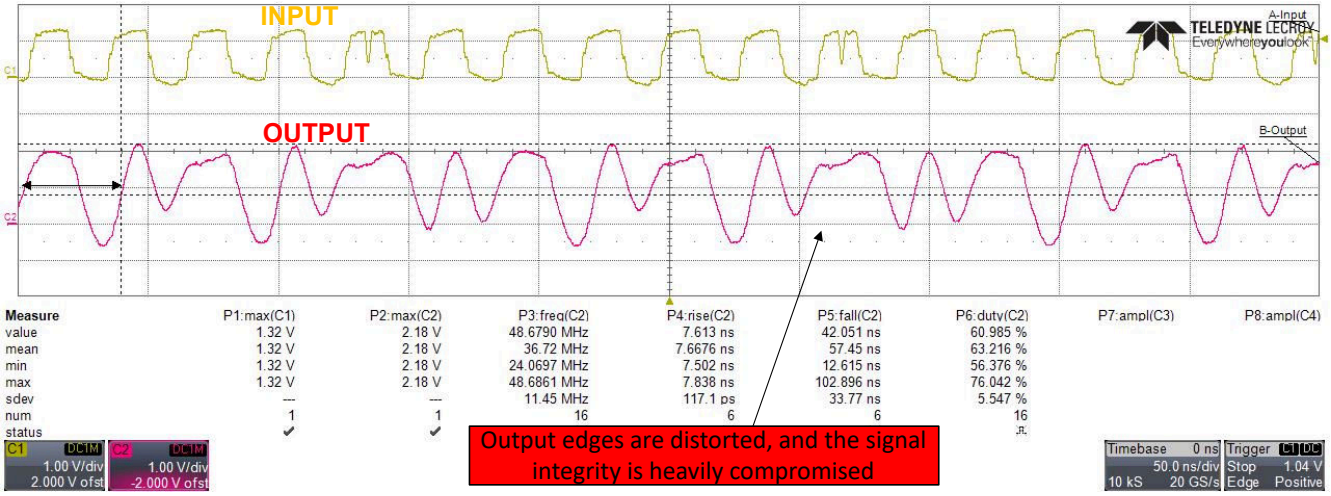

Figure 3-14. Competitor, 1.2V to 1.8V, Output Cload = 20in. Trace + 50pF, 33MHz

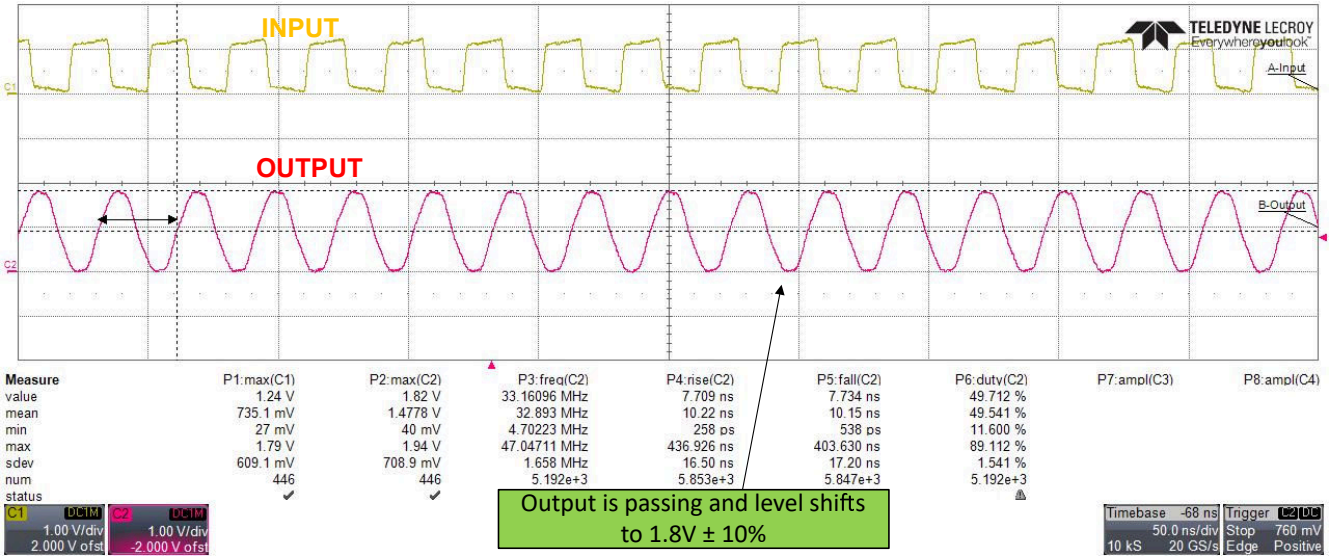

Figure 3-15. TXB0604, 1.2V to 1.8V, Output Cload = 20in. Trace + 50pF, 33MHz

The TXB0104 and competitor device cannot accommodate long cables due to excessive parasitics; the low-level output voltage becomes coupled to the transmission line, causing a glitch that raises VOL to nearly 800 mV. The TXB0604 observes the best signal integrity in this application.

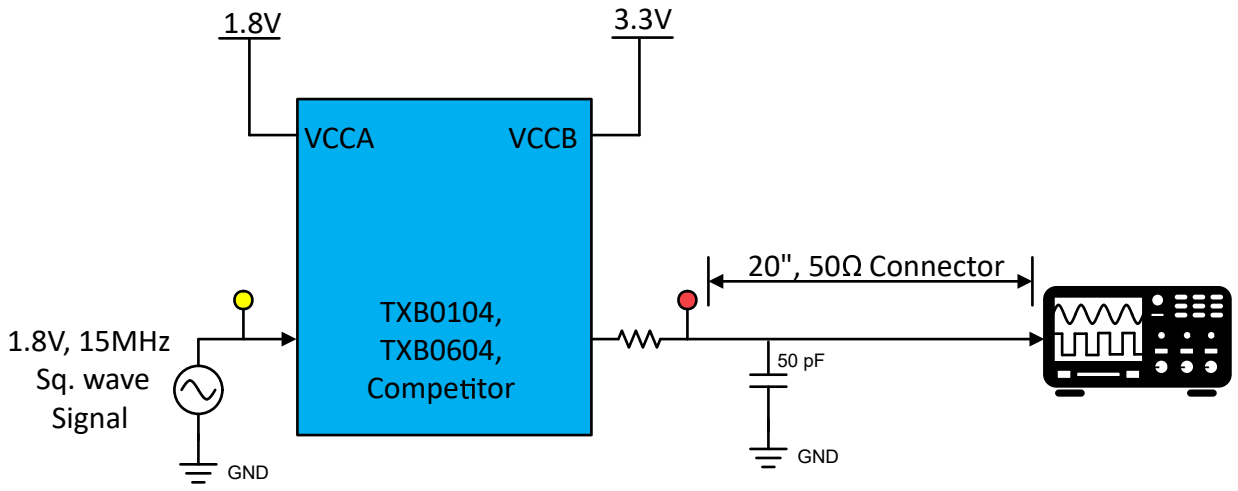

Figure 3-16. Heavy Distributed Capacitive Load Bench Setup, 1.8V to 3.3V

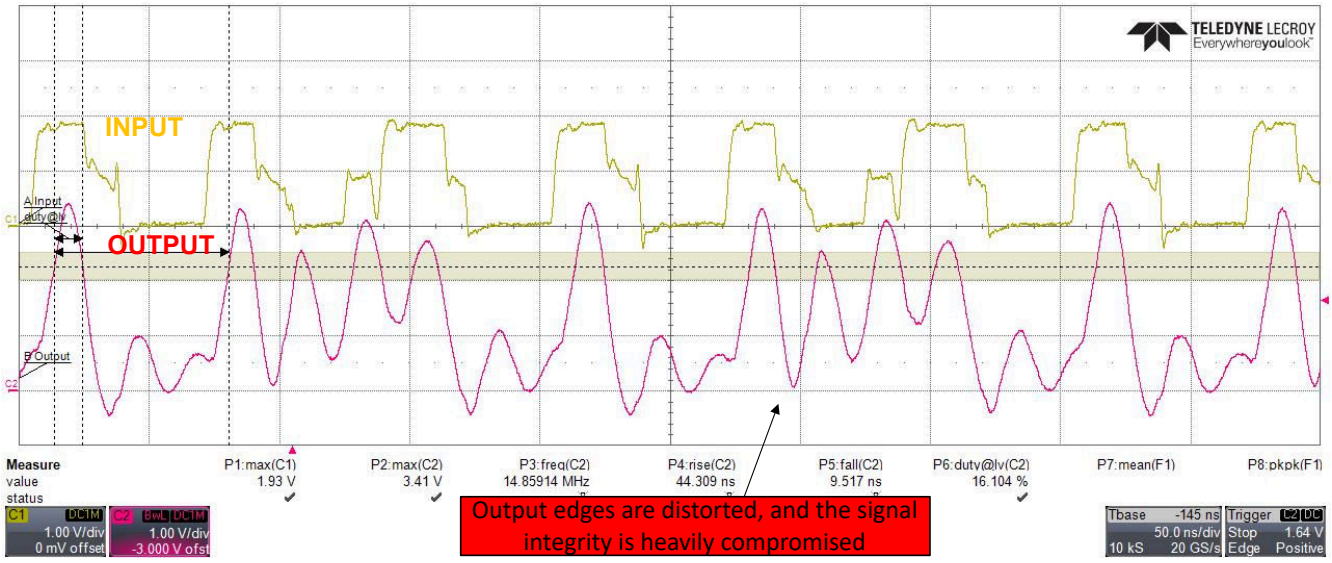

Figure 3-17. TXB0104, 1.8V to 3.3V, Output Cload = 20in. Trace + 50pF, 15MHz

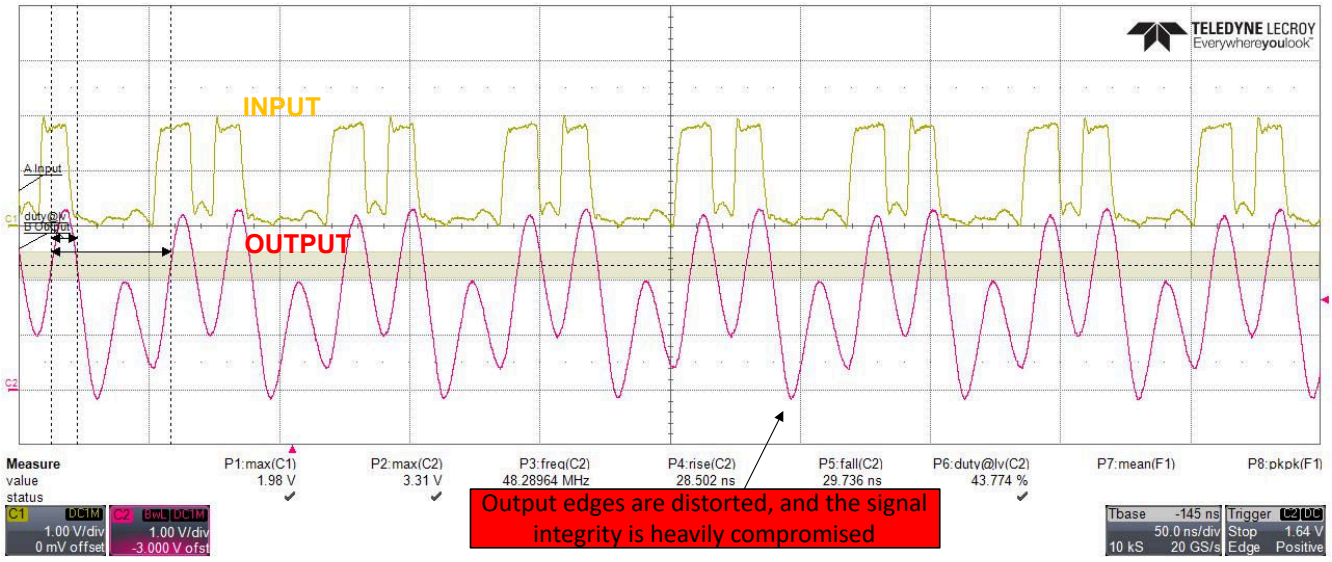

Figure 3-18. Competitor, 1.8V to 3.3V, Output Cload = 20in. Trace + 50pF, 15MHz

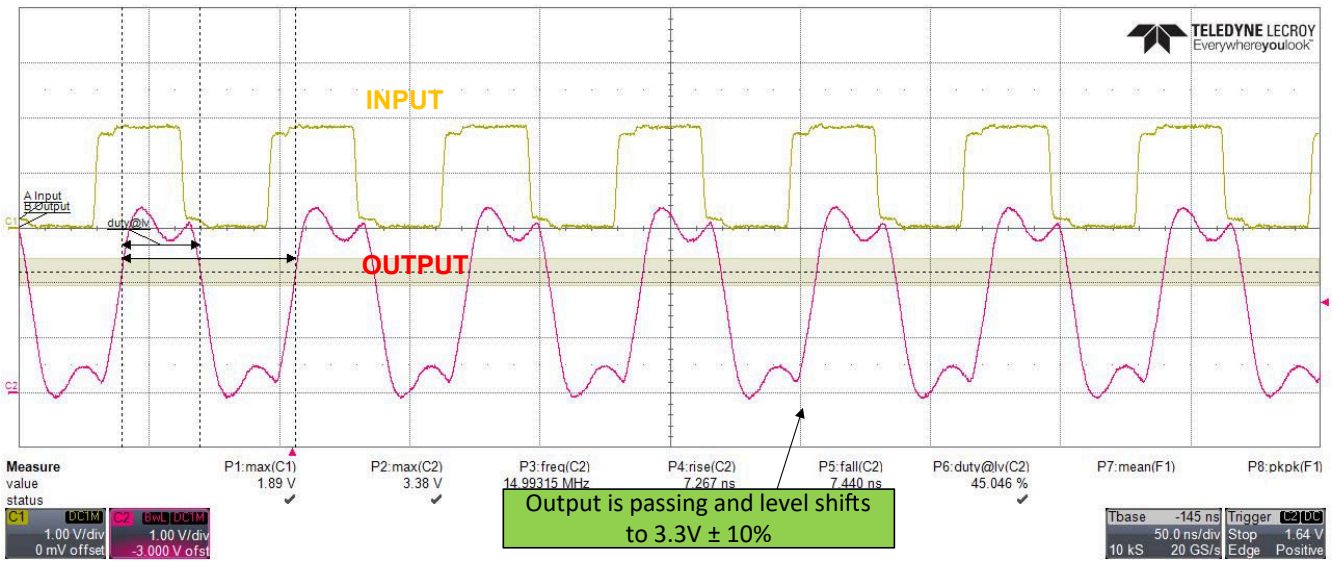

Figure 3-19. TXB0604, 1.8V to 3.3V, Output Cload = 20in. Trace + 50pF, 15MHz

The output behavior is unacceptable for the legacy and competitor waveform as the output data is drastically different from the input signal. In Figure 3-19, observe that the input signal edges become corrupted as the output side drives back into the input. The TXB0604 however, is able to observe improved signal integrity for test case in comparison to the TXB0104 and competitor device.

4 Design Considerations with the TXB0604/ TXB0606

While the TXB0604 and TXB0606 can be used to resolve signal integrity concerns surrounding transmission lines, there are some design considerations to consider to achieve the best performance.

4.1 Impedance Matching

Overshoot and undershoot are common symptoms of driving long transmission lines if they are not properly addressed. These problems arise because the strong output impedance of the level shifter during state transitions do not match the impedance of the transmission medium. Adding damping resistors can mitigate this effect. System designers should use series termination resistors as close as possible to the output of the TXB0604 to better match the output impedance of the driver to the transmission line. Verify that the impedance values are properly fitted and tested depending on impedance characteristics of the system.

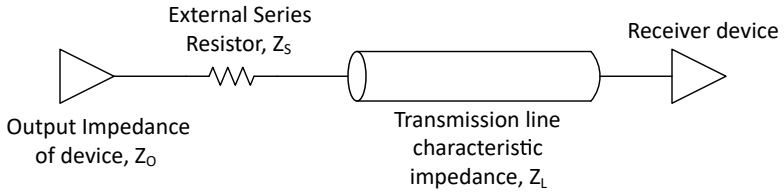

Figure 4-1. Impedance Matching with External Series Resistor

$$Z_O + Z_S = \quad Z_L \tag{1}$$

The provided example below shows the TXB0604 under identical bench setups except the inclusion of the dampening resistor on Figure 4-2. Observe the higher V_{OH} (2.22V) compared to the expected 1.8V as shown in Figure 4-2.

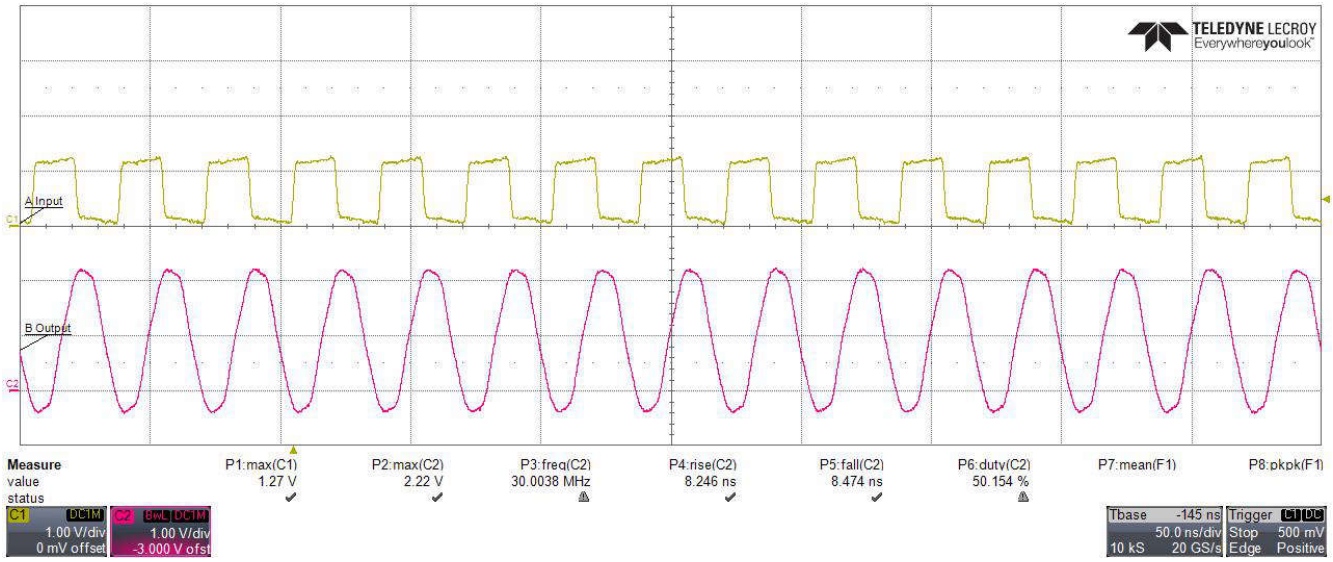

Figure 4-2. TXB0604, 1.2V to 1.8V with Improper Impedance Matching

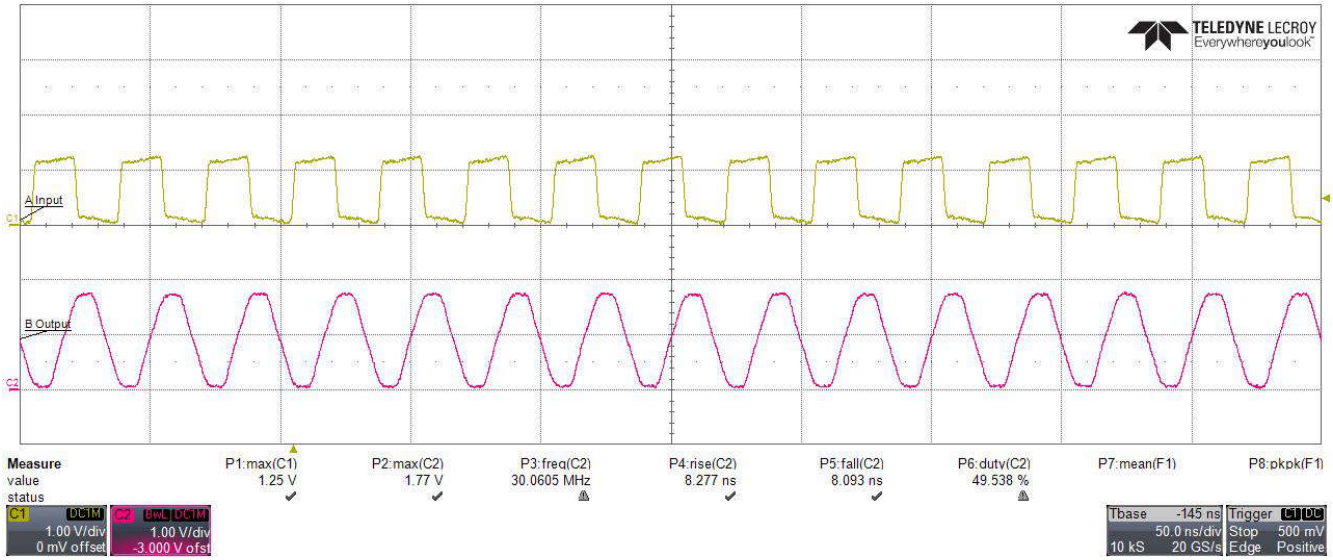

Figure 4-3. TXB0604, 1.2V to 1.8V with Proper Impedance Matching

4.2 Direction Change Wait Time, T_{DCW}

While the device supports auto-bidirectional signaling, it requires a brief idle period during which no communication takes place. This pause allows the I/O drivers on the A→B and B→A sides to settle and ensures the signal direction changes correctly. The time required to switch direction is referred to as T_{DCW} (Direction-Change Wait time). System designers should respect this interval and ensure that signals do not propagate through the device in the opposite direction until the drivers have settled in their new state. Otherwise, the signal will be ignored and will not be able to drive back into the device. The T_{DCW} specification is listed in the Switching Ch. Table for the respective VCCA values of the TXB0604/ TXB0606 datasheet.

In QSPI applications, the I/O lines are often bidirectional, and the interface uses dummy cycles between read and write operations. These dummy cycles effectively provide the minimum turnaround time required by the MCU, the external flash, aas well as for the TXB0604/TXB0606. System designers must calculate the total time taken from the sum of the dummy cycles needed to meet this minimum turnaround time to satisfy all components.

Observing the T_{DCW} is critical to prevent communication errors, missed data bits, and incorrect data capture.

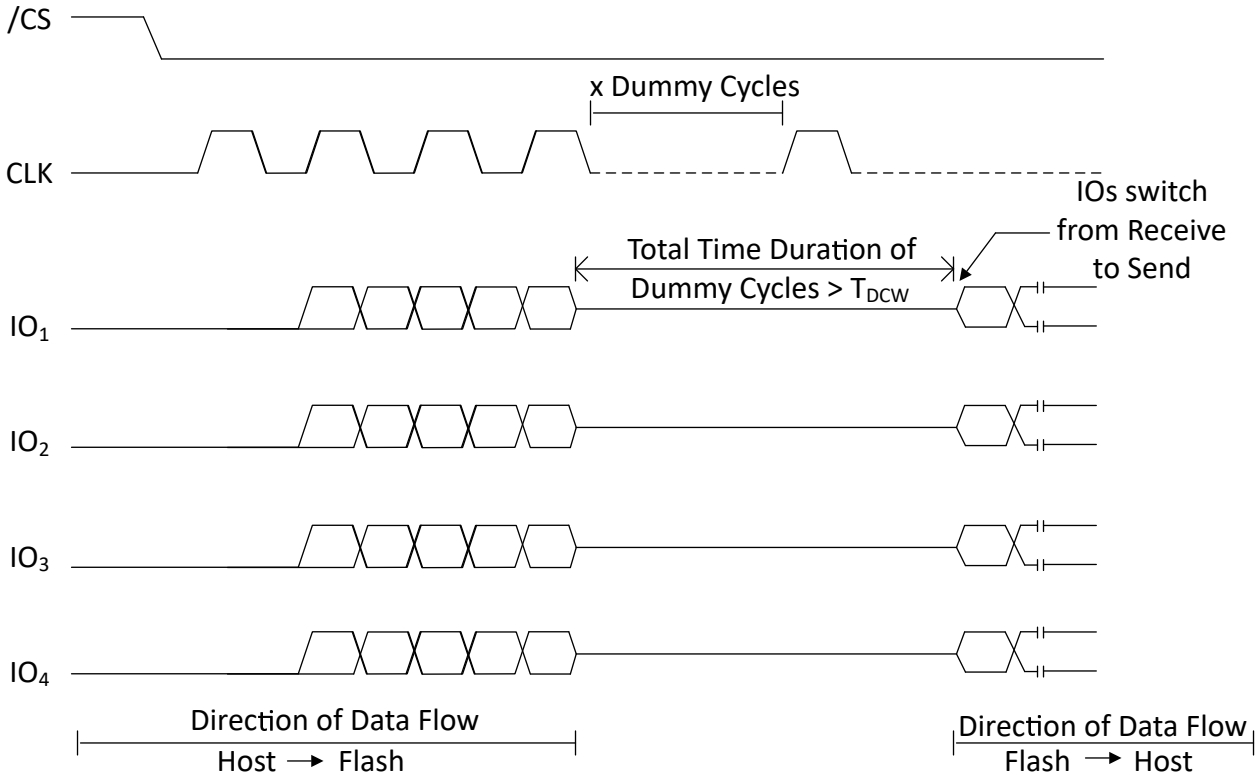

Figure 4-4. Determining the Dummy Cycles Needed in Auto-Directional Data Flow

5 Summary

In this app note, the performance of the TXB0604 is provided through a series of different test setups in comparison to legacy counterparts (for example, TXB0104) and competition equivalent. As the results show, the TXB0604 consistently outperforms peers and provides system designers with an alternative, cost effective design for signal integrity concerns.

6 References

- Texas Instruments, *From Bottleneck to Breakthrough: QSPI Optimization in Data Centers with TXB0604/TXB0606*, application note.
- Texas Instruments, *A Guide to Voltage Translation With TXB-Type Translators*, application note.
- Texas Instruments, *From Bottleneck to Breakthrough: QSPI Optimization in Data Centers with TXB0604/TXB0606,*, application note.
- Texas Instruments, *Schematic Checklist - A Guide to Designing with Auto- Bidirectional Translators*, application note.
- Texas Instruments, *Do's and Don'ts for TXB and TXS Voltage Level-Shifters with Edge Rate Accelerators,* application note.

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