Functional Safety Information

LM74720-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for LM74720-Q1 (WSON package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

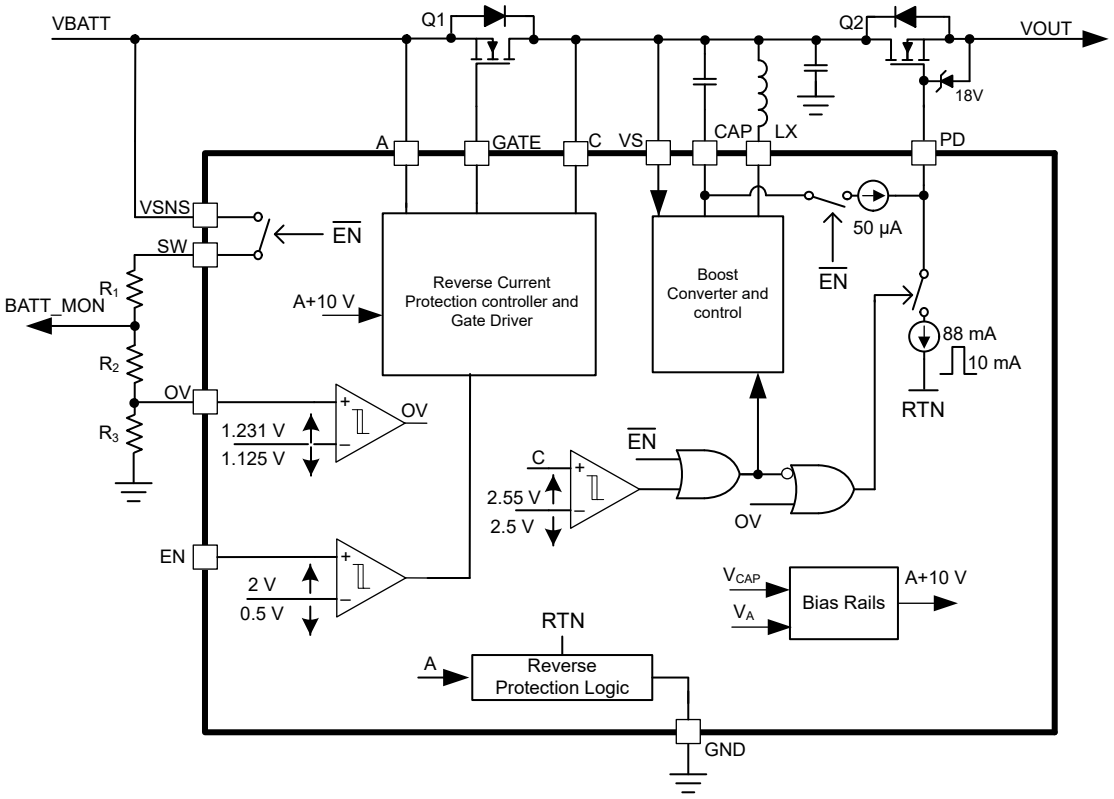

Figure 1-1. Functional Block Diagram

LM74720-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for LM74720-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	7
Die FIT rate	3
Package FIT rate	4

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 0.36mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM74720-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
GATE output functional, not in specification voltage or timing	18
GATE stuck at high	11
GATE stuck at low	18
PD output functional, not in specification voltage or timing	12
PD stuck at high	6
PD stuck at low	21
OV fails to trip or false trip	9
Pin-to-pin short	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LM74720-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LM74720-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the LM74720-Q1 data sheet.

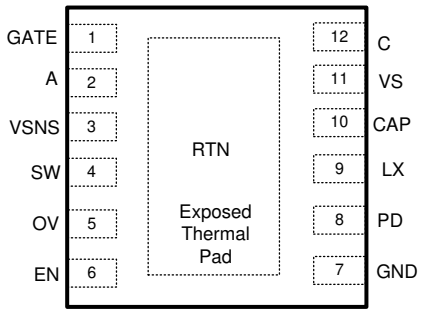

Figure 4-1. WSON 12-Pin DRR Transparent Top View

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is operating under the specified ranges within the *Recommended Operating Conditions* section of the data sheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
DGATE	1	The device is damaged due to internal conduction. The external DGATE FET can also be damaged due to a violation of the maximum VGS rating.	A
A	2	Input supply shorted to ground. Device not functional.	B
VSNS	3	The input supply monitoring feature is not available.	B
SW	4	No device damage is expected if VSNS is floating. The device is damaged if VSNS is connected to A.	A
OV	5	The overvoltage protection functionality is disabled.	B
EN	6	The device is in shutdown mode.	B
GND	7	No impact on device functionality.	D
PD	8	The HGATE gate drive is off.	B
LX	9	The externals FETs are always OFF. VBATT is short to GND; the inductor can be damaged.	A
CAP	10	The device is damaged due to internal conduction between VS and CAP.	A
VS	11	The device does not power up. BFET is damaged. VBATT is short to GND.	A

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
C	12	BFET is damaged. VBATT is short to GND.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GATE	1	The external FET is not controlled. The system is still protected by the body diode of the FET.	B
A	2	The DGATE drive is off. The system is still protected by the body diode of the FET.	B
VSNS	3	The input supply monitoring feature is not available.	B
SW	4	The input supply monitoring feature is not available.	B
OV	5	The overvoltage pin is internal pulldown when floating. OV functionality is DISABLED.	B
EN	6	The device is in shutdown mode due to the internal pulldown on the EN pin.	B
GND	7	The device does not power up.	B
PD	8	The HFET is off since the PD gate drive is open.	B
LX	9	The boost output does not switch. BFET is OFF. The output is at VIN-2VD.	B
CAP	10	The device detects *CAP open* and shuts off.	B
VS	11	The boost converter is OFF due to no supply. Both FETS are OFF.	B
C	12	The part powers up but latches off after one full boost cycle. The latch is cleared by the EN pin or power cycling.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
GATE	1	A	The DGATE FET is always off as the external FET GATE to SOURCE is shorted.	B
A	2	VSNS	No impact on device functionality.	D
VSNS	3	SW	The input supply monitoring feature is always available. There is a higher system Iq when EN = low, due to constant current drawn through the external R-ladder.	B
SW	4	OV	The PD turns off, provided the voltage of the SW pin is higher than the overvoltage threshold of the overvoltage comparator.	B
OV	5	EN	The PD is *on* or *off* based on the voltage level of the EN/UVLO pin being lower or higher than the overvoltage threshold of the overvoltage comparator.	B
EN	6	GND	The device is always OFF. No impact on device operation.	B
GND	7	PD	The PD is pulled low and the external FET is off.	B
PD	8	LX	N/A	B
LX	9	CAP	The boost converter diode is bypassed. The device shuts off boost after detecting the fault.	B
CAP	10	VS	The boost operation is in closed loop (the inductor builds up from C and discharges back to VS or C) at every switching cycle. Continuous switching of boost.	B
VS	11	C	VS follows C. No impact on device operation.	D
C	12	N/A	No impact on device operation.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GATE	1	The diode FET is always off since the external FET GATE to SOURCE is shorted.	B
A	2	No impact on device operation.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VSNS	3	No impact on device operation.	D
SW	4	The input supply monitoring feature is always available.	B
OV	5	When the input of the overvoltage comparator is higher than the overvoltage threshold, the PD is off.	B
EN	6	The device is always on. The undervoltage functionality is not available.	B
GND	7	The input supply is shorted to ground. The device does not power up.	B
PD	8	The PD gate drive is off when EN = high. The PD internal pulldown FET is damaged when EN = low.	A
LX	9	The device shuts off boost after detecting the fault.	B
CAP	10	The charge pump does not power up. DGATE and HGATE drive remain off.	B
VS	11	No impact on the operation of the device when the supply voltage is positive. The device is damaged when the supply voltage is negative.	A
C	12	The reverse-current blocking functionality is lost when the supply is positive. The device is damaged when the supply voltage is negative.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2025	*	Initial Release

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