Functional Safety Information

TPS748A-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the TPS748A-Q1 (VSON packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

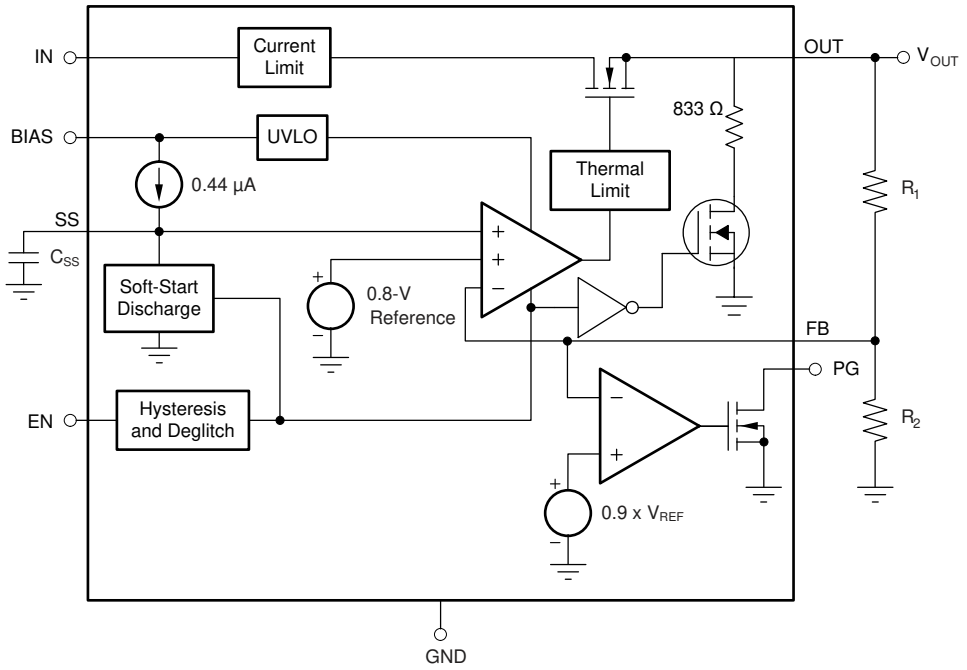

Figure 1-1. Functional Block Diagram

The TPS748A-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 VSON Package

This section provides functional safety failure in time (FIT) rates for the VSON package of the TPS748A-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	11
Die FIT rate	9
Package FIT rate	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 1400mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	Power amplifier and regulator > 1 Watt – (LDO)	100 FIT	90°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS748A-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT no output (GND)	35
OUT high (following input)	10
OUT not in specification voltage or timing	45
PG false trip, fails to trip	5
Short circuit any two pins	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS748A-Q1 (VSON package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device must maintain the same pin configuration as with the VSON-10 packages.
- The device operates across virtual junction temperatures ranging from -40°C to 150°C.
- The device operates at an input voltage less than 6V and output current less than 3.1A.
- The device operates according to the recommended operating conditions and does not exceed the absolute maximum ratings.

4.1 VSON Package

Figure 4-1 shows the TPS748A-Q1 pin diagram for the VSON package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS748A-Q1 data sheet.

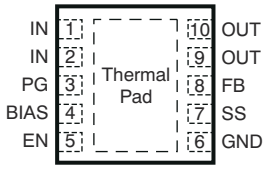

Figure 4-1. Pin Diagram (VSON Package)

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	Device does not turn on. No damage to device.	B
IN	2	Device does not turn on. No damage to device.	B
PG	3	No damage to device. PG functionality does not work. No impact on remaining functionality.	B
BIAS	4	No damage to device. Since band gap and control circuits do not power up, the output voltage is not regulated and remains low at 0V.	B
EN	5	Device does not turn on. No damage to device.	B
GND	6	No Impact. Normal operation.	D
SS	7	Quiescent current increases. Device output remains at 0V. No damage to device.	B
FB	8	Loss of functionality, device does not regulate. Output voltage tracks input voltage and equals V_{IN} minus the dropout. No damage to device.	B
OUT	9	Device hits a current limit state. If the power dissipation is significant, the device hits a thermal shutdown state, and can continue to cycle between the two states. Continuously running the device above the rated current degrades device reliability.	A
OUT	10	Same as pin 9.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	Normal operation. Power supply is still connected to the remaining IN pin (2). There is a small risk that the bond wire connecting to the remaining IN pin can fuse under heavily loaded conditions.	A D
IN	2	Same as pin 1.	A D
PG	3	No damage to device. PG functionality does not work. No impact on remaining functionality.	B
BIAS	4	No damage to device. Since band gap and control circuits do not power up, the output voltage is not regulated and remains low at 0V.	B
EN	5	Since the voltage floats to an indeterminate value, the device can disable.	B
GND	6	With the reference pin floating, the voltages at the remaining pins are also floating and the device is not functional. There is a risk of violating the absolute maximum ratings.	A B
SS	7	No impact. Normal operation. Start-up time defaults to 200µs, approximately.	D
FB	8	Loss of functionality. The output pin voltage is not regulated and remains in an indeterminate state.	B
OUT	9	No impact. Normal operation. Load is still connected to the remaining OUT pin (10). There is a small risk that the bond wire connecting to the remaining OUT pin can fuse under heavily loaded conditions.	A D
OUT	10	Same as pin 9.	A D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
IN	1	IN	No impact. Normal operation.	D
IN	2	PG	Very high risk of damage to the PG pin and device, resulting from excess current drawn when the PG open drain becomes low impedance.	A
PG	3	BIAS	Very high risk of damage to the PG pin and device, resulting from excess current drawn when the PG open drain becomes low impedance.	A
BIAS	4	EN	Device remains ON regardless of the enable signal value.	B
EN	5	GND	Device remains OFF regardless of the enable signal value.	B
GND	6	SS	Quiescent current increases. Device output remains at 0V. No damage to device.	B
SS	7	FB	The error amplifier output rails to either one of the supplies, and the LDO output is either at 0V or tracks V_{IN} and equals V_{IN} – dropout.	B
FB	8	OUT	V_{OUT} is set to V_{FB} = 0.8V.	B
OUT	9	OUT	No impact. Normal operation.	D
OUT	10	IN	Output voltage is not regulated and equals V_{IN}.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN	1	No impact. Normal operation.	D
IN	2	No impact. Normal operation.	D
PG	3	Very high risk of damage to the PG pin and device, resulting from excess current drawn when the PG open drain becomes low impedance.	A
BIAS	4	Normal operation is only established if there is sufficient dropout ($V_{IN} \geq V_{OUT} + V_{DO}$, where $V_{DO} = I_{OUT} \times (1.6 / 1.5)$ and V_{IN} ($V_{IN} \geq 2.7V$) are provided. Device does not turn on for lower values of V_{IN}, and V_{OUT} remains at 0V.	B
EN	5	Device remains ON regardless of the enable signal value.	B
GND	6	Device does not turn on.	B
SS	7	The LDO output pin voltage is not regulated and tracks V_{IN}. V_{OUT} equals V_{IN} – dropout.	B
FB	8	The LDO output pin voltage is not regulated and equals V_{IN} (under no-load conditions).	B
OUT	9	Device is not functional, the output voltage is not regulated and equals V_{IN}.	B
OUT	10	Same as pin 9.	B

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2025	*	Initial Release

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