Functional Safety Information

TPS7A21-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

1 Overview 2
2 Functional Safety Failure In Time (FIT) Rates 3
2.1 VSON Package 3
2.2 WSON (DSG0008B) Package 4
2.3 WSON (DSG0008A) Package 5
3 Failure Mode Distribution (FMD) 6
4 Pin Failure Mode Analysis (Pin FMA) 7
4.1 VSON Package 7
4.2 WSON (DSG0008B) Package 9
4.3 WSON (DSG0008A) Package 11
5 Revision History 12

Trademarks

1 Overview

This document contains information for the TPS7A21-Q1 (VSON, WSON (DSG0008B), and WSON (DSG0008A) packages) to aid in the design of a functional safety system. Information provided includes:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

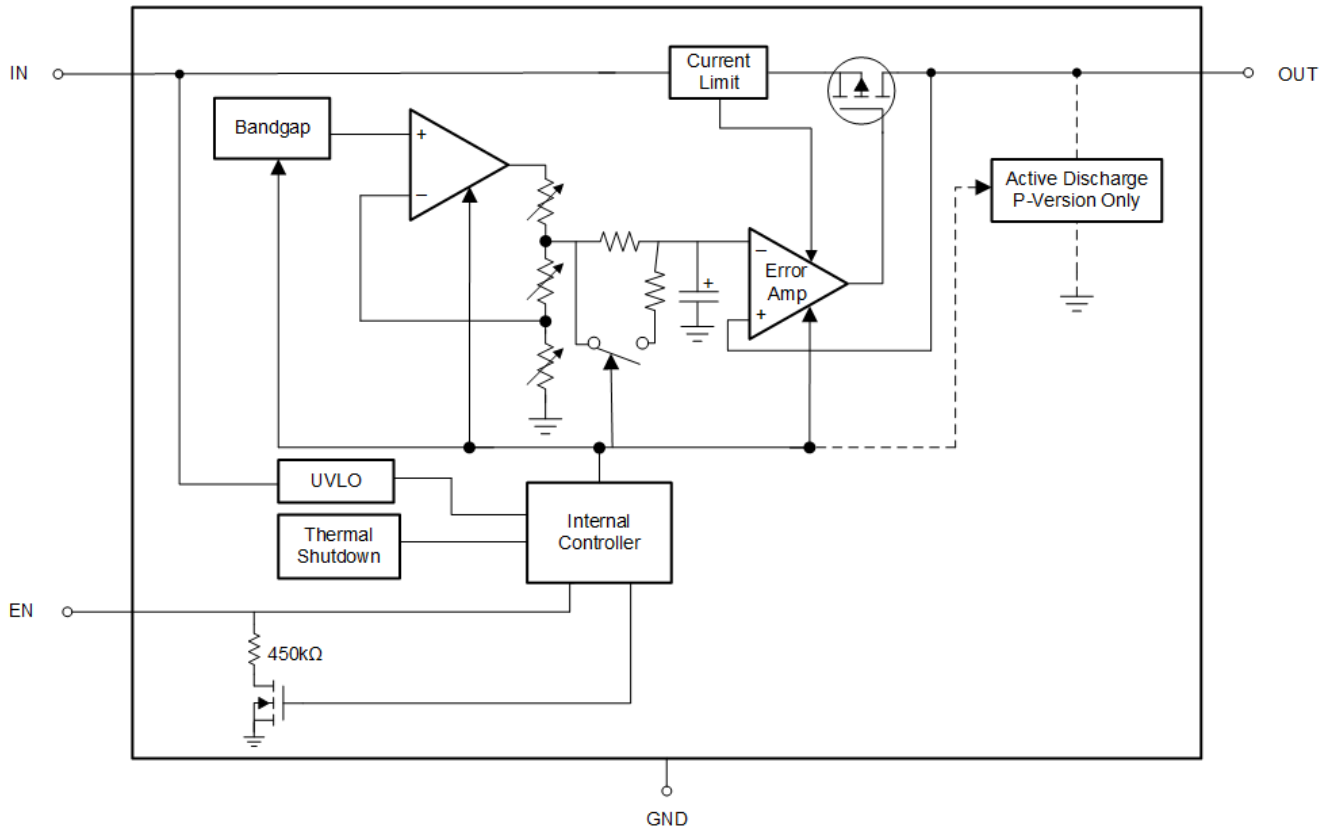

Figure 1-1. Functional Block Diagram

The TPS7A21-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 VSON Package

This section provides functional safety failure in time (FIT) rates for the VSON package of the TPS7A21-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	8
Die FIT rate	4
Package FIT rate	4

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 500mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs, analog, and mixed = <50V supply	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 WSON (DSG0008B) Package

This section provides functional safety failure in time (FIT) rates for the WSON (DSG0008B) package of the TPS7A21-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	6
Die FIT rate	4
Package FIT rate	2

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 500mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs, analog, and mixed = <50V supply	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.3 WSON (DSG0008A) Package

This section provides functional safety failure in time (FIT) rates for the WSON (DSG0008A) package of the TPS7A21-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-5. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	6
Die FIT rate	4
Package FIT rate	2

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 500mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-6. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS ASICs, analog, and mixed = <50V supply	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS7A21-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
V_{OUT} high (following V_{IN})	40
V_{OUT} low (no output)	40
Short any two pins	10
V_{OUT} not in specification (voltage or timing)	10

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS7A21-Q1 (VSON, WSON (DSG0008B), and WSON (DSG0008A) packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2, Table 4-6, and Table 4-10)
- Pin open-circuited (see Table 4-3, Table 4-7, and Table 4-11)
- Pin short-circuited to an adjacent pin (see Table 4-4, Table 4-8, and Table 4-12)
- Pin short-circuited to supply (see Table 4-5, Table 4-9, and Table 4-13)

Table 4-2 through Table 4-13 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device operates at free-air temperatures between -40°C and 150°C.
- Device operates at an input voltage of at least 2V and no more than 6V.
- Device operates according to all recommended operating conditions, and the absolute maximum ratings in the device data sheet are not exceeded.

4.1 VSON Package

Figure 4-1 shows the TPS7A21-Q1 pin diagram for the VSON package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7A21-Q1 data sheet.

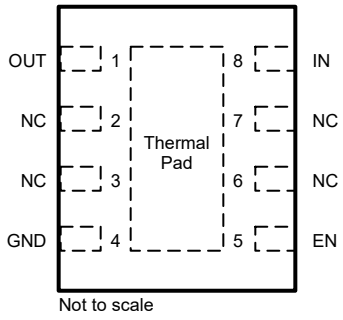

Figure 4-1. Pin Diagram (VSON) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Current limit is triggered, and the device can repeatedly enter and exit thermal shutdown depending on power dissipation.	B
NC	2	No effect. Normal operation.	D
NC	3	No effect. Normal operation.	D
GND	4	No effect. Normal operation.	D
EN	5	The device is disabled, resulting in no output voltage.	B
NC	6	No effect. Normal operation.	D
IN	7	Power is not supplied to the device. System performance depends on upstream current limiting.	B
IN	8	Power is not supplied to the device. System performance depends on upstream current limiting.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Device parasitics are increased and transient performance is degraded.	C
OUT	2	Device parasitics are increased and transient performance is degraded.	C
NC	3	No effect. Normal operation.	D
GND	4	Device biasing has no current path. The device is not operational and does not regulate.	B
EN	5	The smart enable feature keeps the output turned off.	B
NC	6	No effect. Normal operation.	D
IN	7	Device parasitics are increased and transient performance is degraded.	C
IN	8	Device parasitics are increased and transient performance is degraded.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	2 - OUT	No effect. Normal operation.	D
OUT	2	3 - NC	No effect. Normal operation.	D
NC	3	4 - GND	No effect. Normal operation.	D
EN	5	6 - NC	No effect. Normal operation.	D
NC	6	7 - IN	No effect. Normal operation.	D
IN	7	8 - IN	No effect. Normal operation.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation is not possible.	B
OUT	2	Regulation is not possible.	B
NC	3	No effect. Normal operation.	D
GND	4	No output voltage. System performance depends on the upstream current limiting.	B
EN	5	Device is always enabled.	B
NC	6	No effect. Normal operation.	D
IN	7	No effect. Normal operation.	D
IN	8	No effect. Normal operation.	D

4.2 WSON (DSG0008B) Package

Figure 4-2 shows the TPS7A21-Q1 pin diagram for the WSON (DSG0008B) package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7A21-Q1 data sheet.

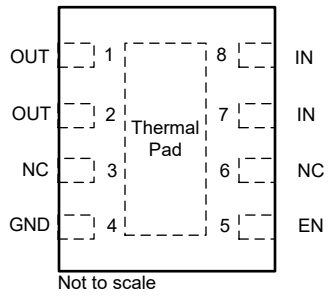

Figure 4-2. Pin Diagram (WSON (DSG0008B) Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Current limit is triggered, and the device can repeatedly enter and exit thermal shutdown depending on power dissipation.	B
OUT	2	Current limit is triggered, and the device can repeatedly enter and exit thermal shutdown depending on power dissipation.	B
NC	3	No effect. Normal operation.	D
GND	4	No effect. Normal operation.	D
EN	5	The device is disabled, resulting in no output voltage.	B
NC	6	No effect. Normal operation.	D
IN	7	Power is not supplied to the device. System performance depends on upstream current limiting.	B
IN	8	Power is not supplied to the device. System performance depends on upstream current limiting.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Device parasitics are increased and transient performance is degraded.	C
OUT	2	Device parasitics are increased and transient performance is degraded.	C
NC	3	No effect. Normal operation.	D
GND	4	Device biasing has no current path. The device is not operational and does not regulate.	B
EN	5	The smart enable feature keeps the output turned off.	B
NC	6	No effect. Normal operation.	D
IN	7	Device parasitics are increased and transient performance is degraded.	C
IN	8	Device parasitics are increased and transient performance is degraded.	C

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	2 - OUT	No effect. Normal operation.	D
OUT	2	3 - NC	No effect. Normal operation.	D
NC	3	4 - GND	No effect. Normal operation.	D
EN	5	6 - NC	No effect. Normal operation.	D
NC	6	7 - IN	No effect. Normal operation.	D
IN	7	8 - IN	No effect. Normal operation.	D

Table 4-9. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Regulation is not possible.	B
OUT	2	Regulation is not possible.	B
NC	3	No effect. Normal operation.	D
GND	4	No output voltage. System performance depends on the upstream current limiting.	B
EN	5	Device is always enabled.	B
NC	6	No effect. Normal operation.	D
IN	7	No effect. Normal operation.	D
IN	8	No effect. Normal operation.	D

4.3 WSON (DSG0008A) Package

Figure 4-2 shows the TPS7A21-Q1 pin diagram for the WSON (DSG0008A) package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7A21-Q1 data sheet.

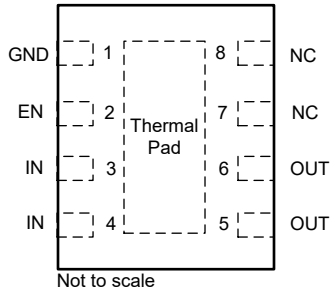

Figure 4-3. Pin Diagram (WSON (DSG0008A) Package)

Table 4-10. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	No effect. Normal operation.	D
EN	2	The device is disabled, resulting in no output voltage.	B
IN	3	Power is not supplied to the device. System performance depends on upstream current limiting.	B
IN	4	Power is not supplied to the device. System performance depends on upstream current limiting.	B
OUT	5	Current limit is triggered, and the device can repeatedly enter and exit thermal shutdown depending on power dissipation.	B
OUT	6	Current limit is triggered, and the device can repeatedly enter and exit thermal shutdown depending on power dissipation.	B
NC	7	No effect. Normal operation.	D
NC	8	No effect. Normal operation.	D

Table 4-11. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	Device biasing has no current path. The device is not operational and does not regulate.	B
EN	2	The smart enable feature keeps the output turned off.	B
IN	3	Device parasitics are increased and transient performance is degraded.	C
IN	4	Device parasitics are increased and transient performance is degraded.	C
OUT	5	Device parasitics are increased and transient performance is degraded.	C
OUT	6	Device parasitics are increased and transient performance is degraded.	C
NC	7	No effect. Normal operation.	D
NC	8	No effect. Normal operation.	D

Table 4-12. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
GND	1	2 - EN	The device is disabled, resulting in no output voltage.	B
EN	2	3 - IN	The device is always enabled.	B
IN	3	4 - IN	No effect. Normal operation.	D
OUT	5	6 - OUT	No effect. Normal operation.	D
OUT	6	7 - NC	No effect. Normal operation.	D
NC	7	8 - NC	No effect. Normal operation.	D

Table 4-13. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
GND	1	No output voltage. System performance depends on the upstream current limiting.	B
EN	2	Device is always enabled.	B
IN	3	No effect. Normal operation.	D
IN	4	No effect. Normal operation.	D
OUT	5	Regulation is not possible.	B
OUT	6	Regulation is not possible.	B
NC	7	No effect. Normal operation.	D
NC	8	No effect. Normal operation.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2025	*	Initial Release

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265