Functional Safety Information

TLV61047-Q1 and TLV61040-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the TLV61047-Q1 and TLV61040-Q1 (SOT23-5 package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagrams for reference.

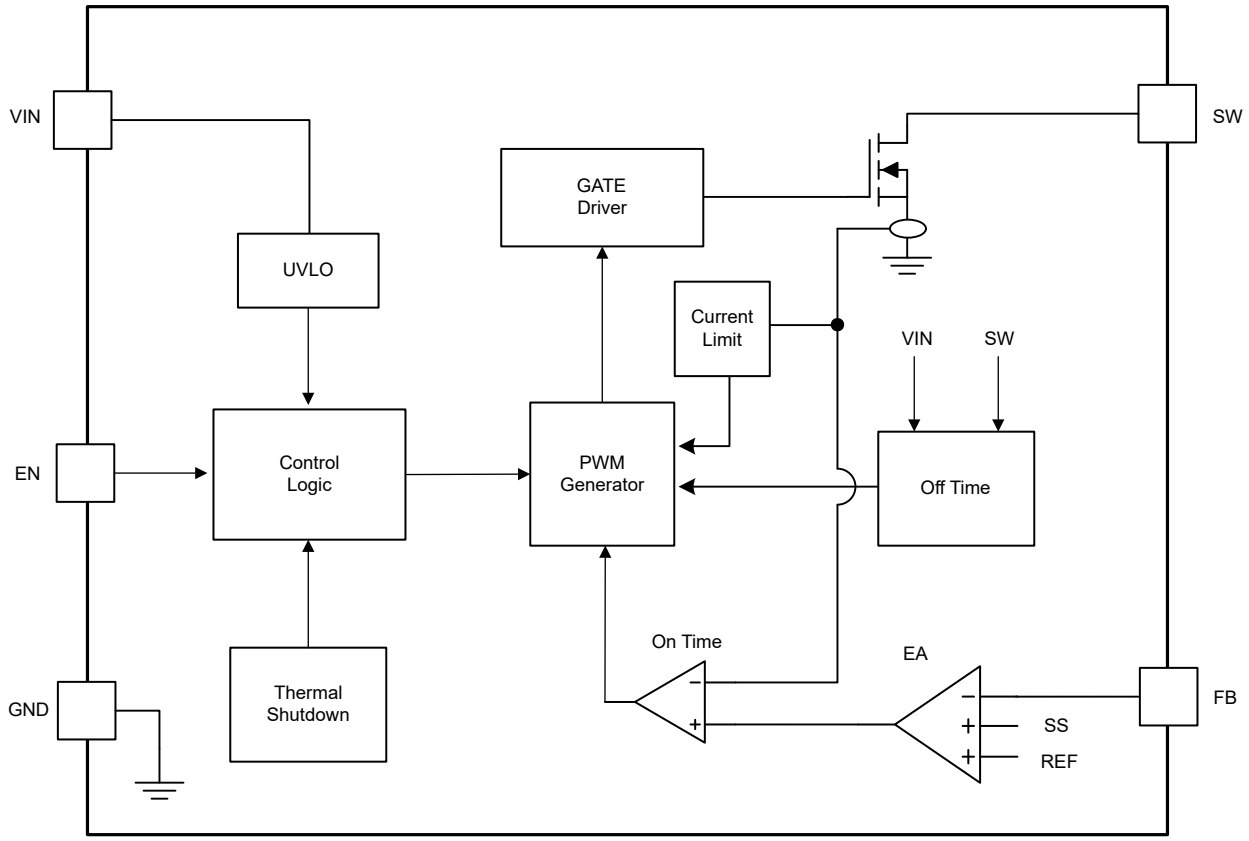

Figure 1-1. TLV61047-Q1 and TLV61040-Q1 Functional Block Diagram

The TLV61047-Q1 and TLV61040-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TLV61047-Q1 and TLV61040-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	23
Die FIT rate	21
Package FIT rate	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 500mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TLV61047-Q1 and TLV61040-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
VO not in specification voltage or timing	80
SW FETs stuck on	10
EN enable fails or false enable	5
Short circuit any two pins	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TLV61047-Q1 and TLV61040-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TLV61047-Q1 and TLV61040-Q1 pin diagrams. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TLV61047-Q1 and TLV61040-Q1 datasheets.

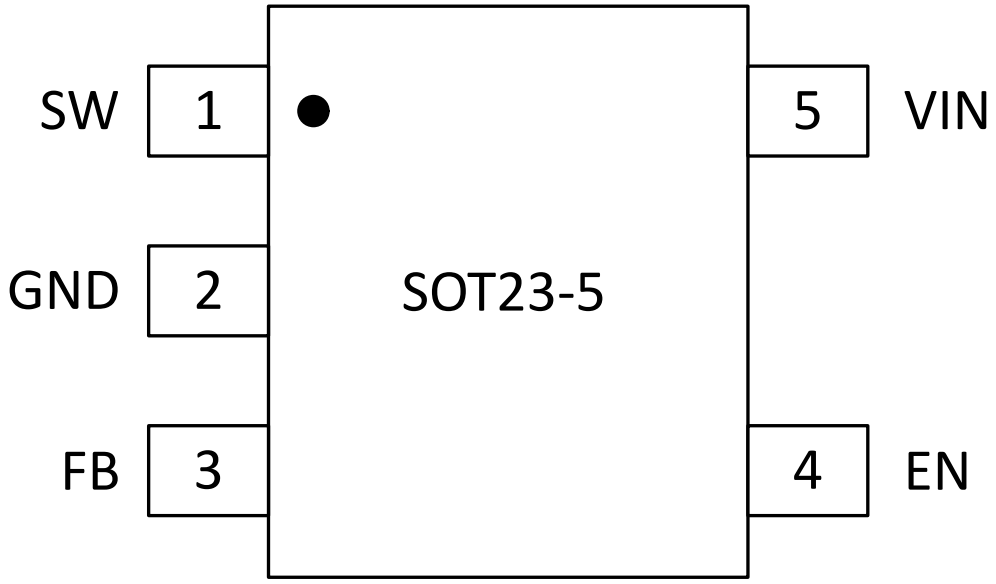

Figure 4-1. TLV61047-Q1 and TLV61040-Q1 Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is used within the *Recommended Operating Conditions* and the *Absolute Maximum Ratings* found in the TLV61047-Q1 and TLV61040-Q1 datasheets.
- The configuration is as shown in the *Application and Implementation* section found in the TLV61047-Q1 and TLV61040-Q1 datasheets.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SW	1	There is possible damage to the inductor and pin.	A
GND	2	There is no effect on the device.	D
FB	3	There is possible damage to the device.	A
EN	4	There is no output voltage.	B
VIN	5	There is no output voltage.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SW	1	There is no output voltage.	B
GND	2	There is no output voltage.	B
FB	3	There is possible damage to the device.	A
EN	4	There is no output voltage.	B
VIN	5	There is no output voltage.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
SW	1	GND	The power supply is shorted. There is possible damage to the inductor. There is no output voltage.	A
GND	2	FB	There is possible damage to the device.	A
FB	3	EN	N/A	N/A
EN	4	VIN	There is a loss of the disable function.	B
VIN	5	SW	N/A	N/A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
SW	1	There is possible damage to the device.	A
GND	2	There is no output voltage. The power supply is shorted.	B
FB	3	If the voltage IN is higher than 6V, the FB pin is potentially damaged.	A
		If the voltage IN is not higher than 6V, there is a loss of regulation on the output voltage.	B
EN	4	There is a loss of the disable function.	B
VIN	5	There is no effect on the device.	D

5 Revision History

Changes from February 25, 2026 to June 23, 2026 (from Revision * (February 2026) to Revision A (June 2026)) **Page**

- Added *Shorted to* column in the *Pin FMA for Device Pins Short-Circuited to Adjacent Pin* table..... 5

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