

Functional Safety Information

TLV9161-Q1

Functional Safety FIT Rate, FMD and Pin FMA



Table of Contents

1 Overview.....2

2 Functional Safety Failure In Time (FIT) Rates.....3

 2.1 SOT-23 (DBV) – 5 Package.....3

 2.2 SOT-SC70 (DCK) – 5 Package.....3

3 Failure Mode Distribution (FMD).....5

4 Pin Failure Mode Analysis (Pin FMA).....6

 4.1 SOT-23 (DBV) – 5 Package.....6

 4.2 SOT-SC70 (DCK) – 5 Package.....8

5 Revision History.....9

Trademarks

All trademarks are the property of their respective owners.

1 Overview

This document contains information for TLV9161-Q1 (SOT-23 (DBV) – 5 and SOT-SC70 (DCK) – 5 packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

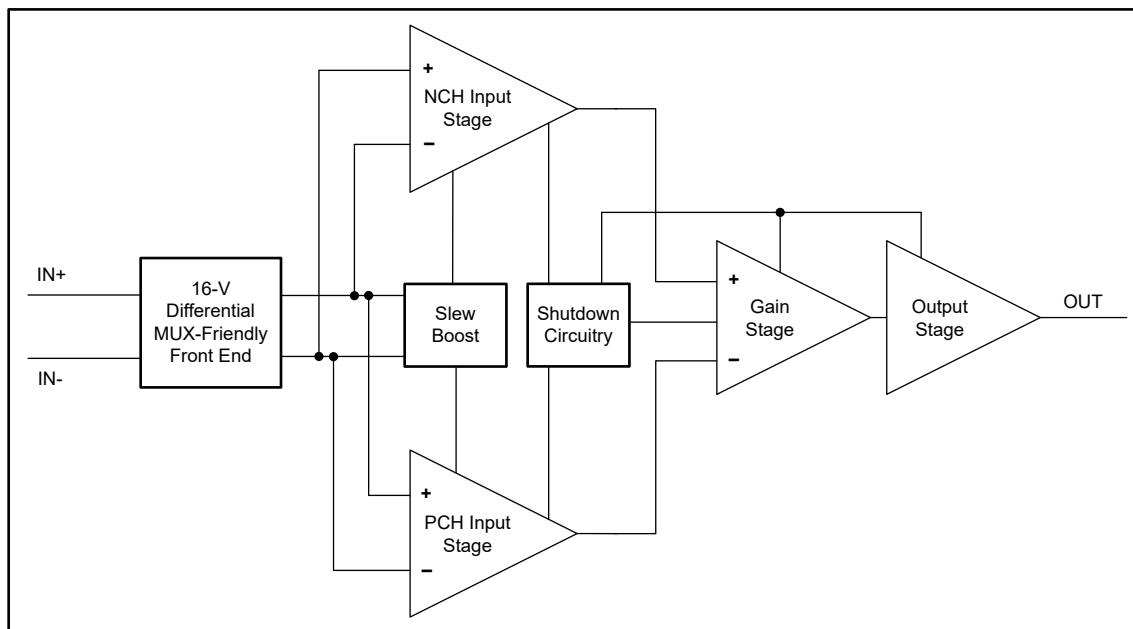


Figure 1-1. Functional Block Diagram

The TLV9161-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 SOT-23 (DBV) – 5 Package

This section provides functional safety failure in time (FIT) rates for the SOT-23 (DBV) – 5 package of the TLV9161-Q1 based on two different industry-wide used reliability standards:

- [Table 2-1](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-2](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total component FIT rate	5
Die FIT rate	3
Package FIT rate	2

The failure rate and mission profile information in [Table 2-1](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 46.72mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in [Table 2-2](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 SOT-SC70 (DCK) – 5 Package

This section provides functional safety failure in time (FIT) rates for the SOT-SC70 (DCK) – 5 package of the TLV9161-Q1 based on two different industry-wide used reliability standards:

- [Table 2-3](#) provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- [Table 2-4](#) provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10 ⁹ Hours)
Total component FIT rate	4
Die FIT rate	3
Package FIT rate	1

The failure rate and mission profile information in [Table 2-3](#) comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 46.72mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T _J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in [Table 2-4](#) come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TLV9161-Q1 in [Table 3-1](#) comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output open (Hi-Z)	20
Output saturate high	25
Output saturate low	25
Output functional, not in specification voltage or timing	30

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TLV9161-Q1 (SOT-23 (DBV) – 5 and SOT-SC70 (DCK) – 5 packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see [Table 4-2](#) and [Table 4-6](#))
- Pin open-circuited (see [Table 4-3](#) and [Table 4-7](#))
- Pin short-circuited to an adjacent pin (see [Table 4-4](#) and [Table 4-8](#))
- Pin short-circuited to supply (see [Table 4-5](#) and [Table 4-9](#))

[Table 4-2](#) through [Table 4-9](#) also indicate how these pin conditions can affect the device as per the failure effects classification in [Table 4-1](#).

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Following are the assumptions of use and the device configuration for the pin FMA in this section:

- *Short circuit to power* means *short to V+*
- *Short circuit to GND* and *short circuit to ground* mean *short to V–*
- V+ is equivalent to VCC
- V– is equivalent to VEE

4.1 SOT-23 (DBV) – 5 Package

[Figure 4-1](#) shows the TLV9161-Q1 pin diagram for the SOT-23 (DBV) – 5 package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TLV9161-Q1 datasheet.

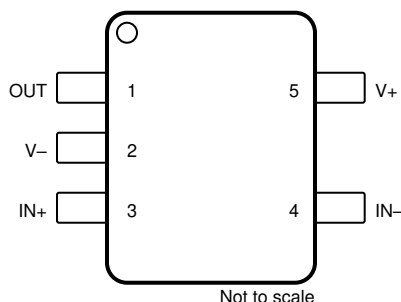


Figure 4-1. Pin Diagram (SOT-23 (DBV) – 5) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Depending on the circuit configuration, the device is forced into a short-circuit condition with the OUT voltage forced to the V– voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
IN+	3	Device common-mode is tied to the negative rail. Depending on the circuit configuration, the output cannot respond because the device is in an invalid common-mode condition.	C
IN–	4	The device does not receive negative feedback. Depending on the circuit configuration, the output can move to the negative supply.	B
V+	5	Op amp supplies are shorted together, leaving the V+ pin at a voltage between the V+ and V– sources (depending on the source impedance).	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	There is no negative feedback or ability for OUT to drive the application.	B
V–	2	The negative supply is left floating. The op amp ceases to function because no current can source or sink to the device.	B
IN+	3	Device common-mode is disconnected. The op amp is not provided with common-mode bias, and the device output can result at the positive or negative rail. The IN+ pin voltage can result at the positive or negative rail because of leakages on the ESD diodes.	B
IN–	4	The inverting pin of the op amp is left floating. Negative feedback is not provided to the device and can result in the device output moving between the positive and negative rails. The IN– pin voltage likely ends up at the positive or negative rail because of leakage on the ESD diodes.	B
V+	5	The positive supply is left floating. The op amp ceases to function because no current can source or sink to the device.	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	1	V–	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the OUT voltage ultimately forced to the V– voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
V–	2	IN+	Device common-mode is tied to the negative rail. Depending on the circuit configuration, the output likely does not respond because the device is in an invalid common-mode condition.	C
IN+	3	VIN–	Both inputs are tied together. Depending on the offset of the device, the output voltage can move to near midsupply.	D
IN–	4	V+	The device does not receive negative feedback. Depending on the noninverting input voltage and circuit configuration, the output can move to the negative supply.	B
V+	5	OUT	Depending on the circuit configuration, the device is forced into a short-circuit condition with the V+ voltage forced to the OUT voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
OUT	1	Depending on the circuit configuration, the device can be forced into a short-circuit condition with the OUT voltage ultimately forced to the V+ voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
V–	2	Op amp supplies are shorted together, leaving the V– pin at some voltage between the V– and V+ sources (depending on the source impedance).	A
IN+	3	Depending on the circuit configuration, the application cannot function because device common-mode voltage is connected to IN+.	B
IN–	4	The device does not receive negative feedback. Depending on the noninverting input voltage and circuit configuration, the output can move to the negative supply.	B

4.2 SOT-SC70 (DCK) – 5 Package

Figure 4-2 shows the TLV9161-Q1 pin diagram for the SOT-SC70 (DCK) – 5 package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TLV9161-Q1 datasheet.

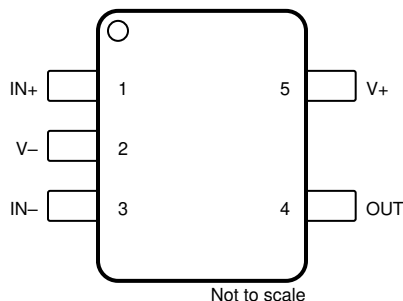


Figure 4-2. Pin Diagram (SOT-SC70 (DCK) – 5 Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN+	1	Device common-mode is tied to the negative rail. Depending on the circuit configuration, the output does not respond because the device is in an invalid, common-mode condition.	C
IN–	3	The device does not receive negative feedback. Depending on the circuit configuration, the output moves to the negative supply.	B
OUT	4	Depending on the circuit configuration, the device is forced into a short-circuit condition with the OUT voltage ultimately forced to the V– voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
V+	5	Op amp supplies are shorted together, leaving the V+ pin at some voltage between the V+ and V– sources (depending on the source impedance).	A

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN+	1	Device common-mode is disconnected. The op amp is not provided with common-mode bias, and the device output results at the positive or negative rail. The IN+ pin voltage results at the positive or negative rail because of leakages on the ESD diodes.	B
V–	2	The negative supply remains floating. The op amp ceases to function because no current can source or sink to the device.	B
IN–	3	The inverting pin of the op amp is left floating. Negative feedback is not provided to the device, resulting in the device output moving between the positive and negative rails. The IN– pin voltage ends up at the positive or negative rail because of leakages on the ESD diodes.	B
OUT	4	There is no negative feedback or ability for OUT to drive the application.	B
V+	5	The positive supply is left floating. The op amp ceases to function because no current sources or sinks to the device.	A

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
IN+	1	V–	Device common-mode is tied to the negative rail. Depending on the circuit configuration, the output does not respond because the device is in an invalid common-mode condition.	C
V–	2	IN–	The device does not receive negative feedback. Depending on the circuit configuration, the output moves to the negative supply.	B
IN–	3	OUT	Depending on the circuit configuration, the circuit gain is reduced to unity gain, and the application cannot function as intended.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
OUT	4	V+	Depending on the circuit configuration, the device is likely to be forced into a short-circuit condition with the OUT voltage ultimately forced to the V+ voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A
V+	5	IN+	Depending on the circuit configuration, the application likely does not function because device common-mode voltage is connected to V+.	B

Table 4-9. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
IN+	1	Depending on the circuit configuration, the application does not function because device common-mode voltage is connected to IN+.	B
V–	2	Op amp supplies are shorted together, leaving the V– pin at a voltage amount between the V– and V+ sources (depending on the source impedance).	A
IN–	3	The device does not receive negative feedback. Depending on the noninverting input voltage and circuit configuration, the output can move to the negative supply.	B
OUT	4	Depending on the circuit configuration, the device is forced into a short-circuit condition with the OUT voltage forced to the V+ voltage. Prolonged exposure to short-circuit conditions can result in long-term reliability issues.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2026	*	Initial Release

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025