Functional Safety Information

CD74HC4067-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

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1 Overview

This document contains information for the CD74HC4067-Q1 (DW (SOIC, 24), RGY (QFN, 24), DGS (VSSOP, 24), and PW (TSSOP, 24) packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

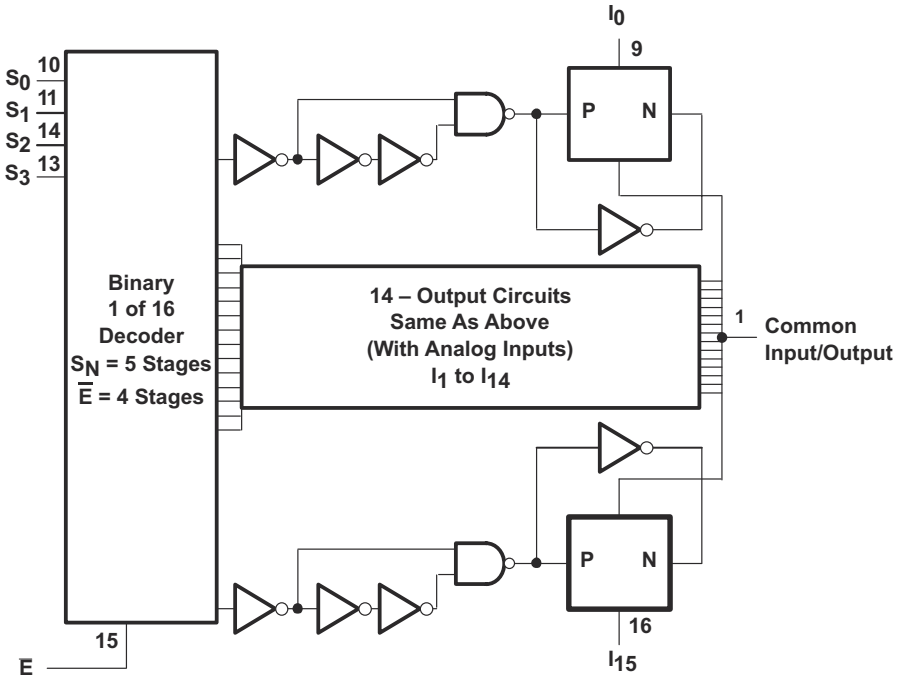

Figure 1-1. Functional Block Diagram

The CD74HC4067-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 DW (SOIC, 24) Package

This section provides functional safety failure in time (FIT) rates for the DW (SOIC, 24) package of the CD74HC4067-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	21
Die FIT rate	3
Package FIT rate	18

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 100mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): From table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 RGY (QFN, 24) Package

This section provides functional safety failure in time (FIT) rates for the RGY (QFN, 24) package of the CD74HC4067-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	13
Die FIT rate	3
Package FIT rate	10

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 and figure 16
- Power dissipation: 100mW
- Climate type: World-wide table 8 and figure 13
- Package factor (lambda 3): From table 17b and figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.3 DGS (VSSOP, 24) Package

This section provides functional safety failure in time (FIT) rates for the DGS (VSSOP, 24) package of the CD74HC4067-Q1 based on two different industry-wide used reliability standards:

- Table 2-5 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-6 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-5. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	15
Die FIT rate	3
Package FIT rate	12

The failure rate and mission profile information in Table 2-5 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 and figure 16
- Power dissipation: 100mW
- Climate type: World-wide table 8 and figure 13
- Package factor (lambda 3): From table 17b and figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-6. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-6 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.4 PW (TSSOP, 24) Package

This section provides functional safety failure in time (FIT) rates for the PW (TSSOP, 24) package of the CD74HC4067-Q1 based on two different industry-wide used reliability standards:

- Table 2-7 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-8 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-7. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	21
Die FIT rate	3
Package FIT rate	18

The failure rate and mission profile information in Table 2-7 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 and figure 16
- Power dissipation: 100mW
- Climate type: World-wide table 8 and figure 13
- Package factor (lambda 3): From table 17b and figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-8. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-8 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the CD74HC4067-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Switch channel stuck on	10
Switch channel stuck off	10
Switch functional – Out of specification leakage	40
Switch functional – Out of specification voltage or timing	40

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the CD74HC4067-Q1 (DW (SOIC, 24), RGY (QFN, 24), DGS (VSSOP, 24), and PW (TSSOP, 24) packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2, Table 4-6, Table 4-10, and Table 4-14)
- Pin open-circuited (see Table 4-3, Table 4-7, Table 4-11, and Table 4-15)
- Pin short-circuited to an adjacent pin (see Table 4-4, Table 4-8, Table 4-12, and Table 4-16)
- Pin short-circuited to supply (see Table 4-5, Table 4-9, Table 4-13, and Table 4-17)

Table 4-2 through Table 4-17 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

4.1 DW (SOIC, 24) Package

Figure 4-1 shows the CD74HC4067-Q1 pin diagram for the DW (SOIC, 24) package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the CD74HC4067-Q1 datasheet.

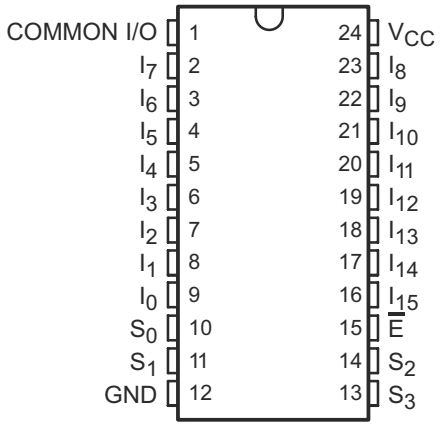

Figure 4-1. Pin Diagram (DW (SOIC, 24)) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
COMMON I/O	1	There is corruption of the signal passed onto the IX pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I7	2	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I6	3	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I5	4	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I4	5	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I3	6	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I2	7	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I1	8	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I0	9	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
S0	10	The address is stuck low. The pin cannot control switch states.	B
S1	11	The address is stuck low. The pin cannot control switch states.	B
GND	12	There is no effect on the device. The device operates as normal.	D
S3	13	The address is stuck low. The pin cannot control switch states.	B
S2	14	The address is stuck low. The pin cannot control switch states.	B
$\overline{E}$	15	EN is stuck low. The pin can no longer disables the device without a power down.	B
I15	16	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I14	17	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I13	18	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I12	19	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I11	20	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I10	21	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I19	22	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I18	23	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
VCC	24	The device is not powered. The device is not functional. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is plausible.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
COMMON I/O	1	There is corruption of the signal passed onto the IX pin.	B
I7	2	There is corruption of the signal passed onto the COMMON pin.	B
I6	3	There is corruption of the signal passed onto the COMMON pin.	B
I5	4	There is corruption of the signal passed onto the COMMON pin.	B
I4	5	There is corruption of the signal passed onto the COMMON pin.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
I3	6	There is corruption of the signal passed onto the COMMON pin.	B
I2	7	There is corruption of the signal passed onto the COMMON pin.	B
I1	8	There is corruption of the signal passed onto the COMMON pin.	B
I0	9	There is corruption of the signal passed onto the COMMON pin.	B
S0	10	The address is stuck low. The pin cannot control switch states.	B
S1	11	The address is stuck low. The pin cannot control switch states.	B
GND	12	There is no effect on the device. The device operates as normal.	A
S3	13	The address is stuck low. The pin cannot control switch states.	B
S2	14	The address is stuck low. The pin cannot control switch states.	B
$\overline{E}$	15	EN is stuck low. The pin no longer disables the device without a power down.	B
I15	16	There is corruption of the signal passed onto the COMMON pin.	B
I14	17	There is corruption of the signal passed onto the COMMON pin.	B
I13	18	There is corruption of the signal passed onto the COMMON pin.	B
I12	19	There is corruption of the signal passed onto the COMMON pin.	B
I11	20	There is corruption of the signal passed onto the COMMON pin.	B
I10	21	There is corruption of the signal passed onto the COMMON pin.	B
I9	22	There is corruption of the signal passed onto the COMMON pin.	B
I8	23	There is corruption of the signal passed onto the COMMON pin.	B
VCC	24	The device is not powered. The device is not functional.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
COMMON I/O	1	I7	There is possible corruption of the signal passed on to the IX pin.	B
I7	2	I6	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I6	3	I5	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I5	4	I4	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I4	5	I3	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I3	6	I2	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I2	7	I1	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I1	8	I0	Possible corruption of the signal passed on to the IX and COMMON pin.	B
I0	9	S0	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
S0	10	S1	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
S1	11	GND	There is possible damage to device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible.	A
GND	12	S3	There is possible damage to device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible.	A
S3	13	S2	Control of the address pin is lost. The pin cannot control switch states.	B
S2	14	$\overline{E}$	There is possible corruption of the signal passed onto the COMMON pin. The switch state is undefined.	B
$\overline{E}$	15	I15	There is possible corruption of the signal passed onto the COMMON pin. The switch state is undefined.	B
I15	16	I14	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I14	17	I13	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I13	18	I12	There is possible corruption of the signal passed on to the IX and COMMON pin.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
I12	19	I11	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I11	20	I10	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I10	21	I9	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I9	22	I8	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I8	23	VCC	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
VCC	24	COMMON I/O	This pin is not considered. This pin is a corner pin.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
COMMON I/O	1	There is corruption of the signal passed on to the IX pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I7	2	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I6	3	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I5	4	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I4	5	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I3	6	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I2	7	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I1	8	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I0	9	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
S0	10	The address is stuck high. The pin cannot control switch states.	B
S1	11	The address is stuck high. The pin cannot control switch states.	B
GND	12	The device is not powered and not functional. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible.	A
S3	13	The address is stuck high. The pin cannot control switch states.	B
S2	14	The address is stuck high. The pin cannot control switch states.	B
$\overline{E}$	15	EN is stuck high. The pin can no longer enable the device.	B
I15	16	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I14	17	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I13	18	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I12	19	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I11	20	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I10	21	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I9	22	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
I8	23	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
VCC	24	There is no effect on the device. The device operates as normal.	D

4.2 RGY (QFN, 24) Package

Figure 4-2 shows the CD74HC4067-Q1 pin diagram for the RGY (QFN, 24) package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the CD74HC4067-Q1 datasheet.

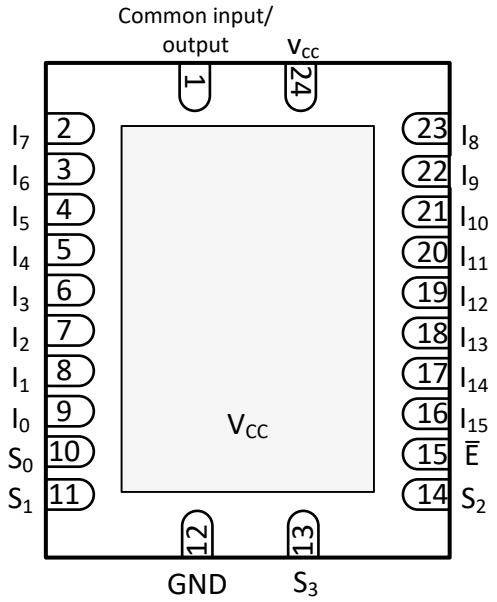

Figure 4-2. Pin Diagram (RGY (QFN, 24) Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
COMMON I/O	1	There is corruption of the signal passed onto the IX pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I7	2	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I6	3	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I5	4	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I4	5	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I3	6	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I2	7	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I1	8	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I0	9	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
S0	10	The address is stuck low. The pin cannot control switch states.	B
S1	11	The address is stuck low. The pin cannot control switch states.	B
GND	12	There is no effect on the device. The device operates as normal.	D
S3	13	The address is stuck low. The pin cannot control switch states.	B
S2	14	The address is stuck low. The pin cannot control switch states.	B
$\overline{E}$	15	EN is stuck low. The pin can no longer disable the device without a power down.	B
I15	16	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I14	17	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I13	18	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I12	19	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I11	20	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I10	21	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I9	22	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I8	23	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
VCC	24	The device is not powered. The device is not functional. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible.	A
Thermal Pad	–	There is no effect on the device. The device operates as normal.	D

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
COMMON I/O	1	There is corruption of the signal passed onto the IX pin.	B
I7	2	There is corruption of the signal passed onto the COMMON pin.	B
I6	3	There is corruption of the signal passed onto the COMMON pin.	B
I5	4	There is corruption of the signal passed onto the COMMON pin.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
I4	5	There is corruption of the signal passed onto the COMMON pin.	B
I3	6	There is corruption of the signal passed onto the COMMON pin.	B
I2	7	There is corruption of the signal passed onto the COMMON pin.	B
I1	8	There is corruption of the signal passed onto the COMMON pin.	B
I0	9	There is corruption of the signal passed onto the COMMON pin.	B
S0	10	The address is stuck low. The pin cannot control switch states.	B
S1	11	The address is stuck low. The pin cannot control switch states.	B
GND	12	There is no effect on the device. The device operates as normal.	A
S3	13	The address is stuck low. The pin cannot control switch states.	B
S2	14	The address is stuck low. The pin cannot control switch states.	B
$\overline{E}$	15	EN is stuck low. The pin can no longer disable the device without a power down.	B
I15	16	There is corruption of the signal passed onto the COMMON pin.	B
I14	17	There is corruption of the signal passed onto the COMMON pin.	B
I13	18	There is corruption of the signal passed onto the COMMON pin.	B
I12	19	There is corruption of the signal passed onto the COMMON pin.	B
I11	20	There is corruption of the signal passed onto the COMMON pin.	B
I10	21	There is corruption of the signal passed onto the COMMON pin.	B
I9	22	There is corruption of the signal passed onto the COMMON pin.	B
I8	23	There is corruption of the signal passed onto the COMMON pin.	B
VCC	24	The device is not powered. The device is not functional.	B
Thermal Pad	–	There is no effect on the device. The device operates as normal.	

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
COMMON I/O	1	I7	There is possible corruption of the signal passed on to the IX pin.	B
I7	2	I6	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I6	3	I5	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I5	4	I4	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I4	5	I3	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I3	6	I2	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I2	7	I1	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I1	8	I0	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I0	9	S0	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
S0	10	S1	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
S1	11	GND	There is possible damage to the device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible.	A
GND	12	S3	There is possible damage to the device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible.	A
S3	13	S2	Control of the address pin is lost. The pin cannot control switch states.	B
S2	14	$\overline{E}$	There is possible corruption of the signal passed onto the COMMON pin. The switch state is undefined.	B
$\overline{E}$	15	I15	There is possible corruption of the signal passed onto the COMMON pin. The switch state is undefined.	B
I15	16	I14	There is possible corruption of the signal passed on to the IX and COMMON pin.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
I14	17	I13	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I13	18	I12	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I12	19	I11	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I11	20	I10	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I10	21	I9	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I9	22	I8	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I8	23	VCC	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
VCC	24	COMMON I/O	This pin is not considered. This is a corner pin.	D

Table 4-9. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
COMMON I/O	1	There is corruption of the signal passed on to the IX pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I7	2	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I6	3	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I5	4	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I4	5	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I3	6	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I2	7	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I1	8	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I0	9	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
S0	10	The address is stuck high. The pin cannot control switch states.	B
S1	11	The address is stuck high. The pin cannot control switch states.	B
GND	12	The device is not powered and not functional. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible.	A
S3	13	The address is stuck high. The pin cannot control switch states.	B
S2	14	The address is stuck high. The pin cannot control switch states.	B
$\overline{E}$	15	EN is stuck high. The pin can no longer enable the device.	B
I15	16	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I14	17	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I13	18	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I12	19	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I11	20	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I10	21	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A

Table 4-9. Pin FMA for Device Pins Short-Circuited to Supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
I9	22	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I8	23	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
VCC	24	There is no effect on the device. The device operates as normal.	D
Thermal Pad	–	No connect pin electrically floating, there is no effect on the device.	D

4.3 DGS (VSSOP, 24) Package

Figure 4-3 shows the CD74HC4067-Q1 pin diagram for the DGS (VSSOP, 24) package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the CD74HC4067-Q1 datasheet.

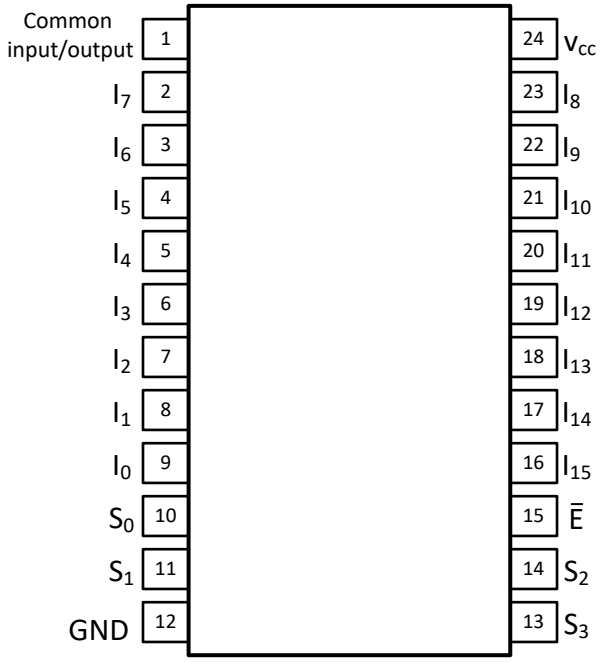

Figure 4-3. Pin Diagram (DGS (VSSOP, 24) Package)

Table 4-10. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
COMMON I/O	1	There is corruption of the signal passed onto the IX pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I7	2	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I6	3	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I5	4	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I4	5	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I3	6	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I2	7	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I1	8	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I0	9	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
S0	10	The address is stuck low. The pin cannot control switch states.	B
S1	11	The address is stuck low. The pin cannot control switch states.	B
GND	12	There is no effect on the device. The device operates as normal.	D
S3	13	The address is stuck low. The pin cannot control switch states.	B
S2	14	The address is stuck low. The pin cannot control switch states.	B
$\overline{E}$	15	EN is stuck low. The pin can no longer disable the device without a power down.	B
I15	16	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I14	17	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I13	18	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I12	19	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I11	20	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I10	21	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I19	22	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I18	23	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
VCC	24	The device is not powered. The device is not functional. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is plausible.	A

Table 4-11. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
COMMON I/O	1	There is corruption of the signal passed onto the IX pin.	B
I7	2	There is corruption of the signal passed onto the COMMON pin.	B
I6	3	There is corruption of the signal passed onto the COMMON pin.	B
I5	4	There is corruption of the signal passed onto the COMMON pin.	B
I4	5	There is corruption of the signal passed onto the COMMON pin.	B

Table 4-11. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
I3	6	There is corruption of the signal passed onto the COMMON pin.	B
I2	7	There is corruption of the signal passed onto the COMMON pin.	B
I1	8	There is corruption of the signal passed onto the COMMON pin.	B
I0	9	There is corruption of the signal passed onto the COMMON pin.	B
S0	10	The address is stuck low. The pin cannot control switch states.	B
S1	11	The address is stuck low. The pin cannot control switch states.	B
GND	12	There is no effect on the device. The device operates as normal.	A
S3	13	The address is stuck low. The pin cannot control switch states.	B
S2	14	The address is stuck low. The pin cannot control switch states.	B
$\overline{E}$	15	EN is stuck low. The pin can no longer disable the device without a power down.	B
I15	16	There is corruption of the signal passed onto the COMMON pin.	B
I14	17	There is corruption of the signal passed onto the COMMON pin.	B
I13	18	There is corruption of the signal passed onto the COMMON pin.	B
I12	19	There is corruption of the signal passed onto the COMMON pin.	B
I11	20	There is corruption of the signal passed onto the COMMON pin.	B
I10	21	There is corruption of the signal passed onto the COMMON pin.	B
I9	22	There is corruption of the signal passed onto the COMMON pin.	B
I8	23	There is corruption of the signal passed onto the COMMON pin.	B
VCC	24	The device is not powered. The device is not functional.	B

Table 4-12. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
COMMON I/O	1	I7	There is possible corruption of the signal passed on to the IX pin.	B
I7	2	I6	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I6	3	I5	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I5	4	I4	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I4	5	I3	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I3	6	I2	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I2	7	I1	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I1	8	I0	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I0	9	S0	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
S0	10	S1	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
S1	11	GND	There is possible damage to the device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible.	A
GND	12	S3	This pin is not considered. This is a corner pin.	D
S3	13	S2	Control of the address pin is lost. The pin cannot control switch states.	B
S2	14	$\overline{E}$	There is possible corruption of the signal passed onto the COMMON pin. The switch state is undefined.	B
$\overline{E}$	15	I15	There is possible corruption of the signal passed onto the COMMON pin. The switch state is undefined.	B
I15	16	I14	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I14	17	I13	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I13	18	I12	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I12	19	I11	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I11	20	I10	There is possible corruption of the signal passed on to the IX and COMMON pin.	B

Table 4-12. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
I10	21	I9	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I9	22	I8	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I8	23	VCC	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
VCC	24	COMMON I/O	This pin is not considered. This is a corner pin.	D

Table 4-13. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
COMMON I/O	1	There is corruption of the signal passed on to the IX pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I7	2	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I6	3	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I5	4	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I4	5	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I3	6	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I2	7	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I1	8	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I0	9	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
S0	10	The address is stuck high. The pin cannot control switch states.	B
S1	11	The address is stuck high. The pin cannot control switch states.	B
GND	12	The device is not powered and not functional. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible.	A
S3	13	The address is stuck high. The pin cannot control switch states.	B
S2	14	The address is stuck high. The pin cannot control switch states.	B
$\overline{E}$	15	EN is stuck high. The pin can no longer enable the device.	B
I15	16	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I14	17	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I13	18	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I12	19	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I11	20	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I10	21	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I9	22	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I8	23	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
VCC	24	There is no effect on the device. The device operates as normal.	D

4.4 PW (TSSOP, 24) Package

Figure 4-4 shows the CD74HC4067-Q1 pin diagram for the PW (TSSOP, 24) package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the CD74HC4067-Q1 datasheet.

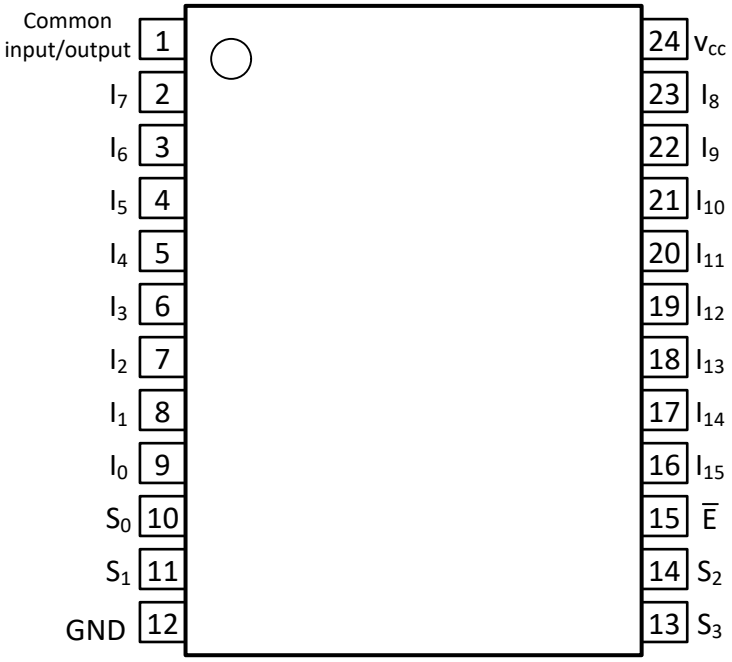

Figure 4-4. Pin Diagram (PW (TSSOP, 24) Package)

Table 4-14. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
COMMON I/O	1	There is corruption of the signal passed onto the IX pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I7	2	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I6	3	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I5	4	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I4	5	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I3	6	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I2	7	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I1	8	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I0	9	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
S0	10	The address is stuck low. The pin cannot control switch states.	B
S1	11	The address is stuck low. The pin cannot control switch states.	B
GND	12	There is no effect on the device. The device operates as normal.	D
S3	13	The address is stuck low. The pin cannot control switch states.	B
S2	14	The address is stuck low. The pin cannot control switch states.	B
$\overline{E}$	15	EN is stuck low. The pin can no longer disable the device without a power down.	B
I15	16	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I14	17	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I13	18	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I12	19	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I11	20	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I10	21	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I19	22	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I18	23	There is corruption of the signal passed onto the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
VCC	24	The device is not powered. The device is not functional. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is plausible.	A

Table 4-15. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
COMMON I/O	1	There is corruption of the signal passed onto the IX pin.	B
I7	2	There is corruption of the signal passed onto the COMMON pin.	B
I6	3	There is corruption of the signal passed onto the COMMON pin.	B
I5	4	There is corruption of the signal passed onto the COMMON pin.	B
I4	5	There is corruption of the signal passed onto the COMMON pin.	B

Table 4-15. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
I3	6	There is corruption of the signal passed onto the COMMON pin.	B
I2	7	There is corruption of the signal passed onto the COMMON pin.	B
I1	8	There is corruption of the signal passed onto the COMMON pin.	B
I0	9	There is corruption of the signal passed onto the COMMON pin.	B
S0	10	The address is stuck low. The pin cannot control switch states.	B
S1	11	The address is stuck low. The pin cannot control switch states.	B
GND	12	There is no effect on the device. The device operates as normal.	A
S3	13	The address is stuck low. The pin cannot control switch states.	B
S2	14	The address is stuck low. The pin cannot control switch states.	B
$\overline{E}$	15	EN is stuck low. The pin can no longer disable the device without a power down.	B
I15	16	There is corruption of the signal passed onto the COMMON pin.	B
I14	17	There is corruption of the signal passed onto the COMMON pin.	B
I13	18	There is corruption of the signal passed onto the COMMON pin.	B
I12	19	There is corruption of the signal passed onto the COMMON pin.	B
I11	20	There is corruption of the signal passed onto the COMMON pin.	B
I10	21	There is corruption of the signal passed onto the COMMON pin.	B
I9	22	There is corruption of the signal passed onto the COMMON pin.	B
I8	23	There is corruption of the signal passed onto the COMMON pin.	B
VCC	24	The device is not powered. The device is not functional.	B

Table 4-16. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
COMMON I/O	1	I7	There is possible corruption of the signal passed on to the IX pin.	B
I7	2	I6	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I6	3	I5	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I5	4	I4	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I4	5	I3	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I3	6	I2	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I2	7	I1	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I1	8	I0	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I0	9	S0	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
S0	10	S1	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
S1	11	GND	There is possible damage to the device if the signal voltage is negative. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible.	B
GND	12	S3	This pin is not considered. This is a corner pin.	D
S3	13	S2	Control of the address pin is lost. The pin cannot control switch states.	B
S2	14	$\overline{E}$	There is possible corruption of the signal passed onto the COMMON pin. The switch state is undefined.	B
$\overline{E}$	15	I15	There is possible corruption of the signal passed onto the COMMON pin. The switch state is undefined.	B
I15	16	I14	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I14	17	I13	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I13	18	I12	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I12	19	I11	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I11	20	I10	There is possible corruption of the signal passed on to the IX and COMMON pin.	B

Table 4-16. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
I10	21	I9	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I9	22	I8	There is possible corruption of the signal passed on to the IX and COMMON pin.	B
I8	23	VCC	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
VCC	24	COMMON I/O	This pin is not considered. This is a corner pin.	D

Table 4-17. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
COMMON I/O	1	There is corruption of the signal passed on to the IX pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I7	2	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I6	3	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I5	4	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I4	5	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I3	6	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I2	7	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I1	8	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I0	9	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
S0	10	The address is stuck high. The pin cannot control switch states.	B
S1	11	The address is stuck high. The pin cannot control switch states.	B
GND	12	The device is not powered and not functional. Observe that the absolute maximum ratings for all pins of the device are met; otherwise, damage to the device is possible.	A
S3	13	The address is stuck high. The pin cannot control switch states.	B
S2	14	The address is stuck high. The pin cannot control switch states.	B
$\overline{E}$	15	EN is stuck high. The pin can no longer enable the device.	B
I15	16	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I14	17	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I13	18	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I12	19	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I11	20	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I10	21	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I9	22	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
I8	23	There is corruption of the signal passed on to the COMMON pin. If there is no limiting resistor in the switch path, then device damage is possible.	A
VCC	24	There is no effect on the device. The device operates as normal.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2026	*	Initial Release

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