

FACT SHEET

Military Semiconductor Products

SNJ55LVDS31 / 5962-9762101QXA,
SNJ55LVDS32 / 5962-9762201QXA

SGYV064, January 1999

QUAD HIGH-SPEED LVDS DIFFERENTIAL DRIVERS AND RECEIVERS

HIGHLIGHTS

A new quadruple differential line driver and receiver from Texas Instruments offers lower power and higher data rates for point-to-point baseband data transmission over controlled impedance media of 100 ohms. The transmission media may be printed circuit board traces, backplanes or cables. This driver and receiver are ideal in applications such as telecommunications and computing.

These devices, designated the SN55LVDS31 for the driver and SN55LVDS32 for the receiver, implement the electrical characteristics of Low Voltage Differential Signaling (LVDS). This signaling technique lowers the output voltage levels of 5 V differential standard levels to reduce the power, increase the switching speeds and allow operation with a 3.3 V supply rail. Any of the four current-mode drivers will deliver a minimum differential output voltage magnitude of 247 mV into a 100 ohm load when enabled by either an active-low or active-high enable input. Any of the four differential receivers will provide a valid logical output state with a +/-100 mV differential input voltage within the input common-mode voltage range. The input common-mode voltage range allows 1 V of ground potential difference between two LVDS nodes.

KEY FEATURES/BENEFITS

- Meets or Exceeds the Requirements of ANSI TIA/EIA-644 Standard
- Low-Voltage Differential Signaling
- Operates from a Single 3.3-V Supply
- Designed for Signaling Rate of Up To 400 Mbps
- Typical Propagation Delay Time of 2.2 ns
- Power Dissipation < = 60 mW Typical
- Bus-Terminal ESD Protection Exceeds 8 kV
- Low-Voltage TTL (LVTTTL) Logic Output/Input Levels
- Pin-Compatible with the AM26LS3x, AM26C3x

DIE SIZE

The current die has a size of: 56 mils x 55 mils.

TECHNOLOGY

- LinBiCMOS™ Process
- Class 3 ESD rating per MIL-STD-883, Method 3015

PACKAGING

Package Option: 16-pin Ceramic Dual in Line Package (JG)
16-pin Ceramic Flat Package (W)
20-pin Leadless Ceramic Chip Carrier (FK)

POWER DISSIPATION

The table below shows modeled data. This data can be used for approximating system thermal characteristics:

Package Thermal Data

Package	R_{θJA}	R_{θJC}
16 Pin DIP	90° C/W	28° C/W
16 Pin Flat Pack	165° C/W	22° C/W
20 Pin LCC	65° C/W	20° C/W

Note: Much better thermal impedances can be achieved by using air flow, or with increasing metal backplane thickness or trace area in the Printed Circuit Board (PCB) that is used.

PROCESS/PERFORMANCE OPTIONS

These LVDS drivers and receivers are processed to MIL-PRF-38535. The DESC Standard Microcircuit Drawings (SMD) for these devices are below.

DSCC SMD

TI Parent	DSCC SMD
SNJ55LVDS31J/FK/W	5962-9762101QEA / 2A / FA
SNJ55LVDS32J/FK/W	5962-9762201QEA / 2A / FA

SUPPORT

For additional information on this and other Data Transmission Products, general questions regarding LVDS visit our Mixed Signal and Analog home page at:

http://www.ti.com/sc/docs/military/product/mix_sig/mixsig_1.htm

Additional information regarding this product is available by calling the Texas Instruments Product Information Center (PIC) at (972) 644-5580 during normal business hours (CST/CDT).

For European PIC information visit <http://www.ti.com/sc/docs/pic/home.htm>

SUPPORT LITERATURE

You can access data sheets via TI's home page on the internet (<http://www.ti.com>) or reference the literature numbers SLLS261D or SLLS262E when contacting the PIC.

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