Application Note

How to Avoid Distortion in TAS58xx

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ABSTRACT

This document was translated from a simplified Chinese source. (ZHCAG97)

TI Class-D audio power amplifier ICs are widely used in consumer electronics and automotive applications due to their high performance, high efficiency, and high fidelity. Among them, flagship products such as the TAS58xx series are extensively utilized in TVs, speakers, soundbars, party boxes, and other fields. The TAS58xx series represents advanced closed-loop architecture Class-D amplifiers introduced by TI for the consumer electronics sector. Compared to open-loop Class-D amplifiers, the closed-loop Class-D architecture significantly reduces distortion by correcting errors introduced by the power stage, filter stage, and non-linear switching. The THD+N of a closed-loop Class-D amplifier is much lower than that of an open-loop Class-D amplifier. Properly designing and applying TI's closed-loop TAS58xx can yield a high-fidelity audio system. There are many stages in a Class-D power amplifier where distortion can be introduced. The most common ones are non-linearity in the power stage and distortion during digital signal processing. This paper briefly explores the basic principles of common distortions, as well as the factors that may cause distortion when designing an audio power amplifier system and their corresponding solutions.

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1 Maximum Non-Clipping Voltage Output by Class-D Amplifiers

To prevent signal distortion after Class-D amplification, it is essential to first determine the maximum voltage that the Class-D amplifier can output. The TAS58xx utilizes BD/1SPW/Hybrid mode modulation to generate a high-frequency PWM wave in the full-bridge circuit, which is then filtered by the subsequent magnetic beads or LC filter to obtain an amplified high-fidelity analog audio signal. Theoretically, a larger input signal leads to a higher PWM duty cycle in the subsequent power stage, resulting in a higher output voltage; when the modulated PWM reaches a 100% duty cycle, the subsequent speaker receives the maximum non-clipped voltage. For instance, when PVDD = 12V, the maximum non-clipping sinusoidal voltage peak that the subsequent stage can obtain is ±12V. However, in practical circuits, the internal resistance of the MOSFETs and inductors creates a voltage drop, so the maximum voltage actually achieved by the speaker will be slightly lower than PVDD.

The simplified Class-D circuit is shown in Figure 1-1 below. Taking into account the voltage division effect of the MOSFET and inductor internal resistance, the maximum voltage that the load can actually receive is:

$$V_{load} = PVDD \times R_{load} / \left(R_{load} + 2 \times \left(Z_{DC} + R_{DS(on)}\right)\right) \quad (1)$$

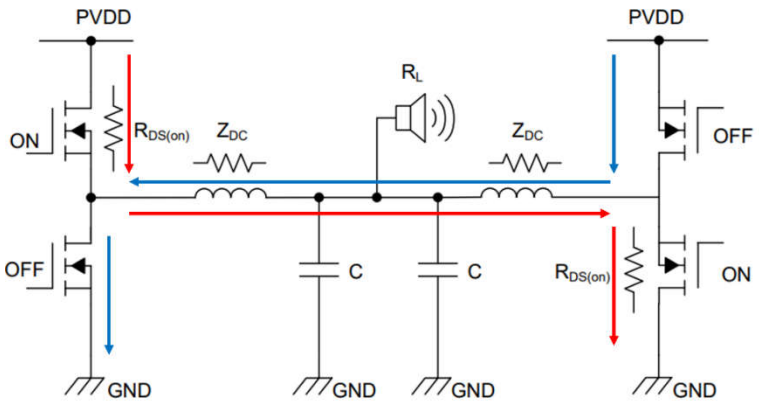

Figure 1-1. Class D Equivalent Circuit

2 Distortion Introduced at the Analog Stage

2.1 Clipping Distortion Caused by Low PVDD

To maintain a high-fidelity audio signal, PVDD must be kept larger than the amplitude of the audio signal, as indicated by the red curve in Figure 2-1 below; the blue curve represents the maximum non-clipped voltage that can be output under a specific PVDD. If the gain is further increased such that the desired output sinusoidal voltage amplitude exceeds PVDD, clipping distortion occurs, as shown by the green curve in Figure 2-1.

Under the default configuration of the TAS58xx series, a 0dB input signal corresponds to an output voltage of 29.5V, which means the default gain of the TAS58xx is approximately 26.4dBV. Under different gain configurations, the corresponding maximum output voltage and the minimum required PVDD are listed below, taking Rload = 4Ω, ESL = 2.3mΩ, and Rds(on) = 120mΩ as an example.

Volume	Analog gain	MAXIMUM Vout (PEAK)	Min PVDD requirement
0dB	0dB	29.5V	31.3V
0dB	-6dB	14.75V	15.65V
-6dB	-6dB	7.38V	7.83V

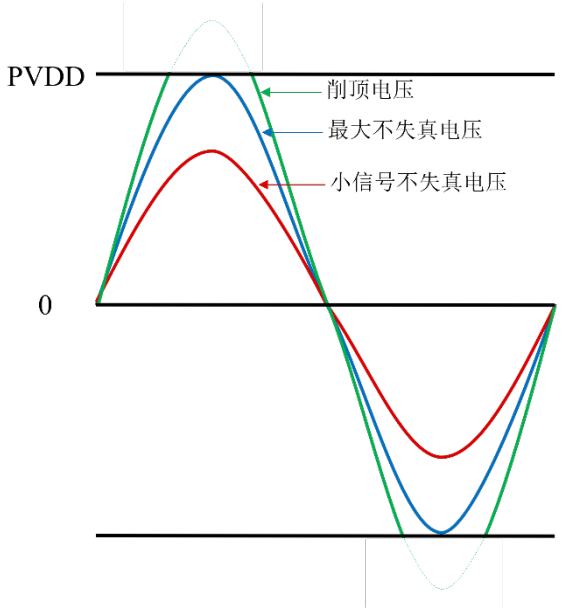

Figure 2-1. Schematic Diagram of Distortion Voltage

2.2 Distortion Due to Insufficient PVDD Power Supply

The common causes of clipping distortion directly resulting from an insufficient PVDD power supply are as follows. Therefore, sufficient margin should be reserved when designing the PVDD.

- In soundbar systems, the AC/DC power supply board typically exhibits errors. If a power supply error of 5% or 10% exists, it may lead to an insufficient PVDD power supply, where the actual PVDD voltage falls below the preset value, thereby causing clipping.
- The margin reserved in the design is insufficient, failing to fully account for the voltage division effects of the MOSFET on-resistance and the internal resistance ESL of the inductor.
- The capacitance connected in parallel at the PVDD terminal is insufficient, causing PVDD to sag or exhibit excessive ripple during the playback of high-dynamic audio (such as drumbeats), rendering the PVDD voltage at the ripple troughs inadequate.

2.3 Distortion Caused by Insufficient Class-H Boosting

In speaker and party box systems, the main power supply PVDD for the audio power amplifier is provided by a lithium battery through a BOOST converter. Audio signals typically exhibit a wide range of dynamic variations. An

inappropriate Class-H design can prevent PVDD from boosting in time; when the signal is output, PVDD has not yet completed its voltage boost to reach the predetermined value, resulting in distortion.

This is illustrated in Figure 2-2 and Figure 2-3 below. Since large capacitors are connected in parallel at the PVDD terminal, according to U=Q/C=I*T/C, lifting PVDD requires a substantial amount of charge, making the dynamic response of the Boost/Buck-Boost converter critical.

Another scenario involves applying a positive gain within the Crossbar while using the Class-H function. The operating principle of Class-H is to sense the signal amplitude in the digital domain, thereby controlling the external DCDC to generate a PVDD voltage that prevents signal distortion. This PVDD voltage will be slightly higher than the output signal. However, Class-H senses the signal prior to the Crossbar, as shown in Figure 2-4 below. Consequently, increasing the digital signal amplitude within the Crossbar will cause the actual output voltage signal to exceed the signal amplitude "seen" by Class-H, and the PVDD controlled by Class-H will fail to meet the requirements. In practical applications, gain can be increased in many places, but the Crossbar gain should be set with caution.

Comparison Diagram of Class-H Boosting

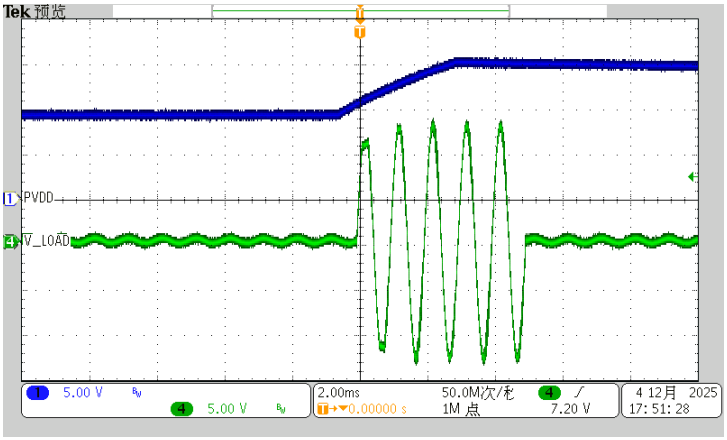

Figure 2-2. a) Class-H Distorted Waveform

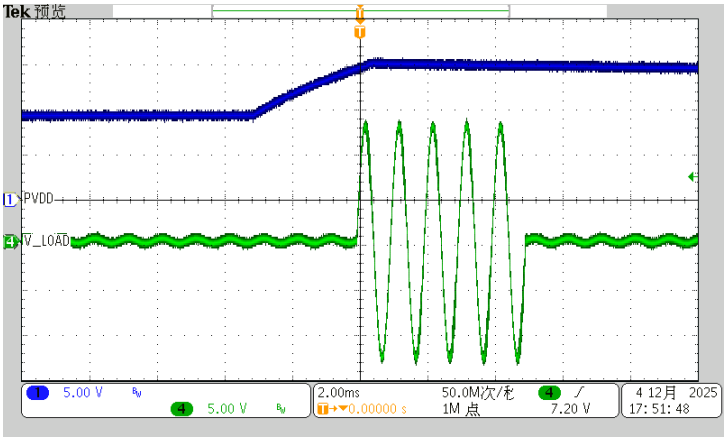

Figure 2-3. b) Class-H Undistorted Waveform

Figure 2-4. Class-H Flowchart in PPC3

2.4 Clipping Distortion Caused by Cycle-By-Cycle Current Limiting

Some TAS58xx power amplifiers, such as the TAS5827, incorporate dual overcurrent protection: first, Cycle-By-Cycle current limiting protection, and second, OCP shutdown.

6.5.1.47 CBC_CONTROL Register (Offset = 77h) [Reset = 00h]

CBC_CONTROL is shown in Figure 6-64 and described in Table 6-54.

Return to the Summary Table.

CBC control

Figure 6-64. CBC_CONTROL Register

7	6	5	4	3	2	1	0
RESERVED			CBCLEVEL_SEL		CBC_EN	CBCWARN_EN	CBCFAULT_EN
R/W-0h			R/W-0h		R/W-0h	R/W-0h	R/W-0h

Table 6-54. CBC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	
4-3	CBCLEVEL_SEL	R/W	0h	These bits set Cycle-By-Cycle current limiting level, which is a percentage of the Over-Current Threshold: **2b'00: 80%** 2b'10: 60% 2b'01: 40% 2b'11: reserved
2	CBC_EN	R/W	0h	**0: Disable CBC function** 1: Enable CBC function
1	CBCWARN_EN	R/W	0h	**0: Disable CBC warning** 1: Enable CBC warning
0	CBCFAULT_EN	R/W	0h	**0: Disable CBC fault** 1: Enable CBC fault

Figure 2-5. CBC Current Setting Register

The purpose of CBC current limiting protection is to restrict the inductor current to a fixed value when encountering large audio signals, in order to maintain high-power output without triggering an overcurrent shutdown. Taking the TAS5827 as an example, the CBC_CONTROL register 0x77 can enable the CBC Overcurrent Limit function and set the current limit value to 80%, 60%, or 40% of the overcurrent protection threshold OCETHRES.

The effect of the Overcurrent Limit is similar to Voltage-Clipping, which specifically manifests as current clipping, limiting the maximum playback current. Current clipping leads to voltage clipping, thereby causing clipping distortion of the output voltage signal. The figures below show the waveform comparison with CBC enabled and disabled, respectively.

Comparison of Current Waveforms with CBC Enabled/Disabled

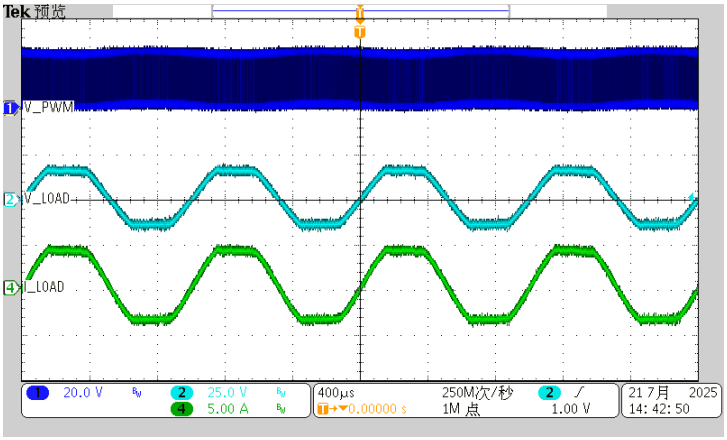

Figure 2-6. a) Current Waveform under Enabled CBC Limiting

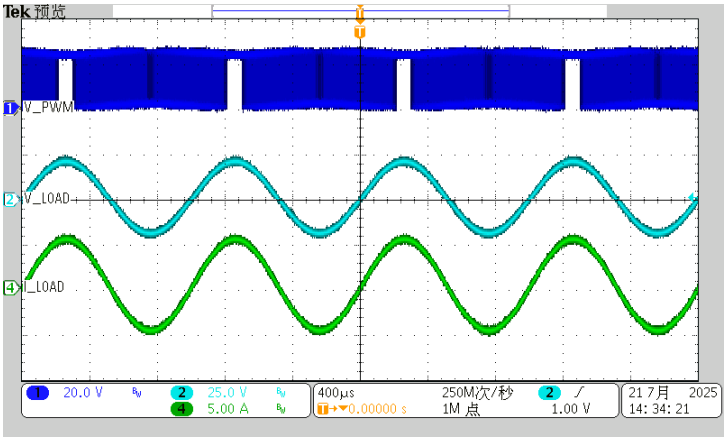

Figure 2-7. b) Current Waveform under Disabled CBC Limiting

3 Signal Distortion in the DSP Digital Domain

3.1 Distortion Caused by Digital Overflow

The TAS58xx is a high-performance digital-input audio power amplifier with an integrated DSP, allowing users to perform tuning, limiting, and other functions within the DSP.

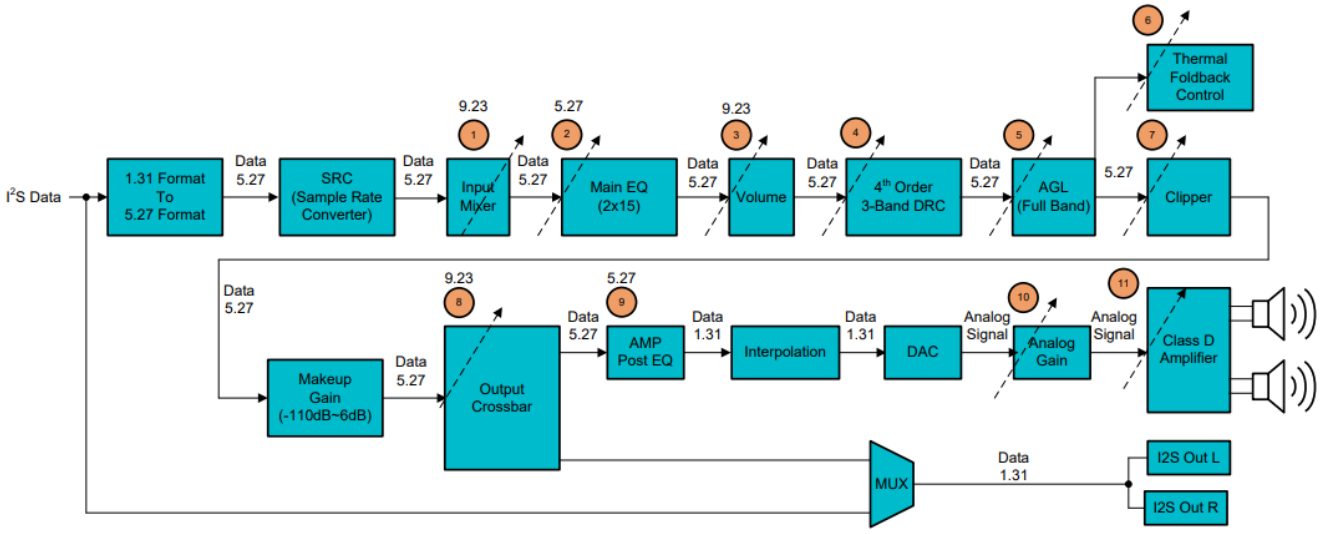

Figure 3-1. DSP Data Format of TAS58xx

The above figure shows the flowchart of the TAS58xx series, including modules such as SRC, DRC, EQ, and AGL. Different modules possess different DSP Headrooms, which correspond to different reserved spaces, and these reserved spaces correspond to different digital signal magnitudes. Taking the 9.23 format as an example, 9.23 indicates that within a 32-bit fixed-point number, there is 1 sign bit, 9 integer bits, and 23 fractional bits. The maximum gain corresponding to the 9.23 format is 20 × log M (2^((9-1))) = 48 dB. Similarly, the 5.27 format corresponds to 24 dB, and 1.31 corresponds to 0 dB.

The above Figure 3-1 includes the maximum gain adjustment capability of each functional module itself, as well as the signal magnitude limitations entering that functional module. Taking Volume and DRC as examples, the maximum gain that can be added in Volume is 48 dB, but the data signal entering the DRC cannot exceed 24 dB. Assuming the gains of the Input mixer and EQ are at their default value of 0 dB, and the input signal from the AP is at a maximum of 0 dB, even though the Volume can provide a gain of 48 dB, the gain setting of the Volume should not exceed 24 dB at most to ensure that the signal entering the DRC does not exceed 24 dB. Otherwise, the signal entering the DRC will exceed 24 dB, leading to digital overflow, and the high-order digits of the signal emerging from the DRC will be discarded, causing clipping distortion of the sinusoidal signal.

Measured Example: Under the default configuration of PPC3, the Volume gain of the power amplifier is set to 10 dB, and the Analog gain is set to -10 dB. Utilizing the AP to provide IIS input signals of -9 dB and -10 dB respectively, the output waveforms of SDOUT are as follows. SDOUT is the signal directly output by the power amplifier DSP. When the AP inputs a -9 dB signal and 10 dB is added in Volume, the signal entering the Interpolation becomes +1 dB, causing a digital overflow, which means the signal entering the DAC is already distorted. When the AP inputs a -10 dB signal, it just happens to avoid distortion.

Waveform Comparison of Digital Overflow in AP

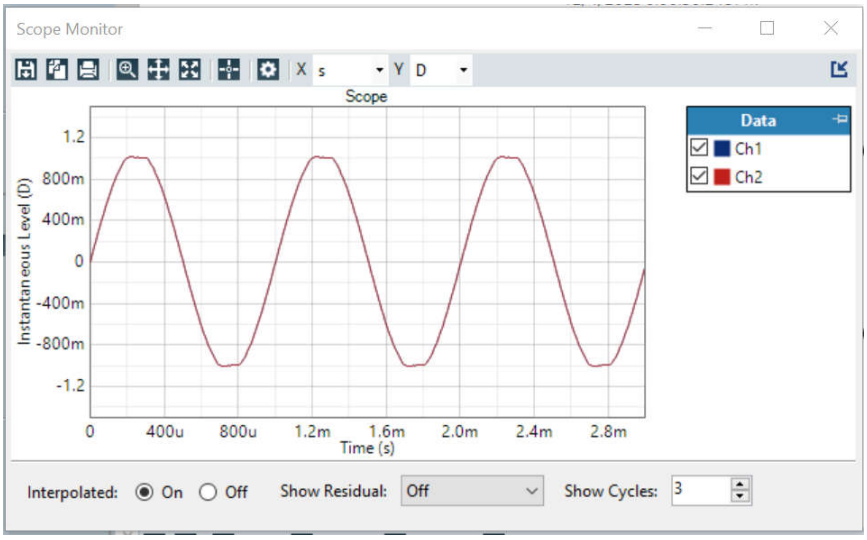

Figure 3-2. a) Distorted Waveform with input = -9dB

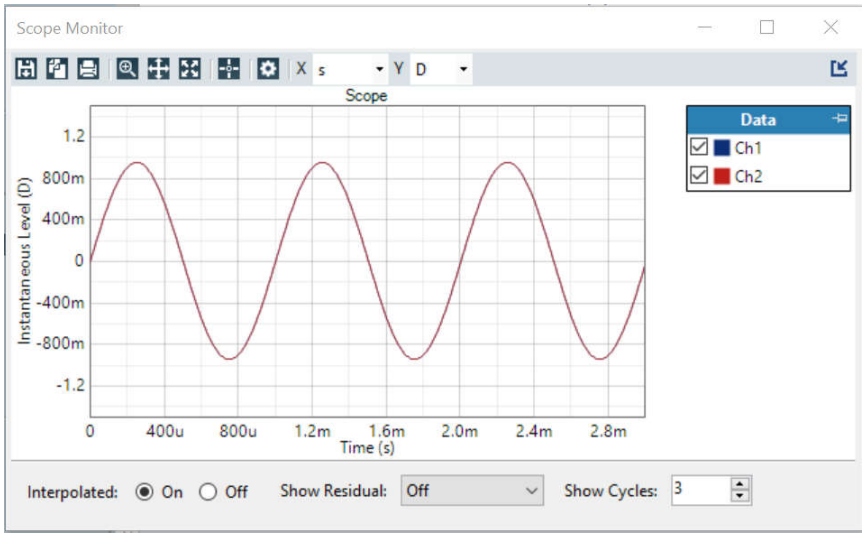

Figure 3-3. b) Undistorted Waveform with input = -10dB

3.2 Distortion Caused by Clipper Module Clipping

The PPC3 Clipper debugging interface is shown in Figure 3-4 above. Unlike DRC/AGL, the Clipper does not have an attack time or release time, nor does it automatically adjust the gain to attenuate the signal amplitude; instead, it directly clips the portion of the signal that exceeds the set threshold within the digital domain.

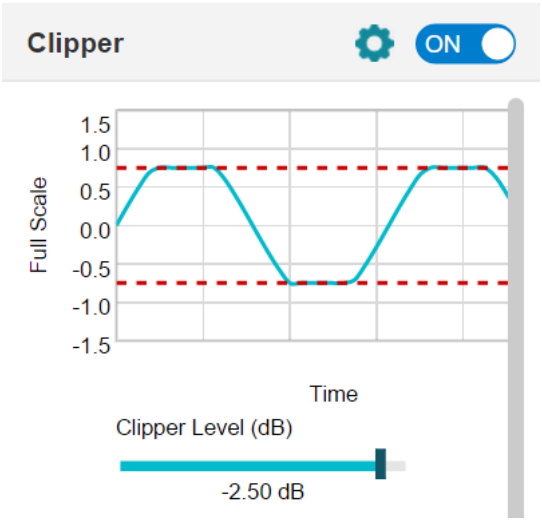

Figure 3-4. Clipper Module in PPC3

3.3 Clipping/Distortion Caused by Incorrect Sample Rate Setting

The 0x28 register of the TAS5828M outlines requirements for the sample rate setting. When the actual LRCLK is 44.1kHz/88.2kHz/176.4kHz, the value of this register must be manually set to the corresponding position. If not set correctly, when the power amplifier converts a 44.1kHz input signal into a 48kHz data stream for DSP processing, it may cause errors in the high-order digits, resulting in signal clipping within the digital domain and limiting the maximum output voltage, as shown in Figure 3-5 below. When the LRCLK is no longer 44.1kHz/88.2kHz/176.4kHz, the 0x28 register needs to be switched to Auto detection; otherwise, a CLK Error will occur.

3	FSMODE	R/W	0	FS Speed Mode These bits select the FS operation mode, which must be set according to the current audio sampling rate. Need set the bit manually if the input FS is 44.1kHz/88.2kHz/176.4kHz. 4 'b0000 Auto detection 4 'b0100 Reserved 4 'b0110 32KHz 4 'b1000 44.1KHz 4 'b1001 48KHz 4'b1010 88.2KHz 4 'b1011 96KHz 4 'b1100 176.4KHz 4 'b1101 192KHz Others Reserved
2-0	RESERVED	R/W	000	This bit is reserved

Figure 3-5. Sample Rate Configuration Register

- Taking TAS5828M as an example, Setup
  - TAS5828M EVM
  - PVDD=24V
  - Input: I2S,1kHz,-3dBFS (~81Wrms)
  - Mono 1.0 PBTL Base/Pro (1.0 48k) process flow, setting 0x28=0x00
  - AP used to generate audio and analyze output
    - Datamonitor on AP sent to oscilloscope to capture wave shape
    - Plot voltage levels are scaled
      - The dark blue is the differential output. Light blue is SDOUT.

- Solution: Register 0x28 = 0x08
  - Device still wants to sample at 48kHz.
  - At high amplitudes results in early clipping in the digital core of the device.
  - Setting register 0x28 to 0x08 tells device to read 44.1kHz only.
  - Set register after loading process flow.

Distortion Caused by Incorrect Sample Rate Setting

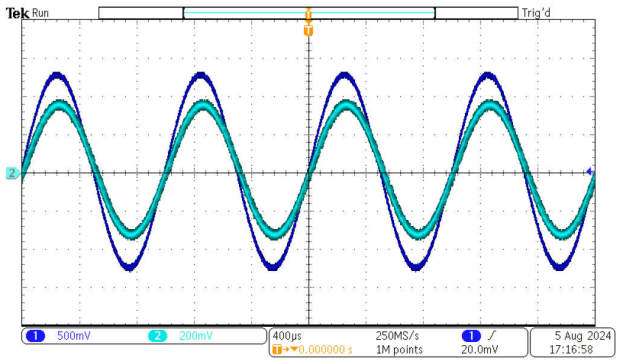

Figure 3-6. a) Undistorted with LRCLK = 48kHz

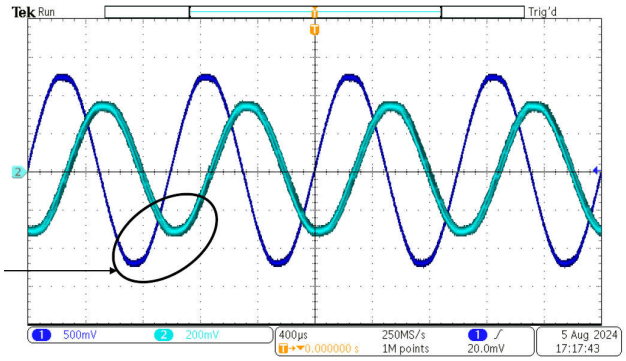

Figure 3-7. b) Distorted with LRCLK = 44.1kHz

4 Summary

High fidelity is critical in audio products, as output signal distortion directly degrades the user's listening experience. Achieving an undistorted output is a primary objective when designing audio systems. By providing an adequate PVDD to prevent clipping within the Power Stage, and ensuring correct configuration to avoid distortion within the DSP, a high-fidelity amplified signal can ultimately be delivered to the speaker terminal, thereby granting end-users an ultimate auditory feast.

5 References

1. Texas Instruments, General Tuning Guide for TAS58xx Family application report.
2. Texas Instruments, TAS5828M 50W Stereo, Digital Input, High Efficiency Closed-Loop Class-D Amplifier with Hybrid-Pro Algorithm datasheet.
3. Texas Instruments, PurePath™- Console 3 (PPC3) Overview Video library.

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