Texas Instruments TUSB73x0 Configuration Options

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ABSTRACT

This document outlines the options available to configure the Texas Instruments TUSB73x0 xHCI Host Controller.

Dynamic D3

This option is provided for customers to realize power savings by allowing the TUSB73x0 to dynamically transition between PCI D0 and PCI D3 depending on downstream port activity.

NOTE: Host platforms wishing to take advantage of DynamicD3 functionality must ensure that WAKE# events are properly supported by both the system BIOS and the system chipset.

XI_WAKE:

This option provides the ability for the TUSB73x0 controller to assert WAKE# in the absence of an external clock source by using the internal ring oscillator. When XI_WAKE functionality is enabled, the controller does not require a running USB clock to wake from device suspend states.

Without XI_WAKE functionality enabled, the TUSB73x0 requires a running USB clock at all times in order to assert WAKE#.

NOTE: Enabling XI_WAKE functionality (and as a result, the internal ring oscillator) increases device power consumption by 200 mW in devices suspend states. System designers should take this into consideration when deciding to implement this feature.

There are two methods to enable or disable the functionality described in Table 1:

Table 1. Equalizer Control Register (PCI 0xE8 31:24)

Bit	Field Name	Description
31	DYNAMIC_D3_EN	Dynamic D3 Control -If this bit is set to '1', and PORT4_EQ_OV (PCI 0xEC, bit 26) is set to '0', the driver shall enable Dynamic D3 functionality.
30	XI_WAKE_EN	XI_WAKE Control -If this bit is set to '1', and PORT4_EQ_OV (PCI 0xEC, bit 26) is set to '0', the driver shall enable XI_WAKE functionality.
29	RFU	Reserved for future use. Must be '0'.
28	RFU	Reserved for future use. Must be '0'.
27	RFU	Reserved for future use. Must be ''0'.
26	RFU	Reserved for future use. Must be '0'.
25	RFU	Reserved for future use. Must be '0'.
24	RFU	Reserved for future use. Must be '0'.

Method 1: BIOS

If the customer has control of the host BIOS, the relevant bits at PCI offset 0xE8 (see Table 1) can be set directly from the BIOS. No EEPROM or software modifications are required. This is the preferred method for most customers.

Method 2: EEPROM

For an add-in card, or in cases where the customer does not have control of the BIOS, the relevant bits can be programmed via an attached EEPROM (EEPROM Offset 0x15).

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