

Maintain Isolation Ratings in Half the Size with DFB and DFP Digital Isolator Packaging



Scott Monroe

ABSTRACT

The modern small form factor DFP and DFB package families from Texas Instruments for digital isolators provide up to 56% PCB package footprint area savings over the traditional isolation packages while maintaining the same creepage and clearance distances and high voltage performance.

The DFP and DFB package families, using 0.5mm pin pitch, provide significant board area reduction, especially in the critical dimension (Y) along the isolation barrier. These smaller packages allow system designers to place more isolation channels in the same space or reduce the total system size. Alternatively, thanks to the shorter dimension along the isolation barrier, routing critical signals across the isolation barrier is easier in the layout thanks to the smaller package. The smaller package and Y dimension provides more flexibility in where and how to place the digital isolator with respect to the devices using the signal on both sides of the isolation barrier.

This application note provides a package by package comparison for the common two, three, four and six channel digital isolators in both the 4mm and 8mm creepage and clearance distance packaging classes. Devices using these packages have certification levels of galvanic (functional isolation), basic certified isolation, and reinforced certified isolation. Refer to the data sheet of the specific device for the certification level or levels.

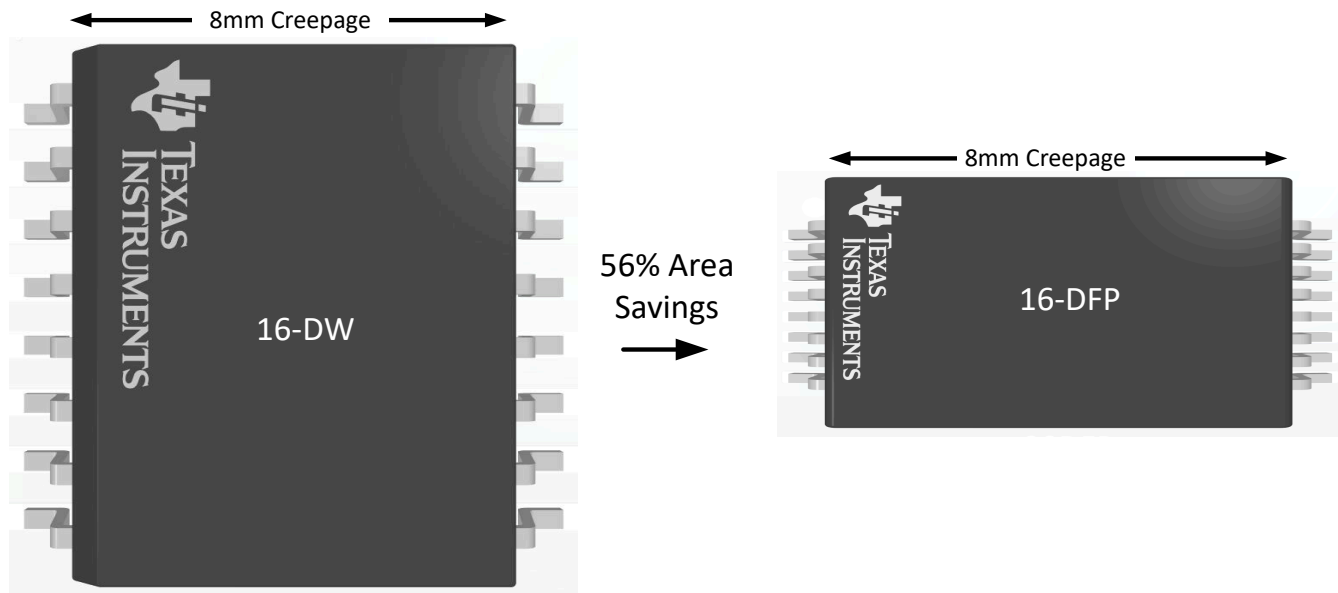


Figure 1-1. Traditional 16-DW (Wide-SOIC) Package Versus 16-DFP (Wide-SSOP) Small Form Factor Package

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1 Introduction

Supporting system designers with PCB layout flexibility, especially along the isolation barrier, smaller system sizes or more isolation channels in the same size, TI developed the [DFP](#) and [DFB](#) small form factor package families for digital isolators. These packages are being introduced in the [ISO64xx](#), [ISO64xx-Q1](#) and [ISO60xx](#) device families.

In addition to the DFP and DFP package families, TI continues to develop creepage and clearance optimized packages for many applications. If working voltages are lower and no certifications are needed, the [8-REU](#) (DFN) in the [ISO65xx](#) family is the smallest digital isolation package. For the widest creepage and clearance, 21.2mm, TI introduced the [16-DUW](#) package in the [ISO774xU](#) family.

This application note uses TI's packaging nomenclature. Within the industry there are many variations of SOIC and SOP packages in various widths. Relative terms such as narrow, wide, thin, WB (wide body), NB (narrow body) are used but not standardized. Thus the TI small form factor DFP and DFP packages can also replace NB SOIC, SOIC_N, Narrow-SOIC, WB, SOIC, SOIC_W, Wide-SOIC, WB SSOIC, QSOP, WSOP, SSOP, TSSOP, and SOW while reducing PCB area and maintaining equivalent high voltage specifications.

2 Narrow Body Package Comparisons for 3.7mm and 4mm Creepage and Clearance Packages

Two channel digital isolators are in the narrow SOIC 8 pin package (8-D) and 3, 4 and 6 channel digital isolators are in the narrow SSOP 16 pin package (16-DBQ). The 8-D and 16-DBQ have become the traditional packages supporting 4mm and 3.7mm creepage and clearance requirements.

The new small form factor, narrow SSOP, DFB family is used in the latest digital isolator families in addition to the traditional packages. DFB supports 4mm creepage and clearance while using 0.5mm pitch pins to significantly reduce the Y dimension along the isolation barrier of the packages.

2.1 Two Channel Devices in Narrow Body Package Comparisons

Table 2-1 summarizes the advantages of the 10-DFB with respect to the traditional 8-D package for two channel devices.

Table 2-1. 2 Channel Digital ISO in Narrow, 4mm Creepage and Clearance Packages

Package	Channel Count	Device ISO Rating	Creepage and Clearance (mm)	% area savings vs Traditional Package (8-D)	Area (mm ²)	X (mm)	Y (mm)	Pin Pitch (mm)	Z (mm)
						(PCB land pattern lead to lead maximum)	(package body size maximum)		(height of package above PCB maximum)
10-DFB (SSOP)	2	Reinforced, Basic	> 4	44%	19.3	6.9	2.8	0.5	1.75
8-D (SOIC) (Traditional Package)	2	Reinforced, Basic, Galvanic	>4	Traditional (Reference)	34.8	6.95	5	1.27	1.75



Figure 2-1. 2 Channel Digital ISO Area Comparison (mm²): Traditional 8-D (SOIC) vs Small Form Factor 10-DFB (SSOP)

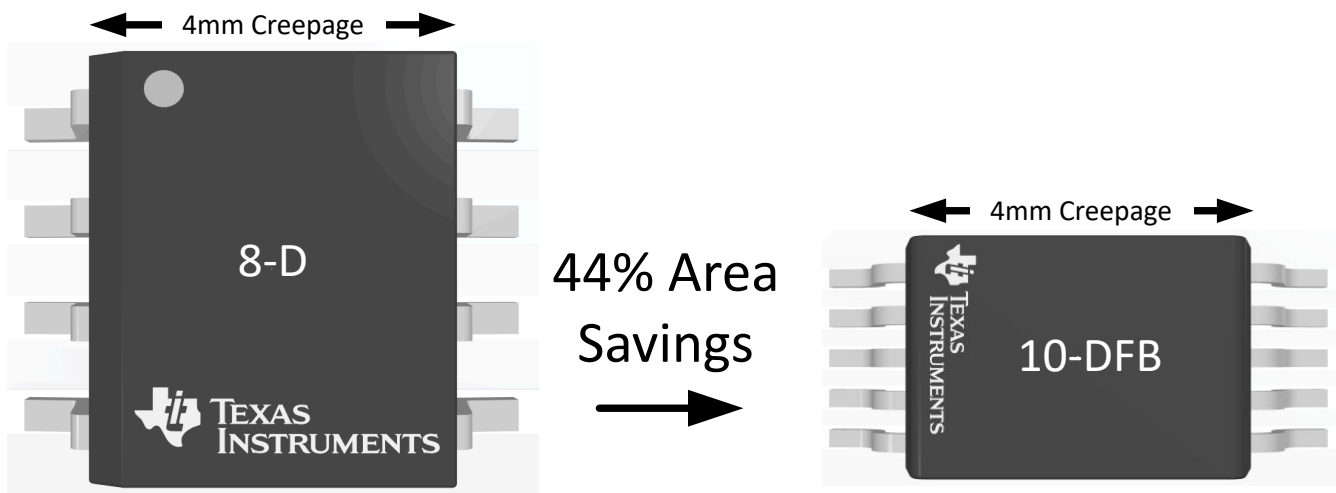


Figure 2-2. 2 Channel Digital ISO Package Percentage Comparison: Traditional 8-D (SOIC) vs Small Form Factor 10-DFB (SSOP)

2.2 3, 4, and 6 Channel Devices in Narrow Body Package Comparisons

Table 2-2 summarizes the advantages of the 16-DFB, used for 3 and 4 channel devices, and the 20-DFB, used for 6 channel devices, with respect to the traditional 16-DBQ package for 3, 4, and 6 channel devices. The DFB packages provide 4mm of creepage and clearance versus the 3.7mm provided by the 16-DBQ.

Table 2-2. 3, 4 and 6 Channel Digital ISO in Narrow, 3.7mm and 4mm Creepage and Clearance Packages

Package	Channel Count	Device ISO Rating	Creepage and Clearance (mm)	% area savings vs Traditional Package (16-DBQ)	Area (mm ²)	X (mm)	Y (mm)	Pin Pitch (mm)	Z (mm)
						(PCB land pattern lead to lead maximum)	(package body size maximum)		(height of package above PCB maximum)
20-DFB (SSOP)	6	Reinforced, Basic	> 4	-1.5% ⁽¹⁾	35.5	6.9	5.15	0.5	1.75
16-DBQ (SSOP) (Traditional Package)	3, 4, 6	Reinforced, Basic, Galvanic	>3.7	Traditional (Reference)	35.0	7	5	0.635	1.75
16-DFB (SSOP)	3, 4	Reinforced, Basic	> 4	15% ⁽²⁾	29.7	6.9	4.3	0.5	1.75

- (1) Six channel devices use the 20-DFB package. The 20-DFB package is only 0.5mm² (1.5%) larger than the traditional 16-DBQ package but offers 4mm of creepage and clearance vs the traditional 3.7mm. The 20-DFB adds a functional pin, providing additional features, such as output enable (ENx) for the ISO60xx family, in a 6 channel device in 20-DFB package versus devices in the traditional 16-DBQ.
- (2) Three and four channel devices use the 16-DFB package. The 16-DFB is 5.8mm² (15%) smaller than the 16-DBQ package and offers 4mm of creepage and clearance vs 3.7mm. The 16-DFB has the functional pin for three and four channel devices, the same as the traditional 16-DBQ package .

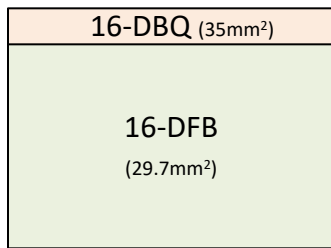


Figure 2-3. 3 and 4 Channel Digital ISO in Narrow Packages, Area Comparison (mm²): Traditional 16-DBQ (SSOP) vs Small Form Factor 16-DFB (SSOP)

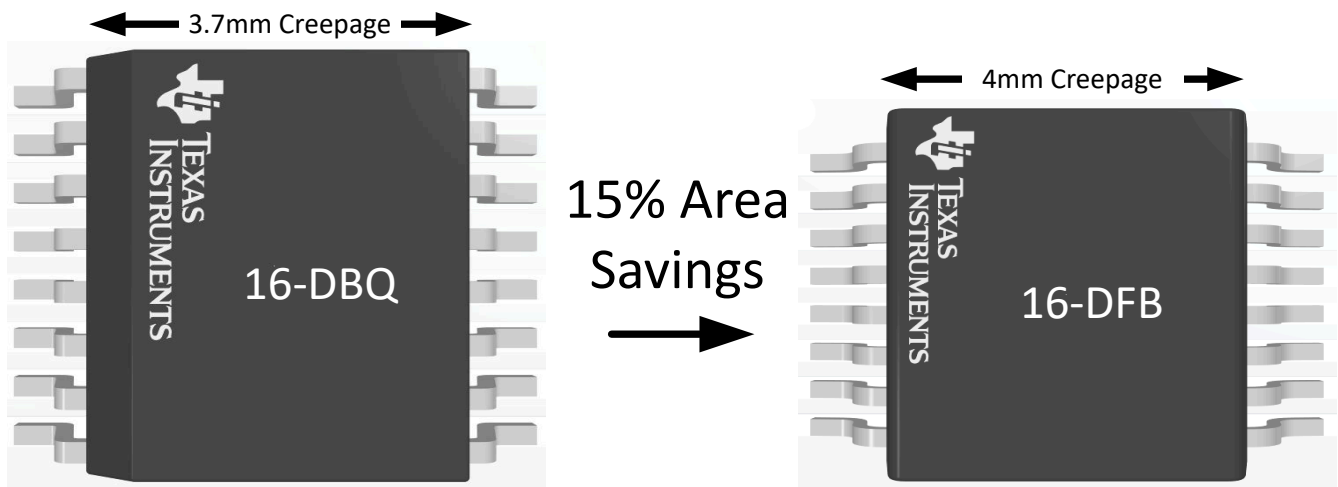


Figure 2-4. 3 and 4 Channel Digital ISO in Narrow Packages, Package Percentage Comparison: Traditional 16-DBQ (SSOP) vs Small Form Factor 16-DFB (SSOP)

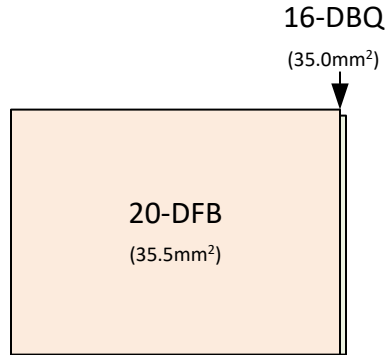


Figure 2-5. 6 Channel Digital ISO in Narrow Packages, Area Comparison (mm²): Traditional 16-DBQ (SSOP) vs Small Form Factor 20-DFB (SSOP)

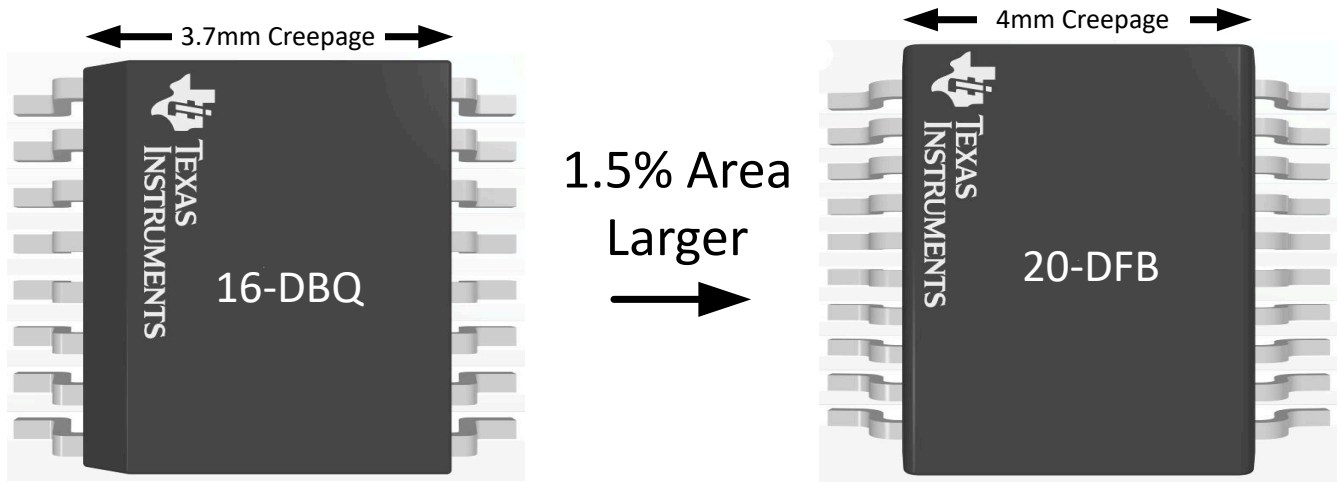


Figure 2-6. 6 Channel Digital ISO in Narrow Packages, Package Percentage Comparison: Traditional 16-DBQ (SSOP) vs Small Form Factor 20-DFB (SSOP)

3 Wide Body Package Comparisons for 8mm Creepage and Clearance

Two channel digital isolators are in the wide SOIC 8 pin package (8-DWV) and 16 pin package (16-DW). The 3, 4 and 6 channel digital isolators are in the wide SOIC 16 pin package (16-DW). The 8-DWV and 16-DW have become the traditional packages supporting 8mm creepage and clearance requirements.

The new small form factor, wide SSOP, DFP family is used in the latest digital isolator families in addition to the traditional packages. DFP supports 8mm creepage and clearance while using 0.5mm pitch pins to significantly reduce the Y dimension along the isolation barrier of the packages.

3.1 2 Channel Devices in Wide Body Package Comparisons

Table 3-1 summarizes the advantages of the 12-DFP with respect to the traditional 8-DWV and 16-DW package for 2 channel devices. The 2 channel devices in a 12-DFP gain an extra functional pin per side which is utilized for new functionality in some digital isolator families.

Table 3-1. 2 Channel Digital ISO in Wide, 8mm Creepage and Clearance Packages

Package	Channel Count	Device ISO Rating	Creepage and Clearance (mm)	% area savings vs Traditional Package (8-DWV)	Area (mm ²)	X (mm)	Y (mm)	Pin Pitch (mm)	Z (mm)
						(PCB land pattern lead to lead maximum)	(package body size maximum)		(height of package above PCB maximum)
16-DW (Wide-SOIC)	2	Reinforced, Basic	>8	-58%	119.7	11.4	10.5	1.27	2.65
12-DFP (Wide-SSOP)	2	Reinforced	>8	45%	41.4	10.9	3.8	0.5	2.65
8-DWV (Wide-SOIC) (Traditional Package)	2	Reinforced	>8.5	Traditional (Reference)	75.6	12.7	5.95	1.27	2.8



Figure 3-1. 2 Channel Digital ISO Area Comparison (mm²): Traditional 8-DWV (Wide-SOIC) vs Small Form Factor 12-DFP (Wide-SSOP)

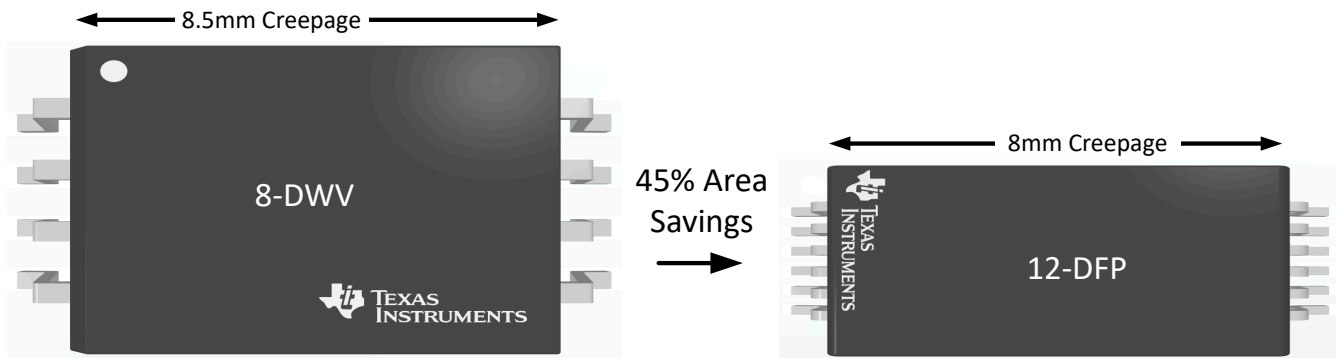


Figure 3-2. 2 Channel Digital ISO Package Percentage Comparison: Traditional 8-DWV (Wide-SOIC) vs Small Form Factor 12-DFP (Wide-SSOP)

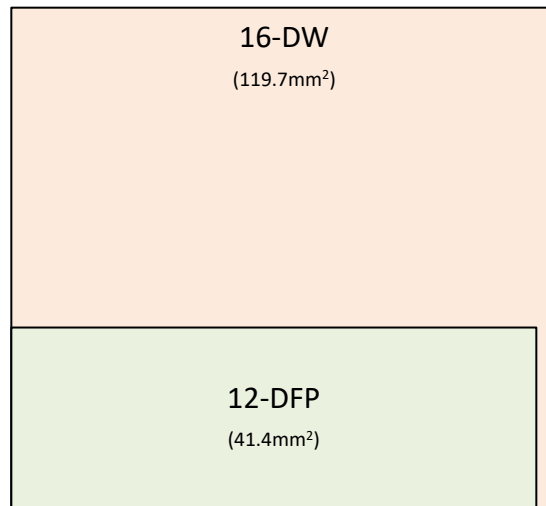


Figure 3-3. 2 Channel Digital ISO Area Comparison (mm²): 16-DW (Wide-SOIC) vs Small Form Factor 12-DFP (Wide-SSOP)

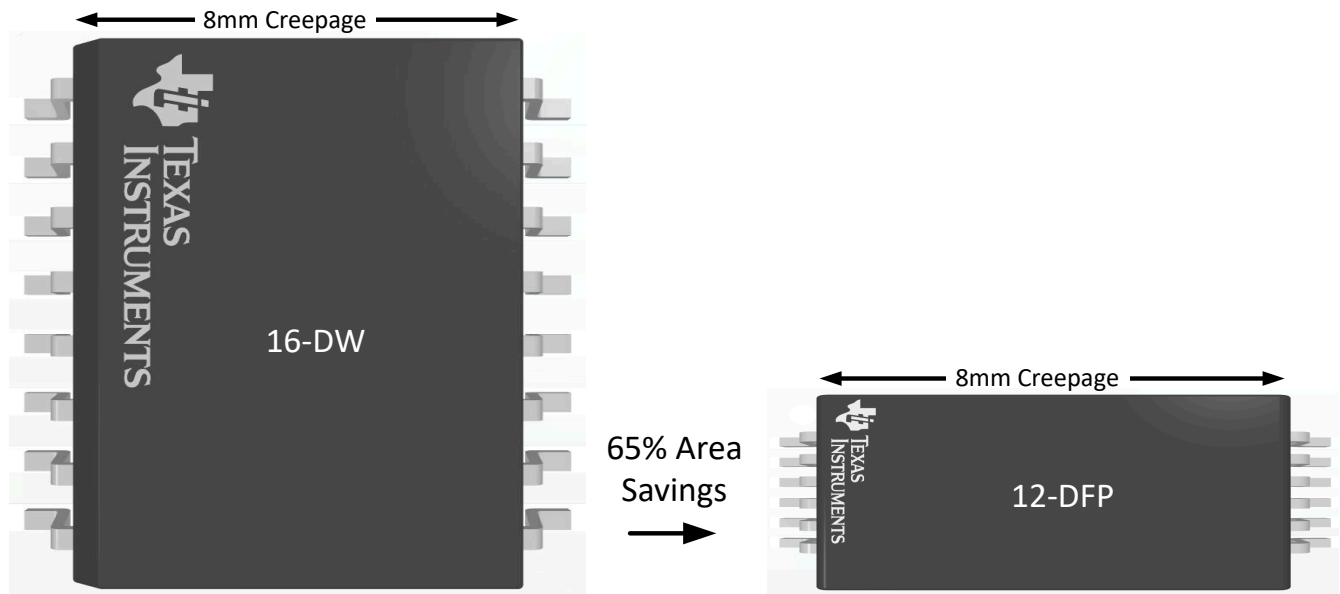


Figure 3-4. 2 Channel Digital ISO Package Percentage Comparison: 16-DW (Wide-SOIC) vs Small Form Factor 12-DFP (Wide-SSOP)

3.2 3, 4, and 6 Channel Devices in Wide Body Package Comparisons

Table 3-2 summarizes the advantages of the 16-DFP, used for 3 and 4 channel devices, and the 20-DFP, used for 6 channel devices, with respect to the traditional 16-DW package for 3, 4, and 6 channel devices. The 6 channel devices gain an extra functional pin per side in a 20-DFP, which is utilized for new functionality in some digital isolator families.

Table 3-2. 3, 4 and 6 Channel Digital ISO in wide, 8mm creepage and clearance packages

Package	Channel Count	Device ISO Rating	Creepage and Clearance (mm)	% area savings vs Traditional Package (16-DW)	Area (mm ²)	X (mm)	Y (mm)	Pin Pitch (mm)	Z (mm)
						(PCB land pattern lead to lead maximum)	(package body size maximum)		(height of package above PCB maximum)
20-DFP (Wide-SSOP)	6	Reinforced	>8	47%	63.2	10.9	5.8	0.5	2.65
16-DW (Wide-SOIC) (Traditional Package)	3, 4, 6	Reinforced, Basic	>8	Traditional (Reference)	119.7	11.4	10.5	1.27	2.65
16-DFP (Wide-SSOP)	3, 4	Reinforced	>8	56%	52.3	10.9	4.8	0.5	2.65

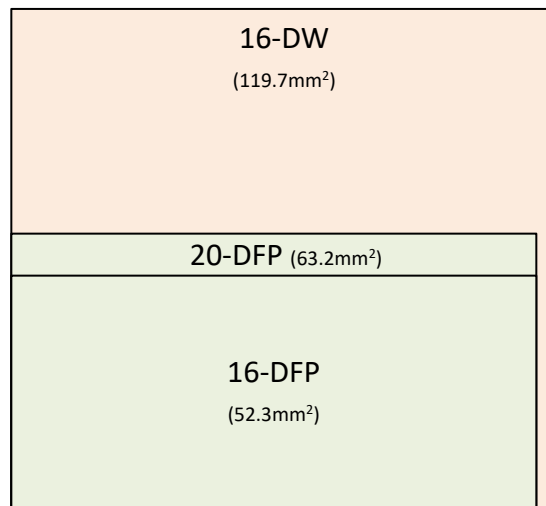


Figure 3-5. 3, 4 and 6 Channel Digital ISO in Wide Packages, Area Comparison (mm²): Traditional 16-DW (Wide-SOIC) vs Small Form Factor 16-DFP and 20-DFP (Wide-SSOP)

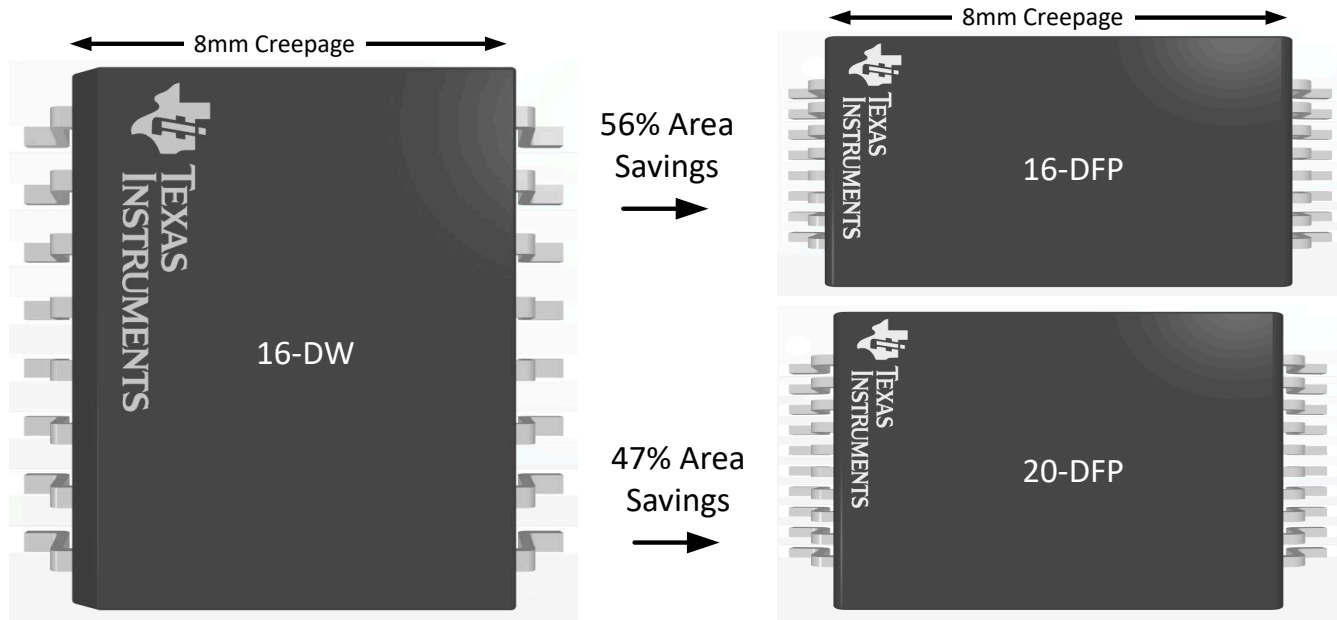


Figure 3-6. 3, 4 and 6 Channel Digital ISO in Wide Packages, Package Percentage Comparison: Traditional 16-DW (Wide-SOIC) vs Small Form Factor 16-DFP and 20-DFP (Wide-SSOP)

4 Summary

TI's small form factor DFB and DFP packages provide system designers PCB layout flexibility, especially along the isolation barrier, to develop a smaller system or increase the number of isolated channels in the same PCB area with respect to the traditional digital isolator packages. TI's modern packages maintain the high voltage specifications and creepage and clearance distances of the traditional packages and reduce overall system area and PCB costs.

5 References

1. Texas Instruments, TI Digital Isolators on the [Online Parametric Tool](#), isolation device search tool.
 - [ISO60xx](#) device family.
 - [ISO64xx](#) and [ISO64xx-Q1](#) device family.
2. Texas Instruments, [Considerations for Selecting Digital Isolators](#), application brief.
3. Texas Instruments, [Digital Isolator Design Guide](#), application note.
4. Texas Instruments, [High-voltage reinforced isolation: Definitions and test methodologies](#), technical article.
5. Texas Instruments, [Improve Your System Performance by Replacing Optocouplers with Digital Isolators](#), technical white paper.
6. Texas Instruments, [Top 9 Design Questions about Digital Isolators](#), technical article.
7. Texas Instruments, [Digital Isolators - Top Questions, Answered - TI E2E support forums](#), application support.
8. Texas Instruments, [TI E2E™ Isolation Support Forum](#), on-line application assistance.

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