Application Note

TCAN455x-Q1 Peripheral Circuit and Clock Design Application Note

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ABSTRACT

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The TCAN455x-Q1, introduced by Texas Instruments in 2019, is an automotive system basis chip (SBC) that integrates a Controller Area Network with Flexible Data Rate (CAN FD) controller and transceiver. It utilizes a common MCU Serial Peripheral Interface (SPI) bus to configure the CAN FD interface, thereby increasing the number of CAN FD bus ports in the system. By employing the TCAN455x-Q1, customers can retain their existing MCU-based architectures and conveniently upgrade or expand CAN FD capabilities.

This article begins with a basic introduction to the TCAN4550x-Q1 series, followed by a detailed list of considerations for hardware circuit design. It then focuses on the principles of the clock module and crystal oscillator circuit design experience. Improper design in this area may cause the device to erroneously enter single-ended clock mode, resulting in communication failure. Corresponding solutions and test waveforms are also provided.

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1 Basic Introduction to TCAN455x-Q1

1.1 What is an SBC?

A System Basis Chip (SBC) is a semiconductor device that integrates a Controller Area Network (CAN) or Local Interconnect Network (LIN) transceiver with power management components. The power management components may include a Low-Dropout Regulator (LDO), a DC/DC converter, or both. SBCs help reduce component count and board space, and TI SBCs offer lower power consumption than discrete solutions, thereby extending battery life. For automotive and industrial designers, the high integration and reliability of SBCs enable lighter-weight and lower-cost system designs.

The TCAN4550-Q1 is an advanced SBC that bridges SPI to CAN FD, integrating a CAN FD controller and CAN FD transceiver in a single package. It supports a local wake-up pin, a watchdog timer, and a 70mA LDO output. When the MCU does not support a CAN FD interface or has an insufficient number of CAN FD interfaces, the TCAN4550-Q1 provides a convenient way to expand the CAN FD interface. Figure 1-1 shows the block diagram of the TCAN4550-Q1 and its connection to the MCU via SPI.

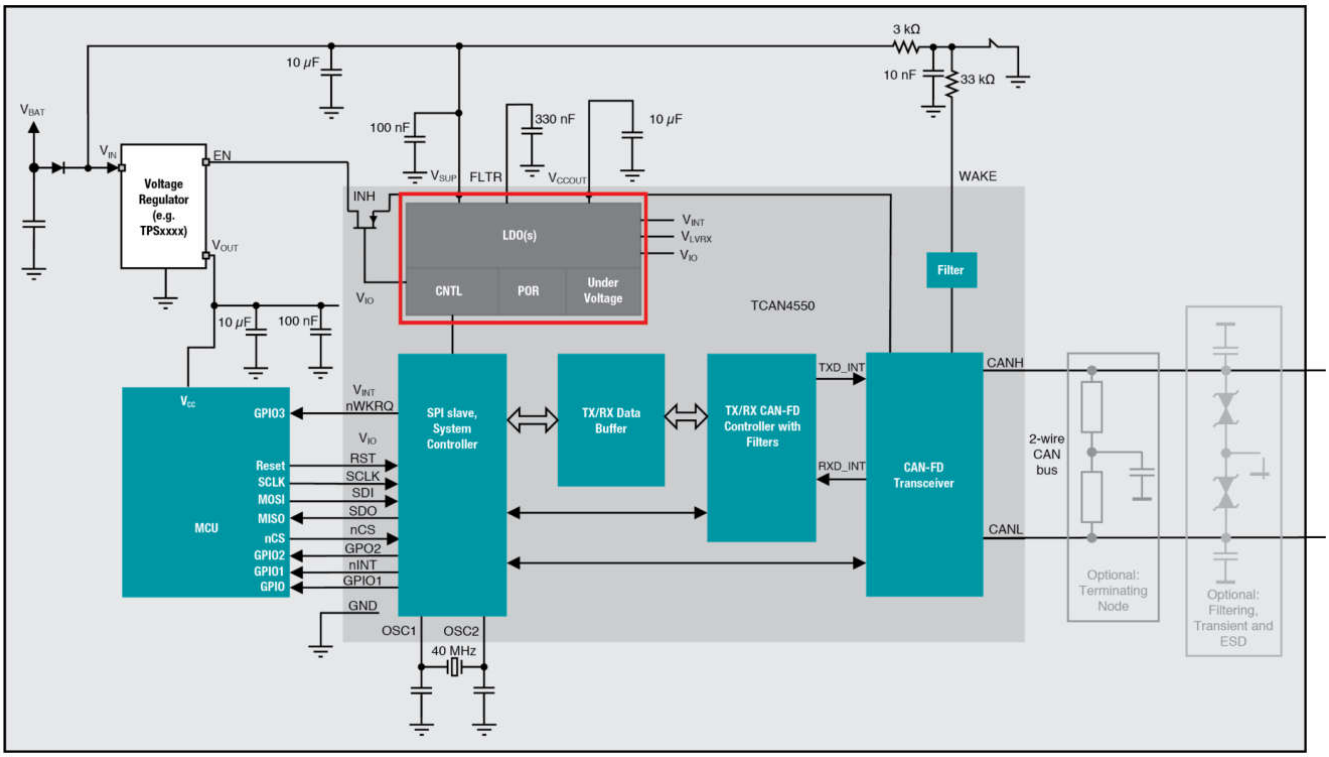

Figure 1-1. TCAN4550-Q1 to MCU Connection Block Diagram

1.2 What is CAN FD?

The CAN FD communication protocol is an upgrade to the original CAN bus standard (also known as "Classic CAN"). It helps increase in-vehicle network data rates and throughput, supporting data rates up to 5Mbps and payloads up to 64 bytes, and is widely used in automotive applications. For a detailed introduction to CAN FD, please refer to the TI training videos.

1.3 What are the advantages of the TCAN455x-Q1?

- Easy Upgrade and Expansion of CAN FD Bus

  If the MCU has a limited number of CAN FD ports, customers can use the TCAN455x-Q1 to add CAN FD buses through the existing SPI port in the automotive system. Typically, such bus expansion would require a system redesign, but the TCAN4550-Q1 allows for convenient and straightforward upgrading and expansion of the CAN FD bus.
- Small Package Size Reduces Board Space

By integrating a 125mA LDO, the TCAN4550-Q1 can not only power itself but also provide up to 70mA of external output to external sensors or other devices, reducing the space occupied by external power supply designs.

- Enhanced Design Flexibility

  The TCAN455x-Q1 integrates ±58VDC bus fault protection, a watchdog timer, and fail-safe modes, while remaining compatible with the Classic CAN protocol. It also features a VIO pin that supports 1.8V/3.3V, and 5V ±5% IO voltage levels to interface with different MCUs.

1.4 Difference between TCAN4550-Q1 and TCAN4551-Q1

The TCAN4550-Q1 and TCAN4551-Q1 belong to the same series and have similar parameters. There are two main differences: (1) The internal 5V LDO of the TCAN4550-Q1 can supply up to 70mA externally; the internal 5V LDO of the TCAN4551-Q1 cannot supply external power and is used only for internal power. (2) The TCAN4550-Q1 supports a watchdog function, while the TCAN4551-Q1 does not. A detailed comparison is shown in Figure 1-2 below.

	Differentiated Features	
Feature / Device	TCAN4550-Q1	TCAN4551-Q1
Advanced bus fault diagnostics		
Programmable GPIO	(1) GPIO (1) GPO	(2) GPO
Watchdog	✓	
LDO Output	**5V @ 70 mA**	
SPI CRC		
INH / WAKE	✓	✓
CAN TRX Voltage (V) (V_{CC} rail voltage)	5	5
V_{IO} Range (V)	3.3 - 5	1.8 - 5
V_{WK} Range (V)		
Device Voltage Rail	V_{SUP}	V_{SUP}
Package / Pins	QFN – 20	QFN - 20
Status	Production	Production

Figure 1-2. TCAN4550-Q1 and TCAN4551-Q1 Parameter Comparison

2 TCAN455x-Q1 Peripheral Circuit Design

2.1 Power Supply Pins

V_{SUP} Pin: The V_{SUP} pin has a withstand voltage of 42V and a maximum recommended operating voltage of 30V. It can be connected directly to the battery. It supplies power to the internal digital core, CAN transceiver, and V_{CCOUT}. A 100nF decoupling capacitor must be placed as close as possible to the V_{SUP} pin.

V_{IO} Pin: The V_{IO} pin has a withstand voltage of 6V and a recommended operating voltage range of 3.135–5.25V (TCAN4550-Q1)/1.71–5.25V (TCAN4551-Q1). It supplies power to the internal digital IO pins (SPI IO, GPIO, GPO). When matching different MCU IO voltages, the V_{IO} pin eliminates the need for a level shifter. A 100nF decoupling capacitor must be placed as close as possible to the V_{IO} pin.

V_{CCOUT} Pin (TCAN4550-Q1): The internal LDO of the TCAN4550-Q1 provides a total of 125mA for the integrated CAN transceiver and the V_{CCOUT} pin. In normal mode, it can supply up to 70mA externally. In bus fault or sleep mode, this LDO is disabled and cannot supply external current. A capacitor of at least 10µF must be placed as close as possible to the V_{CCOUT} pin.

V_{CCFLTR} Pin (TCAN4551-Q1): The V_{CCFLTR} pin provides filtering for the internal 5V transceiver regulator. A capacitor of at least 10µF to ground must be placed.

GND Pin: The GND pin is the ground pin and is also the thermal pad. It must be connected to the PCB ground plane to ensure proper heat dissipation.

2.2 SPI and IO Pins

SCLK, SDI, SDO, nCS Pins: The SCLK pin is the SPI clock input, with an internal weak pull-up. The SDI pin is the SPI data input, with an internal weak pull-up. The SDO pin is the SPI data output. The nCS pin is the chip select (active low), with an internal weak pull-up to remain de-asserted.

GPIO/GPO Pins:

For TCAN4550-Q1:

- The GPIO1 pin default output is M_CAN_INT 1 (active-low interrupt). By configuring register 16'h0800[15:14] = 00, this pin is configured as a GPO output pin, and via register 16'h0800[11:10], it can be set to different GPO functions. By configuring register 16'h0800[15:14] = 10, this pin is configured as a watchdog input reset pin.
- The GPO2 pin is an open-drain output pin and requires a pull-up resistor to V_{IO}. Register 16'h0800[23:22] configures different GPO outputs, and it can be set as a watchdog output reset pin.

For TCAN4551-Q1:

- The GPO1 pin default output is M_CAN_INT 1 (active-low interrupt). Via register 16'h0800[11:10], this pin can also be configured as an SPI fault interrupt or undervoltage/overtemperature interrupt.
- The GPO2 pin is an open-drain output pin and requires a pull-up resistor to V_{IO}. Register 16'h0800[23:22] configures different GPO outputs.

2.3 CAN Pins

CANH, CANL Pins: The CANH and CANL pins are the differential CAN bus pins, connected to the CAN transceiver and the WUP CAN receiver. A 120Ω termination resistor is required at each end of the CAN bus. The TCAN455x-Q1 CAN communication complies with ISO 11898-1:2015 and the Bosch CAN protocol specification 3.2.1.1.

2.4 Clock Pins

OSC1, OSC2 Pins: The OSC1 and OSC2 pins connect to an external quartz crystal, or the OSC1 pin can be used as an external single-ended clock input (with the OSC2 pin grounded). The choice of clock source depends on the customer's application. To support 2Mbps and 5Mbps CAN FD data rates, the crystal/external clock input must have a frequency accuracy of 0.5%. A minimum of 20MHz is required to support 2Mbps CAN FD, and a 40MHz crystal/external clock input is recommended for 5Mbps CAN FD. Detailed requirements are provided in Section 3.

2.5 Other Pins

INH Pin: The INH pin is a high-voltage output pin whose voltage is V_{SUP} minus a diode drop. It can serve as an enable (EN) signal for an external regulator (typically supplying the MCU and V_{IO} pin). In sleep mode, the INH pin turns off and enters a high-impedance state to achieve ultra-low power consumption. If this function is not required, set register 16'h0800[9] = 1 to disable it. If the application does not require a wake-up function, the INH pin can be left floating. Note that the INH pin is not a power pin and cannot supply power to external systems; its recommended operating current is less than 1mA.

FLTR Pin: The FLTR pin provides filtering for the internal digital core regulator. A capacitor of at least 300nF to ground must be placed.

WAKE Pin: The WAKE pin is a high-voltage input pin with a withstand voltage of 42V, used for local wake-up (LWU). By default, this pin triggers LWU on either a rising or falling edge. Through register 16'h0800[31:30], it can be configured to trigger on rising edge only or falling edge only. A capacitor of at least 10nF to ground must be placed to enhance noise immunity. If the local wake-up function is not used, connect the WAKE pin directly to V_{SUP} or GND.

RST Pin: The RST pin is the device reset pin, with an internal weak pull-down to ensure proper operation. When TCAN455x communication stops, applying a high-level pulse to the RST pin with a duration longer than t_{PULSE_WIDTH} resets the device, restoring all registers to default values and entering standby mode. After an RST reset, wait at least 700µs before reading from or writing to the TCAN455x.

nINT Pin: The nINT pin is an open-drain output for global interrupts, requiring an external pull-up to V_{IO}. This pin is pulled low whenever any interrupt occurs.

nWKRQ Pin: The nWKRQ pin indicates a wake-up request, including bus wake-up (WUP), local wake-up (LWU), and power-on (PWRON). By default, this pin remains low after a wake-up request and can be used as an alternative to the INH pin to enable an external regulator. By setting register 16'h0800[8] = 1, this pin is configured as a wake-up interrupt pin; it outputs low upon a wake-up interrupt and returns high after the interrupt is cleared. The nWKRQ pin has an internal pull-up to the internal 3.6 V rail in sleep mode. Setting register 16'h0800[19] = 1 changes the pull-up supply from the internal voltage to the external V_{IO} rail. When using the V_{IO} pull-up supply, if V_{IO} is powered down, the nWKRQ pin cannot indicate wake-up interrupts until V_{IO} is restored; additionally, this pin becomes an open-drain output and requires an external pull-up resistor to the V_{IO} rail.

3 Clock Circuit Design for the TCAN455x-Q1

3.1 Internal Clock Circuit and Operating Principles

The TCAN455x supports two modes: an external quartz crystal or an external single-ended input clock.

The internal clock circuit of the TCAN455x consists primarily of three modules: an amplifier and bias control block, a comparator and filter block, and a clock input detection block, as shown in the block diagram in Figure 3-1 below.

- The **comparator** compares the voltage difference between the OSC1 and OSC2 pins and generates the CLKOUT signal (from either the quartz crystal or the single-ended input clock). The comparator's positive input connects to the OSC1 pin, and its negative input connects to the OSC2 pin. In single-ended clock mode, the clock signal is applied to the OSC1 pin, and the OSC2 pin is grounded.
- **The amplifier and bias control module** provides the current source for crystal oscillation start-up and maintenance in quartz crystal mode. This block is disabled in single-ended clock mode. It features Automatic Gain Control (AGC) and Peak Detection (PD) circuitry that adjusts the bias current to maintain a stable oscillation of approximately 1Vpp peak-to-peak on OSC1 and OSC2, or a differential 2Vpp swing (with a 180° phase difference), as shown in Figure 3-2 below. However, actual OSC1 and OSC2 voltage amplitudes may vary depending on the external load circuit.
- **The clock input detection module** monitors the voltage on the OSC2 pin to determine the mode. If the OSC2 voltage is below the 90mV–150mV threshold, the device identifies single-ended input clock mode and disables the amplifier block (the customer must ground the OSC2 pin for this mode). If the OSC2 pin is not grounded and its voltage exceeds the threshold, quartz crystal clock mode is identified and the amplifier module is enabled.

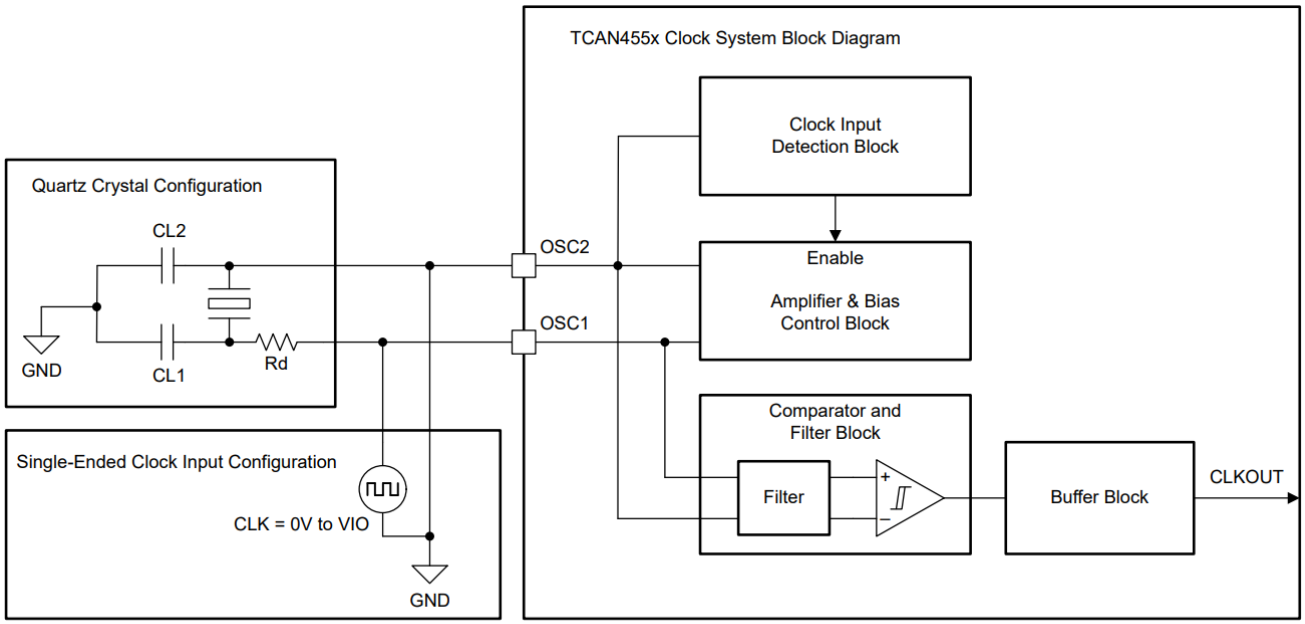

Figure 1-1. TCAN455x Clock Simplified Block Diagram

Figure 3-1. TCAN455x Clock Block Diagram

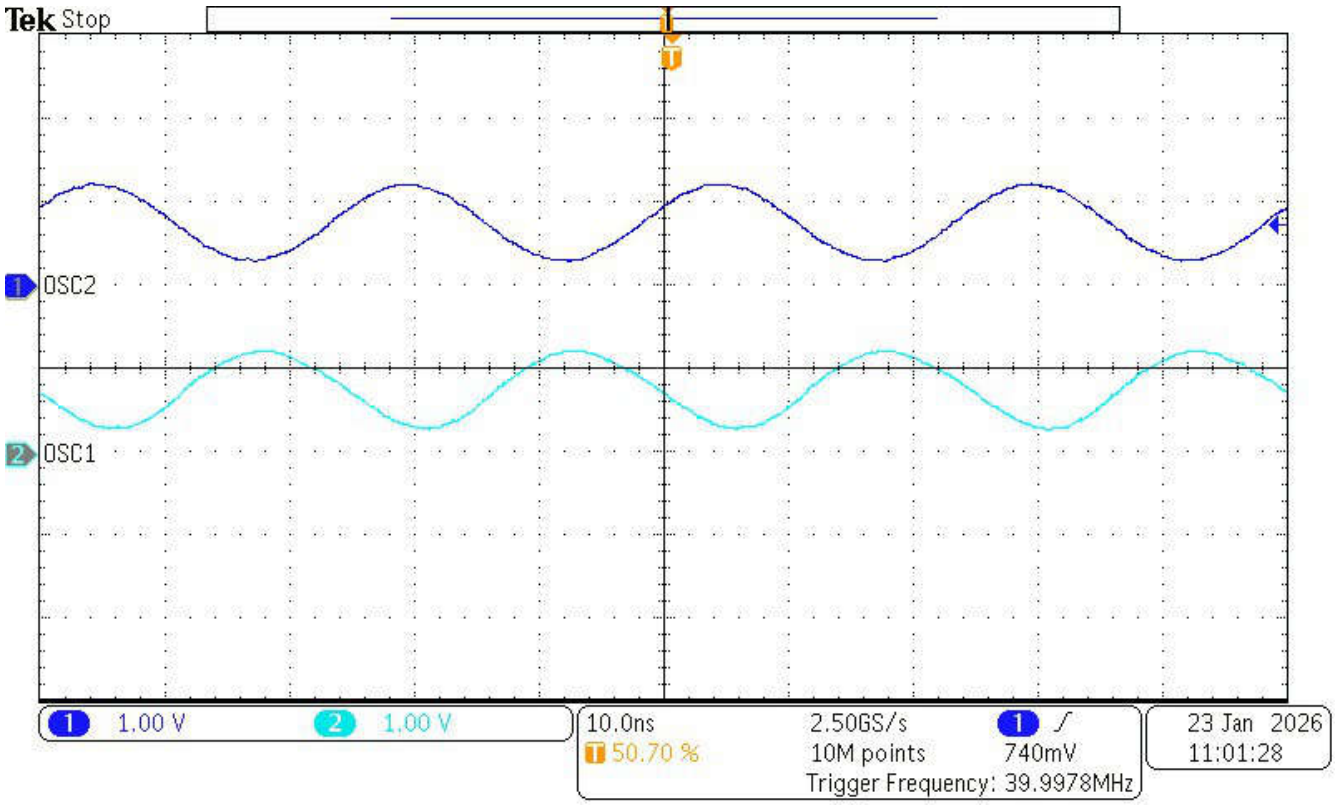

Figure 3-2. TCAN455x OSC1 and OSC2 Waveforms in Quartz Crystal Clock Mode

3.2 Quartz Crystal Clock Mode Principle

The TCAN455x employs a Pierce oscillator architecture. An internal current source drives the external crystal and capacitors to initiate and sustain oscillation, as shown in Figure 3-3 below. Oscillation is generated by the charging and discharging of the load capacitors at each end of the crystal—one side charges while the other discharges. Once the oscillation process begins, it continues unless the system lacks sufficient energy to sustain it.

At start-up, the amplifier output bias current is at its highest level to rapidly charge the discharged OSC1 capacitor. After the OSC1 capacitor is fully charged, it discharges through the crystal, and the OSC2 capacitor begins to charge. When the OSC2 capacitor is fully charged, it discharges back into the OSC1 capacitor, generating oscillation. After start-up, the TCAN455x reduces the bias current, requiring only enough to compensate for energy losses due to parasitic resistance in the circuit.

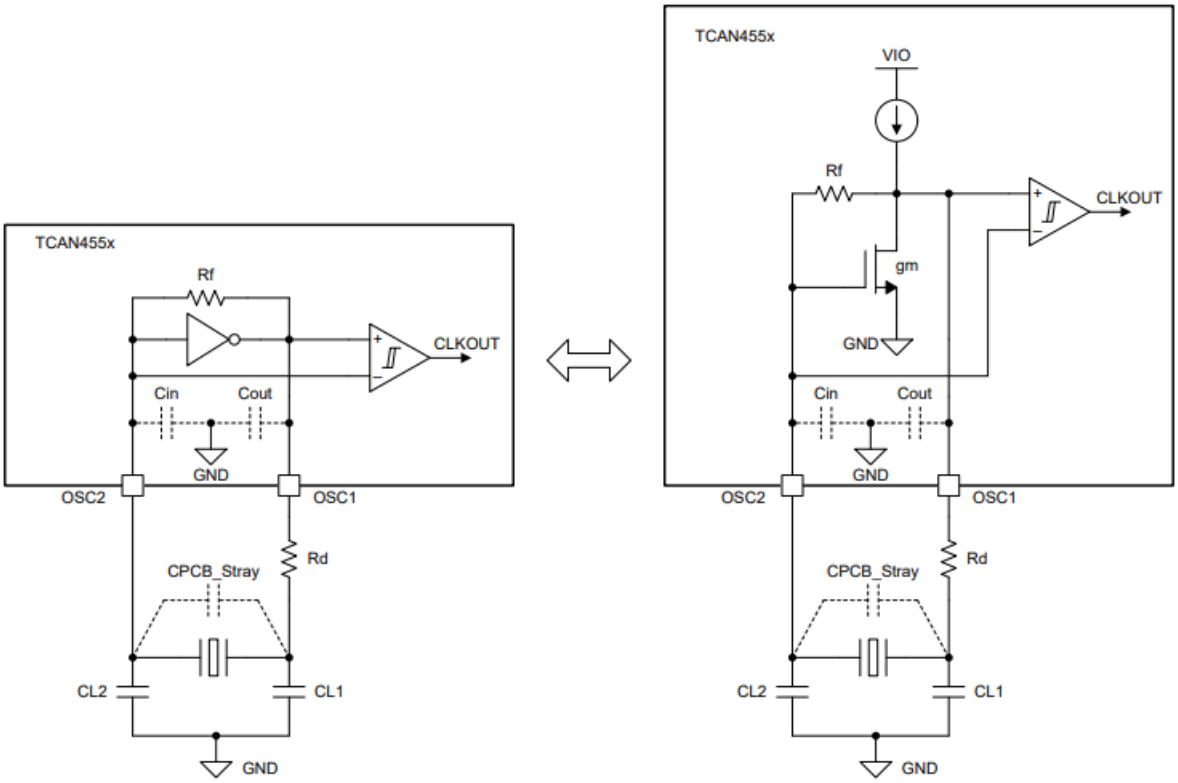

Figure 3-1. TCAN455x Pierce Oscillator Simplified Circuit Representations

Figure 3-3. TCAN455x Pierce Oscillator Simplified Schematic

3.3 Quartz Crystal Parameters

The design goals for the quartz crystal oscillator circuit include:

1. Ensuring the crystal and external circuitry meet oscillation conditions. This requires a sufficiently large negative resistance $-R_{neg}$ to effectively "cancel" the crystal's positive resistance, allowing the crystal to start and maintain oscillation.
   - It is generally recommended that the negative resistance $|-R_{neg}|$ be 3–5 times the load resistance R_{Load}.
   - If the $-R_{neg}$ margin is low and R_{Load} is too high, safe crystal operation cannot be guaranteed. This may require adjusting the load capacitance C_{Load} by increasing external capacitors C_{L1} and C_{L2} to reduce the total load resistance R_{Load}. However, capacitor adjustments may shift the crystal frequency, so the oscillation frequency should be measured to ensure it remains within specification.
2. Avoiding overdriving the crystal and controlling crystal power dissipation. Excessive drive level DL can reduce lifetime, accelerate aging, cause mechanical damage, and generate spurious or harmonic responses.
   - Crystal manufacturers typically specify a maximum DL that must not be exceeded.
   - Excessive DL may cause the OSC2 oscillation amplitude to increase and approach GND, potentially causing the TCAN455x to erroneously enter single-ended clock mode (see Section 3.4.1). To avoid this, it is recommended to add a damping resistor Rd to reduce DL.
3. Minimizing crystal frequency deviation.
   - Crystal manufacturers typically specify the load capacitance C_{Load} required to achieve the stated frequency accuracy. If C_{Load} is too small, the actual frequency may be higher than the target; conversely, if CLoad is too large, the frequency may be lower.

Therefore, during design, customers must balance the trade-offs among $-R_{neg}$, DL, and f performance to determine the appropriate crystal and external component selection.

3.4 Quartz Crystal Selection

Refer to the application manual. It is recommended that customers select a 40MHz crystal with a maximum ESR of 60Ω and a load capacitance C_{Load} between 8pF and 24pF.

The equivalent load capacitance is shown in Figure 3-4, and the calculation formula is given in Equation 1.

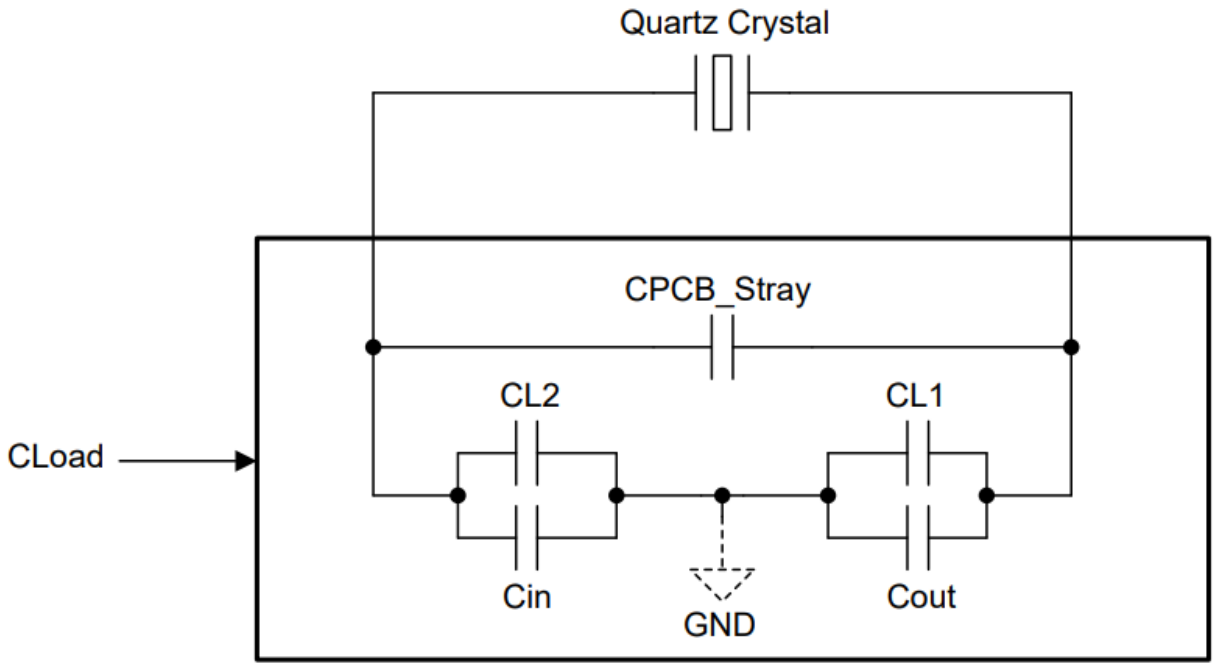

Figure 3-4. TCAN455x Crystal Load Capacitance Equivalent Circuit

$$C_{Load} = \frac{(C_{in} + C_{L2}) \times (C_{L1} + C_{out})}{C_{in} + C_{L2} + C_{L1} + C_{out}} + C_{PCB\_stray} \quad (1)$$

Where:

- C_{out}: Equivalent capacitance of the TCAN455x OSC1 output pin, approximately 10pF;
- C_{in}: Equivalent capacitance of the TCAN455x OSC2 input pin, approximately 9pF;
- C_{L1}, C_{L2}: External capacitors from TCAN455x OSC1 and OSC2 to ground, with $C_{L1} = C_{L2}$;
- C_{PCB_stray}: PCB stray capacitance.

After selection, it is recommended that customers measure the waveform at the TCAN455x OSC2 pin **under all operating conditions to verify that the voltage is always above 150mV.** Otherwise, the device may erroneously switch from quartz crystal clock mode to single-ended clock mode, leading to communication failure (see Section 3.4.1).

3.4.1 Issue of Erroneous Entry into Single-Ended Clock Mode

When the TCAN455x crystal oscillator circuit is improperly designed and the OSC2 voltage falls below the detection threshold, the clock mode may erroneously switch to single-ended input clock mode. Even though oscillation waveforms may still be present on the OSC1/2 pins, the internal clock is disabled, causing the clock for the digital core and MCAN controller to be interrupted, resulting in SPI communication and CAN communication failure.

Figure 3-5 shows the waveform of the TCAN455x internal clock signal routed to the GPIO1 pin in test mode, where intermittent internal clock interruptions can be observed.

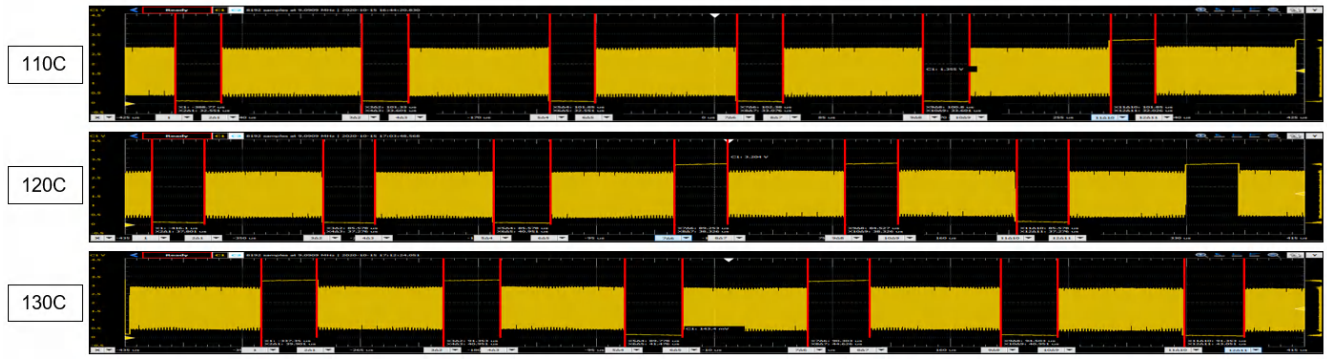

Figure 3-5. Internal Clock Waveform When Erroneously Entering Single-Ended Clock Mode

Specifically, the device intermittently enters single-ended clock mode. The OSC oscillation waveform can still be observed and does not completely disappear. The process is as follows: When the device switches to single-ended clock mode, the transconductance amplifier is disabled, the current source supplying the crystal is disabled, and the internal 500kΩ feedback resistor between the OSC1 and OSC2 pins is disconnected. The impedance changes, causing the common-mode voltage of the OSC waveform to ring or dip abruptly, although the crystal continues to oscillate. As energy in the circuit decreases due to parasitic resistance and the lack of new current supply from the amplifier, the OSC Vpp amplitude diminishes. When the OSC2 waveform rises above the detection threshold, the device switches back to quartz crystal mode and supplies current to the crystal, causing the Vpp amplitude to increase. When the amplitude increases to the trigger threshold, the device re-enters single-ended clock mode. This process repeats periodically, as illustrated in Figure 3-6 below.

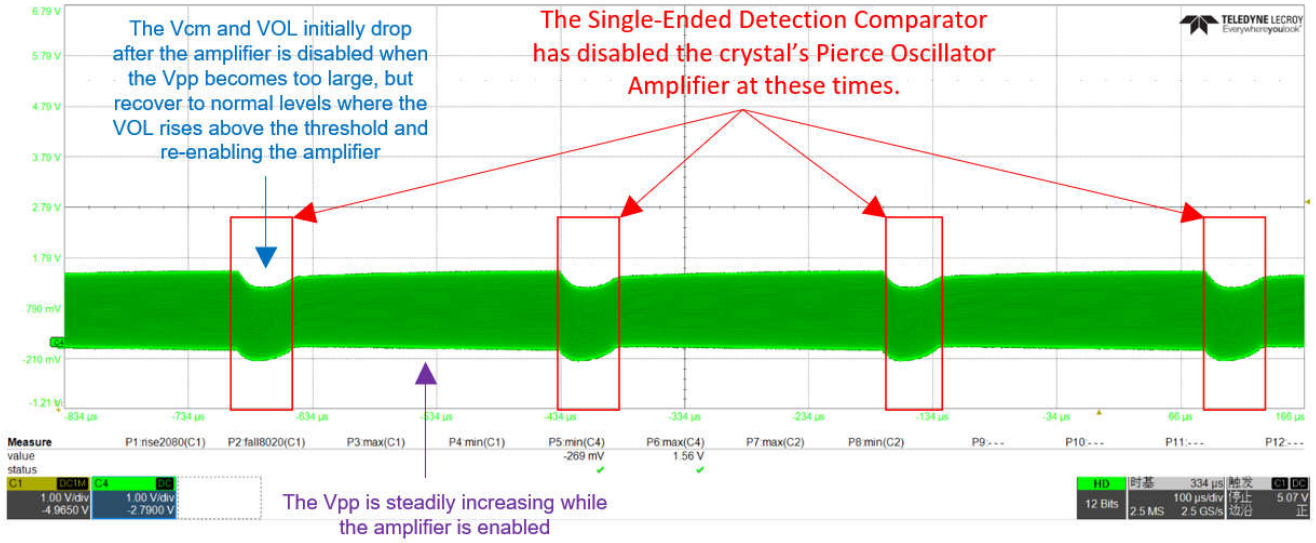

Figure 3-6. OSC2 Waveform When Erroneously Entering Single-Ended Clock Mode

3.4.2 Solutions for Erroneous Entry into Single-Ended Clock Mode

In some cases, the crystal manufacturer has matched the crystal and load capacitance C_{Load} in a way that cannot be changed, and the actual OSC2 valley voltage is already close to the threshold, posing a risk of mode switching. Figure 3-7 below shows the OSC2 waveform using the ABM11AIG-40.000MHZ-4-1Z-T (4pF, 60Ω) crystal, with a valley voltage of approximately 168mV, which is close to the 150mV detection threshold.

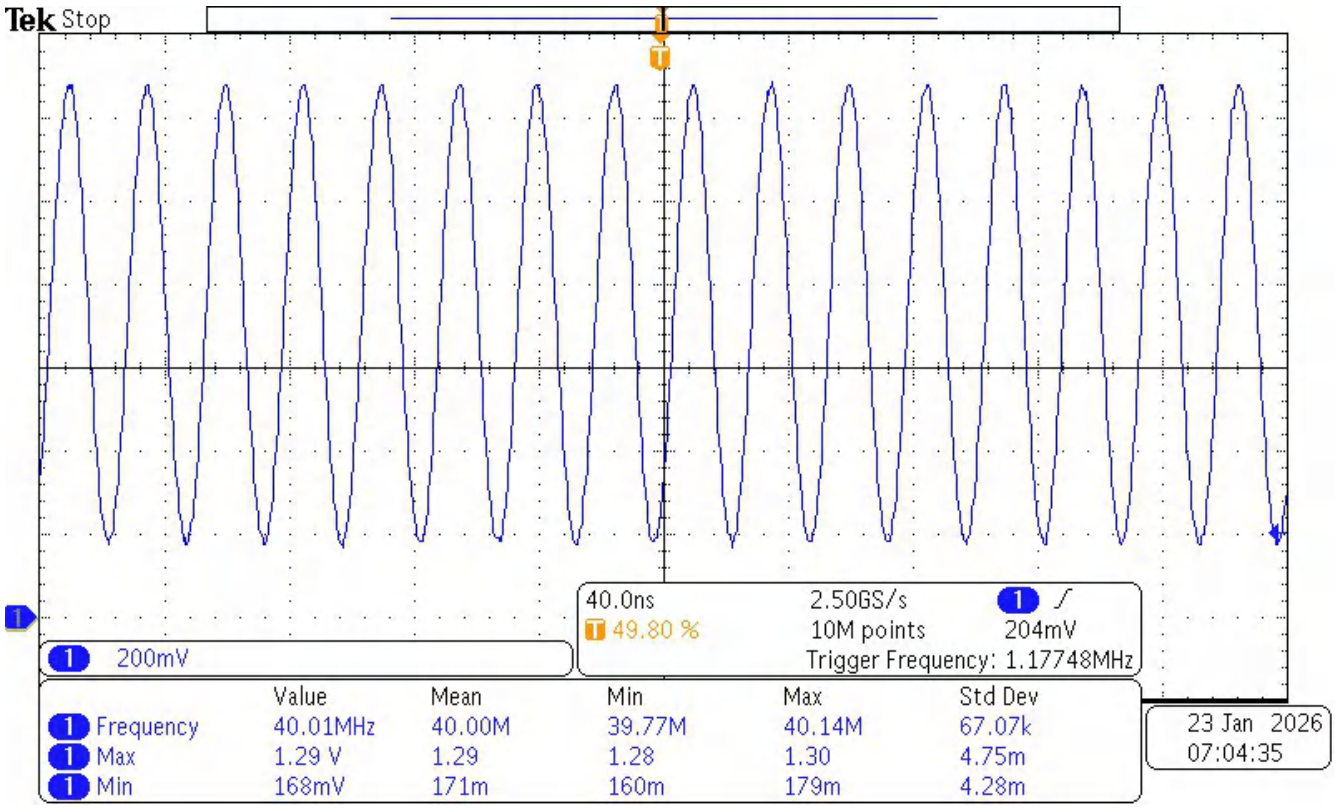

Figure 3-7. OSC2 Waveform (Close to 150mV Threshold, at Risk)

To avoid clock mode switching, it is recommended to add a **damping resistor Rd** in series between the OSC1 pin and the crystal, as shown in Figure 3-8 below. OSC1 is the output pin in crystal clock mode; the bias current flows out of the OSC1 pin to the crystal to initiate and sustain oscillation. Adding Rd limits the current and reduces the drive level DL, thereby reducing the oscillation amplitude. Note: $DL = I_{rms}^2 \times R_{Load}$. Increasing C_{Load} reduces R_{Load} and thereby reduces DL; when C_{Load} cannot be changed, reducing I_{rms} also reduces DL.

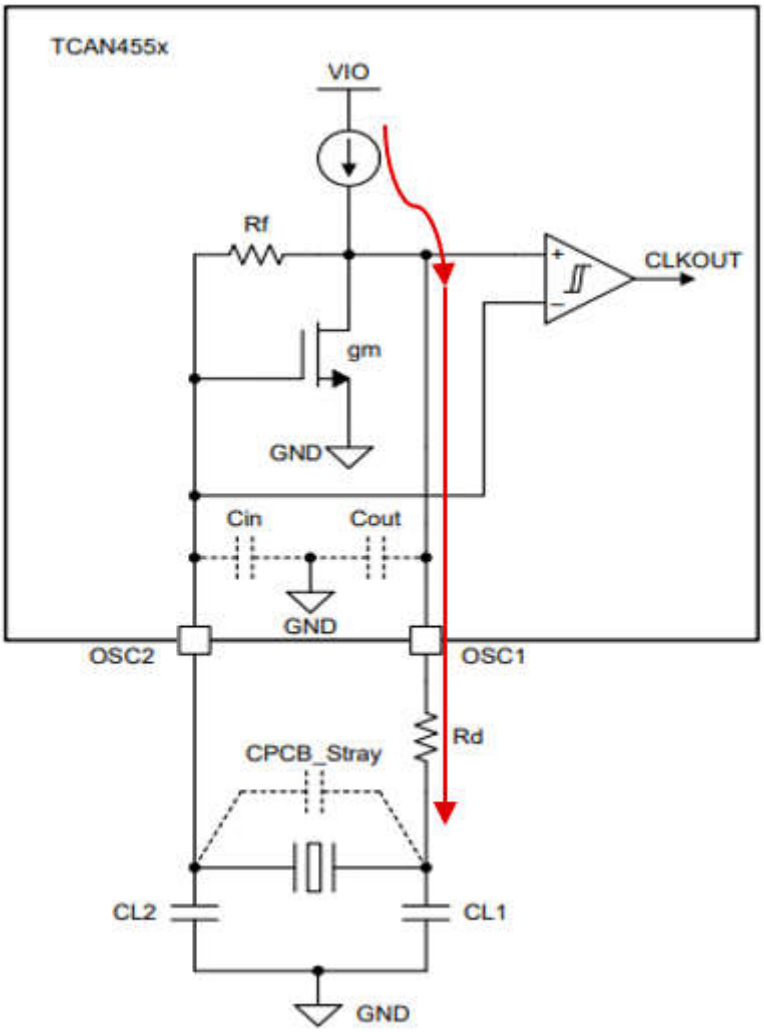

Figure 3-8. OSC1 Damping Resistor Rd

Figure 3-9 below shows the OSC2 waveform after adding a 100Ω Rd. Compared to Figure 3-7, the minimum voltage improves from 168mV to 424mV, a significant improvement that provides ample margin to avoid clock mode switching.

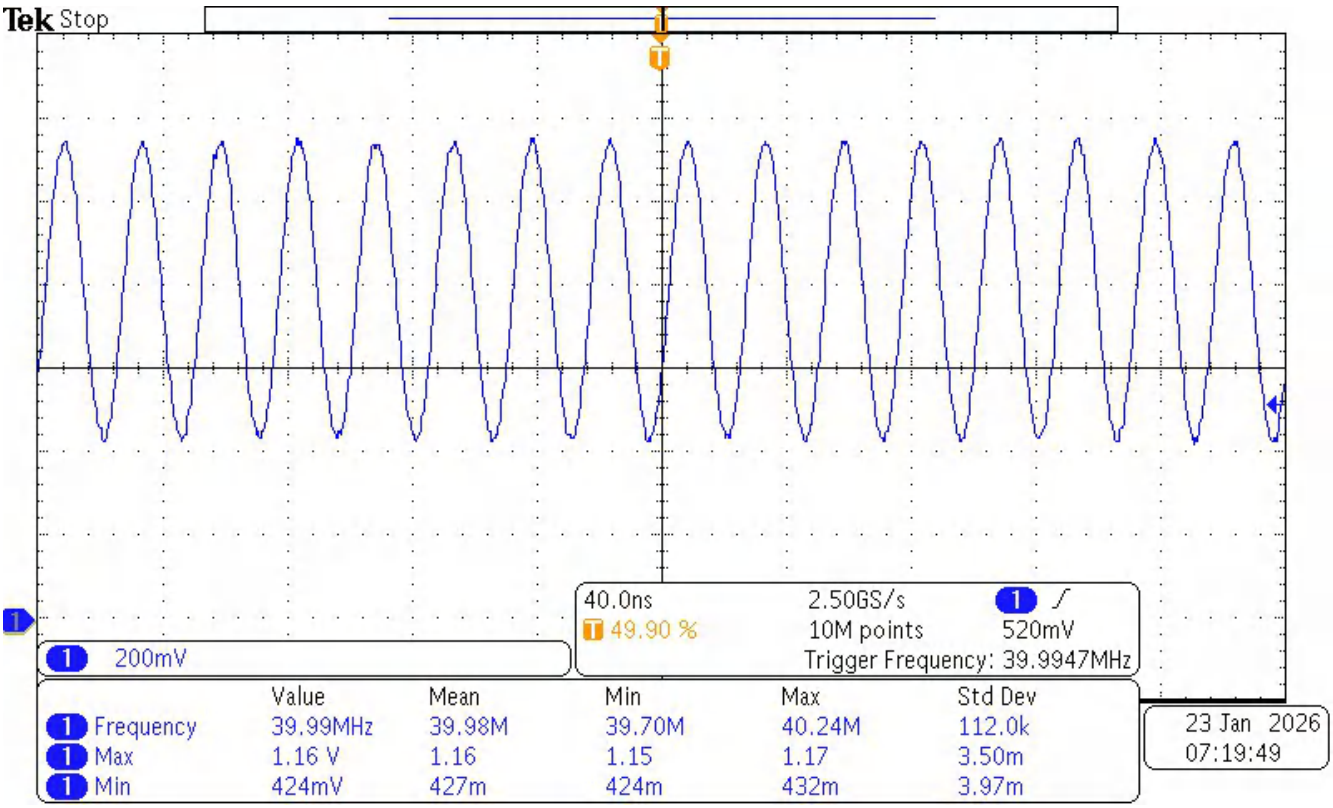

Figure 3-9. OSC2 Waveform (After Adding 100Ω Rd, Significantly Improved)

4 Conclusion

This article first introduced the basic functions of the TCAN455x-Q1 series products, then listed the peripheral circuit design considerations for each pin, and finally focused on the clock circuit operating principles and quartz crystal selection. It is essential to ensure that the OSC2 pin voltage remains above 150mV to prevent erroneous entry into single-ended clock mode. Solutions and test waveforms have been provided.

5 References

1. TCAN4550-Q1 Datasheet (SLLSEZ5D)
2. TCAN4551-Q1 Datasheet (SLLSEZ4A)
3. System Basis Chip 101 – A Beginner's Guide to CAN, CAN FD, and LIN SBCs (ZHCT498A)
4. Precision Labs Series: CAN & LIN Transceivers & SBCs
5. CDCE6214-Q1 Crystal-Based Oscillator Design
6. TCAN455x Clock Optimization and Design Guidelines (SLLA549)
7. TCAN4550-Q1: Osc1 Osc2 Amplitude Requirement – Interface – INTERNAL Forum – Interface – INTERNAL – TI E2E Support Forums

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