



TPS40009-Based, 5-A Converter in Less Than One Square Inch

User's Guide

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TPS40009-Based 5-A Converter in Less Than One Square Inch

Mark Dennis

Systems Power

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1 Introduction

The TPS40009 is a voltage-mode, synchronous buck PWM controller that uses TI's proprietary Predictive Gate Drive™ technology to wring maximum efficiency from step-down converters. This controller provides a bootstrap charging circuit to allow the use of an N-channel MOSFET as the topside buck switch to reduce conduction losses and increase silicon device utilization. Predictive Gate Drive™ technology controls the delay from main switch turn-off to synchronous rectifier turn-on and also the delay from rectifier turn-off to main switch turn-on. This allows minimization of the losses in the MOSFET body diodes by reducing conduction and reverse recovery time. This user's guide provides details on a 5-A buck converter that converts 3.3 V down to a 1.2-V level using the TPS40009 controller, with less than one square inch board area.

A schematic for the board is shown in Figure 1. A list of material is provided in the final section.

2 Features

The specification for this board is as follows:

- $V_{IN} = 3.0\text{ V to }3.6\text{ V}$
- $V_{OUT} = 1.2\text{ V} \pm 3\%$
- $0\text{ A} \leq I_{OUT} \leq 5\text{ A}$
- Efficiency > 90% with a load of 2 A
- Output voltage ripple < 2% V_{OUT}
- Physical size < 1 square inch circuit area

3 Schematic

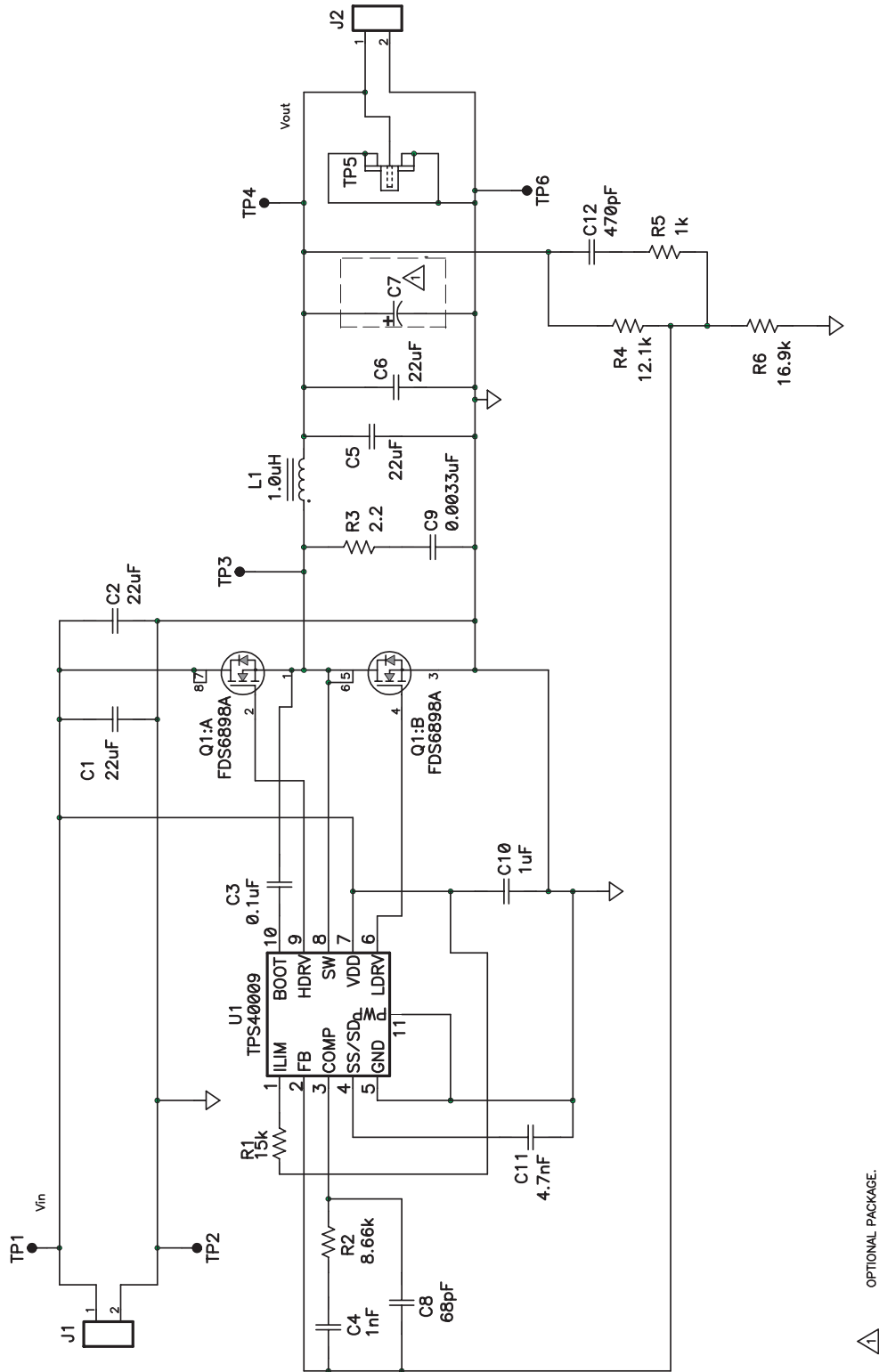


Figure 1. Application Diagram for the TPS40009

4 Design Procedure

4.1 Controller Selection

The TPS40009 synchronous buck controller is selected for this small size application because the 600-kHz switching frequency enables the selection of minimally sized filter components. The TPS40007 is available for applications needing 300-kHz operation for designs where efficiency is to be optimized.

4.2 Inductance Value

The output inductor value is selected to set the ripple current to a value most suited to overall circuit functionality. The inductor value is calculated in equation (1).

$$L = \frac{V_{OUT}}{f \times I_{RIPPLE}} \left(1 - \frac{V_{OUT}}{V_{IN(max)}} \right) = \frac{1.2 \text{ V}}{600 \text{ kHz} \times 1.25 \text{ A}} \times \left(1 - \frac{1.2 \text{ V}}{3.6 \text{ V}} \right) = 1.07 \text{ } \mu\text{H} \quad (1)$$

where I_{RIPPLE} is chosen to be 25% of I_{OUT} , or 1.25 A. A common value of 1 μH is selected.

4.3 Input Capacitor Selection

Bulk input capacitor selection is based on allowable input voltage ripple and required RMS current carrying capability. In typical buck converter applications, the converter is fed from an upstream power converter with its own output capacitance. In this converter, onboard capacitance is provided to supply the current required during the top MOSFET on-time while keeping ripple within acceptable limits. For this power level, input voltage ripple of 150 mV is reasonable, and a conservative minimum value of capacitance is calculated in equation (2).

$$C = \frac{I \times \Delta t}{\Delta V} = \frac{5 \text{ A} \times 606 \text{ ns}}{0.15 \text{ V}} = 20 \text{ } \mu\text{F} \quad (2)$$

To meet this requirement with the lowest size and cost, a single 22 μF , X5R ceramic capacitor might be considered. Although these capacitors have an extremely small resistance a typical datasheet indicates that the part undergoes a 30°C temperature rise with 2 A_{RMS} current at 500 kHz. With $V_{IN} = 3.0 \text{ V}$ our circuit requires nearly 2 A_{RMS} of current, so for a conservative design two capacitors are selected to allow for conservative current derating. These capacitors function as power bypass components and should be located near the MOSFET package, to keep the high frequency current flow in a tight loop. The low impedance characteristics of the dual ceramic capacitors help to reduce noise on the V_{DD} supply of the device. Specifically, the high side MOSFET current sense is referenced to this point, so noise at the device must be kept to a low level.

4.4 Output Capacitor Selection

Selection of the output capacitor is based on many application variables, including function, cost, size, and availability. The minimum allowable output capacitance is determined by the amount of inductor ripple current and the allowable output ripple in equation (3).

$$C_{\text{OUT(min)}} = \frac{I_{\text{RIPPLE}}}{8 \times f \times V_{\text{RIPPLE}}} = \frac{1.25 \text{ A}}{8 \times 600 \text{ kHz} \times 12 \text{ mV}} = 22 \mu\text{F} \quad (3)$$

In this design, $C_{\text{OUT(min)}}$ is 22 μF with $V_{\text{RIPPLE}} = 12 \text{ mV}$ to allow for some margin. However, this only affects the capacitive component of the ripple voltage. In addition, the voltage component due to the capacitor ESR must be considered in equation (4).

$$\text{ESR}_{\text{Cout}} \leq \frac{V_{\text{RIPPLE}}}{I_{\text{RIPPLE}}} = \frac{0.012 \text{ V}}{1.25 \text{ A}} = 9.6 \text{ m}\Omega \quad (4)$$

For compactness while maintaining transient response capability, two 22- μF ceramic capacitors are fitted in parallel. The total ESR of these capacitors is below 3 $\text{m}\Omega$, and contributes only a few mV to the output voltage ripple.

4.5 MOSFET Selection

The small physical size of this design requires the use of a single SO-8 package which contains dual N-channel MOSFETs. MOSFETs with an $R_{\text{DS(on)}}$ of 18 $\text{m}\Omega$ are selected to keep the conduction losses to a manageable amount at full load.

4.6 Short Circuit Protection

The TPS40009 implements short circuit protection by comparing the voltage across the topside MOSFET while it is on to a voltage dropped from V_{DD} by R_{LIM} due to an internal current source of 15 μA inside pin 1. Due to tolerances in the current source and variations in the power MOSFET on-voltage versus temperature, the short circuit level can protect against gross overcurrent conditions only, and should be set higher than rated load. In this particular case, R_{LIM} is selected as:

$$R_{\text{LIM}} = R1 = \frac{2.5 \times I_{\text{OUT}} \times 0.018 \Omega}{15 \mu\text{A}} = 15 \text{ k}\Omega \quad (5)$$

For this design, $R_{\text{LIM}} = 15 \text{ k}\Omega$, and the factor of 2.5 in the equation accounts for the variations in component tolerances over temperature and output current ripple.

4.7 Compensation Design

The TPS40009 uses voltage mode control in conjunction with a high frequency error amplifier. For the fastest transient response, the loop crossover frequency is set at $1/10 f_S$, or 60 kHz. The power circuit L-C double pole corner frequency f_C is situated at 24 kHz, and the output capacitor ESR zero is far higher at approximately 1MHz. The feedback compensation network is implemented to provide two zeroes and three poles. The first pole is placed at the origin to improve dc regulation.

The first zero is placed at approximately $2/3 f_C$, 18 kHz,

$$f_{z1} = \frac{1}{2 \times \pi \times R_2 \times C_4} \quad (6)$$

The second zero is selected at f_C ,

$$f_{z2} = \frac{1}{2 \times \pi \times (R_4 + R_5) \times C_{12}} \quad (7)$$

The two poles are placed at approximately 300 kHz, which is one-half the switching frequency,

$$f_{p1} = \frac{1}{2 \times \pi \times R_2 \times \left(\frac{C_4 \times C_8}{C_4 + C_8} \right)} \quad (8)$$

and

$$f_{p2} = \frac{1}{2 \times \pi \times R_5 \times C_{12}} \quad (9)$$

Figure 2 shows the plots for the closed loop gain and phase with $V_{IN} = 3.3\text{ V}$ and $I_{OUT} = 4.4\text{ A}$. At the crossover frequency of 60 kHz the phase margin is approximately 51 degrees.

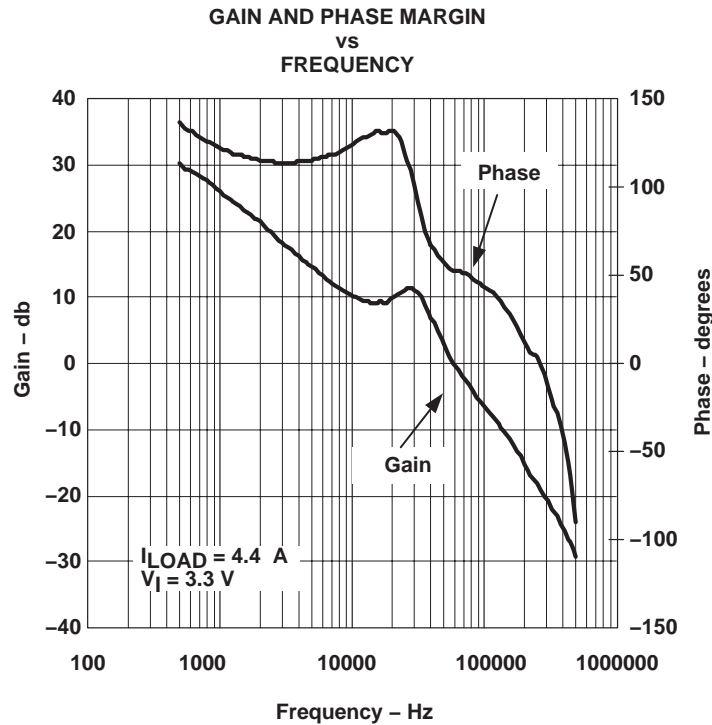


Figure 2.

4.8 Snubber Component Selection

The switch node where Q1 and L1 come together is very noisy. An R-C network fitted between this node and ground can help reduce ringing and voltage overshoot on Q1:B. This ringing noise should be minimized to prevent it from confusing the control circuitry which is monitoring this node for current limit and Predictive Gate Drive™.

As a starting point, the snubber capacitor, C9, is generally chosen to be 5 to 8 times larger than the parasitic capacitance at the node, which is primarily C_{OS} of Q1:B. Since C_{OS} is 440 pF for Q1:B, C9 is chosen to be 3.3 nF. R3 is empirically determined to be 2.2 Ω , which minimizes the ringing and overshoot at the switch node. With low input voltages the power loss, $1/2 \times C \times V^2 \times f$, is relatively small at 24 mW.

5 PowerPAD™ Packaging

The TPS4000X family is available in the DGQ version of TI's PowerPAD™ thermally enhanced package. In the PowerPAD™, a thermally conductive epoxy is used to attach the integrated circuit die to the leadframe die pad, which is exposed on the bottom of the completed package. The leadframe die pad can be soldered to the PCB using standard solder flow techniques when maximum heat dissipation is required. However, depending on power dissipation requirements, the PowerPAD™ may not need to be soldered to the PCB.

The PowerPAD™ package helps to keep the junction temperature rise relatively low even with the power dissipation inherent in the onboard MOSFET drivers. This power loss is proportional to switching frequency, drive voltage, and the gate charge needed to enhance the N-channel MOSFETs. Effective heat removal allows the use of ultra small packaging while maintaining high component reliability.

To effectively remove heat from the PowerPAD™ package, a thermal land should be provided directly underneath the package whether the package needs to be soldered or not. This thermal land usually has vias that help to spread heat to internal copper layers and/or the opposite side of the PCB. The vias should not have thermal reliefs that are often used on ground planes, because this reduces the copper area which transfers heat. Additionally, the vias should be small enough so that the holes are effectively plugged when plated. This prevents the solder from wicking away from the connection between the PCB surface and the bottom of the part. A typical construction uses a few vias of 0.013" diameter plated with 1 ounce copper in the land under the TPS40009. A typical layout pattern is shown in Figure 2, but does not show the copper land which would encompass the vias above and below the device.

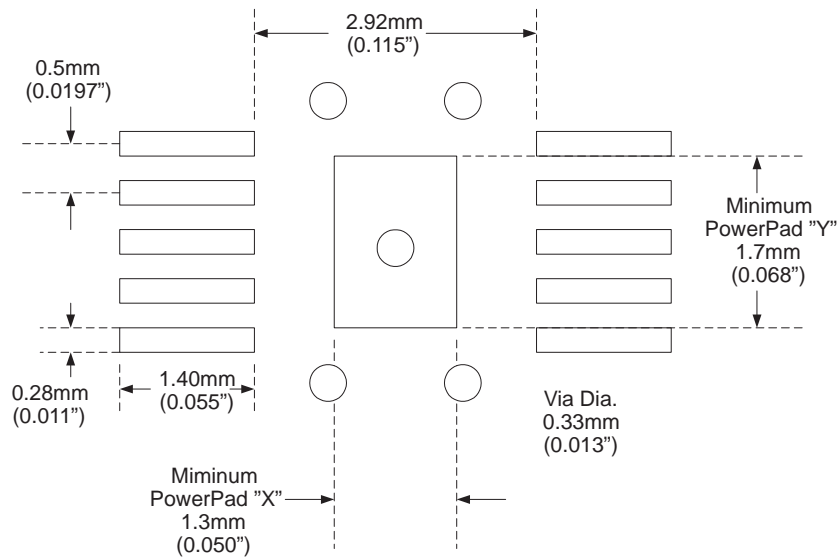


Figure 3. PowerPAD PCB Layout Guidelines

The Texas Instrument document, PowerPAD™ Thermally Enhanced Package Application Report (SLMA002) should be consulted for more information on the PowerPAD™ package. This report offers in-depth information on the package, assembly and rework techniques, and illustrative examples of the thermal performance of the PowerPAD™ package.

6 Test Results/Performance Data

The test setup is shown in figure 4

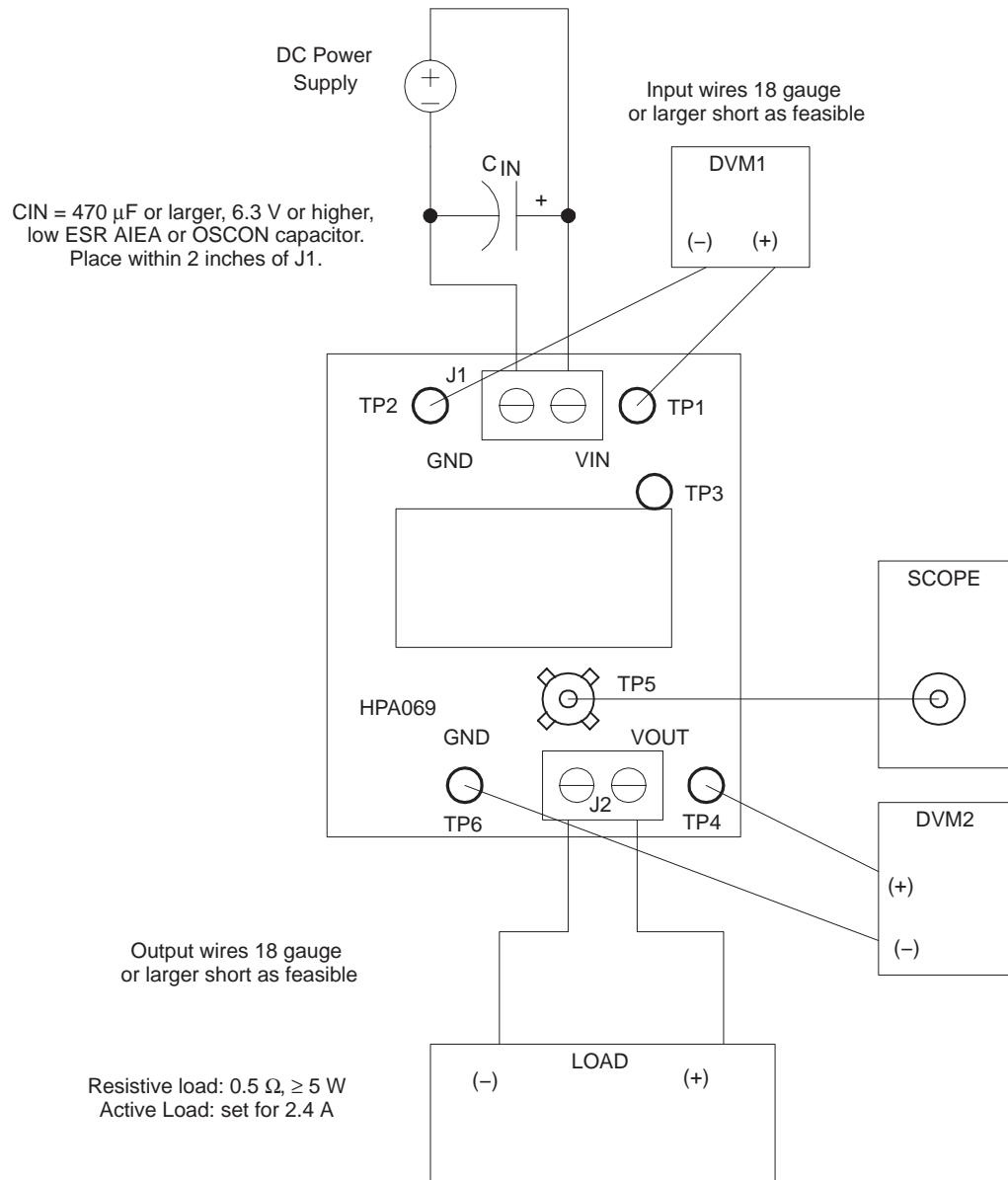


Figure 4.

Typical efficiency curves are shown in Figure 5 for an input of 3.3 V.

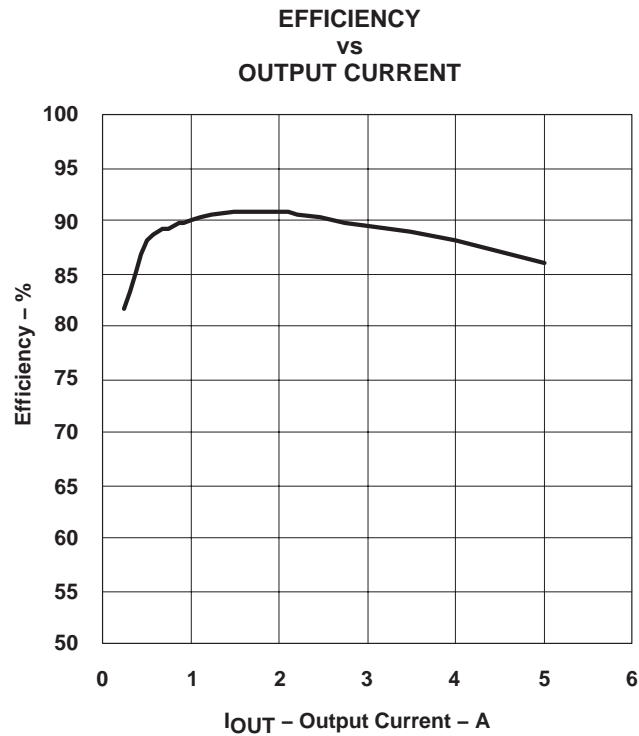


Figure 5.

Figure 6 shows the switch node during typical operation at full load. Note that there is very minimal body diode conduction in the bottom MOSFET. This is a result of using the predictive delay control implementation. This technique is able to dynamically change the delays in the MOSFET drive circuit to account for variations in line, load, and between devices.

TYPICAL SWITCH NODE WAVEFORM

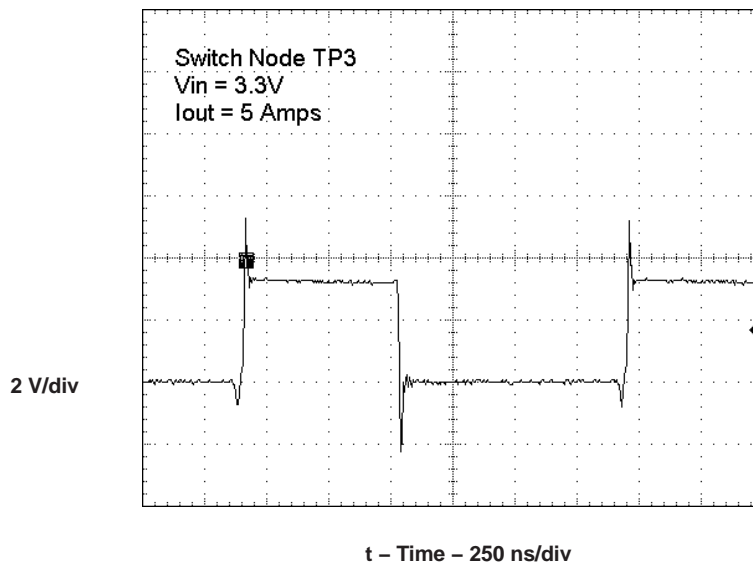


Figure 6.

Circuit operation with an output short circuit is shown in Figure 7. After each restart into a short circuit the pulses terminate for a period of approximately 6 ms. This causes the input power to collapse to minuscule levels, and the circuit is protected.

SHORT CIRCUIT OPERATION

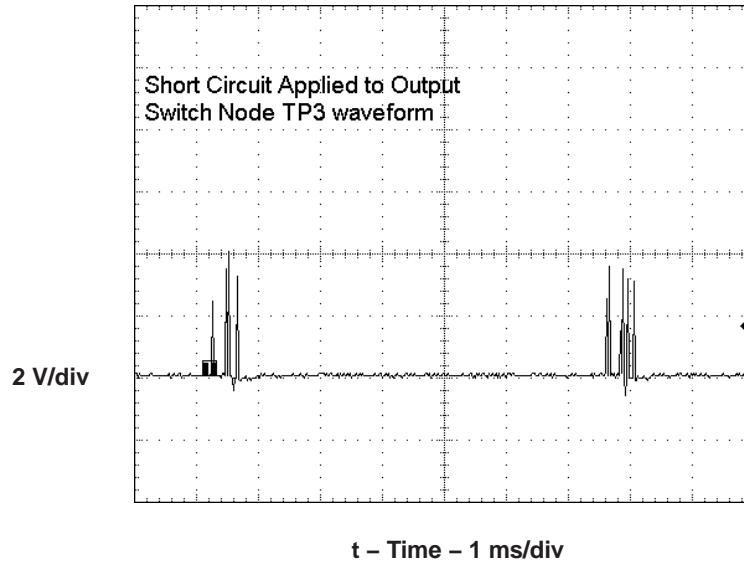


Figure 7.

Figure 8 shows the output voltage ripple which is approximately half the 24-mV limit.

OUTPUT VOLTAGE RIPPLE

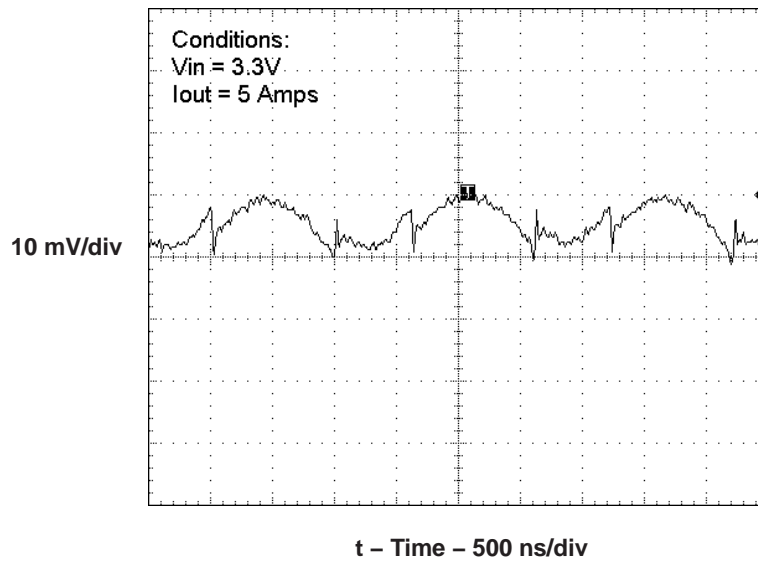


Figure 8.

Figure 9 shows the startup waveforms with an input voltage of 3.3 V and a load of 0.3 Ω. Note that the output is held low until V_{SS} (pin 4) goes above 0.12 V, and then the output comes up smoothly under closed loop softstart control.

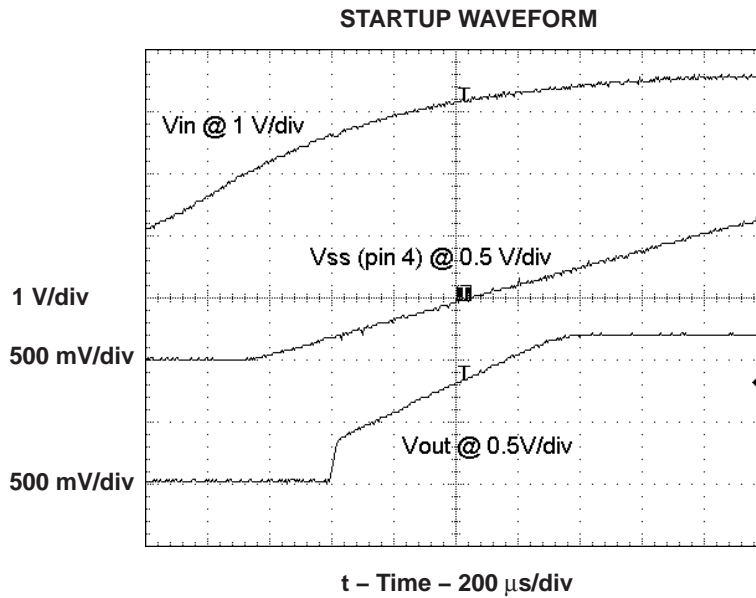


Figure 9.

Figure 10 shows the transient response for a fast load step from 1 A to 2 A.

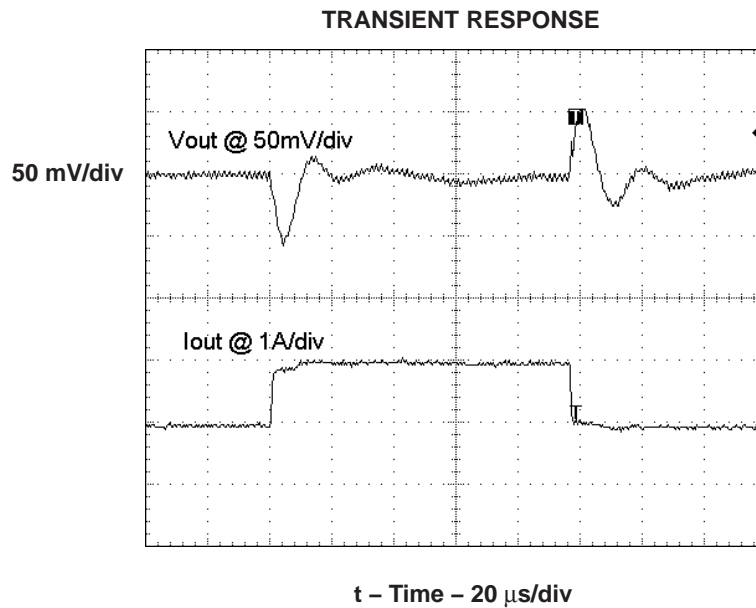


Figure 10.

7 PCB Layout

Figures 11 through 13 show the top copper layer, the bottom copper layer, and top assembly layer, of HPA069.

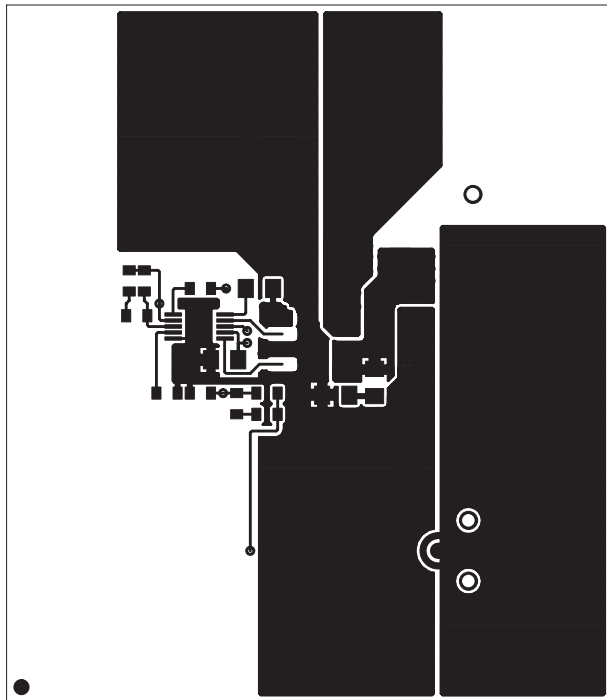


Figure 11

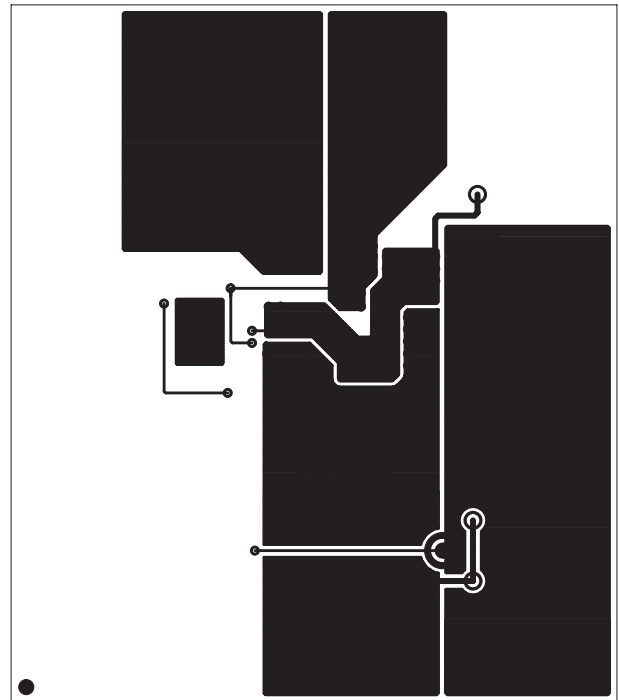


Figure 12

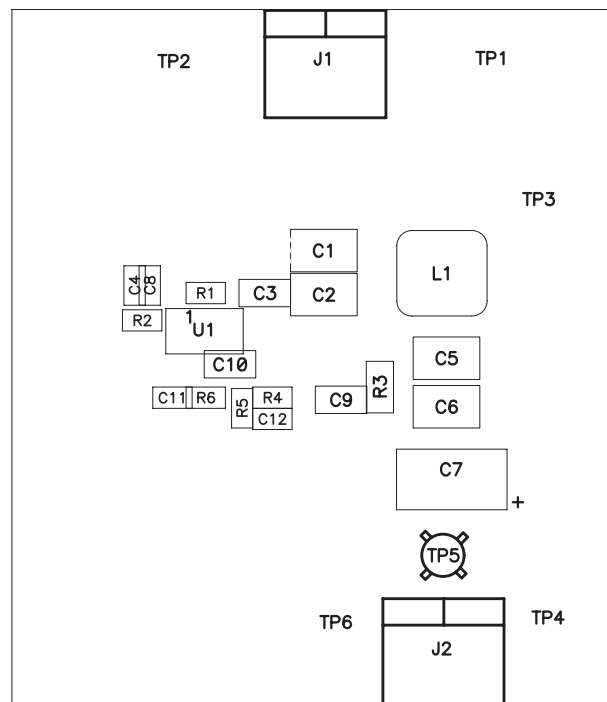
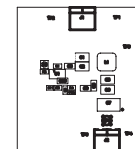


Figure 13



actual size

8 List of Material

Table 1 lists the components used in this design. With minor component tweaks this design could be modified to meet a wide range of applications.

	Reference	Qty	Description	Manufacturer	Part Number
Capacitor	C1, C2, C5, C6	4	Ceramic, 22 μ F, 6.3 V, X5R, 20%, 1210	Panasonic	ECJ-4YB0J226M
	C10	1	Ceramic, 0.001 μ F, 10 V, X5R, 10%, 805	Panasonic	ECJ-2YB1A105K
	C11	1	Ceramic, 0.0047 μ F, 50 V, X7R, 10%	Vishay	VJ0603Y472KXAAT
	C12	1	Ceramic, 470 pF, 50 V, X7R, 10%	Vishay	VJ0603Y471KXAAT
	C3	1	Ceramic, 0.1 μ F, 50 V, X5R, 10%	Vishay	VJ0805Y104KXAAT
	C4	1	Ceramic, 0.001 μ F, 50 V, X7R, 10%	Vishay	VJ0603Y102KXAAT
	C8	1	Ceramic, 68 pF, 50 V, NPO, 10%	Vishay	VJ0603A680KXAAT
	C9	1	Ceramic, 0.0033 μ F, 50 V, X7R, 10%	Vishay	VJ0805Y332KXAAT
Terminal Block	J1, J2	2	2 pin, 15 A, 5.1 mm	OST	ED1609
Inductor	L1	1	SMT, 1.0 μ H, 8.5 A, 10 m Ω	Vishay	IHLP-2525CZ-01
MOSFET	Q1	1	Dual N-channel, 20 V, 9.4 A, 18 m Ω	Fairchild	FDS6898A
Resistor	R1	1	Chip, 15 k Ω , 1/16W, 1%	Std	Std
	R2	1	Chip, 8.66 k Ω , 1/16 W, 1%	Std	Std
	R3	1	Chip, 2.2 Ω , 1/10 W, 5%	Std	Std
	R4	1	Chip, 12.1 k Ω , 1/16 W, 1%	Std	Std
	R5	1	Chip, 1 k Ω , 1/16 W, 1%	Std	Std
	R6	1	Chip, 16.9 Ω , 1/16 W, 1%	Std	Std
JACK	TP1, TP3, TP4,	5	Test point, red	Farnell	240-345
JACK	TP2, TP6	2	Test point, black	Farnell	240-333
Adaptor	TP5	1	3.5-mm probe clip (or 131-5031-00)	Tektronix	131-4244-00
Device	U1	1	Synchronous buck controller, 600 kHz	TI	TPS40009DGQ

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CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

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Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

3.3 Japan

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

<https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html>

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。技術適合証明を受けていないものご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。日本テキサス・イ

ンスツルメンツ株式会社

東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。 <https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html>

3.4 European Union

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):*

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

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4. *EVM Use Restrictions and Warnings:*
 - 4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.
 - 4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.
 - 4.3 *Safety-Related Warnings and Restrictions:*
 - 4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.
 - 4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.
 - 4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.
 5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.
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