Application Note

An empirical analysis of the impact of board layout on LDO thermal performance

Gerard Copeland

ABSTRACT

This application report investigates the impact of the printed circuit board (PCB) layout on low dropout (LDO) regulator thermal performance, specifically the junction-to-ambient thermal resistance, θ_{JA}. This parameter is measured for the TPS745 (WSON package), TPS7B82-Q1 (TO-252 package), and TLV755P (SOT-23 package) devices. Each device is tested with five layouts, each containing increasing amounts of copper coverage on both internal and external layers. Increasing the amount of copper coverage reduces θ_{JA}, but reaches a point of diminishing returns. Copper coverage is more effective on packages with thermal pads. These results are used to provide layout tips for system designers to improve thermal performance. Although the devices tested in this study are exclusively LDOs, the effects of the PCB layout and conclusions drawn in this application report are extended to other power dissipative devices.

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1 Introduction

LDOs are the most common DC/DC converter in electronic power designs due to their relative simplicity and cost advantage. As applications become increasingly integrated and compact, power designs must become smaller and cheaper, resulting in more LDO content. As a result, thermal performance is an even more important system design factor as LDOs are linear converters and inherently power dissipative. While JEDEC has standardized the method to measure and report semiconductor thermal metrics in a uniform manner, the standard is not fully optimized for thermal performance. One of the most significant factors that affects thermal performance falls on the system designer, PCB layout. The goal of this application report is to aid these designers by investigating the effect of PCB layout on the thermal performance of LDOs. Although the *LDOs thermal performance in small SMD packages application report* and the *AN-1520 a guide to board layout for best thermal resistance for exposed packages application report* previously discussed this topic, this study aims to be more applicable by collecting data in a functional setting. This setting includes functional PCB layouts with passive components that emulate TI Evaluation Modules (EVMs), and thermal measurements taken through active powering. Active powering refers to placing the LDO in a normal operation and varying the input voltage and the load current to increase the power dissipation and generate heat at the junction of the device.

The most popular metric for evaluating semiconductor thermal performance is the junction-to-ambient thermal resistance, θ_{JA}. Equation 1 shows that this parameter is defined as the difference between the operating temperature and junction temperature of a device per watt of power dissipated in the device:

$$\theta_{JA} = \frac{T_J - T_A}{P_D} \tag{1}$$

A design with a smaller θ_{JA} has a lower junction temperature for a given level of power dissipation, improving longevity and reliability. *Semiconductor and IC package thermal metrics application report* explains that the two factors that have a large impact on θ_{JA} are the PCB layout and IC package. Three LDOs in common packages, the TPS745 (WSON package), TPS7B82-Q1 (TO-252 package), and TLV755P (SOT-23 package) are tested with five different PCB layouts and are chosen to investigate how much these two factors affect thermal performance.

The dependence of semiconductor thermal performance on additional external factors including air flow, altitude, and ambient temperature has resulted in the need for JEDEC to standardize measurement procedures and test boards for θ_{JA} and other thermal metrics. For this application report, approximations of the Low Effective Thermal Conductivity Test Board, described in https://www.jedec.org/system/files/docs/JESD51-3.PDF, and the High Effective Thermal Conductivity Test Board, described in https://www.jedec.org/system/files/docs/jesd51-7.PDF, are designed for each package along with three custom layouts. The area and layer stack of each board follow the JEDEC standard test board approximations: 4layer PCBs with an area of 9-in^2 (3-in by 3-in). The outer layers contain two ounce copper thickness while the inner layers contain one ounce copper thickness. The five layouts fabricated for each package contain increasing amounts of copper connected to the device with the intent to measure θ_{JA} and show an inverse relationship versus copper coverage. To improve the consistency of the results across the three packages, the amount of copper used for heat sinking in each type of layout is kept equal. In order of least to greatest copper content, the layout types are referred to as:

- 1S0P Approximation
- Internally Disconnected
- JEDEC High-K Approximation
- Thermally Enhanced
- Thermally Saturated

Thermal vias are also included in the thermal landing pad for all WSON and TO-252 layouts according to the JEDEC standard specified in https://www.jedec.org/system/files/docs/JESD51-9.pdf. These vias have a 20 millimeter (mm) diameter, 10-mm hole size, and 17-µm copper plating.

Two different θ_{JA} values are used as benchmarks for comparison. The first is $\theta_{JA,\ datasheet}$ as specified in the Thermal Information table in the datasheet of each device as $R_{\theta JA}$. $\theta_{JA,\ datasheet}$ is derived using a thermal model of the JEDEC High-K Thermal Test Board and is the most popular metric used by designers to evaluate

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thermal performance. The second value is $\theta_{JA,1S0P}$, as measured with the 1S0P Approximation layout. This value provides an example of the expected thermal performance for a worst-case layout. Figure 1-1 through Figure 1-5 show 3D generated images for each of the layouts designed for the TPS745 in the WSON package. Drawings of all four layers for each layout can be found in Appendix A. Table 1-1 provides descriptions for each design layout and copper coverage.

Table 1-1. Layout Identifiers and Descriptions

BOARD	ATTRIBUTE	DESCRIPTION	CONNECTED COPPER AREA(in^2)	DISCONNECTED COPPER AREA(in^2)
1S0P Approximation	Top Layer	Traces only	None	None
	Internal Layer 1	No copper		
	Internal Layer 2	No copper		
	Bottom Layer	Traces only		
	Additional Thermal Vias	None		
Internally Disconnected	Top Layer	Traces only	0.07	16.8
	Internal Layer 1	Medium, unconnected, discontinuous planes [1]		
	Internal Layer 2	Medium, unconnected, discontinuous planes [1]		
	Bottom Layer	Traces and one small ground plane		
	Additional Thermal Vias	None		
JEDEC High-K Approximation	Top Layer	Traces only	10.2	8.53
	Internal Layer 1	One large ground plane		
	Internal Layer 2	Traces and one large, unconnected plane		
	Bottom Layer	One medium ground plane		
	Additional Thermal Vias	None		
Thermally Enhanced	Top Layer	Traces and one small ground plane	10.5	8.43
	Internal Layer 1	Small ground plane and two unconnected planes		
	Internal Layer 2	Traces and one medium ground plane		
	Bottom Layer	One medium ground plane		
	Additional Thermal Vias	Only around the device		
Thermally Saturated	Top Layer	Large ground and power planes	34.1	None
	Internal Layer 1	One large ground plane		
	Internal Layer 2	Traces and one large ground plane		
	Bottom Layer	One large ground plane		
	Additional Thermal Vias	Around the device and throughout the PCB		

(1) Intended to represent high density applications without a dedicated ground plane.

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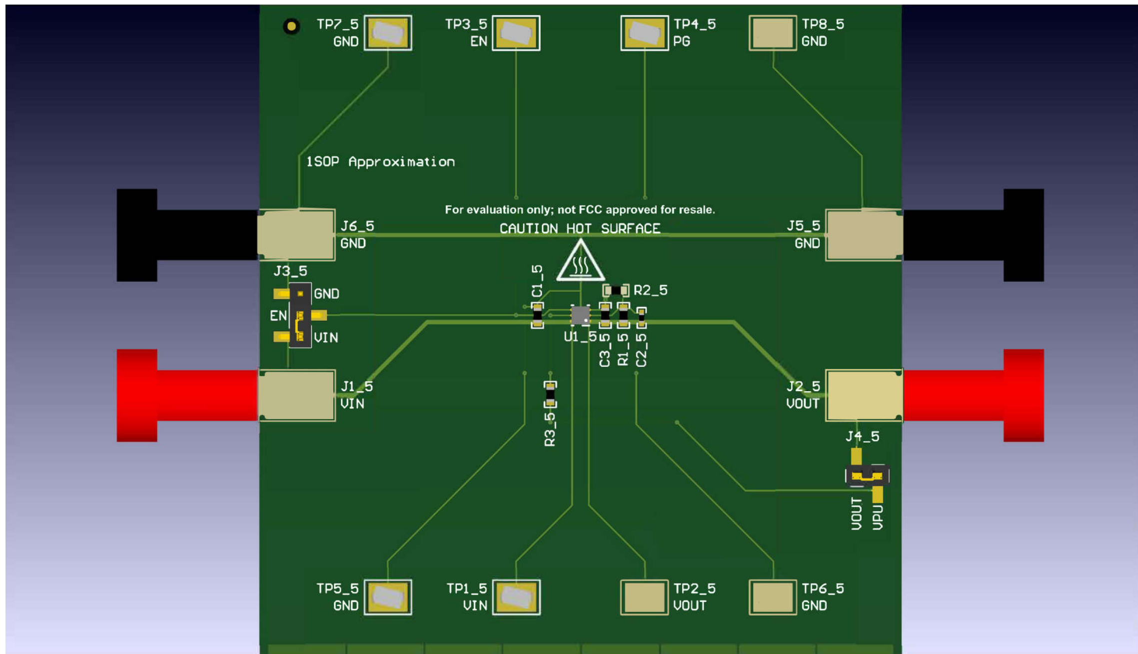

Figure 1-1. TPS745 (WSON) 1S0P Approximation Layout

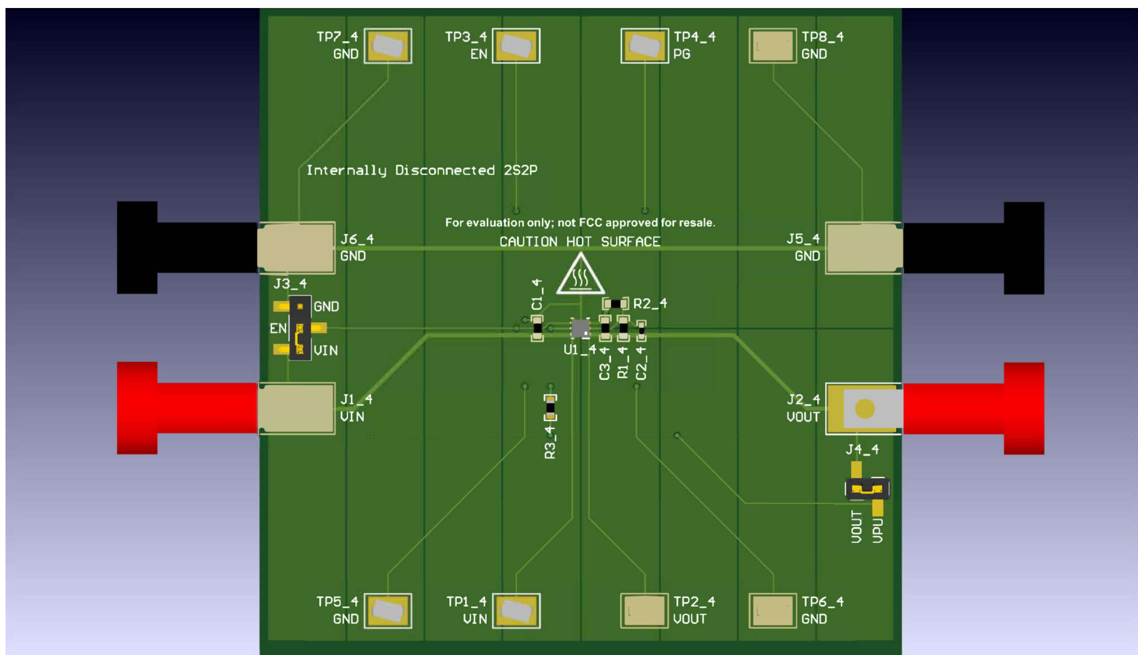

Figure 1-2. TPS745 (WSON) Internally Disconnected Layout

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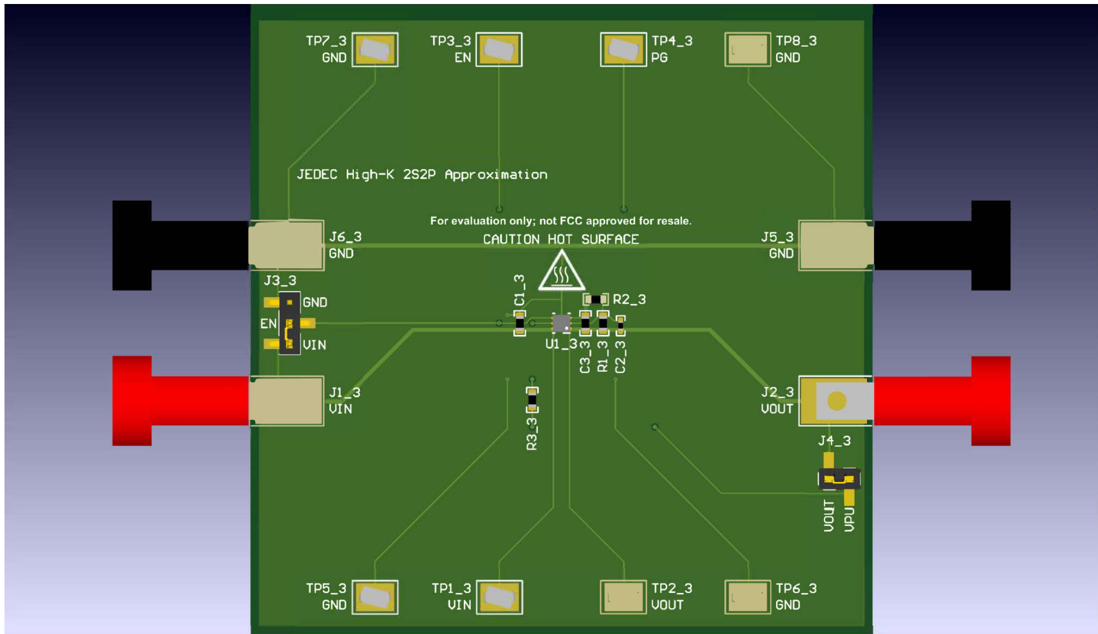

Figure 1-3. TPS745 (WSON) JEDEC High-K Approximation Layout

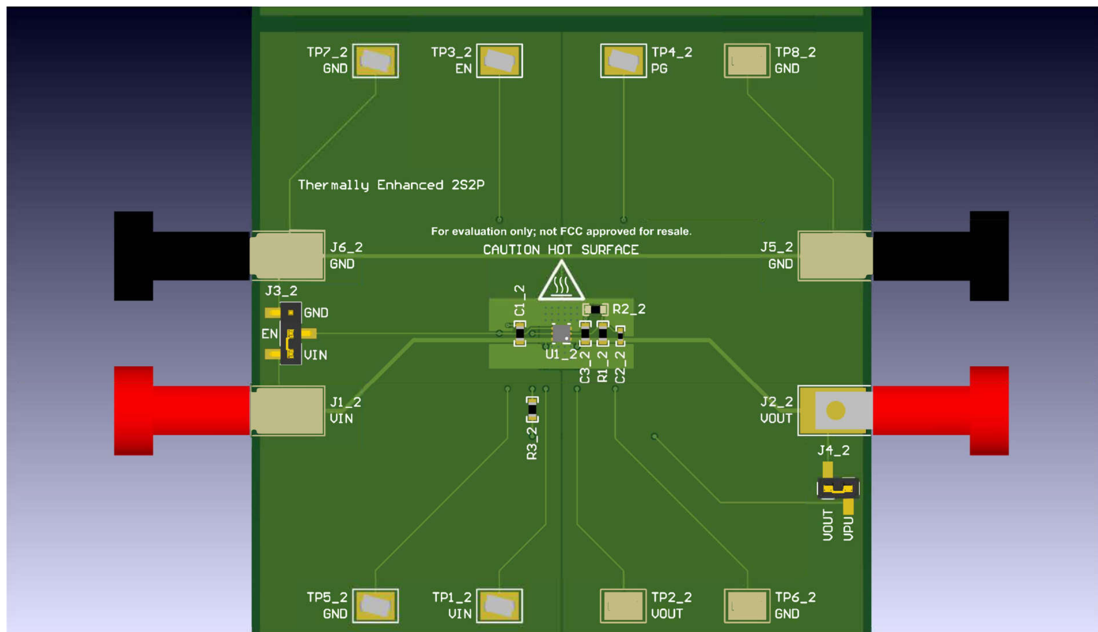

Figure 1-4. TPS745 (WSON) Thermally Enhanced Layout

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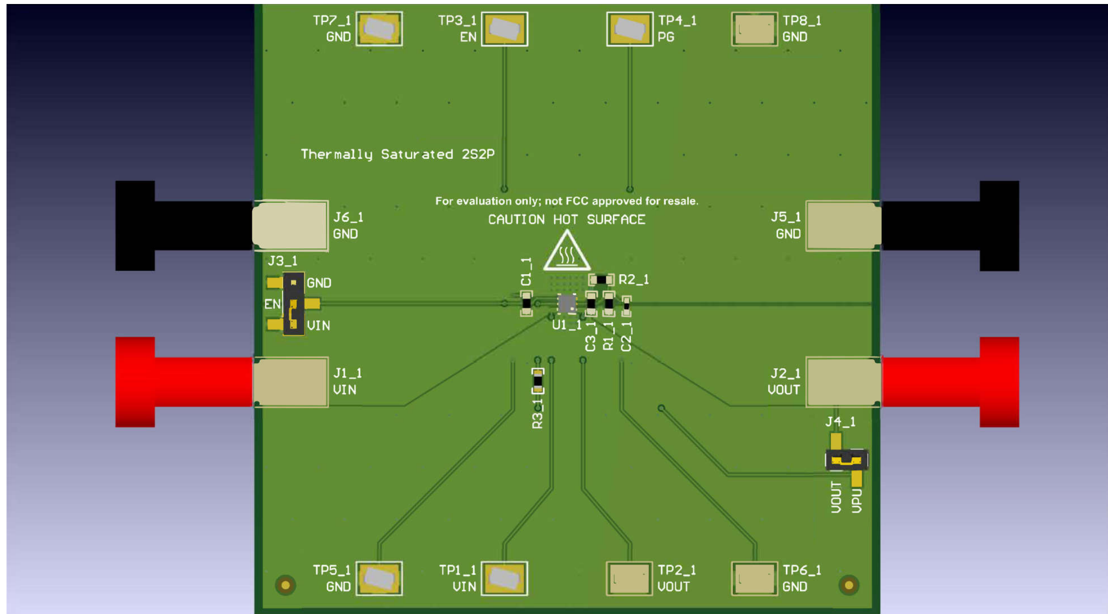

Figure 1-5. TPS745 (WSON) Thermally Saturated Layout

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2 Procedure

Most modern LDOs include a thermal shutdown feature to protect the device from excessive damage at high junction temperatures. For a given level of power dissipation, an LDO with thermal shutdown has a maximum ambient temperature it can operate at before thermal shutdown is triggered and the device shuts off. Equation 2 shows the substitution of the thermal shutdown temperature for the junction temperature and the rearrangement of Equation 1 :

$$T_{A,max} = T_{SD} - \theta_{JA} \times P_D \tag{2}$$

The *Measuring the thermal impedance of LDOs in Situ application report* explains how this equation provides a way to determine θ_{JA} without needing direct access to the junction of the device. First, a small amount of power dissipation is chosen so that the maximum operating ambient temperature is essentially the thermal shutdown temperature of the LDO. A hot oven is used to set the ambient temperature and the LDO is allowed to soak for five minutes. The hot oven must then be turned off to stop any airflow as JEDEC standard models assume no forced convection. An oscilloscope is then used to monitor whether the LDO is shutting off the output. This behavior indicates that thermal shutdown has been triggered. If the LDO does not enter thermal shutdown, the ambient temperature is increased, and the procedure is repeated to determine the maximum operating ambient temperature. This procedure is repeated for increasing levels of power dissipation to provide a sufficient linear regression when calculating θ_{JA} by using Equation 2.

There are some limitations to the accuracy of this procedure as the ambient temperature and power dissipation are susceptible to change while making the measurement. Turning the hot oven off to ensure natural convection causes the ambient temperature to gradually decrease. Removing any cooling due to the convection created by the hot oven simultaneously increases the junction temperature of the device. Due to the bandgap of the LDO reference drift over temperature, the output voltage decreases, increasing the power dissipated in the pass transistor. The accuracy of the measured θ_{JA} is also reduced by the measurement accuracy of the hot oven, which is typically ±2°C. To address these limitations, a wide range of power dissipation levels must be chosen to illustrate a wide maximum ambient temperature range. Equation 2 shows that θ_{JA} is defined as the slope of the trendline between these two variables. As such, verifying that linearity is maintained across a wide range of temperatures and power dissipation increases the credibility of the θ_{JA} measurement.

The major advantage of this procedure lies in its relative simplicity. It can be used to measure θ_{JA} on any board since it does not require modifications to the PCB or LDO to measure the specific board or junction temperature, allowing for a more functional PCB layout and testing environment that is more applicable to system designers at the slight expense of accuracy. Because the goal of this application report is to aid designers by investigating general trends between PCB layout and thermal performance across multiple packages, the creation of a functional test setup is prioritized.

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3 Test Results and Discussion

Figure 3-1 shows the maximum ambient temperature versus power dissipation for the TPS745 (WSON package) in the 1S0P Approximation layout. The slope of the trendline indicates a θ_{JA} of 169.2 C/W. The range and linearity of the data collected support the expected relationship between the power dissipation of the LDO and the maximum operating ambient temperature described by Equation 2.

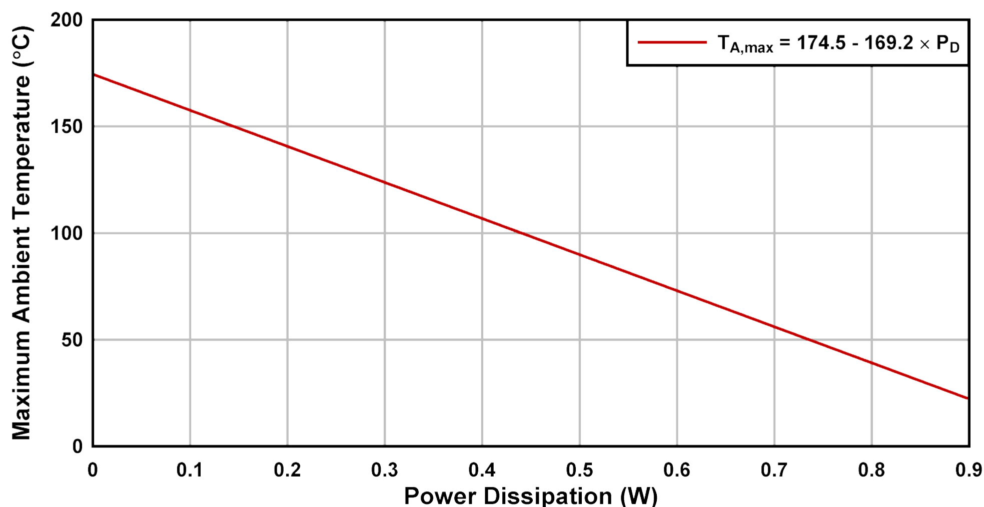

Figure 3-1. TPS745 (WSON) 1S0P Approximation Layout Test Results

See Appendix B for similar data is collected for all packages and layouts. Figure 3-2 and Figure 3-3 provide the resulting θ_{JA} values for the TPS745 (WSON) and TPS7B82-Q1 (TO-252). These packages display similar trends in thermal performance across all five layouts. The Internally Disconnected layout reduces θ_{JA} by almost 50% despite only having a connected copper area of 0.07-in^2, showing that including copper on the internal layers can significantly improve thermal performance, even if this copper is not directly connected to the LDO. The remaining layouts with increasing copper and thermal vias content show further, smaller reductions of θ_{JA} until the maximum reduction is reached at slightly larger than 70%. Based on the data collected, a thermally efficient layout is crucial for the WSON and TO-252 packages. If the layout is inefficient, θ_{JA} is significantly larger than the datasheet specified value, resulting in more complex thermal performance calculations, a reduced maximum operating ambient temperature, and potentially degraded device longevity and reliability.

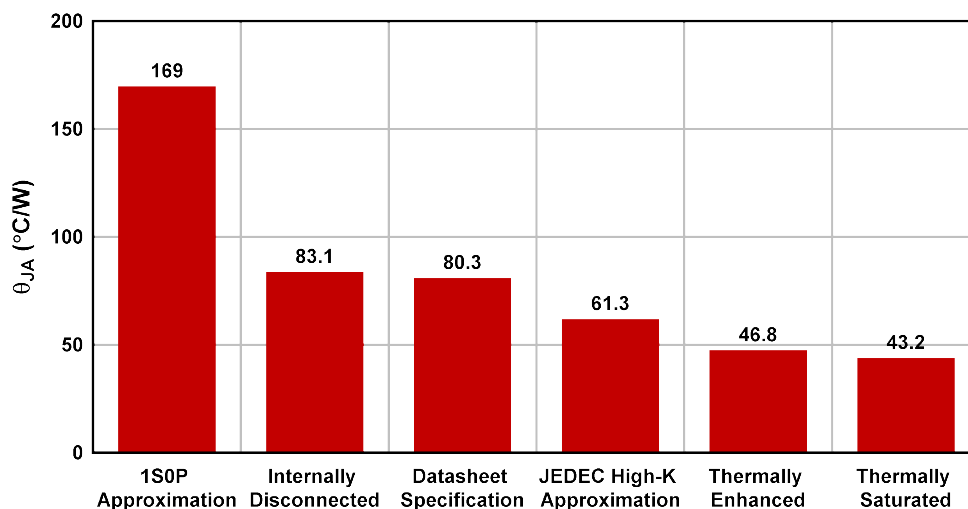

Figure 3-2. TPS745 (WSON) θ_{JA} vs. Board Layout

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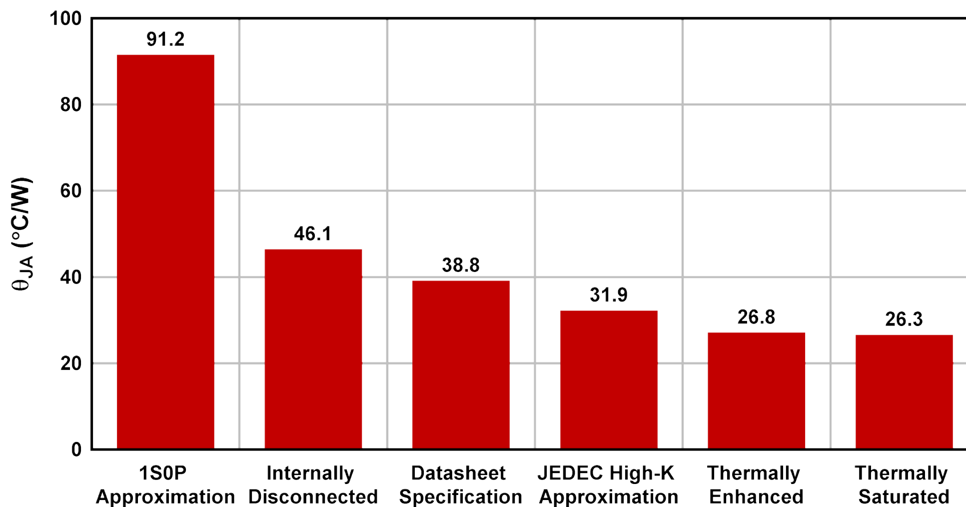

Figure 3-3. TPS7B82-Q1 (TO-252) θ_{JA} vs. Board Layout

Figure 3-4 shows the measured θ_{JA} values for the TLV755P (SOT-23). The difference in the θ_{JA} trend for the SOT-23 package is due to the lack of a thermal pad. The JEDEC standard does not permit the addition of thermal vias on the High-K Thermal Test Board for packages without thermal pads. A small amount of heat is able to dissipate to the internal and bottom layers, resulting in very similar performance between the 1S0P Approximation and the thermal model of the JEDEC High-K Test Board from which the datasheet specification is derived. To prevent identical performance across multiple different layouts, one thermal via is included underneath the device on the Internally Disconnected layout to connect the top layer ground trace to the bottom ground plane. In comparison, the JEDEC High-K Approximation layout has similar performance with two vias connecting the top ground trace to the internal layers. Adding one more via does not provide enough heat transferring capability to warrant much improvement in θ_{JA} despite the additional copper present in the JEDEC High-K Approximation layout.

The Thermally Enhanced and Thermally Saturated boards displayed about a 33% reduction to θ_{JA} compared to the JEDEC High-K Approximation board, significantly larger than the same comparison for the TPS745 and TPS7B82-Q1. This is explained by the lack of a thermal pad in the SOT-23 package. The Thermally Enhanced and Thermally Saturated layouts are the only layouts that include copper planes on the top layer. The lack of a thermal pad in this package results in the majority of heat dissipating on the top layer. As such, the inclusion of top layer copper is much more effective. Furthermore, the additional thermal vias included in the Thermally Enhanced and Thermally Saturated packages are the only path for heat to spread to the internal and bottom layers. In contrast, the TPS745 and TPS7B82-Q1 layouts include thermal vias directly under the thermal pad, reducing the effectiveness of additional thermal vias.

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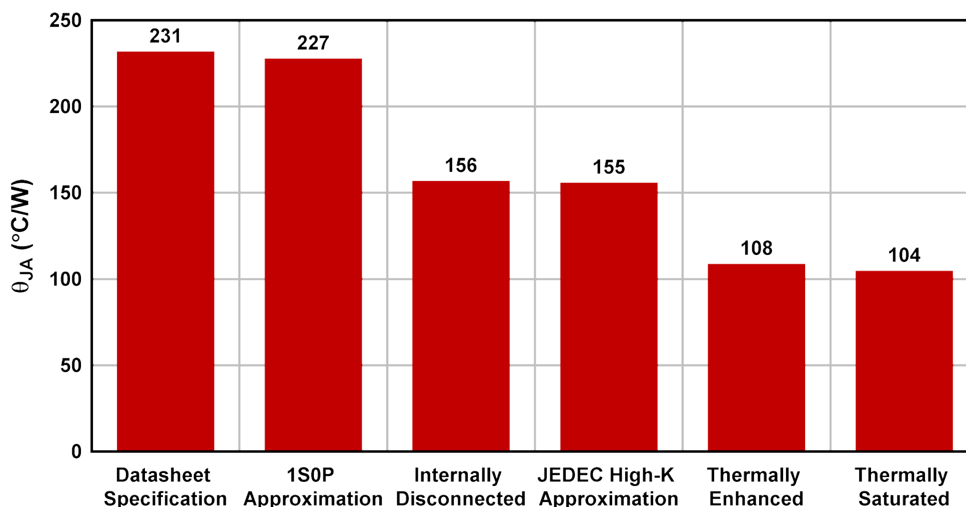

Figure 3-4. TLV755P (SOT-23) θ_{JA} vs. Board Layout

Figure 3-5 compares the effectiveness of PCB layout versus the package type. The effectiveness is calculated as a percentage reduction of θ_{JA}. As calculated with Equation 3, a thermally efficient layout is capable of reducing the θ_{JA} specified in the datasheet by between 32% and 55% depending on the package. The datasheet specified θ_{JA} can be used to provide a conservative estimate of the rise in junction temperature of the LDO. However, referring to Equation 2, the empirical rise in junction temperature can be reduced by 32% to 55% with a thermally efficient layout. Accounting for this improvement allows for a higher operating ambient temperature, a higher level of power dissipation, or some combination of the two. A comparison to the 1S0P Approximation layout using Equation 4 illustrates the importance of a thermally efficient layout. Compared to this worst-case layout, a thermally efficient layout provides a measured θ_{JA} that is up to four times smaller.

$$\text{Reduction of } \theta_{JA} \text{ compared to Datasheet Specification} = \left(1 - \frac{\theta_{JA,saturated}}{\theta_{JA,datasheet}}\right) \times 100 \tag{3}$$

$$\text{Reduction of } \theta_{JA} \text{ compared to 1S0P Approximation} = \left(1 - \frac{\theta_{JA,saturated}}{\theta_{JA,1S0P}}\right) \times 100 \tag{4}$$

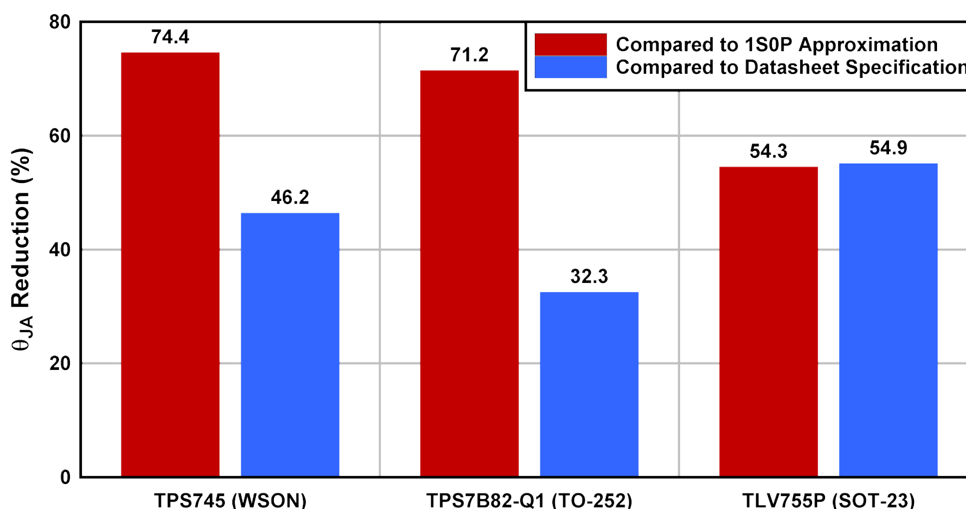

Figure 3-5. θ_{JA} Reduction for Each Device

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Figure 3-6 normalizes the results from the Figure 3-2, Figure 3-3, and Figure 3-4 relative to the datasheet specification using Equation 5.

$$\theta_{JA,normalized} = \frac{\theta_{JA,measured}}{\theta_{JA,datasheet}} \tag{5}$$

This figure condenses the data collected across the three packages to illustrate the important findings of this study. Firstly, there is an inverse relationship between PCB copper content and θ_{JA} that saturates as the copper content increases. This relationship is observable regardless of package. As shown by the significant drop between the 1S0P Approximation and Internally Disconnected layouts, the copper content does not need to be connected to the LDO to improve thermal performance. Additional thermal vias around the device also improve thermal performance by providing more paths for the heat generated by the LDO to dissipate to the internal and bottom layers. These vias are especially important for packages like the SOT-23 that do not have a dedicated thermal pad. However, as shown by the minimal improvement between the Thermally Enhanced and Thermally Saturated layouts, the improvement in θ_{JA} from the additional thermal vias saturates.

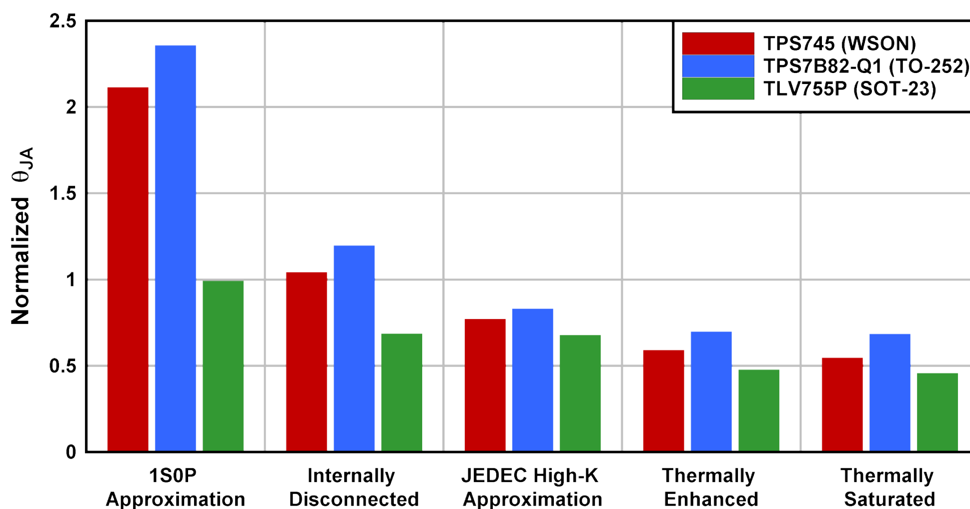

Figure 3-6. Normalized θ_{JA} for Each Device vs. Board Layout

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4 Conclusion

The thermal performance of the LDO in terms of its junction-to-ambient thermal resistance, θ_{JA}, is highly dependent on the PCB design. However, the impact of the PCB is ultimately limited by the package of the LDO. Packages with thermal pads, like the WSON and TO-252 packages, are more thermally dissipative and, therefore, see a larger overall reduction in θ_{JA} at 74% and 71% respectively when compared to the worst-case 1S0P approximation layout. The SOT-23 package sees a smaller, but still significant, reduction at 54%. Figure 3-5 illustrates that θ_{JA} can be reduced between 32% and 55% with a thermally optimized layout compared to the data sheet specifications. This result indicates that using the datasheet specified θ_{JA} for thermal calculations provides a conservative estimate of thermal performance. However, a designer must keep in mind that a thermally efficient layout allows for a higher operating ambient temperature, a higher level of power dissipation, or some combination of these two advantages.

Figure 3-6 shows that regardless of package type, thermal performance saturates as copper content in the PCB increases. For all three packages, The Thermally Enhanced layout contained about half the copper area of the Thermally Saturated layout, but provided a θ_{JA} within 8%. Similarly, the improvement in thermal performance due to additional thermal vias also saturates. Stitching additional vias through the PCB yields little benefit as seen from the Thermally Saturated layouts. A design with sufficient thermal performance can be achieved with a layout similar to the Thermally Enhanced board. For more compact designs, see Figure 3-4, which show the results from the TLV755P (SOT-23) measurements. These results indicate that copper must be maximized on the top and bottom layers as these layers are not surrounded by additional PCB material and are therefore the most effective for heat dissipation. Additional thermal vias only need to be included around the device to effectively spread the heat generated by the LDO to other copper layers. These vias are especially critical when designing with packages that do not have a thermal pad, like the SOT-23 package. In these cases, thermal vias can also be placed directly under the device where the most heat is generated. Packages with thermal pads maximize the amount of thermal vias in the landing pad according to https://www.jedec.org/system/files/docs/JESD51-9.pdf. Lastly, data from all Internally Disconnected layouts Figure 3-6 show that additional copper on internal layers must be included if possible and have a positive impact on thermal performance, even if not directly connected to the LDO.

5 Future Study

There are a couple of areas that can be addressed in a future study. The first is to investigate these or similar layouts' effect on ultra small (less than 1 mm^2) packages like the DSBGA and X2SON that traditionally have poor thermal performance. Due to poor heat dissipative capability inherent to small packages, the PCB layout can have a reduced effect on the thermal performance compared to the WSON, TO-252, and SOT-23 packages. Another more complex extension of this study can develop an equation or Figure of Merit (FOM) that incorporates connected copper area, disconnected copper area, the location of these areas relative to the board stack up, number of thermal vias, and so forth. This FOM, which would correlate to an equivalent thermal impedance of the board, can be applied to provide a more targeted value for the expected θ_{JA} of a given layout.

6 References

1. *LDOs thermal performance in small SMD packages application report*
2. *AN-1520 a guide to board layout for best thermal resistance for exposed packages application report*
3. *Semiconductor and IC package thermal metrics*
4. *Low effective thermal conductivity test board for leaded surface mount packages*
5. *High effective thermal conductivity test board for leaded surface mount packages*
6. *Test boards for area array surface mount package thermal measurements*
7. *Measuring the thermal impedance of LDOs in Situ application report*

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7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2019) to Revision A (Septemeber 2025)	**Page**
• Updated the numbering format for tables, figures, and cross-references throughout the document.................	2

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A Thermal Test Board Layouts

A.1 TPS745 (WSON) Drawings

A.1.1 1S0P Approximation Layout Drawings

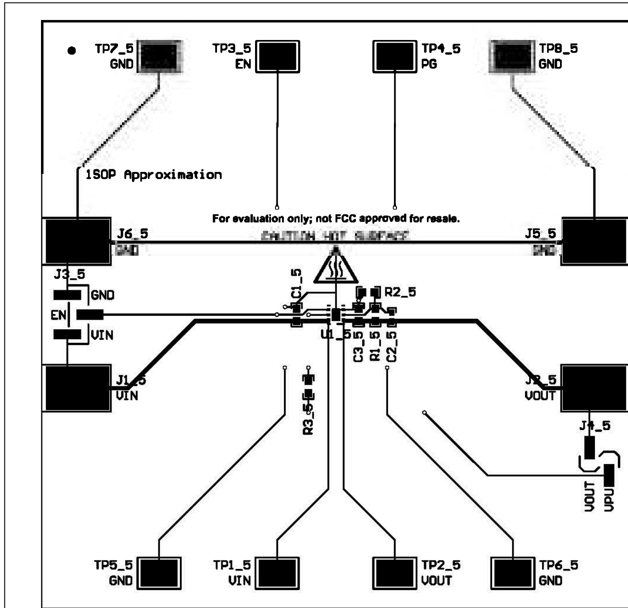

Figure A-1. TPS745 (WSON) 1S0P Approximation Top Layer

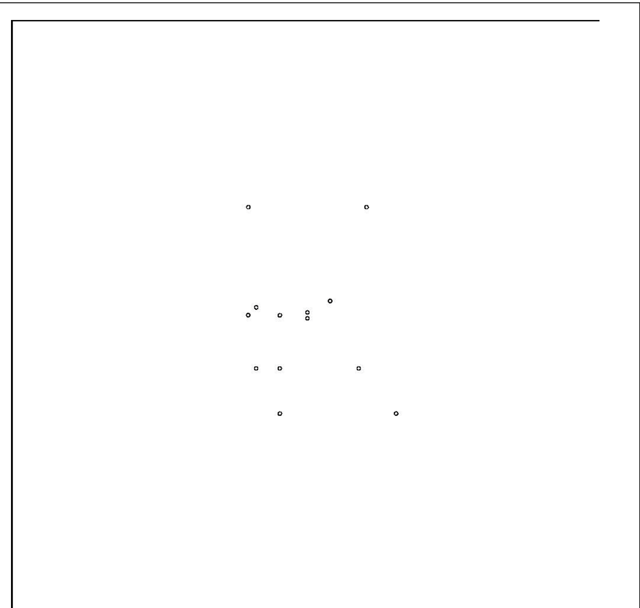

Figure A-2. TPS745 (WSON) 1S0P Approximation Internal Layer 1

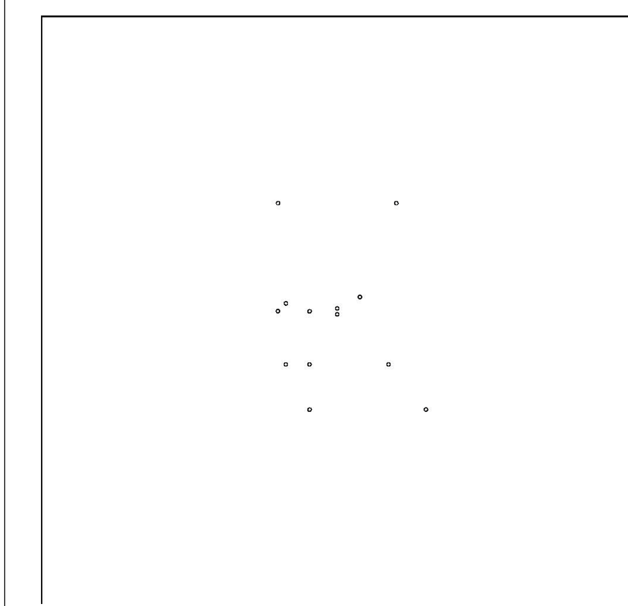

Figure A-3. TPS745 (WSON) 1S0P Approximation Internal Layer 2

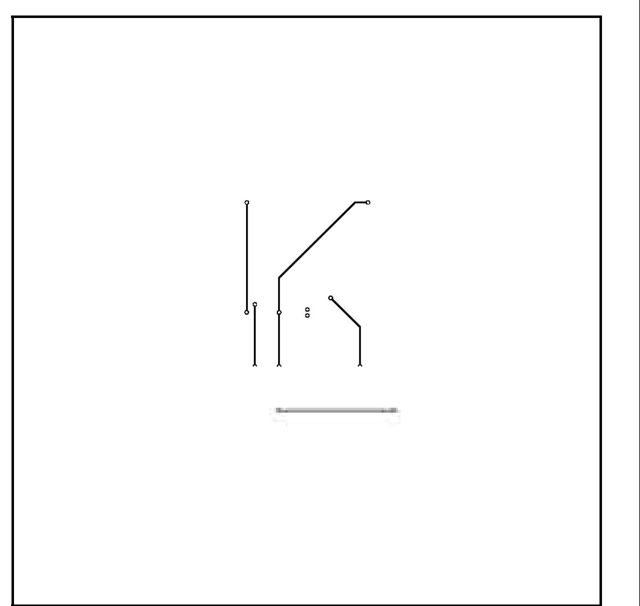

Figure A-4. TPS745 (WSON) 1S0P Approximation Bottom Layer

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A.1.2 Internally Disconnected Layout Drawings

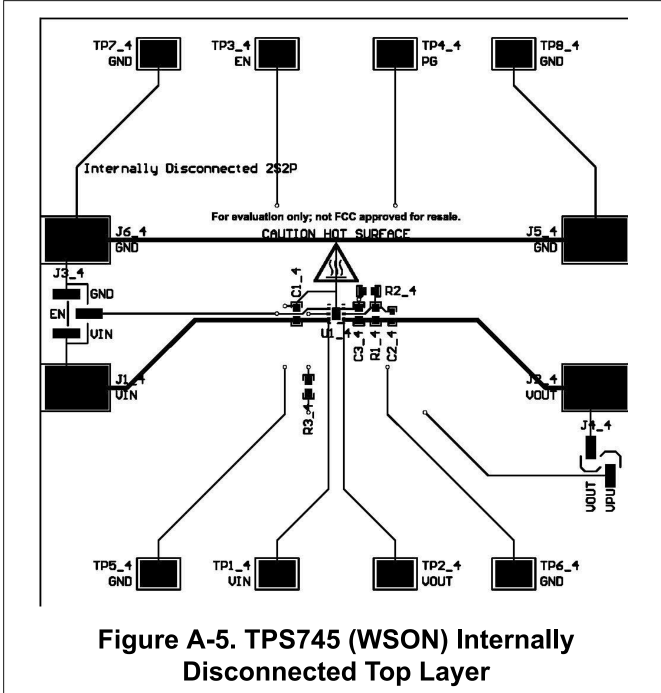

Figure A-5. TPS745 (WSON) Internally Disconnected Top Layer

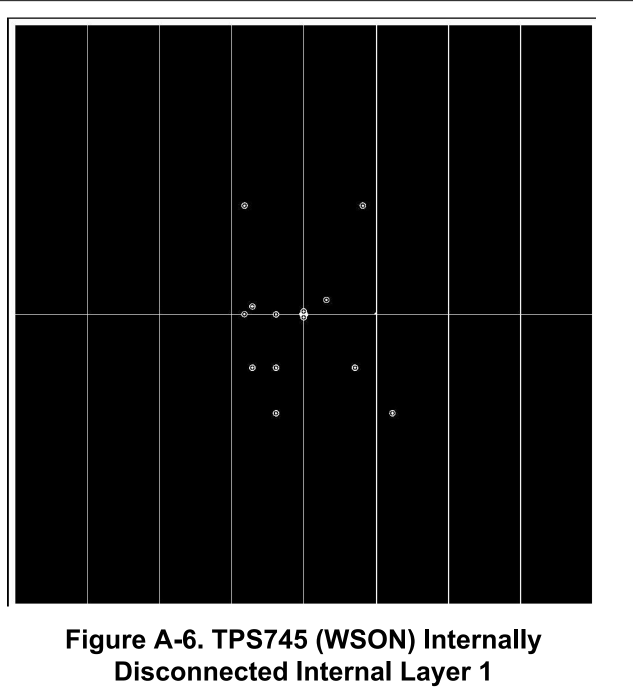

Figure A-6. TPS745 (WSON) Internally Disconnected Internal Layer 1

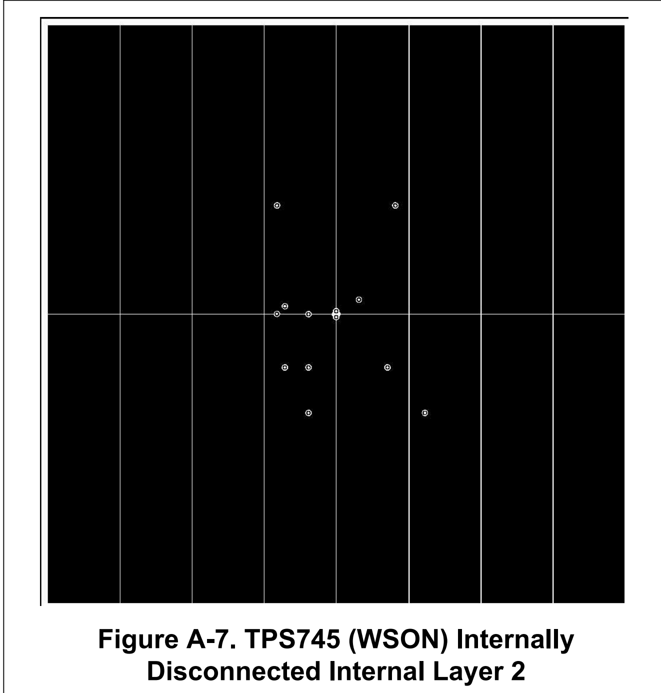

Figure A-7. TPS745 (WSON) Internally Disconnected Internal Layer 2

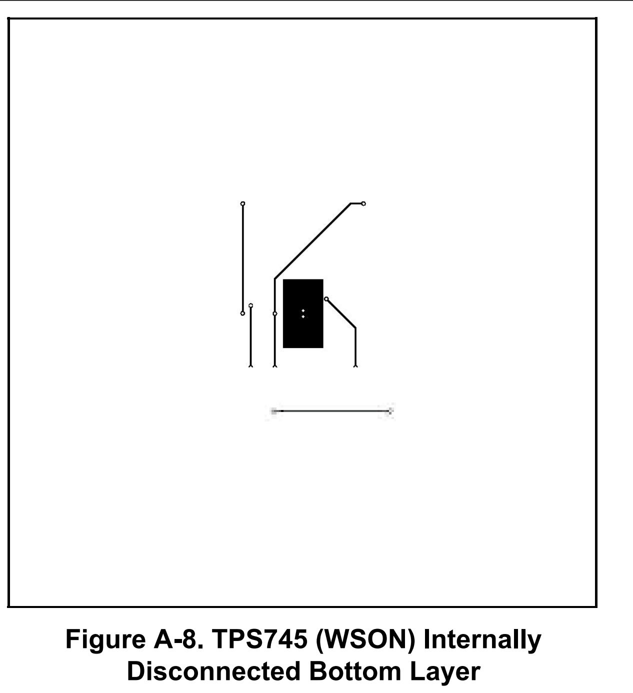

Figure A-8. TPS745 (WSON) Internally Disconnected Bottom Layer

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A.1.3 JEDEC High-K Approximation Layout Drawings

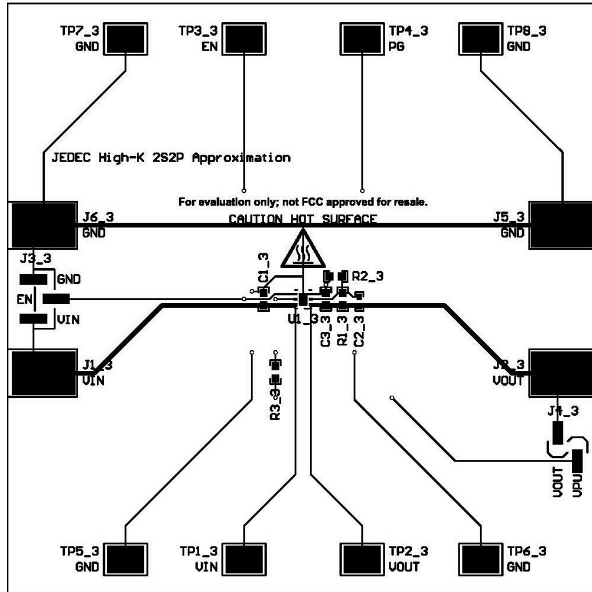

Figure A-9. TPS745 (WSON) JEDEC High-K Approximation Top Layer

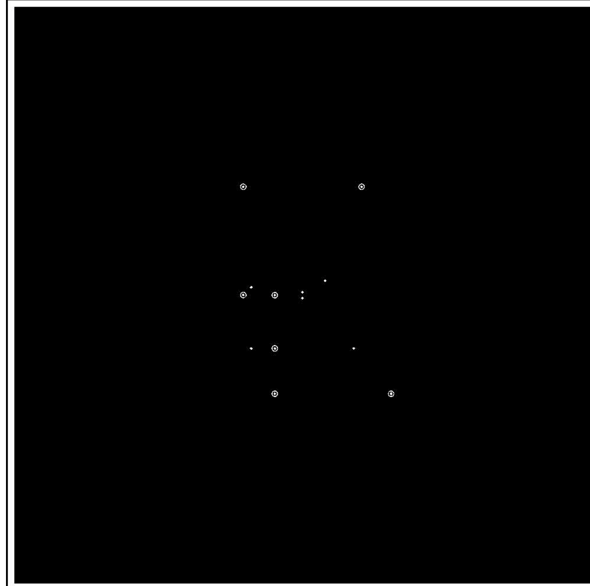

Figure A-10. TPS745 (WSON) JEDEC High-K Approximation Internal Layer 1

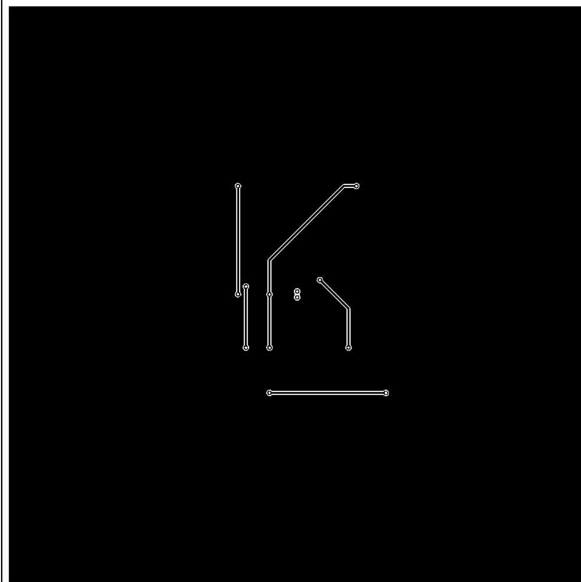

Figure A-11. TPS745 (WSON) JEDEC High-K Approximation Internal Layer 2

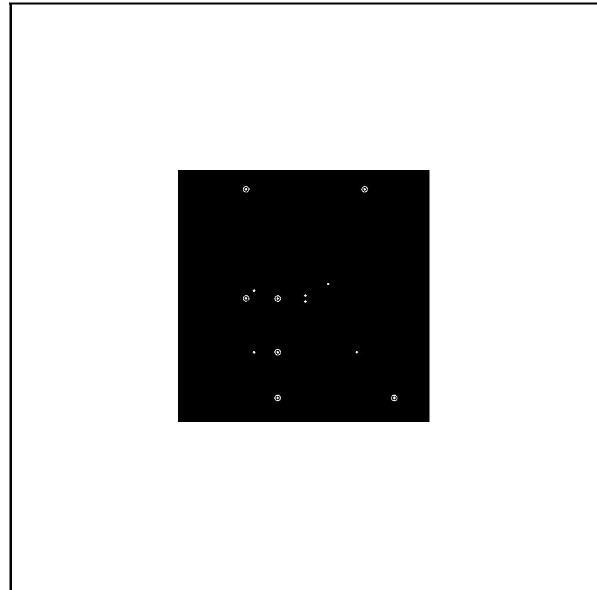

Figure A-12. TPS745 (WSON) JEDEC High-K Approximation Bottom Layer

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A.1.4 Thermally Enhanced Layout Drawings

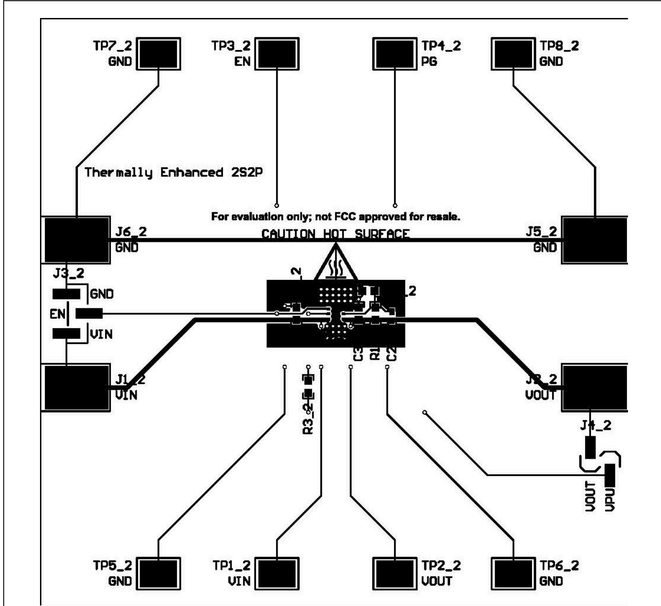

Figure A-13. TPS745 (WSON) Thermally Enhanced Top Layer

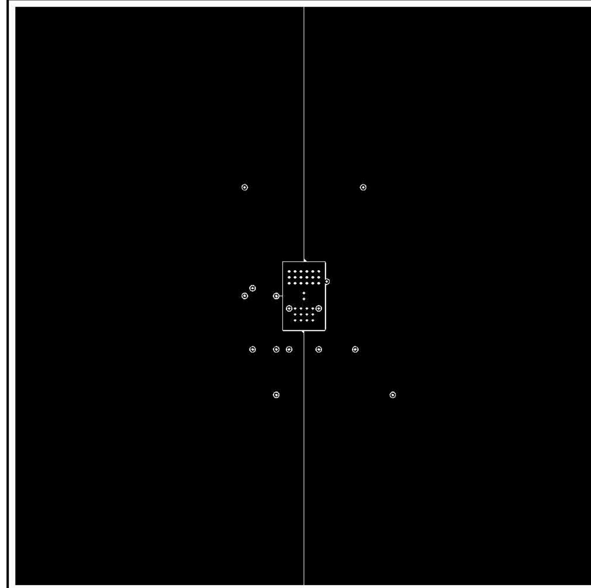

Figure A-14. TPS745 (WSON) Thermally Enhanced Internal Layer 1

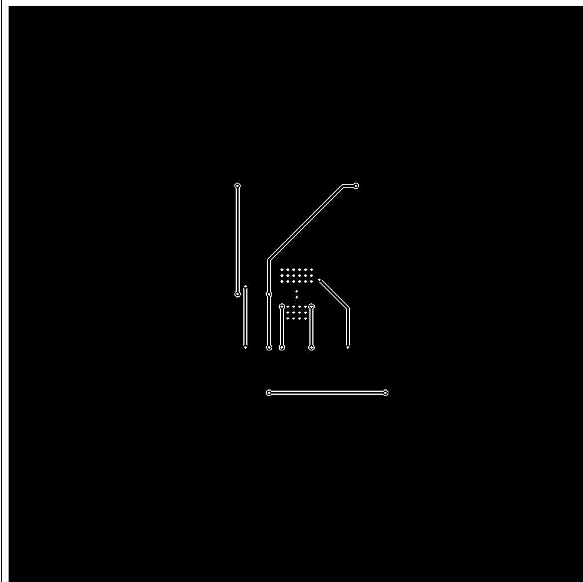

Figure A-15. TPS745 (WSON) Thermally Enhanced Internal Layer 2

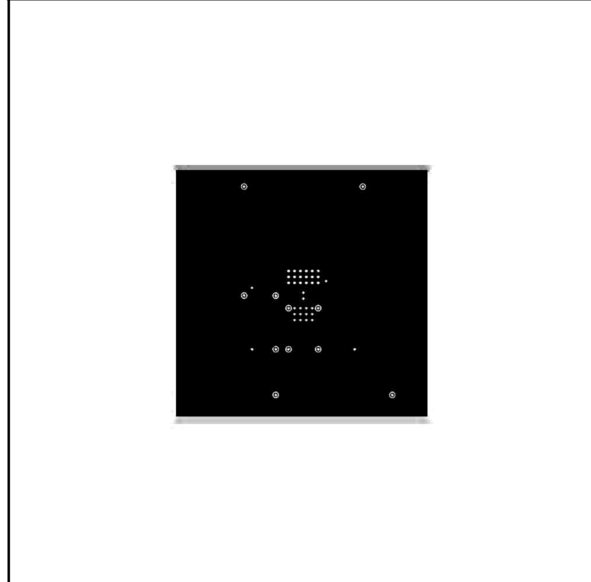

Figure A-16. TPS745 (WSON) Thermally Enhanced Bottom Layer

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A.1.5 Thermally Saturated Layout Drawings

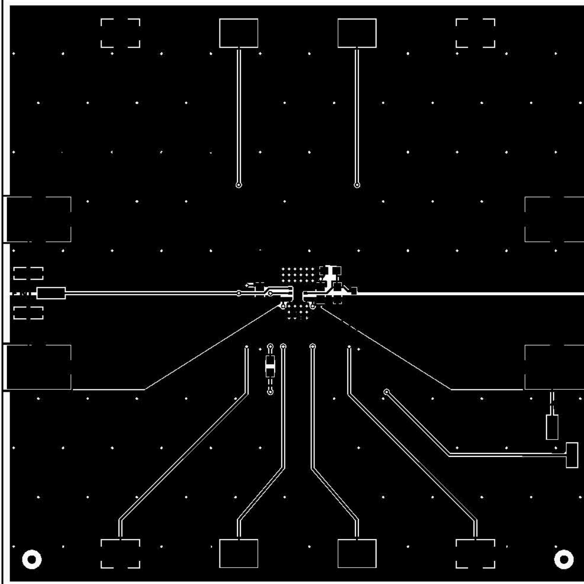

Figure A-17. TPS745 (WSON) Thermally Saturated Top Layer

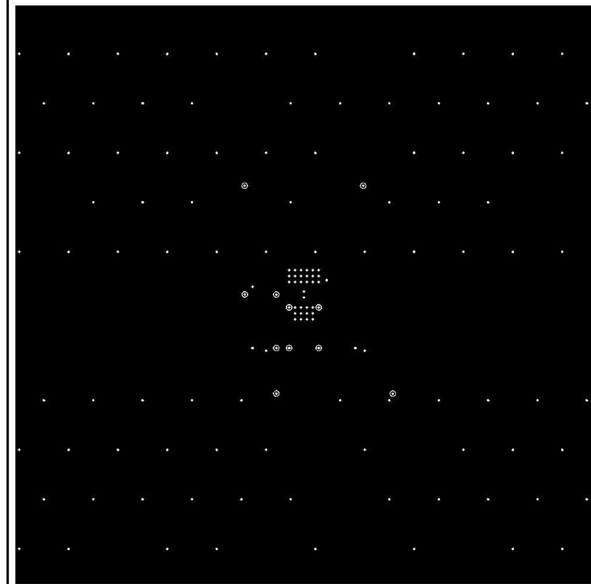

Figure A-18. TPS745 (WSON) Thermally Saturated Internal Layer 1

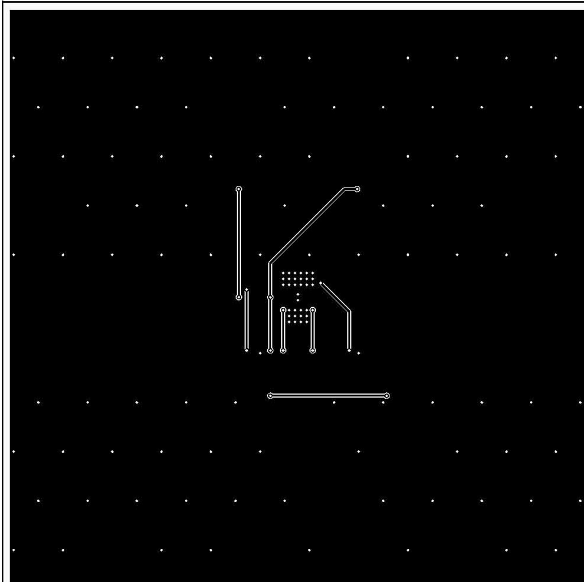

Figure A-19. TPS745 (WSON) Thermally Saturated Internal Layer 2

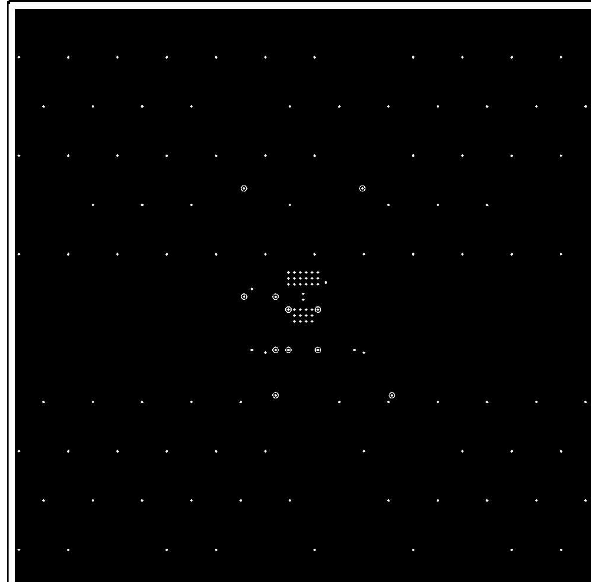

Figure A-20. TPS745 (WSON) Thermally Saturated Bottom Layer

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A.2 TPS7B82-Q1 (TO-252) Drawings

A.2.1 1S0P Approximation Layout Drawings

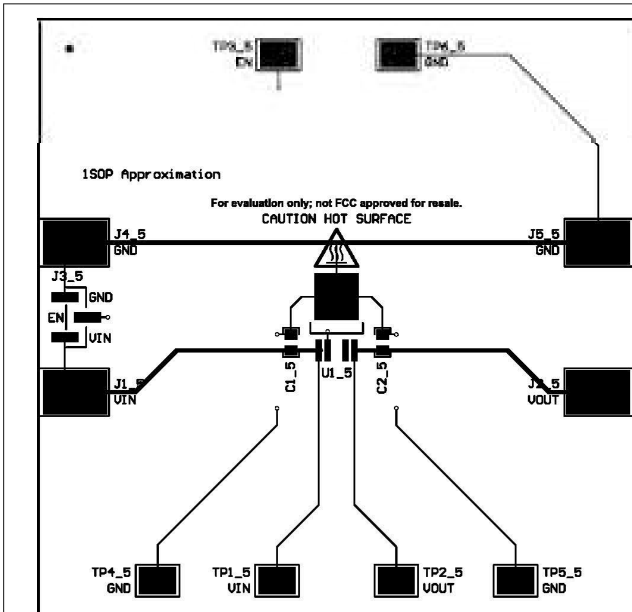

Figure A-21. TPS7B82-Q1 (TO-252) 1S0P Approximation Top Layer

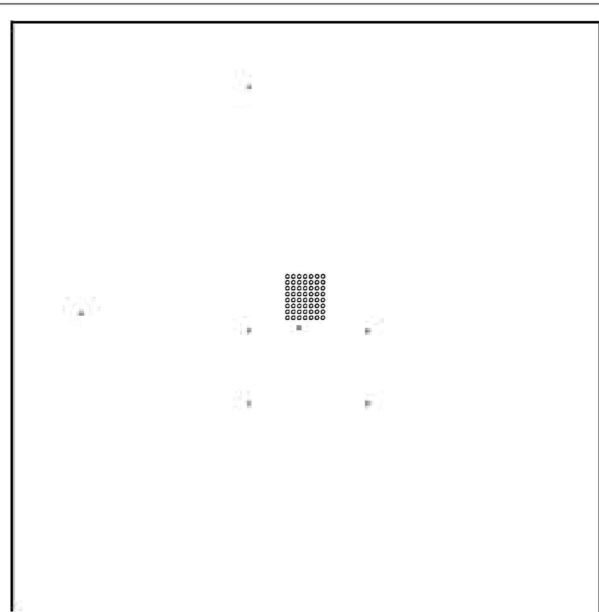

Figure A-22. TPS7B82-Q1 (TO-252) 1S0P Approximation Internal Layer 1

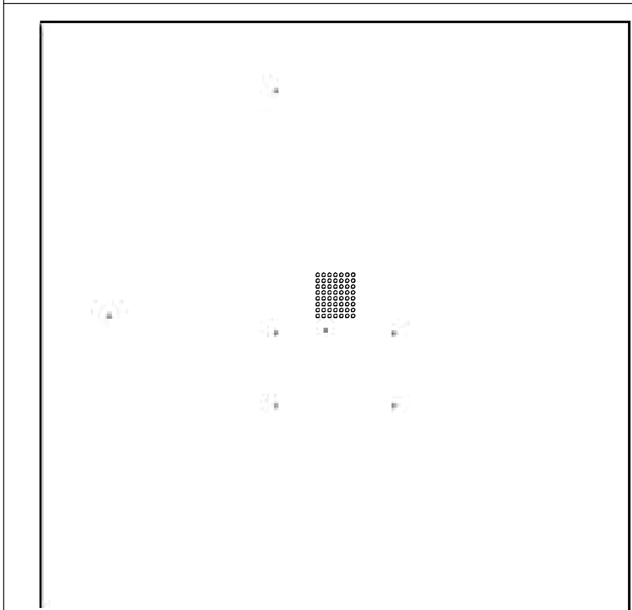

Figure A-23. TPS7B82-Q1 (TO-252) 1S0P Approximation Internal Layer 2

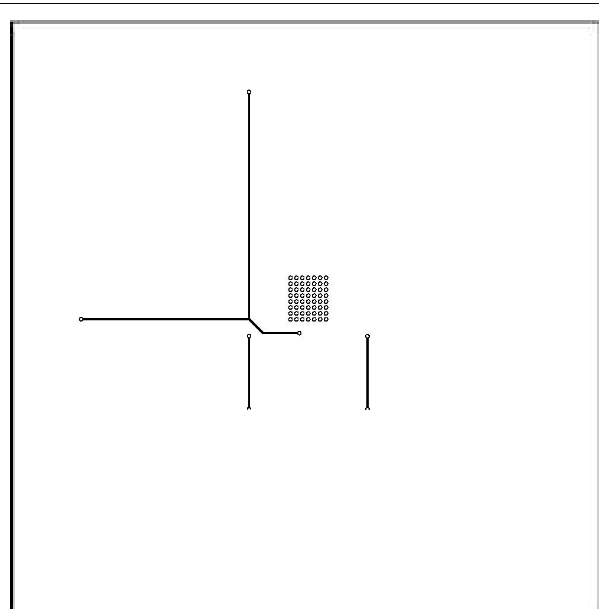

Figure A-24. TPS7B82-Q1 (TO-252) 1S0P Approximation Bottom Layer

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A.2.2 Internally Disconnected Layout Drawings

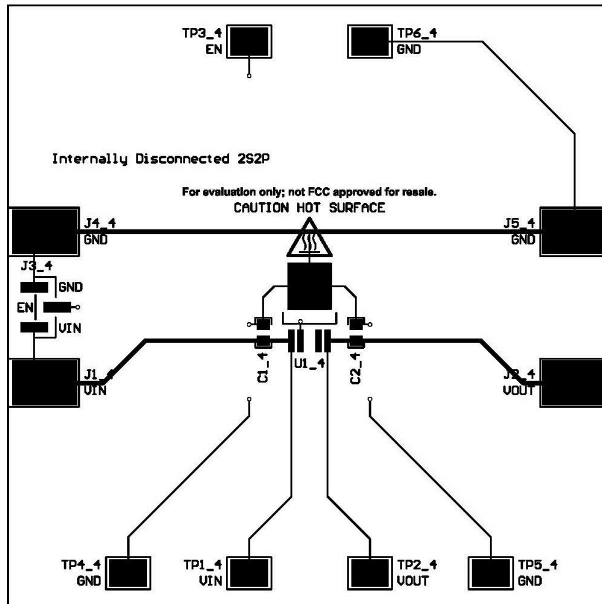

Figure A-25. TPS7B82-Q1 (TO-252) Internally Disconnected Top Layer

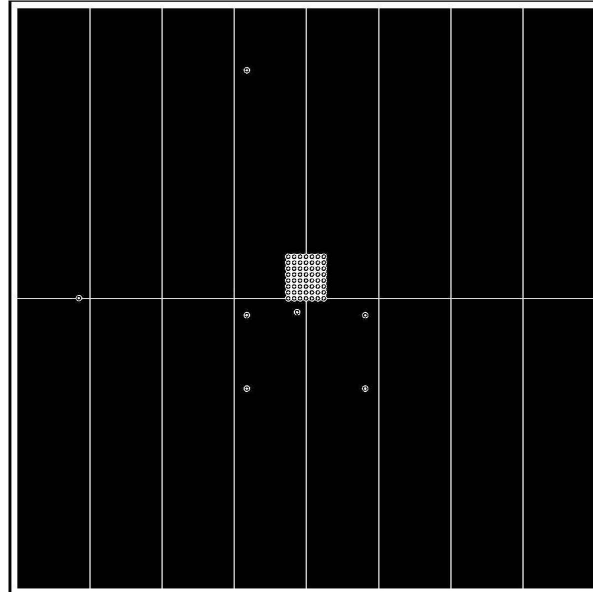

Figure A-26. TPS7B82-Q1 (TO-252) Internally Disconnected Internal Layer 1

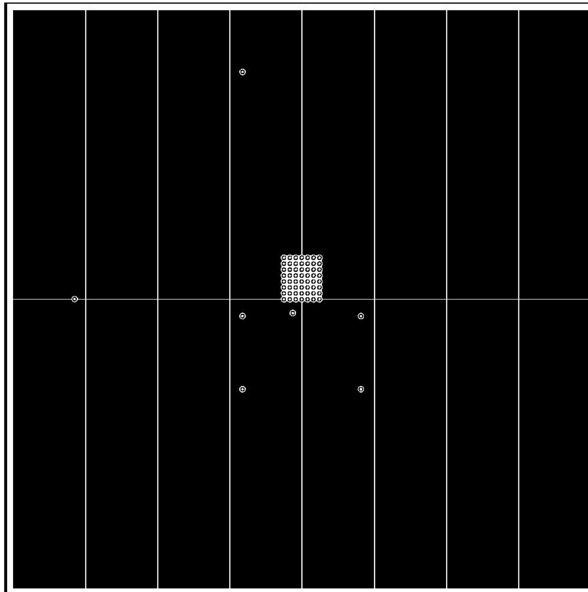

Figure A-27. TPS7B82-Q1 (TO-252) Internally Disconnected Internal Layer 2

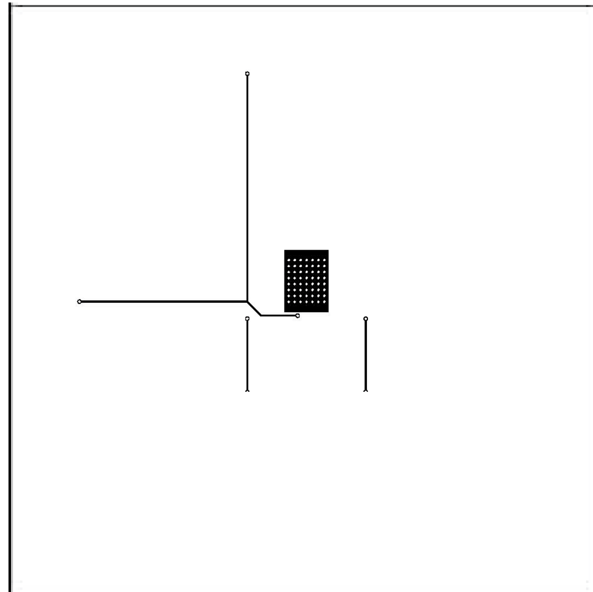

Figure A-28. TPS7B82-Q1 (TO-252) Internally Disconnected Bottom Layer

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A.2.3 JEDEC High-K Approximation Layout Drawings

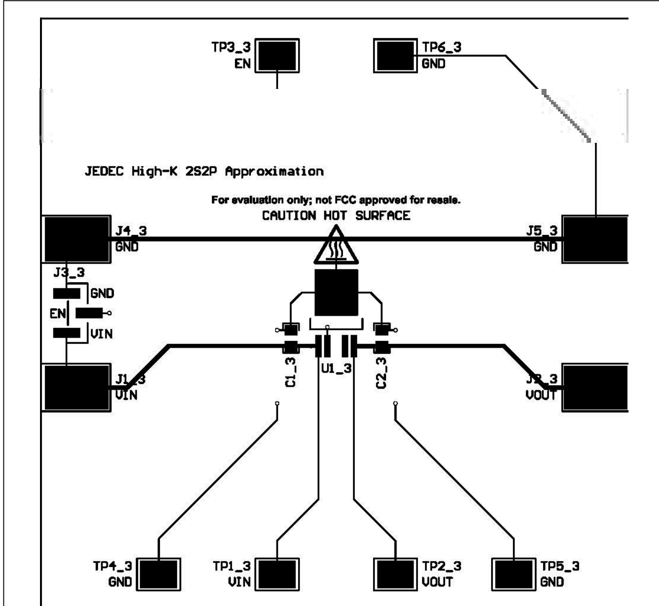

Figure A-29. TPS7B82-Q1 (TO-252) JEDEC High-K Approximation Top Layer

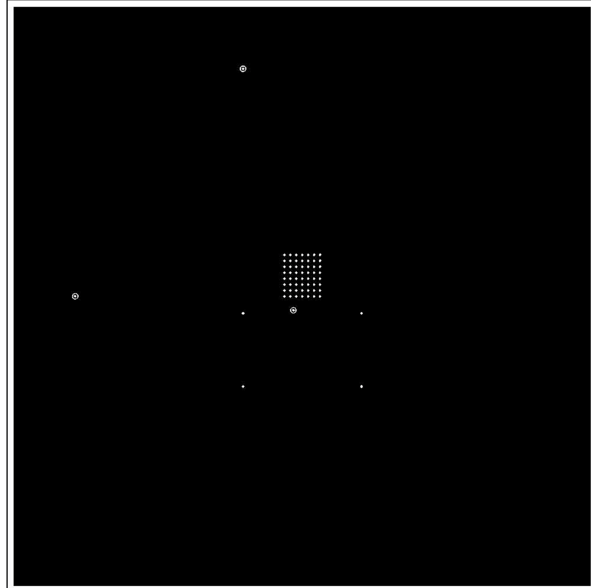

Figure A-30. TPS7B82-Q1 (TO-252) JEDEC High-K Approximation Internal Layer 1

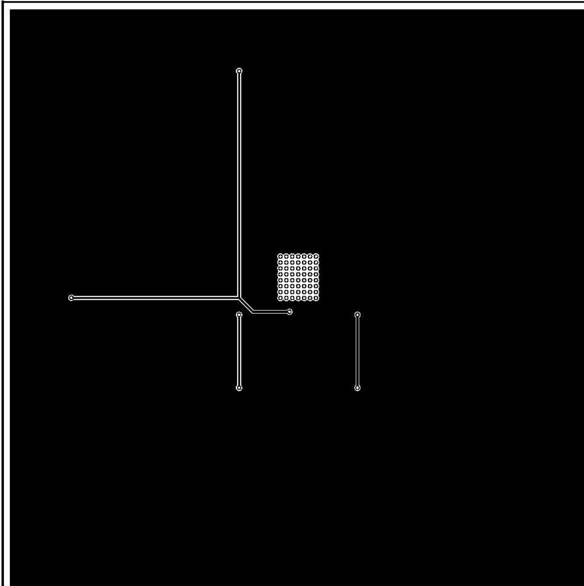

Figure A-31. TPS7B82-Q1 (TO-252) JEDEC High-K Approximation Internal Layer 2

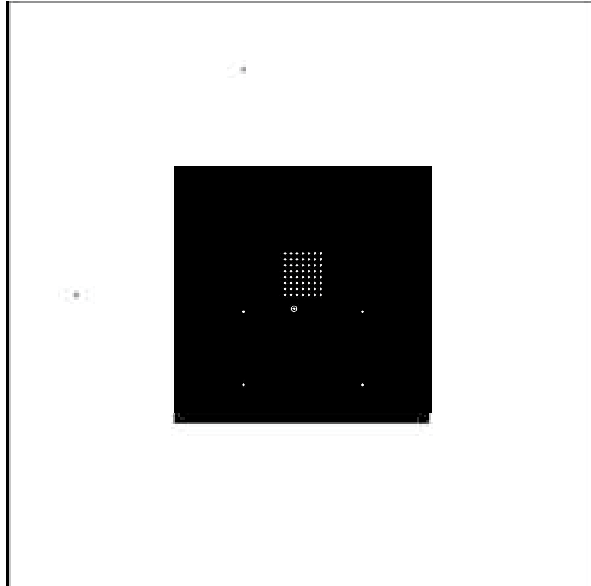

Figure A-32. TPS7B82-Q1 (TO-252) JEDEC High-K Approximation Bottom Layer

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A.2.4 Thermally Enhanced Layout Drawings

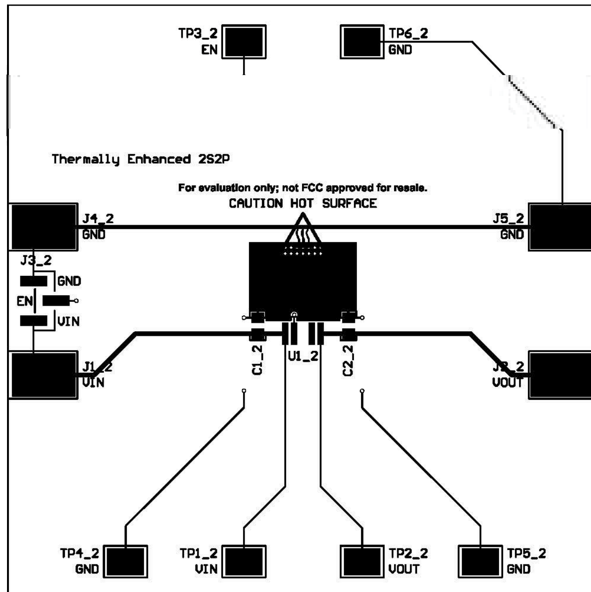

Figure A-33. TPS7B82-Q1 (TO-252) Thermally Enhanced Top Layer

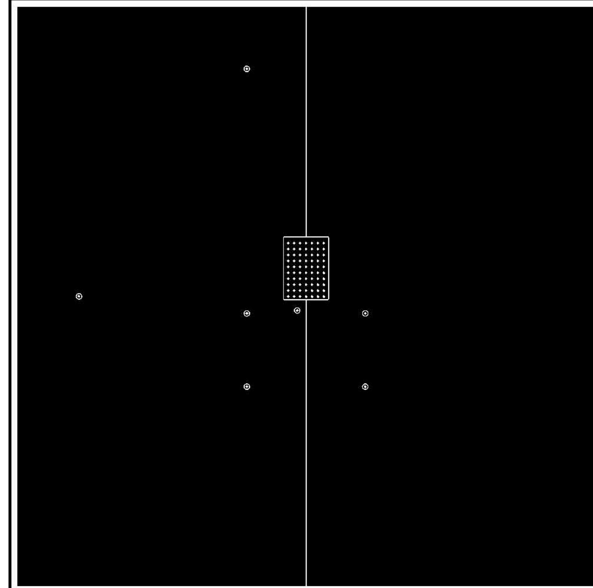

Figure A-34. TPS7B82-Q1 (TO-252) Thermally Enhanced Internal Layer 1

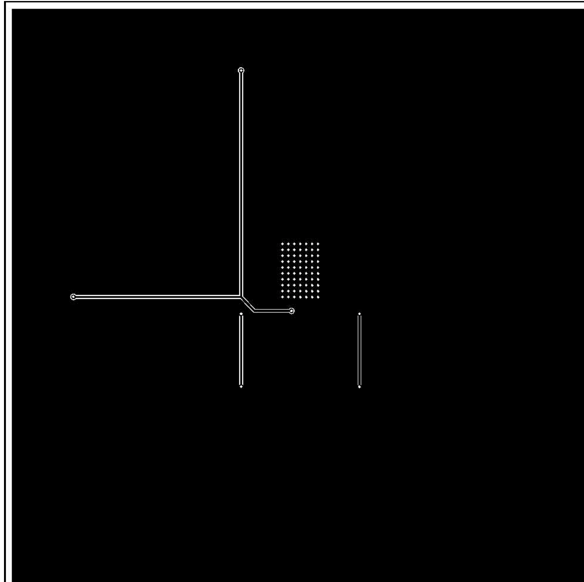

Figure A-35. TPS7B82-Q1 (TO-252) Thermally Enhanced Internal Layer 2

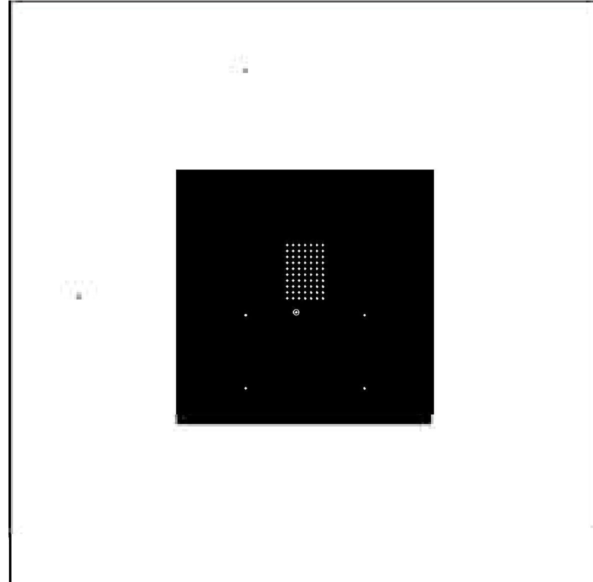

Figure A-36. TPS7B82-Q1 (TO-252) Thermally Enhanced Bottom Layer

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A.2.5 Thermally Saturated Layout Drawings

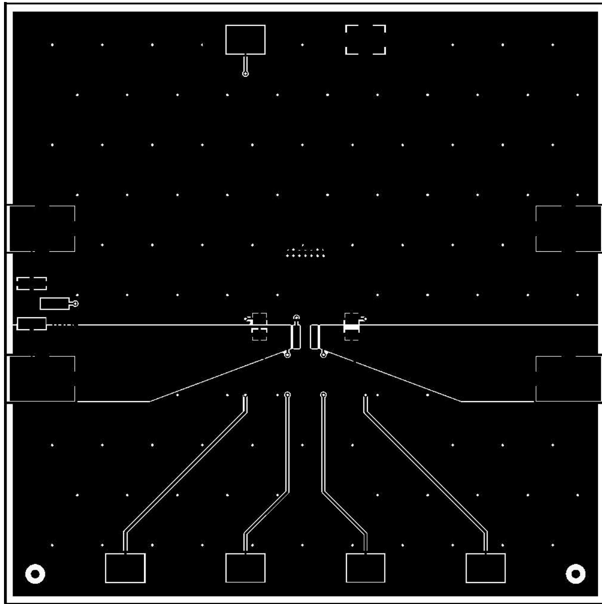

Figure A-37. TPS7B82-Q1 (TO-252) Thermally Saturated Top Layer

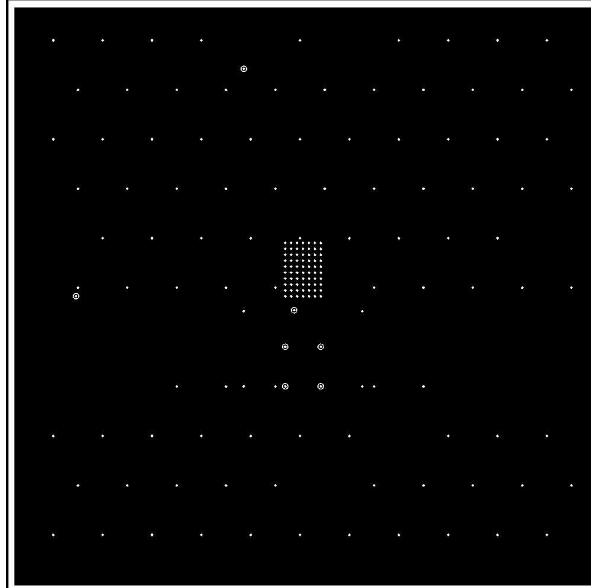

Figure A-38. TPS7B82-Q1 (TO-252) Thermally Saturated Internal Layer 1

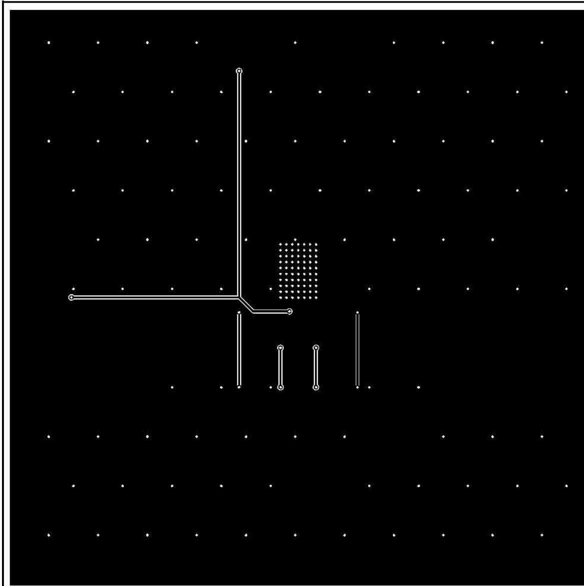

Figure A-39. TPS7B82-Q1 (TO-252) Thermally Saturated Internal Layer 2

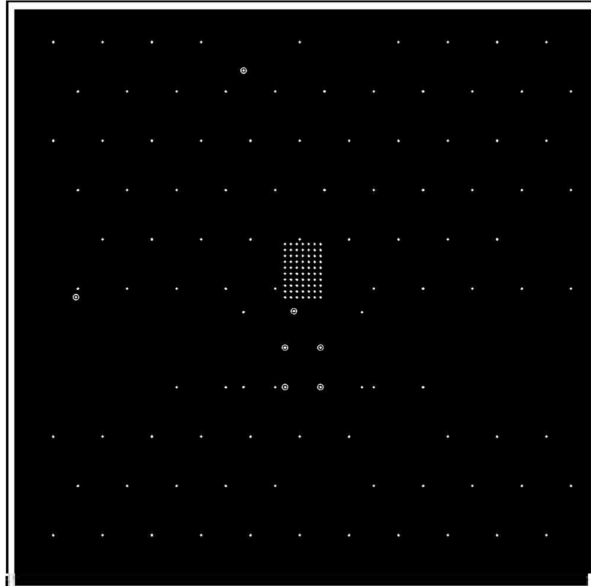

Figure A-40. TPS7B82-Q1 (TO-252) Thermally Saturated Bottom Layer

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A.3 TLV755P (SOT-23) Drawings

A.3.1 1S0P Approximation Layout Drawings

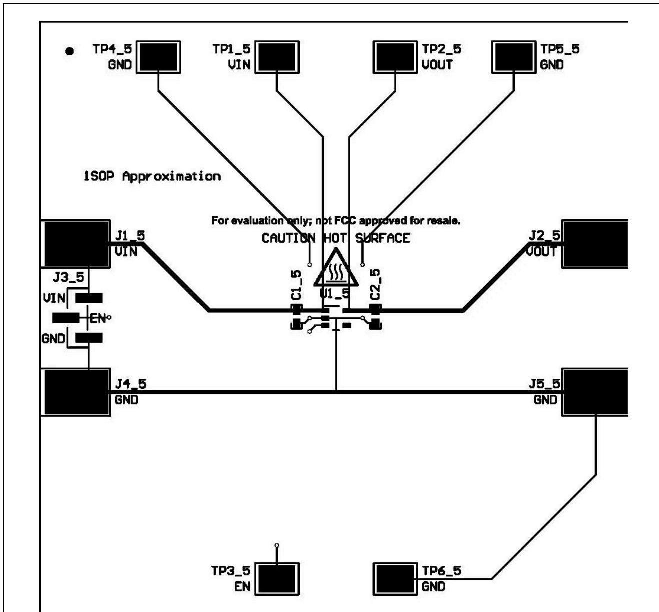

Figure A-41. TLV755P (SOT-23) 1S0P Approximation Top Layer

Figure A-42. TLV755P (SOT-23) 1S0P Approximation Internal Layer 1

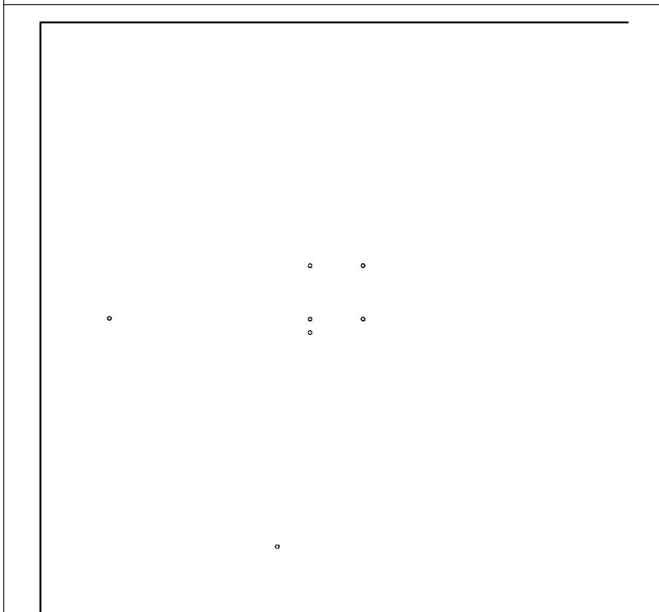

Figure A-43. TLV755P (SOT-23) 1S0P Approximation Internal Layer 2

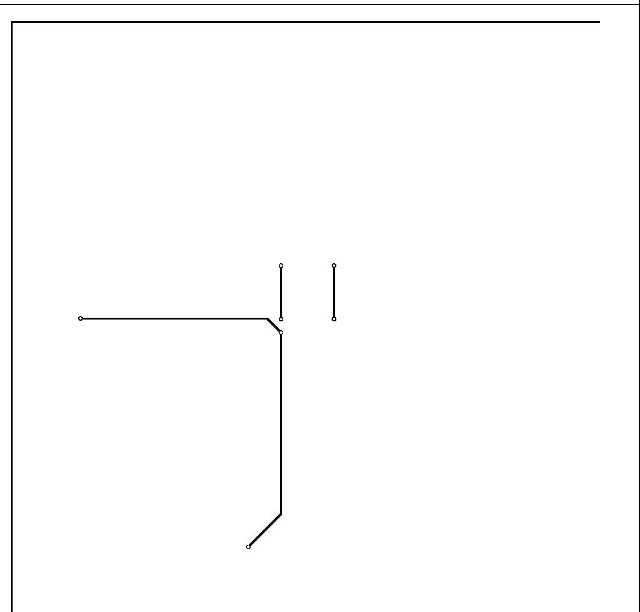

Figure A-44. TLV755P (SOT-23) 1S0P Approximation Bottom Layer

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A.3.2 Internally Disconnected Layout Drawings

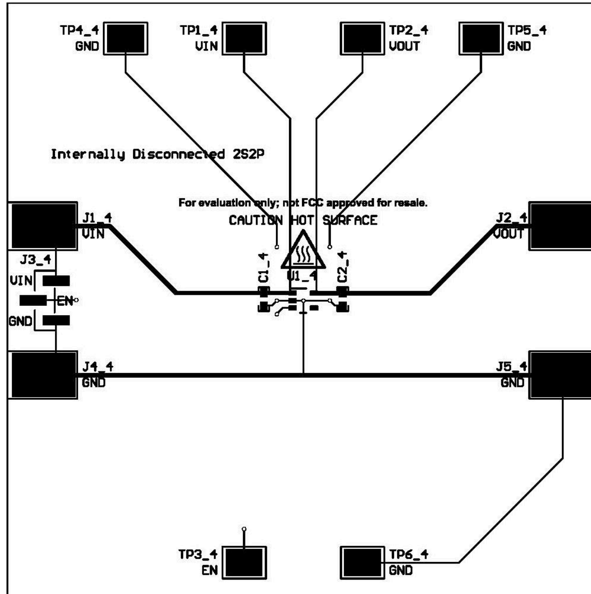

Figure A-45. TLV755P (SOT-23) Internally Disconnected Top Layer

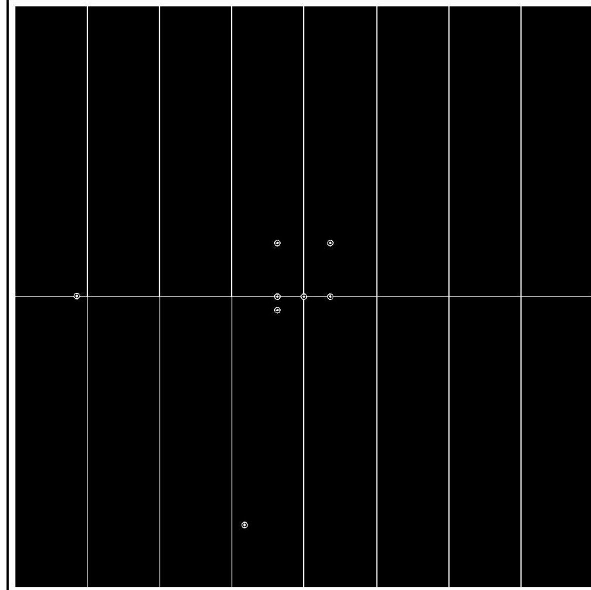

Figure A-46. TLV755P (SOT-23) Internally Disconnected Internal Layer 1

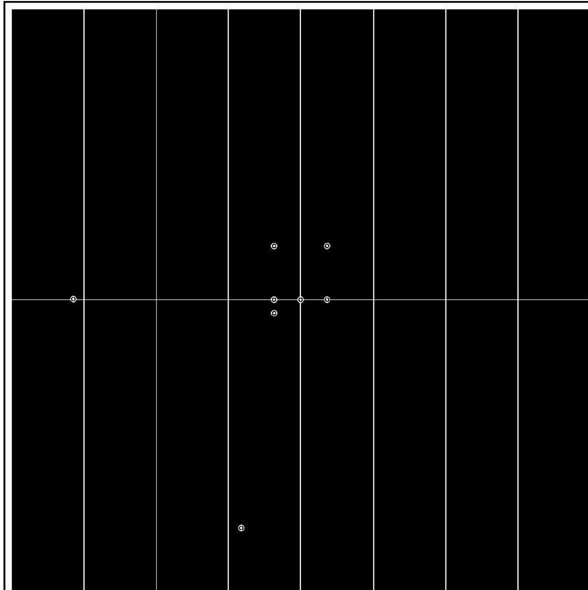

Figure A-47. TLV755P (SOT-23) Internally Disconnected Internal Layer 2

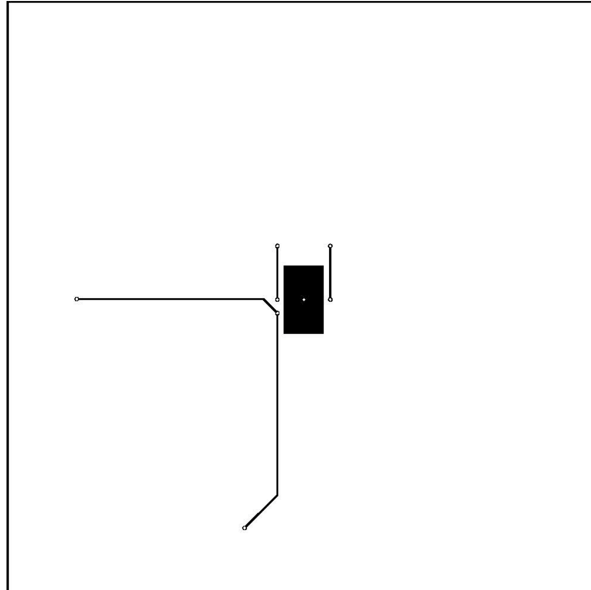

Figure A-48. TLV755P (SOT-23) Internally Disconnected Bottom Layer

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A.3.3 JEDEC High-K Approximation Layout Drawings

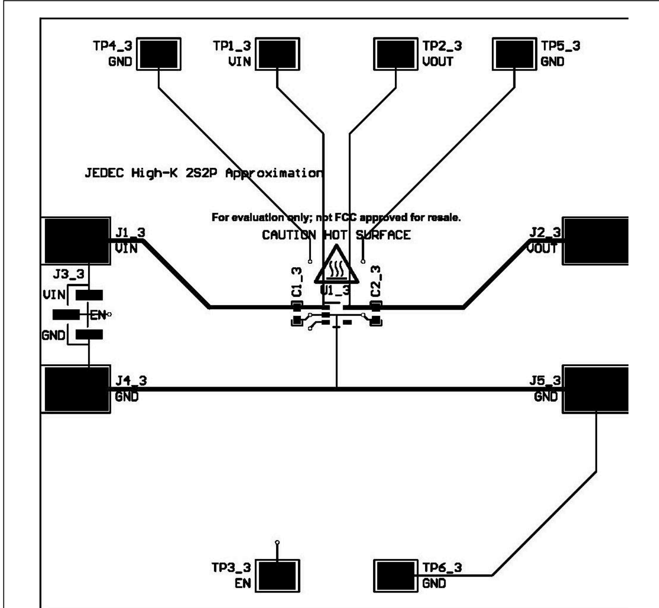

Figure A-49. TLV755P (SOT-23) JEDEC High-K Approximation Top Layer

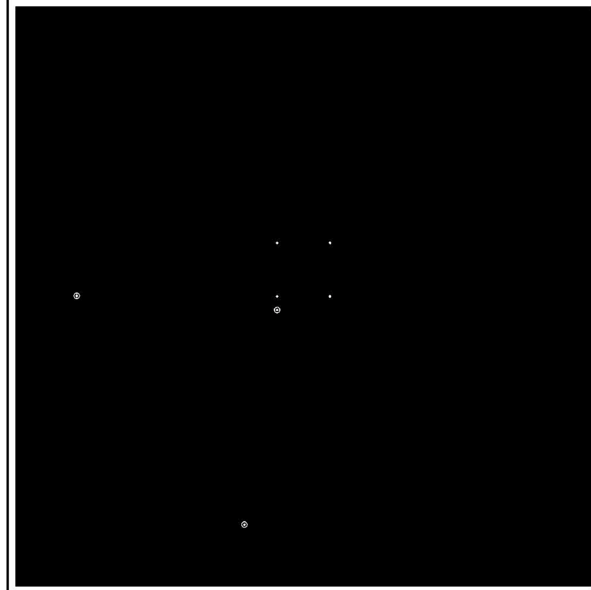

Figure A-50. TLV755P (SOT-23) JEDEC High-K Approximation Internal Layer 1

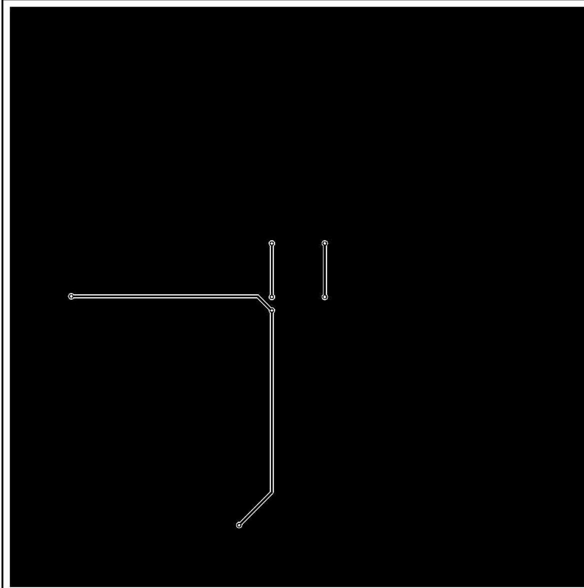

Figure A-51. TLV755P (SOT-23) JEDEC High-K Approximation Internal Layer 2

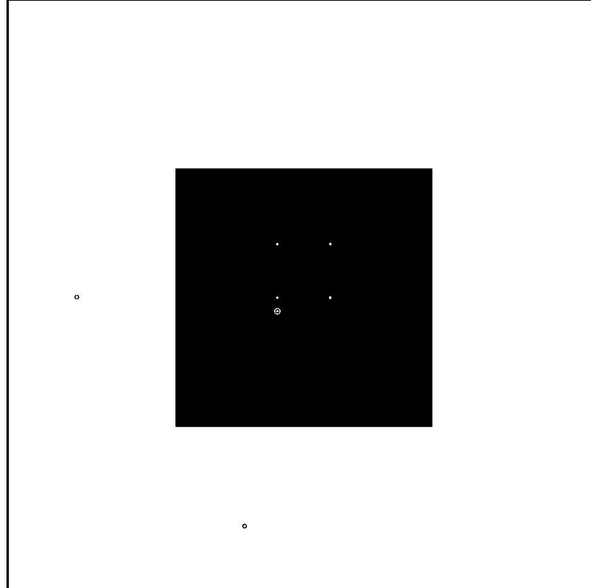

Figure A-52. TLV755P (SOT-23) JEDEC High-K Approximation Bottom Layer

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A.3.4 Thermally Enhanced Drawings

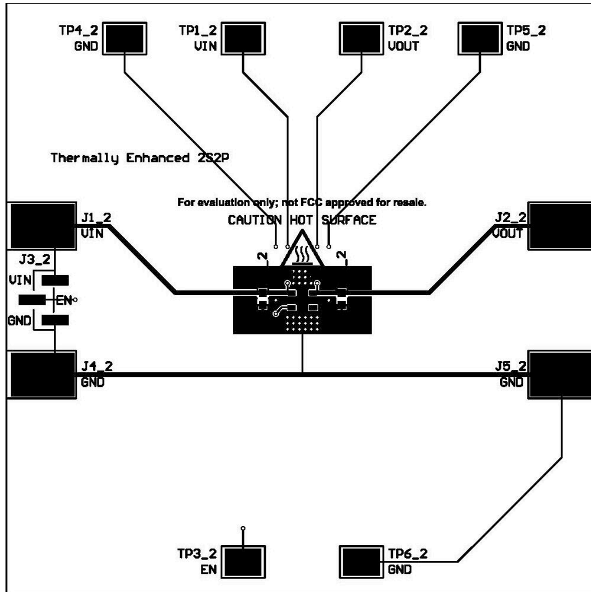

Figure A-53. TLV755P (SOT-23) Thermally Enhanced Top Layer

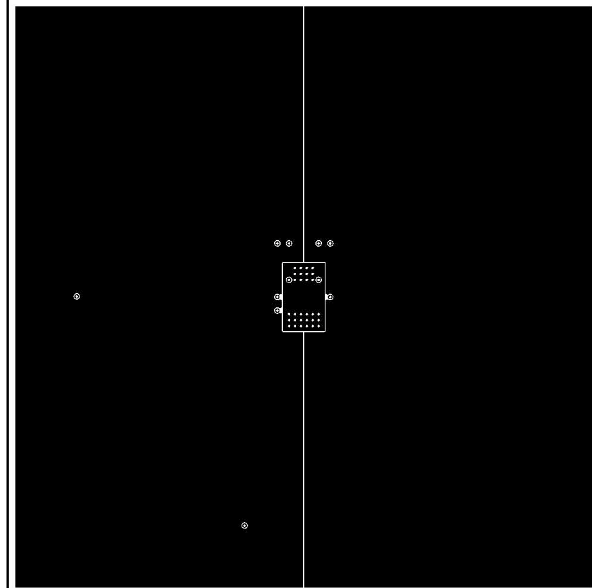

Figure A-54. TLV755P (SOT-23) Thermally Enhanced Internal Layer 1

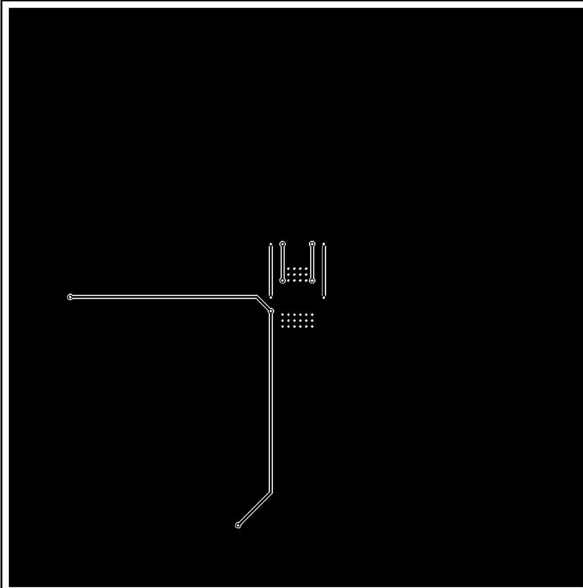

Figure A-55. TLV755P (SOT-23) Thermally Enhanced Internal Layer 2

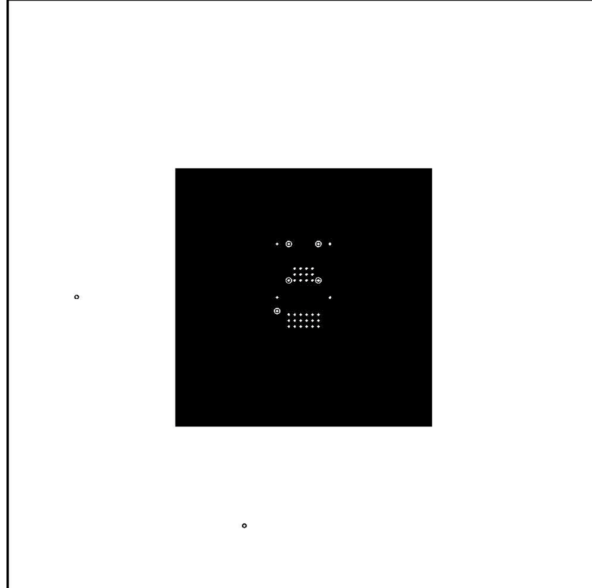

Figure A-56. TLV755P (SOT-23) Thermally Enhanced Bottom Layer

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A.3.5 Thermally Saturated Layout Drawings

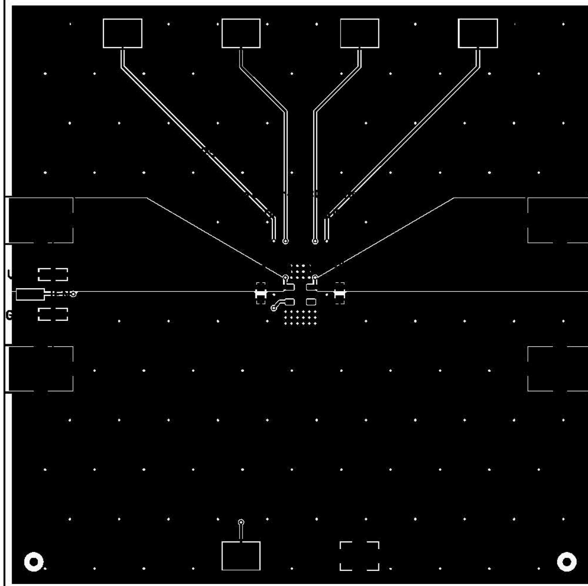

Figure A-57. TLV755P (SOT-23) Thermally Saturated Top Layer

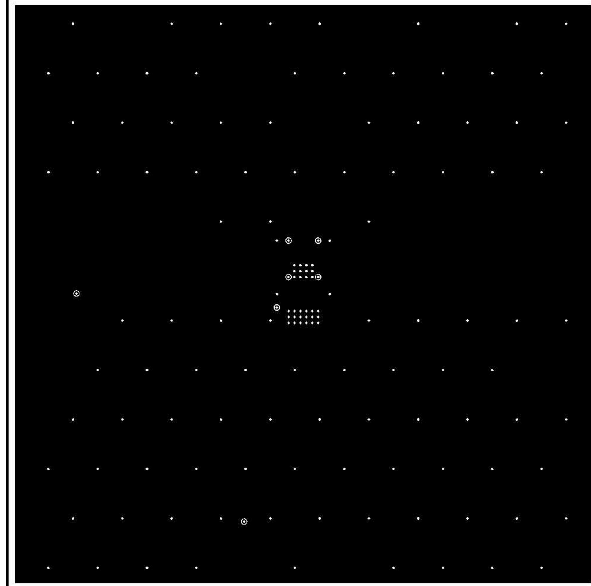

Figure A-58. TLV755P (SOT-23) Thermally Saturated Internal Layer 1

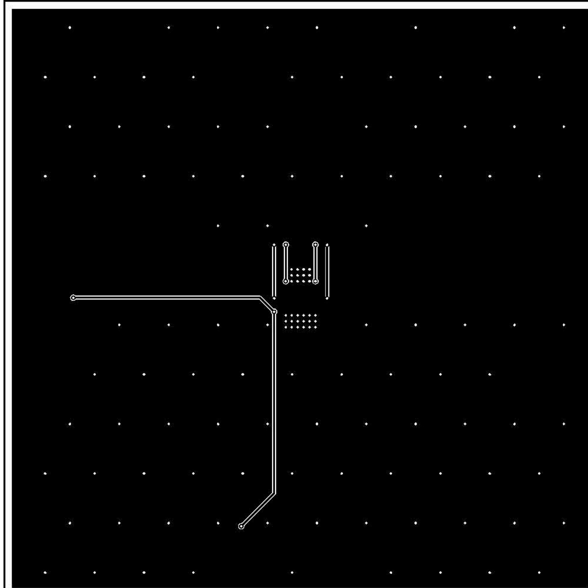

Figure A-59. TLV755P (SOT-23) Thermally Saturated Internal Layer 2

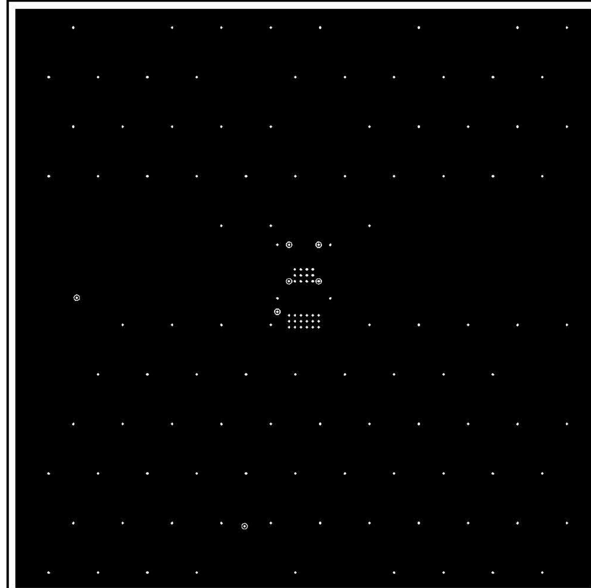

Figure A-60. TLV755P (SOT-23) Thermally Saturated Bottom Layer

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B Thermal Test Results

B.1 Thermal Performance Data

Table B-1. Maximum Ambient Temperature vs. Power Dissipation

	TPS745 (WSON)		TPS7B82-Q1 (TO-252)		TLV755P (SOT-23)	
Board	P_D (W)	$T_{A,max}$ (°C)	P_D (W)	$T_{A,max}$ (°C)	P_D (W)	$T_{A,max}$ (°C)
1S0P Approximation	0.00	175	0.00	182	0.00	165
	0.26	130	0.51	135	0.20	124
	0.51	88	1.00	90	0.39	80
	0.90	23	1.70	27	0.62	24
Internally Disconnected	0.00	178	0.00	178	0.00	164
	0.59	129	1.00	134	0.25	126
	1.14	83	1.95	88	0.49	88
JEDEC High-K Approximation	0.00	178	0.00	180	0.00	163
	0.74	130	1.53	133	0.27	122
	1.49	87	3.01	84	0.53	81
Thermally Enhanced	0.00	179	0.00	178	0.00	166
	0.83	135	1.77	129	0.36	128
	1.73	98	3.51	84	0.69	91
Thermally Saturated	0.00	177	0.00	177	0.00	164
	0.84	139	1.81	128	0.38	127
	1.64	106	3.62	82	0.76	85

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