Application Note

TPS6594/LP8764 PMIC Application Guide (Part 5)

Lijia Zhu

ABSTRACT

This document was translated from a simplified Chinese source. (ZHCAFF0)

With the rapid development of new energy vehicles, automobiles are transitioning from electrification to intelligence. As high-level assisted driving quickly lands across major OEMs and Tier 1 suppliers, TDA4 is being widely used in various terminal applications such as ADAS domain controllers, body domain controllers, and LiDAR. TI's new generation PMIC family, represented by TPS6594/LP8764, is not only the optimal power solution for TDA4 SOCs, but also an excellent choice for powering other models of SOCs. TPS6594/LP8764 features high integration, high scalability, and support for high-level functional safety. Because it has many functions and is relatively complex, there will be considerable difficulty in application. This series of articles will share insights from aspects such as the main internal mechanisms of the TPS6594/LP8764 PMIC chips, system design considerations, common problem troubleshooting ideas, and custom PMIC firmware (NVM). This article is the fifth piece in the series of articles, combining the content discussed in the previous articles, explaining a practical case of custom NVM.

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1 Introduction

The TPS6594/LP8764 series PMIC internally has non-volatile memory (NVM) units, and the NVM configuration is loaded into the register space of the chip during the startup phase. The NVM content determines the output voltage, power-up and power-down sequence, monitoring mechanism, communication interface, and other behavior logics of the device. The TPS6594/LP8764 series PMIC provides a mechanism to access and rewrite the content of the NVM through I2C (refer to the content of the second piece of this series of articles). The sub-models that support customer-side custom NVM are shown in Figure 1-1, in addition to this, TPS6521905 also supports customer custom NVM, but its architecture is different from TPS6594/LP8764, and this article mainly concentrates on TPS6594/LP8764 to conduct discussion.

It needs to be noted that the sub-models supporting customer custom NVM mentioned here refer to that this model is a blank chip when leaving TI factory, and its internal chip version and other information (0x0-0x3 registers) will not conflict with the models pre-burned with NVM when leaving TI factory; in fact, using sub-models with TI pre-burned numbers to update NVM is also possible, and generally this is used in the process of locating problems (refer to the fourth piece of the series of articles). In addition to this mode of customer-side customizing and burning NVM by themselves, there are also two modes: one is that third parties certified by TI can provide burning services, and the second is that TI provides brand new models customized with NVM for customers. For the details of these two modes, please consult the sales team.

General Part Number	Programmable version full Part number
TPS6594-Q1	TPS65940400RWERQ1
TPS6593-Q1	TPS65930400RWERQ1
LP8764-Q1	LP876440C0RQKRQ1
LP8769-Q1	LP876940C0RQKRQ1

Figure 1-1. Summary of Customer Custom NVM Sub-models of TPS6594/LP8764 Series PMIC

This article takes LP8764 as an example, combining the content discussed in the series of articles, to introduce a case of custom NVM, and TPS6594 can also refer to this case. The system simplified diagram of this case is shown in Figure 1-2, wherein the power supply system needs to provide several power rails of 3.3V, 1.8V, 1.2V, 1.1V, 5V, 6V, and 55V, wherein 3.3V, 1.8V, 1.2V, and 1.1V are provided by LP8764, 6V is provided by an external LDO, and 55V is provided by an external BOOST, and the overall system requires ASIL QM.

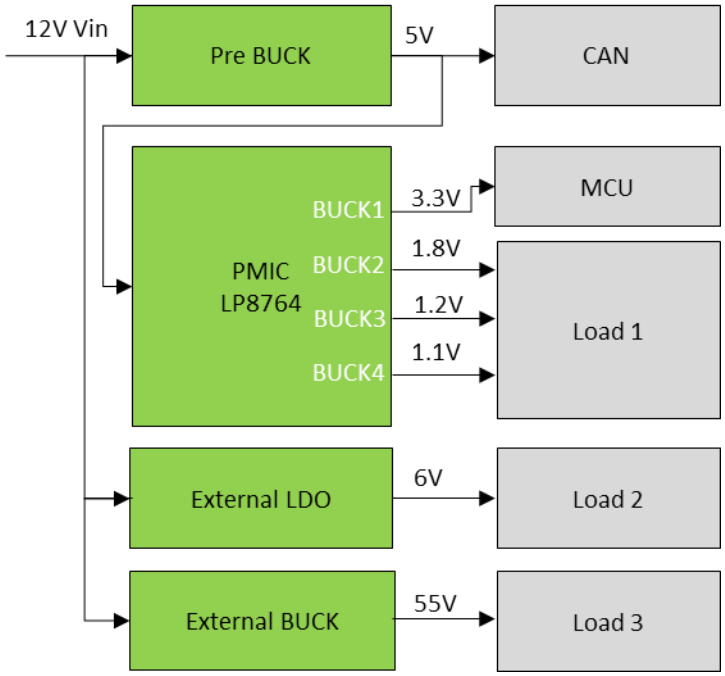

Figure 1-2. System Architecture of LP8764 Custom NVM Case

2 NVM Design

According to the system-level requirements, various settings of LP8764 can be determined. Generally speaking, there are two major categories of settings: one category is static settings, including power output voltage, output power-up and power-down slope, voltage monitoring threshold, power rail group, GPIO multiplexing, communication interface, and functional safety-related mechanisms, etc., corresponding to the content of page 0, page 1, and page 4 of registers; the other category is dynamic settings, including state machine planning and power-up and power-down sequence, etc., corresponding to the content of page 3 of registers.

2.1 Static Settings

LP8764 is a low-voltage input PMIC, and its maximum input voltage value does not exceed 6V, therefore the system needs to increase a stage of high-voltage BUCK at the front stage to provide 5V voltage, while at the same time it can just meet the requirement of system CAN for 5V power supply. The 3.3V power supply is provided by BUCK1 and output to the MCU, and several other low-voltage rails are provided by BUCK2/3/4 respectively to supply the external load Load1. The power supplies of external loads Load2 and Load3 require additional LDO and BOOST to provide, and at the same time it requires that the power-up sequence of these two rails is controllable and the power supply voltage is monitored, therefore the GPO function and VMON function of enable GPIO pins are used to control and monitor these two power supplies.

In order to be able to report fault information through the MCU, for the power fluctuations of VCCA, only an alarm is given, and the PMIC itself does not do any processing, therefore the power domain is set to No rail group, the power supply of the MCU is set in an independent MCU rail group, and several other power supplies (BUCK2/3/4 and VMON1/2 monitoring external LDO/BOOST) are set in the SOC rail group. When several power supplies of the SOC domain have overvoltage, undervoltage, and overcurrent faults, the PMIC only closes several power supplies of the SOC domain while keeping the 3.3V power supply of the MCU continuously existing, until the 3.3V power supply itself has a problem, then it will close all outputs. The current functional safety level is ASIL QM, and the residual voltage detection mechanism is not enabled here (generally ASIL C/D needs to enable this function). The final power supply static settings are shown in Figure 2-1.

Power	Voltage	Slew rate	Max load current	Power group	Monitor	Comments
VCCA Input	5V	/	/	No rail group	OV:+10% UV:-10%	确保CAN随时通信,要求此供电为常电,电压仅监控不处理,监控信息送MCU判决处理
BUCK1	3.3V	10mV/us	0.6A	MCU rail group	OV:+10% UV:-10% Current limit: 5.5A	PMCI关闭所有电源输出
BUCK2	1.8V	10mV/us	0.2A	SOC rail group	OV:+10% UV:-10% Current limit: 5.5A	PMIC 关闭这几路电源，进入MCU only模式
BUCK3	1.2V	10mV/us	2A	SOC rail group	OV:+10% UV:-10% Current limit: 5.5A	
BUCK4	1.1V	10mV/us	2.2A	SOC rail group	OV:+10% UV:-10% Current limit: 5.5A	
GPIO1	/	/	/	/	/	使用GPIO1和GPIO2使能外部LDO和BOOST，使系统上电时序受控
GPIO2	/	/	/	/	/	
VMON1	3V	10mV/us	/	SOC rail group	OV:+10% UV:-10%	监控LDO和BOOST的电压
VMON2	2.74V	10mV/us	/	SOC rail group	OV:+5% UV:-5%	

Figure 2-1. Each Power Supply Output Solution

The external LDO and BOOST need controlled power-up and power-down, and GPIO1 and GPIO2 can be set as GPO function, and the enable of external LDO and BOOST is controlled by the levels of these two GPIOs. At the same time, the PMIC needs an enable pin to control the power-up and power-down of the entire system, here a multiplexed function of GPIO4 is used, setting it as the Enable input pin. Note that the functions that each GPIO can multiplex are different from each other, and it needs to consult the manual to allocate reasonably.

Aiming at the requirement of needing to monitor the output voltages of external LDO and BOOST, GPIO7 and GPIO8 are multiplexed into VMON1 and VMON2 functions respectively, and in the hardware circuit, after dividing the output voltages of LDO and BOOST respectively (1/2 LDO output voltage and 1/20 BOOST output voltage), they are correspondingly sent into VMON1 and VMON2 pins. Just like the output monitoring setting of BUCK, VMON1 and VMON2 need to set corresponding monitoring voltages and monitoring thresholds.

GPIO10 is used here as the de-assertion reset signal of the MCU, and after all power-up sequences are completed, the nRSTOUT pin is pulled high from low, de-asserting reset of the MCU, and the system software starts to run normally. GPIO9 is used as an extra hardware warm reset function, and when the rising edge of the hardware signal outside the module arrives, a negative pulse is generated on nRSTOUT to restart the MCU, and at the same time resets all BUCK output configurations (the MCU might modify the configuration of BUCK through I2C). The GPIO allocation solution is as shown in Figure 2-2, and the final system architecture is as shown in Figure 2-3.

GPIO	GPIO setting	Comments
1	GPO, push pull output	Enable external
2	GPO, push pull output	regulators
3	GPI, internal PD	Not used
4	Enable pin	Enable input
5	GPI, internal PD	Not used
6	GPI, internal PD	Not used
7	VMON1,PG window = 3V +- 10%.	Monitor the external
8	VMON2, PG window = 2.74V +- 5%	regulator
9	GPI, internal PU	Warm reset trigger
10	nRSTOUT	MCU reset control

Figure 2-2. GPIO Allocation Solution

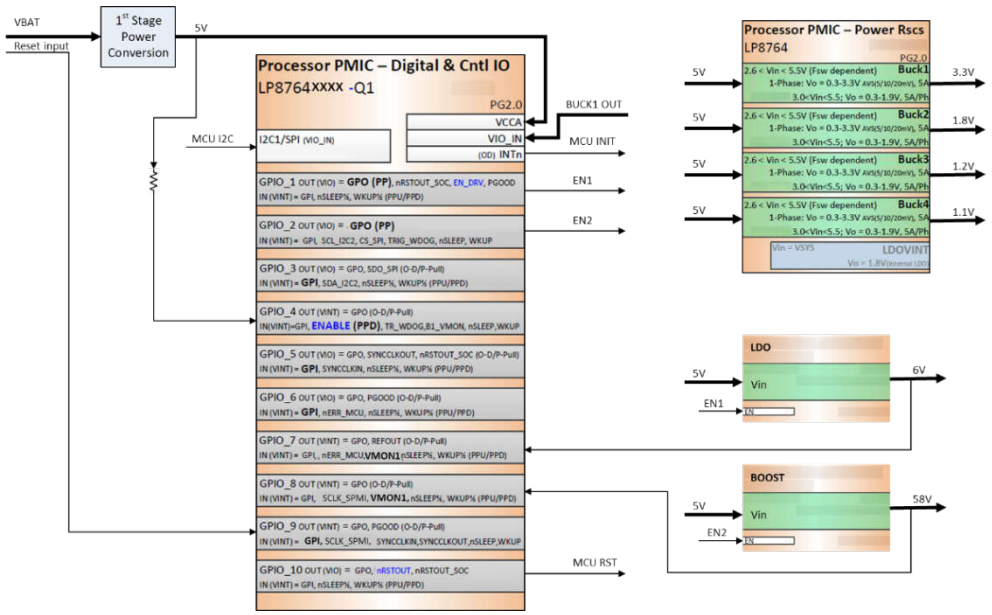

Figure 2-3. System Power Architecture Solution

Referring to the relevant content in the Scalable PMIC GUI documentation, a new NVM project can be conveniently created using the Scalable PMIC GUI software. The final static settings are as shown in Figure 2-4 to Figure 2-9.

Device identification

Register	Field name	Value
DEV_REV	ASIL_QM	QM
	DEVICE_GPN	0x0
	GRADE	Industrial
NVM_CODE_1	TI_NVM_ID	0x0
NVM_CODE_2	TI_NVM_REV	0x0
CUSTOMER_NVM_ID_REG	CUSTOMER_NVM_ID	0x1

Global monitor control

Register	Field name	Value
VCCA_VMON_CTRL	VMON_DEGLITCH_SEL	VCCA 20us, VMON/BUCK 20us

VCCA

Register	Field name	Value
VCCA_VMON_CTRL	VCCA_VMON_EN	Enabled; OV and UV comparators.
VCCA_PG_WINDOW	VCCA_OV_THR	+10%
	VCCA_UV_THR	-10%
	VCCA_PG_SET	5.0 V
RAIL_SEL_3	VCCA_GRP_SEL	No group assigned
GENERAL_REG_3	LPM_EN_DISABLES_VCCA_VMON	VCCA_VMON enabled if VCCA_VMON_EN=1 and LPM_EN=0

Phase configuration

Register	Field name	Value
PHASE_CONFIG	MP_CONFIG	1+1+1+1

Figure 2-4. System Settings

BUCK1

Register	Field name	Value
BUCK1_CTRL	BUCK1_FPWM	PFM and PWM operation (AUTO mode).
	BUCK1_FPWM_MP	Automatic phase adding and shedding.
	BUCK1_VSEL	BUCK1_VOUT_1
	BUCK1_RV_SEL	Disabled
BUCK1_CONF	BUCK1_SLEW_RATE	10 mV/µs
	BUCK1_ILIM	5.5 A
BUCK1_VOUT_1	BUCK1_VSET1	3.30 V
BUCK1_VOUT_2	BUCK1_VSET2	0.3 V
BUCK1_PG_WINDOW	BUCK1_OV_THR	+5% / +50 mV
	BUCK1_UV_THR	-5% / -50 mV
RAIL_SEL_1	BUCK1_GRP_SEL	MCU rail group

BUCK2

Register	Field name	Value
BUCK2_CTRL	BUCK2_FPWM	PFM and PWM operation (AUTO mode).
	BUCK2_VSEL	BUCK2_VOUT_1
	BUCK2_RV_SEL	Disabled
BUCK2_CONF	BUCK2_SLEW_RATE	10 mV/µs
	BUCK2_ILIM	5.5 A
BUCK2_VOUT1	BUCK2_VSET1	1.80 V
BUCK2_VOUT2	BUCK2_VSET2	0.3 V
BUCK2_PG_WINDOW	BUCK2_OV_THR	+5% / +50 mV
	BUCK2_UV_THR	-5% / -50 mV
RAIL_SEL_1	BUCK2_GRP_SEL	SOC rail group

BUCK3

Register	Field name	Value
BUCK3_CTRL	BUCK3_FPWM	PFM and PWM operation (AUTO mode).
	BUCK3_FPWM_MP	Automatic phase adding and shedding.
	BUCK3_VSEL	BUCK3_VOUT_1
	BUCK3_RV_SEL	Disabled
BUCK3_CONF	BUCK3_SLEW_RATE	10 mV/µs
	BUCK3_ILIM	5.5 A
BUCK3_VOUT1	BUCK3_VSET1	1.20 V
BUCK3_VOUT2	BUCK3_VSET2	0.3 V
BUCK3_PG_WINDOW	BUCK3_OV_THR	+5% / +50 mV
	BUCK3_UV_THR	-5% / -50 mV
RAIL_SEL_1	BUCK3_GRP_SEL	SOC rail group

BUCK4

Register	Field name	Value
BUCK4_CTRL	BUCK4_FPWM	PFM and PWM operation (AUTO mode).
	BUCK4_VSEL	BUCK4_VOUT_1
	BUCK4_RV_SEL	Disabled
BUCK4_CONF	BUCK4_SLEW_RATE	10 mV/µs
	BUCK4_ILIM	5.5 A
BUCK4_VOUT_1	BUCK4_VSET1	1.10 V
BUCK4_VOUT_2	BUCK4_VSET2	0.3 V
BUCK4_PG_WINDOW	BUCK4_OV_THR	+5% / +50 mV
	BUCK4_UV_THR	-5% / -50 mV
RAIL_SEL_1	BUCK4_GRP_SEL	SOC rail group

VMON1 & 2

Register	Field name	Value
VCCA_VMON_CTRL	VMON1_RV_SEL	Disabled
	VMON2_RV_SEL	Disabled
VMON1_PG_WINDOW	VMON1_OV_THR	+10% / +100mV / (+500 mV)
	VMON1_UV_THR	-10% / -100 mV / (-500 mV)
	VMON1_RANGE	0.3 - 3.34 V
VMON2_PG_WINDOW	VMON2_OV_THR	+5% / +50 mV / (+250 mV)
	VMON2_UV_THR	-5% / -50 mV / (-250 mV)
	VMON2_RANGE	0.3 - 3.34 V
VMON1_PG_LEVEL	VMON1_PG_SET	3.0 V
VMON2_PG_LEVEL	VMON2_PG_SET	2.74 V
VMON_CONF	VMON1_SLEW_RATE	10 mV/µs
	VMON2_SLEW_RATE	10 mV/µs
RAIL_SEL_3	VMON1_GRP_SEL	SOC rail group
	VMON2_GRP_SEL	SOC rail group

Figure 2-5. BUCK and VMON Settings

Register	Bit field	Value
1 GPIO1_CONF	GPIO1_OD	Push-pull output
	GPIO1_DIR	Output
	GPIO1_SEL	GPIO1
	GPIO1_PU_SEL	Pull-down resistor selected
	GPIO1_PU_PD_EN	Disabled; Pull-up/pull-down resistor.
	GPIO1_DEGLITCH_EN	No deglitch, only synchronization.

Register	Bit field	Value
2 GPIO2_CONF	GPIO2_OD	Push-pull output
	GPIO2_DIR	Output
	GPIO2_SEL	GPIO2
	GPIO2_PU_SEL	Pull-down resistor selected
	GPIO2_PU_PD_EN	Disabled; Pull-up/pull-down resistor.
	GPIO2_DEGLITCH_EN	No deglitch, only synchronization

Register	Bit field	Value
3 GPIO3_CONF	GPIO3_OD	Push-pull output
	GPIO3_DIR	Input
	GPIO3_SEL	GPIO3
	GPIO3_PU_SEL	Pull-down resistor selected
	GPIO3_PU_PD_EN	Enabled; Pull-up/pull-down resistor.
	GPIO3_DEGLITCH_EN	No deglitch, only synchronization.

Register	Bit field	Value
4 GPIO4_CONF	GPIO4_OD	Push-pull output
	GPIO4_DIR	Input
	GPIO4_SEL	ENABLE
	GPIO4_PU_SEL	Pull-down resistor selected
	GPIO4_PU_PD_EN	Enabled; Pull-up/pull-down resistor.
	GPIO4_DEGLITCH_EN	8 us deglitch time.

Register	Bit field	Value
5 GPIO5_CONF	GPIO5_OD	Push-pull output
	GPIO5_DIR	Input
	GPIO5_SEL	GPIO5
	GPIO5_PU_SEL	Pull-down resistor selected
	GPIO5_PU_PD_EN	Enabled; Pull-up/pull-down resistor.
	GPIO5_DEGLITCH_EN	No deglitch, only synchronization.

Register	Bit field	Value
6 GPIO6_CONF	GPIO6_OD	Push-pull output
	GPIO6_DIR	Input
	GPIO6_SEL	GPIO6
	GPIO6_PU_SEL	Pull-down resistor selected
	GPIO6_PU_PD_EN	Enabled; Pull-up/pull-down resistor.
	GPIO6_DEGLITCH_EN	No deglitch, only synchronization.

Register	Bit field	Value
7 GPIO7_CONF	GPIO7_OD	Push-pull output
	GPIO7_DIR	Input
	GPIO7_SEL	VMON1
	GPIO7_PU_SEL	Pull-down resistor selected
	GPIO7_PU_PD_EN	Disabled; Pull-up/pull-down resistor.
	GPIO7_DEGLITCH_EN	No deglitch, only synchronization.

Register	Bit field	Value
8 GPIO8_CONF	GPIO8_OD	Push-pull output
	GPIO8_DIR	Input
	GPIO8_SEL	VMON2
	GPIO8_PU_SEL	Pull-down resistor selected
	GPIO8_PU_PD_EN	Disabled; Pull-up/pull-down resistor.
	GPIO8_DEGLITCH_EN	No deglitch, only synchronization.

Register	Bit field	Value
9 GPIO9_CONF	GPIO9_OD	Push-pull output
	GPIO9_DIR	Input
	GPIO9_SEL	GPIO9
	GPIO9_PU_SEL	Pull-down resistor selected
	GPIO9_PU_PD_EN	Disabled; Pull-up/pull-down resistor.
	GPIO9_DEGLITCH_EN	No deglitch, only synchronization.

Register	Bit field	Value
10 GPIO10_CONF	GPIO10_OD	Push-pull output
	GPIO10_DIR	Output
	GPIO10_SEL	nRSTOUT
	GPIO10_PU_SEL	Pull-down resistor selected
	GPIO10_PU_PD_EN	Disabled; Pull-up/pull-down resistor.
	GPIO10_DEGLITCH_EN	No deglitch, only synchronization.

Figure 2-6. GPIO Settings

REGISTER	BIT FIELD	VALUE
SERIAL_IF_CONFIG	I2C_SPI_SEL	I2C
	I2C1_SPI_CRC_EN	CRC disabled
	I2C2_CRC_EN	CRC disabled
I2C1_ID_REG	I2C1_ID	0x60
I2C2_ID_REG	I2C2_ID	0x12

Figure 2-7. Interface Configuration

REGISTER	BIT FIELD	VALUE
FSM_TRIG_MASK_1	GPIO1_FSM_MASK	Masked
	GPIO1_FSM_MASK_POL	Low; Masking sets signal value to '0'
	GPIO2_FSM_MASK	Masked
	GPIO2_FSM_MASK_POL	Low; Masking sets signal value to '0'
	GPIO3_FSM_MASK	Masked
	GPIO3_FSM_MASK_POL	Low; Masking sets signal value to '0'
	GPIO4_FSM_MASK	Masked
	GPIO4_FSM_MASK_POL	Low; Masking sets signal value to '0'
FSM_TRIG_MASK_2	GPIO5_FSM_MASK	Masked
	GPIO5_FSM_MASK_POL	Low; Masking sets signal value to '0'
	GPIO6_FSM_MASK	Masked
	GPIO6_FSM_MASK_POL	Low; Masking sets signal value to '0'
	GPIO7_FSM_MASK	Masked
	GPIO7_FSM_MASK_POL	Low; Masking sets signal value to '0'
	GPIO8_FSM_MASK	Masked
	GPIO8_FSM_MASK_POL	Low; Masking sets signal value to '0'
FSM_TRIG_MASK_3	GPIO9_FSM_MASK	Masked
	GPIO9_FSM_MASK_POL	Low; Masking sets signal value to '0'

REGISTER	BIT FIELD	VALUE
FSM_TRIG_MASK_3	GPIO10_FSM_MASK	Masked
	GPIO10_FSM_MASK_POL	Low; Masking sets signal value to '0'
MASK_GPIO1_8_FALL	GPIO1_FALL_MASK	Interrupt not generated.
	GPIO2_FALL_MASK	Interrupt not generated.
	GPIO3_FALL_MASK	Interrupt not generated.
	GPIO4_FALL_MASK	Interrupt not generated.
	GPIO5_FALL_MASK	Interrupt not generated.
	GPIO6_FALL_MASK	Interrupt not generated.
	GPIO7_FALL_MASK	Interrupt not generated.
	GPIO8_FALL_MASK	Interrupt not generated.
MASK_GPIO1_8_RISE	GPIO1_RISE_MASK	Interrupt not generated.
	GPIO2_RISE_MASK	Interrupt not generated.
	GPIO3_RISE_MASK	Interrupt not generated.
	GPIO4_RISE_MASK	Interrupt not generated.
	GPIO5_RISE_MASK	Interrupt not generated.
	GPIO6_RISE_MASK	Interrupt not generated.
	GPIO7_RISE_MASK	Interrupt not generated.
	GPIO8_RISE_MASK	Interrupt not generated.
MASK_GPIO9_10	GPIO9_FALL_MASK	Interrupt generated
	GPIO9_RISE_MASK	Interrupt not generated.
	GPIO10_FALL_MASK	Interrupt not generated.
	GPIO10_RISE_MASK	Interrupt not generated.

REGISTER	BIT FIELD	VALUE
MASK_BUCK1_2	BUCK1_ILIM_MASK	Interrupt not generated.
	BUCK1_OV_MASK	Interrupt generated
	BUCK1_UV_MASK	Interrupt generated
	BUCK2_ILIM_MASK	Interrupt not generated.
	BUCK2_OV_MASK	Interrupt generated
	BUCK2_UV_MASK	Interrupt generated
MASK_BUCK3_4	BUCK3_ILIM_MASK	Interrupt not generated.
	BUCK3_OV_MASK	Interrupt generated
	BUCK3_UV_MASK	Interrupt generated
	BUCK4_ILIM_MASK	Interrupt not generated.
	BUCK4_OV_MASK	Interrupt generated
	BUCK4_UV_MASK	Interrupt generated

REGISTER	BIT FIELD	VALUE
FSM_TRIG_SEL_1	MCU_RAIL_TRIG	MCU power error
	SOC_RAIL_TRIG	SOC power error
	OTHER_RAIL_TRIG	Orderly shutdown
	SEVERE_ERR_TRIG	Immediate shutdown
FSM_TRIG_SEL_2	MODERATE_ERR_TRIG	Orderly shutdown

REGISTER	BIT FIELD	VALUE
MASK_VMON	VCCA_OV_MASK	Interrupt not generated.
	VCCA_UV_MASK	Interrupt not generated.
MASK_STARTUP	SOFT_REBOOT_MASK	Interrupt generated
	ENABLE_MASK	Interrupt generated
	FSD_MASK	Interrupt not generated.
MASK_MISC	TWARN_MASK	Interrupt generated
	BIST_PASS_MASK	Interrupt generated
	EXT_CLK_MASK	Interrupt not generated.

REGISTER	BIT FIELD	VALUE
MASK_MODERATE_ERR	BIST_FAIL_MASK	Interrupt generated
	REG_CRC_ERR_MASK	Interrupt generated
	SPMI_ERR_MASK	Interrupt not generated.
	NINT_READBACK_MASK	Interrupt generated
	NRSTOUT_READBACK_MASK	Interrupt generated
MASK_FSM_ERR	IMM_SHUTDOWN_MASK	Interrupt generated
	MCU_PWR_ERR_MASK	Interrupt generated
	SOC_PWR_ERR_MASK	Interrupt generated
	ORD_SHUTDOWN_MASK	Interrupt generated
MASK_COMM_ERR	COMM_FRM_ERR_MASK	Interrupt not generated.
	COMM_CRC_ERR_MASK	Interrupt not generated.
	COMM_ADR_ERR_MASK	Interrupt not generated.
	I2C2_CRC_ERR_MASK	Interrupt not generated.
	I2C2_ADR_ERR_MASK	Interrupt not generated.

REGISTER	BIT FIELD	VALUE
MASK_READBACK_ERR	EN_DRV_READBACK_MASK	Interrupt not generated.
	NRSTOUT_SOC_READBACK_MASK	Interrupt not generated.
MASK_ESM	ESM_MCU_PIN_MASK	Interrupt not generated.
	ESM_MCU_RST_MASK	Interrupt not generated.
	ESM_MCU_FAIL_MASK	Interrupt not generated.

VMON

REGISTER	BIT FIELD	VALUE
MASK_VMON	VMON1_OV_MASK	Interrupt generated
	VMON1_UV_MASK	Interrupt generated
	VMON2_OV_MASK	Interrupt generated
	VMON2_UV_MASK	Interrupt generated

Figure 2-8. MASK Settings

POWERGOOD

REGISTER	BIT FIELD	VALUE
PGOOD_SEL_1	PGOOD_SEL_BUCK1	Masked
	PGOOD_SEL_BUCK2	Masked
	PGOOD_SEL_BUCK3	Masked
	PGOOD_SEL_BUCK4	Masked
PGOOD_SEL_4	PGOOD_SEL_VCCA	Masked
	PGOOD_SEL_TDIE_WARN	Masked
	PGOOD_SEL_NRSTOUT	Masked
	PGOOD_SEL_NRSTOUT_SOC	Masked
	PGOOD_POL	PGOOD signal is high when monitored inputs are valid
	PGOOD_WINDOW	Only undervoltage is monitored
	PGOOD_SEL_VMON1	Masked
	PGOOD_SEL_VMON2	Masked

Spread spectrum

REGISTER	BIT FIELD	VALUE
SPREAD_SPECTRUM_1	SS_EN	Spread spectrum disabled
	SS_DEPTH	No modulation

Functional safety

REGISTER	BIT FIELD	VALUE
GENERAL_REG_0	FAST_BOOT_BIST	LBIST is run during boot BIST
	VMON_ABIST_EN	VMON ABIST enabled
STARTUP_CTRL	FAST_BIST	Logic and analog BIST is run at BOOT BIST.
RECOV_CNT_REG_2	RECOV_CNT_THR	15

Additional configurations

REGISTER	BIT FIELD	VALUE
STARTUP_CTRL	STARTUP_DEST	ACTIVE
	LP_STANDBY_SEL	Normal standby state is used.
PFSM_DELAY_REG_1	PFSM_DELAY1	0x0
PFSM_DELAY_REG_2	PFSM_DELAY2	0x0
PFSM_DELAY_REG_3	PFSM_DELAY3	0x0
PFSM_DELAY_REG_4	PFSM_DELAY4	0x0
PLL_CTRL	EXT_CLK_FREQ	1.1 MHz
ENABLE_CONF	ENABLE_POL	Active high

Additional configurations

REGISTER	BIT FIELD	VALUE
CONFIG_1	TWARN_LEVEL	130C
	I2C1_HS	Standard, fast or fast+ by default, can be set to Hs-mode by Hs-mode master code.
	I2C2_HS	Standard, fast or fast+ by default, can be set to Hs-mode by Hs-mode master code.
	EN_ILIM_FSM_CTRL	Buck regulators ILIM interrupts affect FSM triggers.
	NSLEEP1_MASK	NSLEEP1(B) affects FSM state transitions.
	NSLEEP2_MASK	NSLEEP2(B) affects FSM state transitions.
	TSD_ORD_LEVEL	140C
GENERAL_REG_1	REG_CRC_EN	Register CRC disabled

Figure 2-9. Miscellaneous Settings

2.2 State Machine Planning and Power-up and Power-down Sequence Settings

The power-up sequence required by the system is as follows: Enable pulled up -> BUCK1 power up -> delay 2000us -> BUCK2 power up -> delay 2000us -> BUCK3 power up -> delay 2000us -> BUCK4 power up -> delay 2000us -> external LDO power up -> delay 2000us -> external LDO power up, and the power-down sequence is completely opposite to the power-up sequence.

Combining the previous power rail group settings, arrange the following several PFSM states:

1. PFSM_START: Starting point of the PFSM and bridge state between FFSM and PFSM.
2. WAIT4ENABLE: The state between PFSM START and ACTIVE, the PMIC power rails have no output, and some initialization actions of the device can be completed during the process of entering this state.
3. ACTIVE: Normal operating state with all power rails enabled.
4. STANDBY: The system sleep state, and all power supplies are turned off.
5. MCU_ONLY: MCU only mode, and only the 3.3V of BUCK1 has output.
6. TO_SAFE: Bridge state from PFSM to the FFSM SAFE_RECOVERY state.
7. RUNTIME_BIST: BIST operation actively triggered by the MCU.

After setting up the states, it needs to plan the triggers for switching states:

1. ENABLE pulled up serves as the condition for starting to enter ACTIVE.
2. SOC power error and I2C trigger0 set serve as the conditions for ACTIVE entering MCU ONLY.
3. ENABLE pulled low and I2C trigger2 set serve as the conditions for ACTIVE/MCU ONLY entering STANDBY.
4. ENABLE pulled up and I2C trigger1 set serve as the conditions for STANDBY/MCU ONLY recovering to ACTIVE.
5. I2C trigger3 set serves as the condition for entering RUNTIME BIST.
6. MCU POWER ERROR, ORDERLY SHUTDOWN, and IMMEDIATE SHUTDOWN trigger entry into SAFE_RECOVERY.

7. GPIO9 falling edge serves as the trigger for ANY2WARM.

After defining states and triggers, PMIC actions during state transitions must be configured, namely the power-up and power-down sequences.

1. WAIT4ENABLE sequence, executed when entering the WAIT4ENABLE state, and in this application, the VMON enabling VCCA is set.
2. ANY2ACTIVE sequence: Executed when entering ACTIVE. The sequence is BUCK1 rise -> 2000us delay -> BUCK2 rise -> 2000us delay -> BUCK3 rise -> 2000us delay -> BUCK4 rise -> 2000us delay -> GPIO1 rise -> 2000us delay -> GPIO2 rise -> 30ms delay -> VMON1 enable -> 30ms delay -> VMON2 enable -> nRSTOUT rise

   Since the external LDO and BOOST have relatively slow startup slew rates, additional delays are required to ensure that their output voltages stabilize at the expected values. Therefore, additional delays of 30ms and 60ms are inserted after GPIO2 is asserted.
3. ANY2MCU sequence: Executed when transitioning from ACTIVE to MCU_ONLY. Sequence: VMON2 disable -> 30ms delay -> VMON1 disable -> 30ms delay -> GPIO2 down -> 2000us delay -> GPIO1 down -> 2000us delay -> BUCK4 off -> 2000us delay -> BUCK3 off -> 2000us delay -> BUCK2 off.
4. ORDERLYOFF sequence, executed when going from ACTIVE/MCU ONLY state to STANDBY state, and the sequence is nRSTOUT down -> VMON2 disable -> 30ms delay -> VMON1 disable -> 30ms delay -> GPIO2 down -> 2000us delay -> GPIO1 down -> 2000us delay -> BUCK4 off -> 2000us delay -> BUCK3 off -> 2000us delay -> BUCK2 off -> 2000us delay -> BUCK1 off
5. ORDERLYOFF2SAFE sequence: Executed when transitioning from any state to TO_SAFE. Sequence is identical to ORDERLYOFF.
6. IMMEDIATELYOFF2SAFE sequence: Executed when transitioning from any state to TO_SAFE. All power rails are shut down immediately.
7. ANY2WARM sequence: Used in ACTIVE and MCU_ONLY modes. Resets currently enabled BUCKs and toggles nRSTOUT to reset the MCU.

The final state machine is as shown in Figure 2-10.

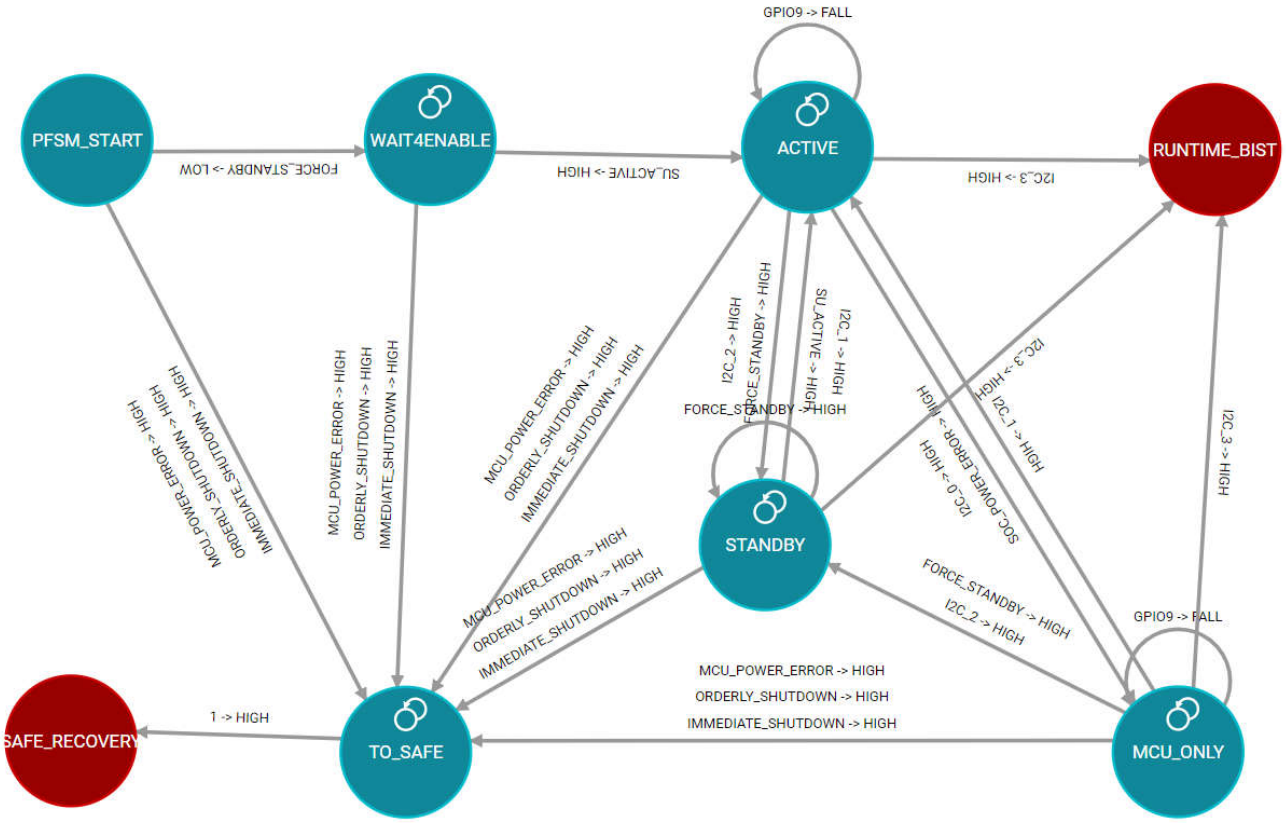

Figure 2-10. PFSM Configuration

3 NVM Effect Measured

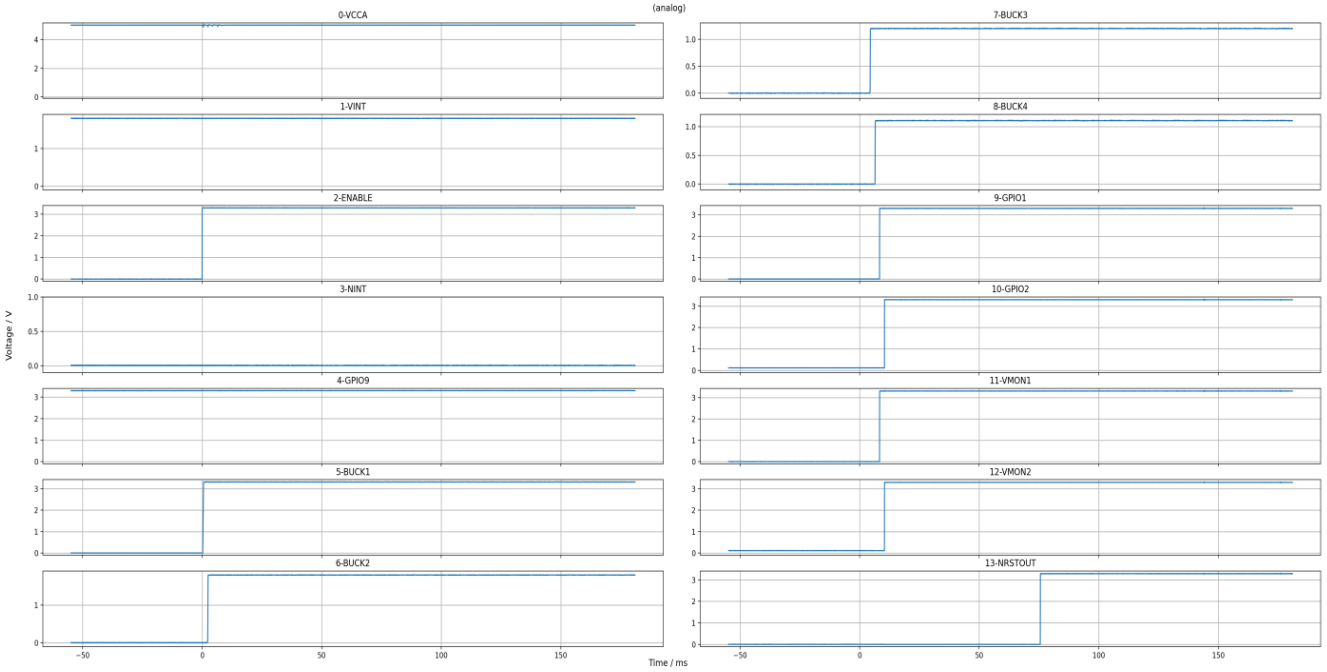

Figure 3-1. START2ACT Sequence Test

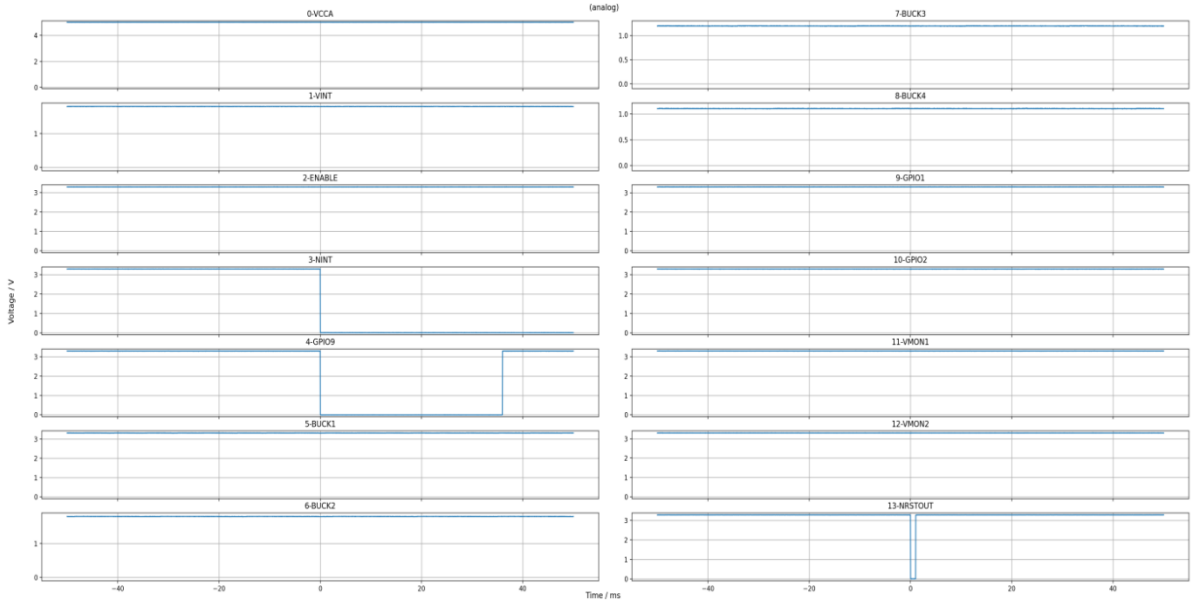

Figure 3-2. ACT2WARM Sequence Test

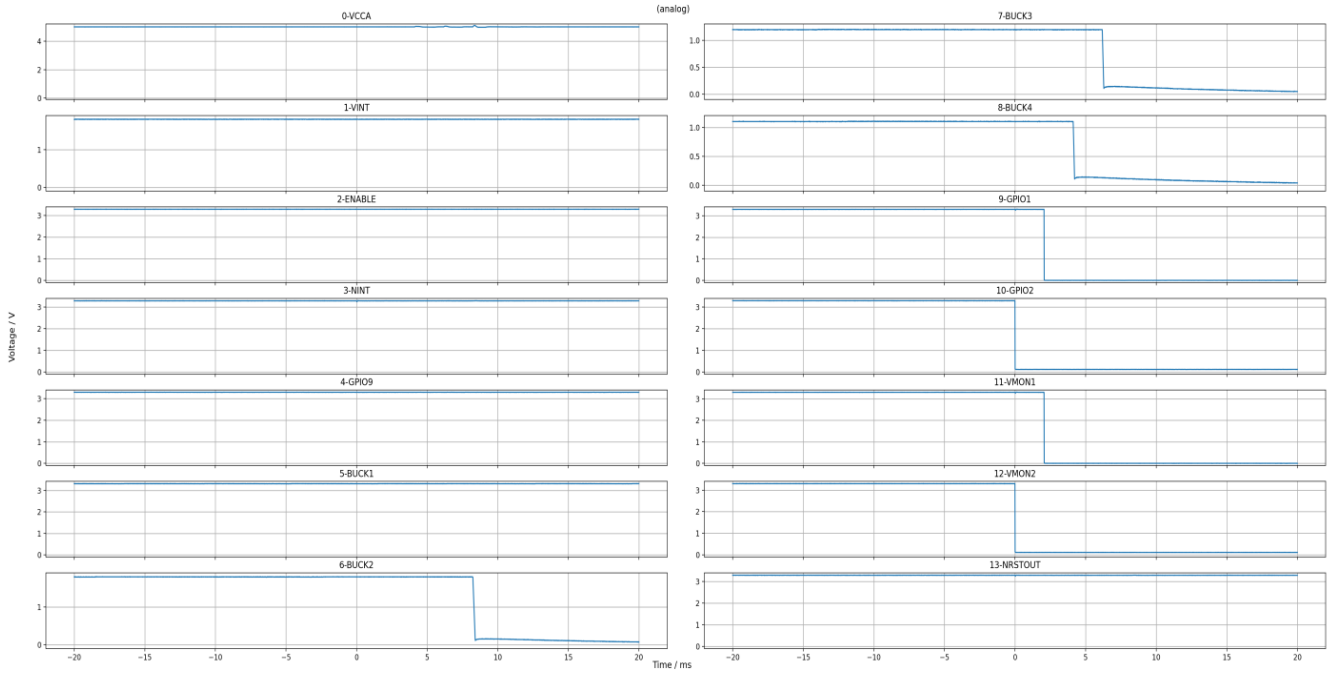

Figure 3-3. ACT2MCU Sequence Test

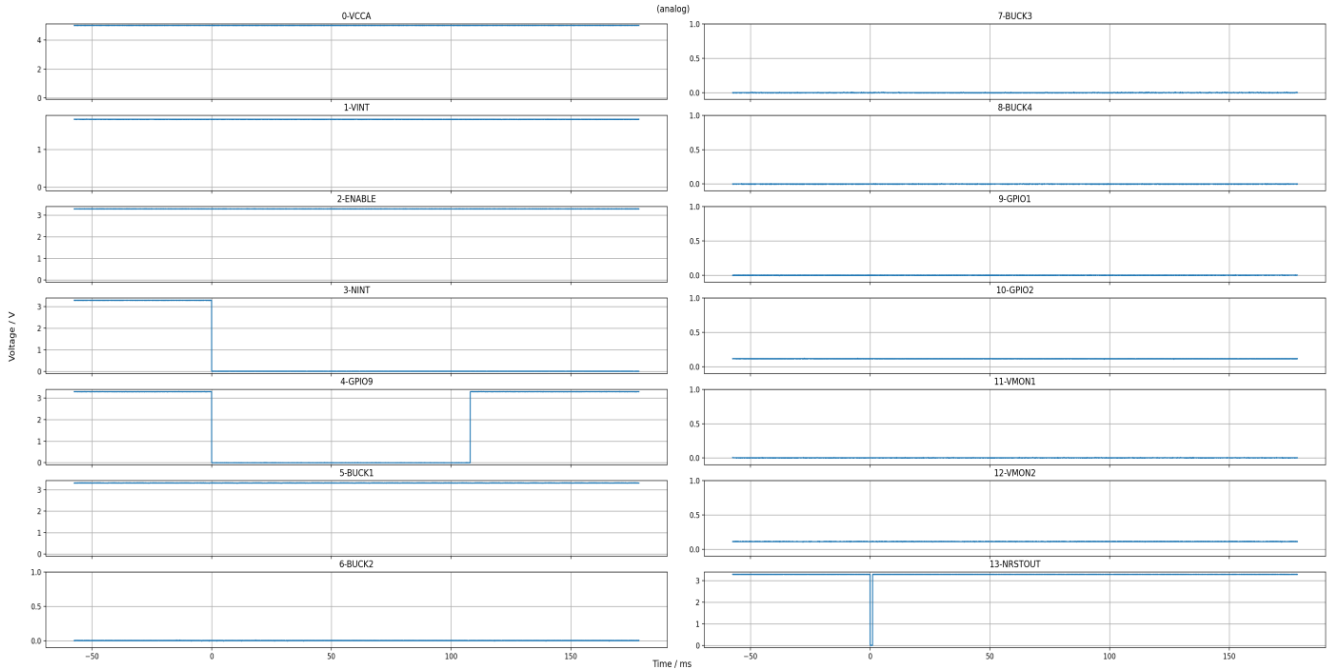

Figure 3-4. MCU2WARM Sequence Test

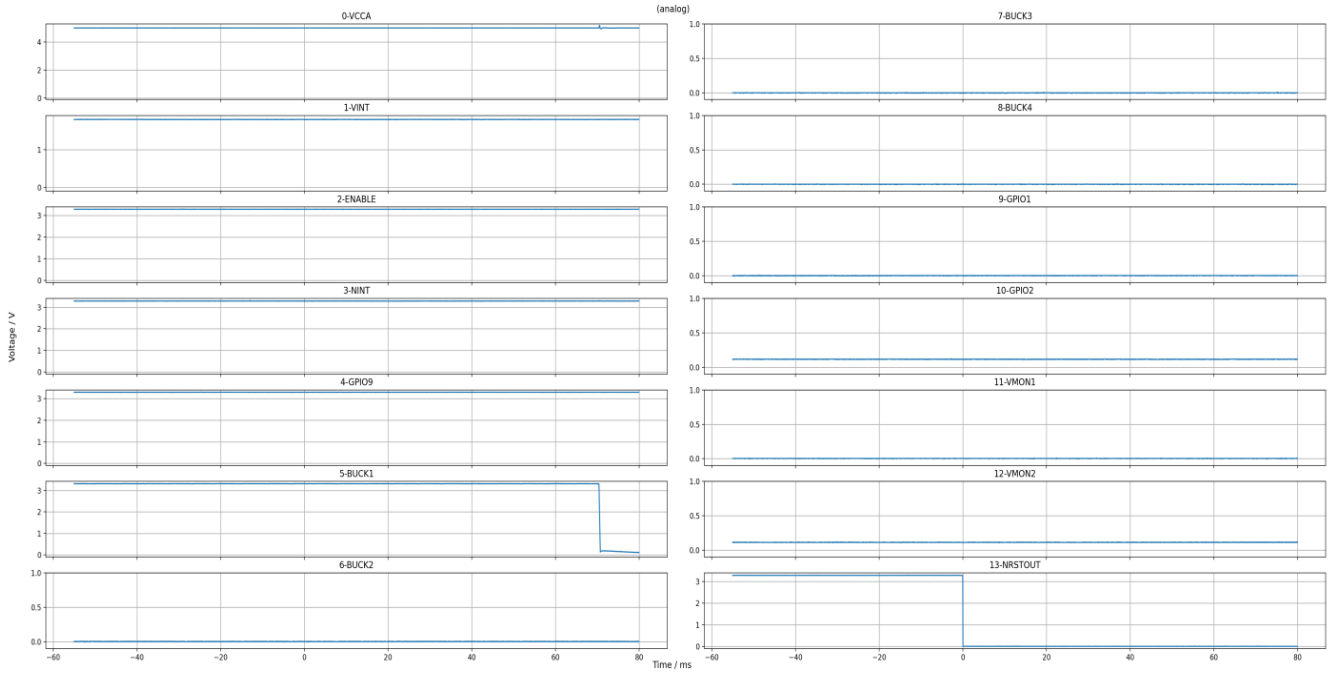

Figure 3-5. MCU2STANDBY Sequence Test

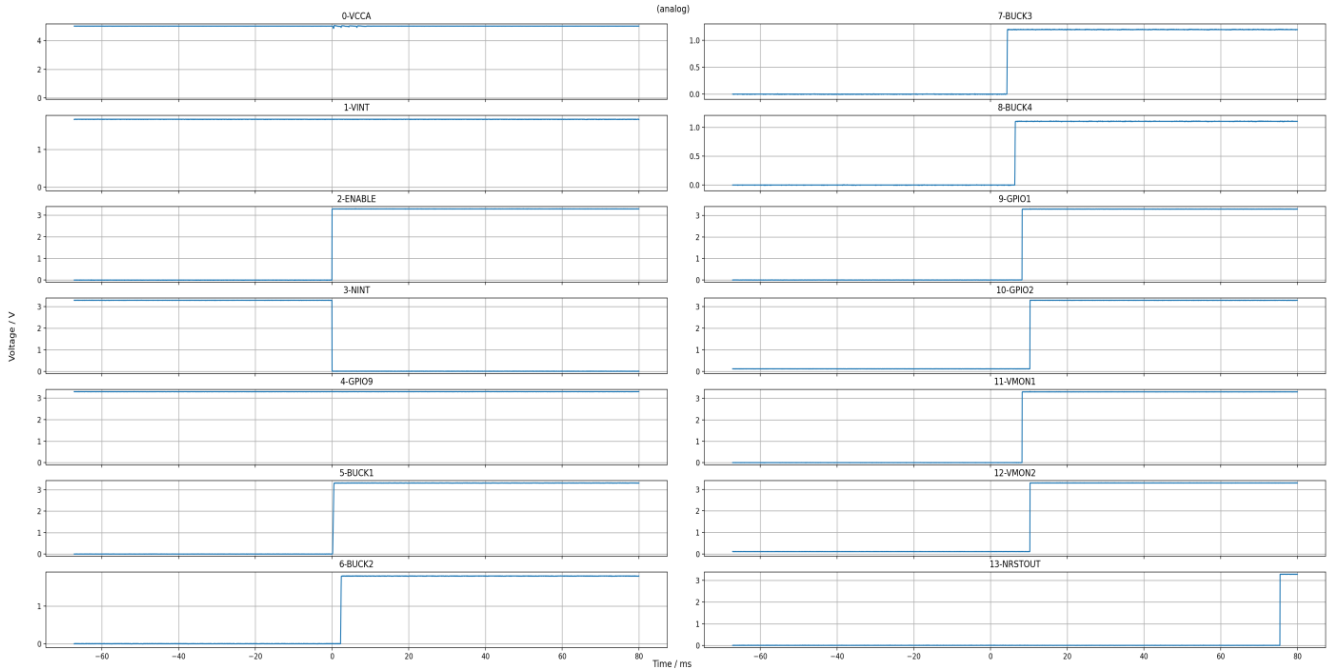

Figure 3-6. STANDBY2ACT Sequence Test

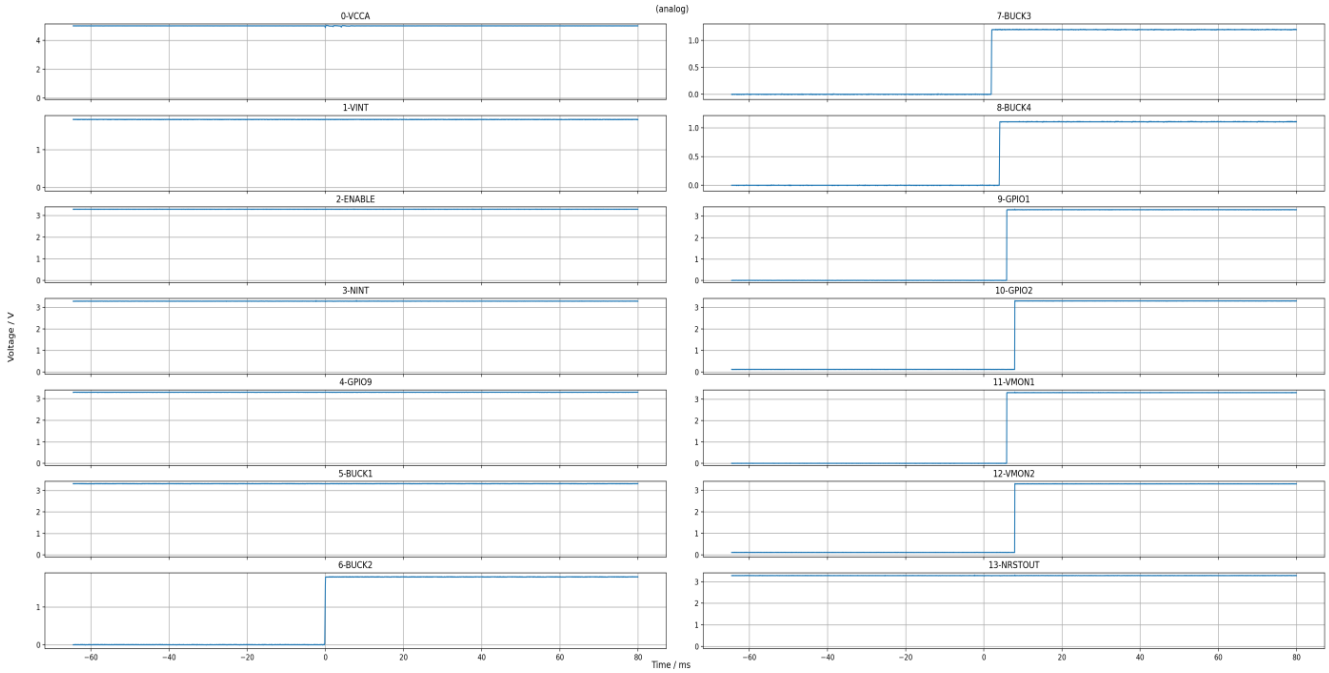

Figure 3-7. MCU2ACT Sequence Test

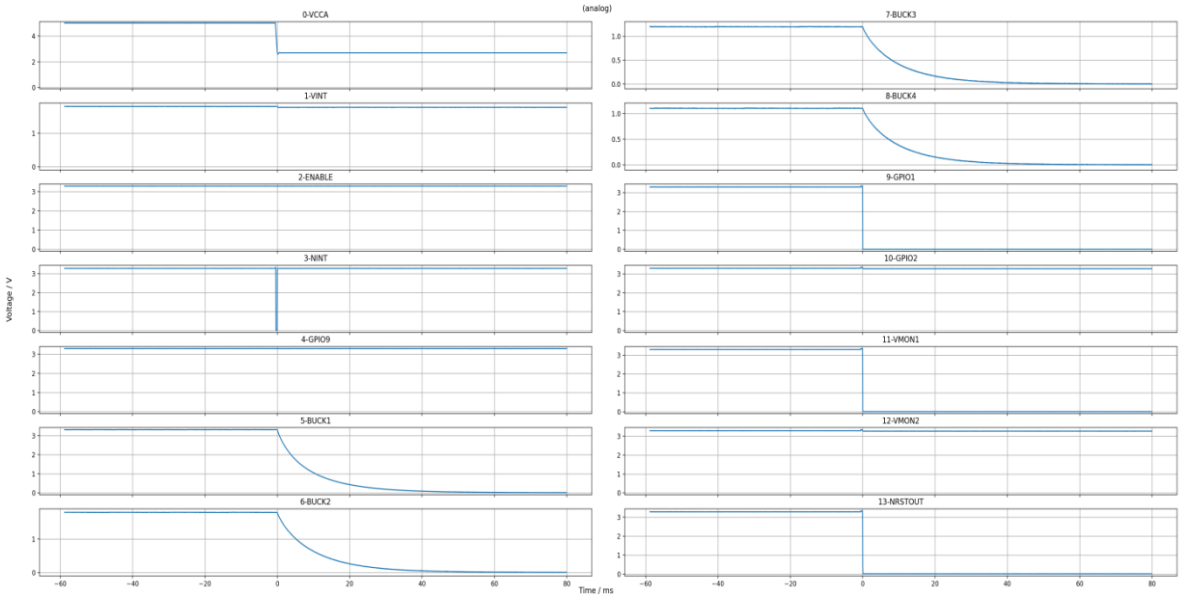

Figure 3-8. ACT2SAFE Sequence Test

4 References

1. Datasheet "TPS6594-Q1 Power Management IC (PMIC) with 5 BUCKs and 4 LDOs for Safety-Relevant Automotive Applications"
2. Datasheet "LP8764-Q1 Four-Phase, 20-A Buck Converter With Integrated Switches"
3. Application Note "Scalable PMIC NVM Update Guide"
4. User's Guide "Scalable PMIC's GUI User's Guide"
5. Errata "LP8764-Q1 Silicon Revision 2.0 Errata"

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