Application Note

DP8382x IEEE 802.3u Compliance and Debug

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ABSTRACT

DP83822, DP83825, and DP83826 (referred throughout this document as DP8382x) devices are a family of 10/100Mbps Industrial Ethernet physical layer (PHY) that is compliant to IEEE 802.3. This application note discusses 100BASE-TX and 10BASE-Te compliance testing and the procedures for operating the DUT for these tests.

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Trademarks

1 Terminology

Table 1-1 provides a list of terminology that is used throughout this application note.

Table 1-1. Terminology

ACRONYM	DEFINITION
DUT	Device Under Test
LP	Link Partner
PHY	Physical Layer Transceiver
SMI	Serial Management Interface
IPG	Inter-Packet Gap
FLP	Fast Link Pulse
NLP	Normal Link Pulse
TX	Transmit – Digital Pins
RX	Receive – Digital Pins
TD	Transmit – Analog Pins
RD	Receive – Analog Pins
AVD	Analog Supply
CT	Magnetic Center Tap
VDDIO	Digital Supply
BIST	Built-In Self-Test
TPM	Twisted Pair Model
AOI	Active Output Interface
AFE	Analog Front-End
MDI	Media Dependent Interface
MDIX	Crossover version of Media Dependent Interface
VoD	Differential Output Voltage

2 Standards and System Requirements

2.1 Standards

The following standards serve as references for the tests described in this document.

- IEEE802.3-2005 Sub Clause 14.3.1
- IEEE802.3-2005 Sub Clause 25.4
- ANSI X3.263-1995

2.2 Test Equipment Suppliers

The following test equipment suppliers are known to offer IEEE 802.3 compliance test equipment.

- Tektronix®
- Spirent®
- Agilent® (Keysight®)
- Rohde & Schwarz®
- Teledyne LeCroy®

2.3 Test Equipment Requirements

The following hardware and software is used in the tests discussed in this application note.

- Oscilloscope with Ethernet physical layer compliance software and test fixture
- Register access to PHY using TI's USB-2-MDIO GUI on the MSP430F5529
- Cables and probes for hardware connection

3 Ethernet Physical Layer Compliance Testing

3.1 Standard Test Setup and Procedures

For Ethernet physical layer compliance testing, the PHY is managed through the serial management interface (SMI – also know as MDIO interface) to configure the required test mode scripts. The testing results are determined and recorded by the Ethernet compliance software of the oscilloscope (for example, the TDSET3 test software from Tektronix). For proper operation of the software, consult the instrument user manual.

The variation between each of the Ethernet physical layer compliance tests is primarily the test mode (see Section 5) of the PHY and the connection to the test fixture Figure 3-1.

The software can typically test for many speed options, but testing for the desired end-application or use-case is important. For 10-Mbps to 100-Mbps testing, one or two channels (depending on MDI or MDIX) needs to be tested.

Accounting for sample sizes and run-to-run variation when conducting testing is important.

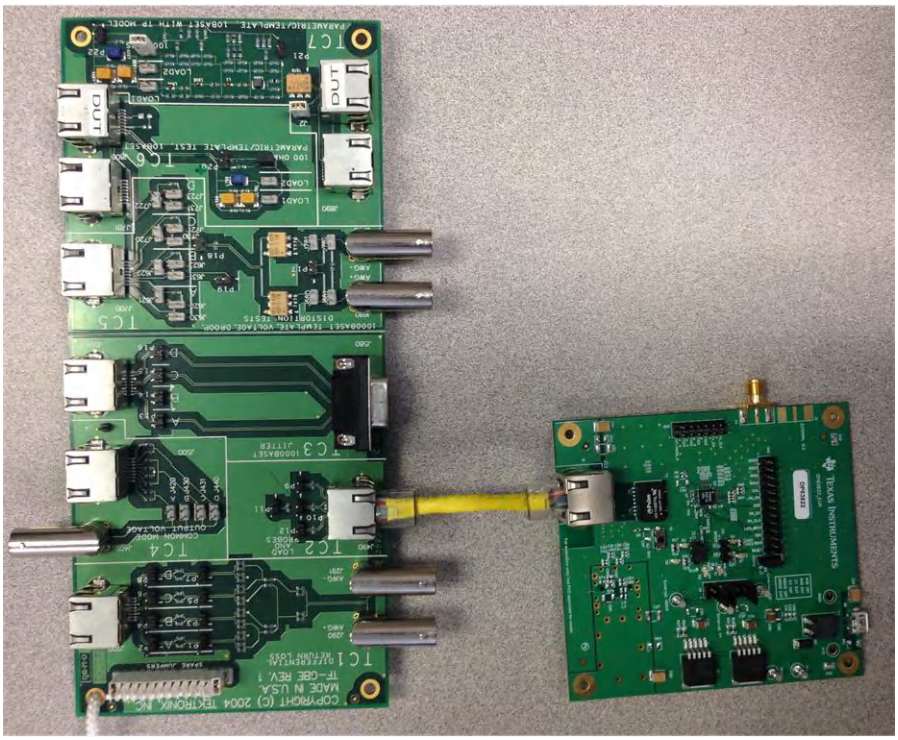

Figure 3-1. DP83822 Connected to a Testing Fixture

3.2 100BASE-TX Compliance Testing

Refer to Section 5 for 100BASE-TX register writes. The following tests are performed with forced MDI, but can also be performed in MDIX mode.

3.2.1 Template (Active Output Interface)

Purpose: To verify that the output fits the transmit template.

Pass Condition: MLT-3 eye fits into the specified ANSI AOI template.

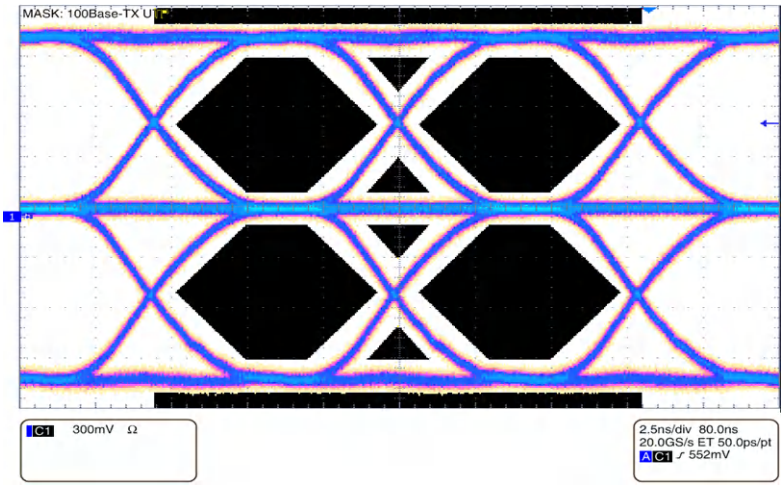

Figure 3-2. 100BASE-TX Template Example Waveform

3.2.2 Differential Output Voltage

Purpose: To verify that the differential output voltage is within the specified bounds.

Pass Condition: The differential output voltage must be within a positive range of 950 mV to 1050 mV and negative range of –950 mV to –1050 mV. The positive and negative peak magnitudes must also be within 2% of each other.

Figure 3-3. 100BASE-TX Differential Output Voltage Example Waveform

3.2.3 Rise and Fall Time

Purpose: To verify that the device rise and fall time are within the specified bounds.

Pass Condition: The rise and fall time (between 10% and 90% of the voltage levels for both positive and negative) must be between 3 ns and 5 ns. The maximum and minimum rise and fall times must be within 0.5 ns.

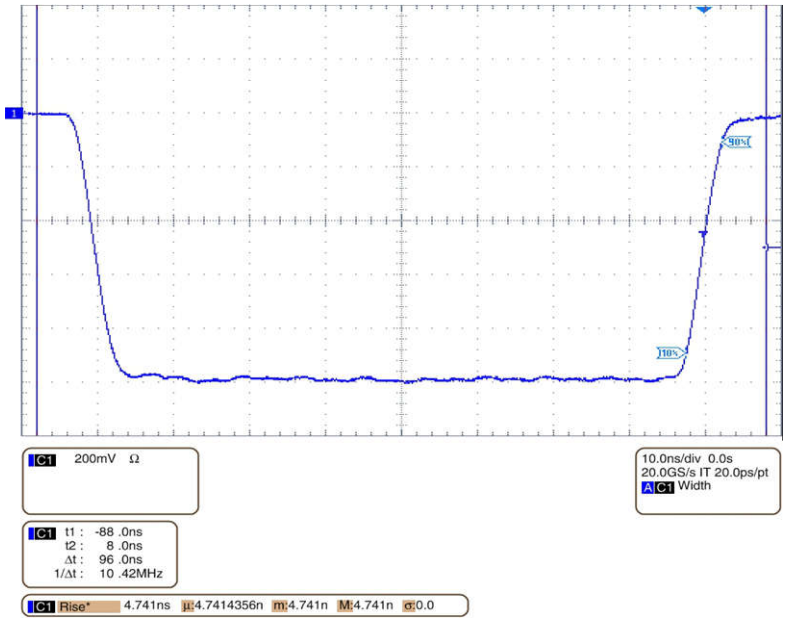

Figure 3-4. 100BASE-TX Rise Time Example Waveform

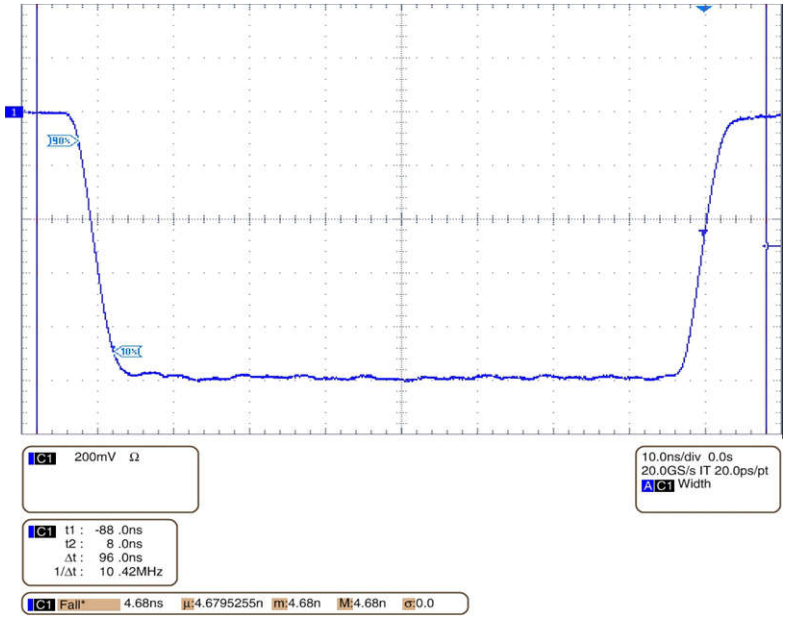

Figure 3-5. 100BASE-TX Fall Time Example Waveform

3.2.4 Waveform Overshoot

Purpose: To verify that the waveform overshoot is below the specified bound.

Pass Condition: The overshoot (both positive and negative maximum voltage level on transition) must not exceed 5% over the steady-state voltage level.

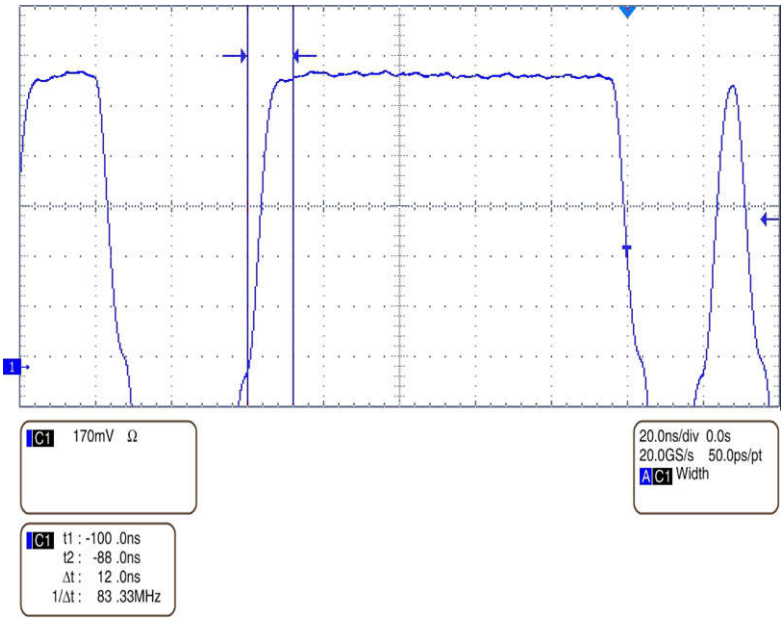

Figure 3-6. 100BASE-TX Waveform Overshoot Example

3.2.5 Jitter

Purpose: To verify that the transmit output jitter is within the specified bounds.

Pass Condition: The transmit output jitter must be less than 1.4 ns.

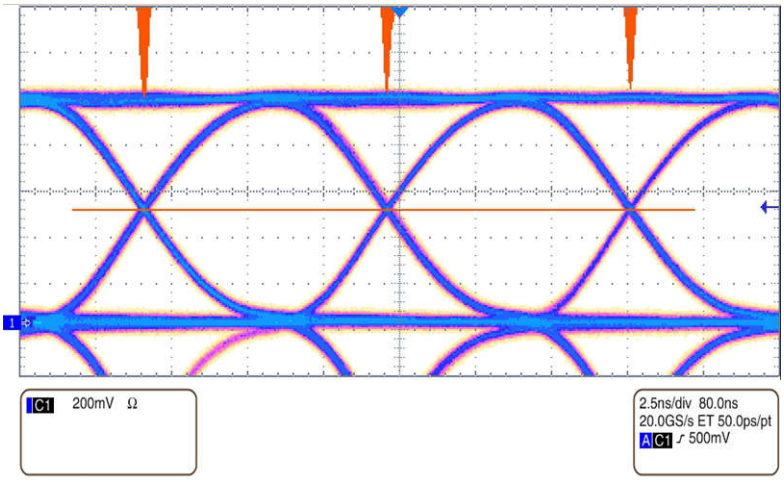

Figure 3-7. 100BASE-TX Jitter Example Waveform

3.2.6 Duty Cycle Distortion

Purpose: To verify that the duty cycle distortion is below the specified bound.

Pass Condition: The duty cycle distortion (defined as above and below 50% of Vout) must not exceed ±0.25 ns.

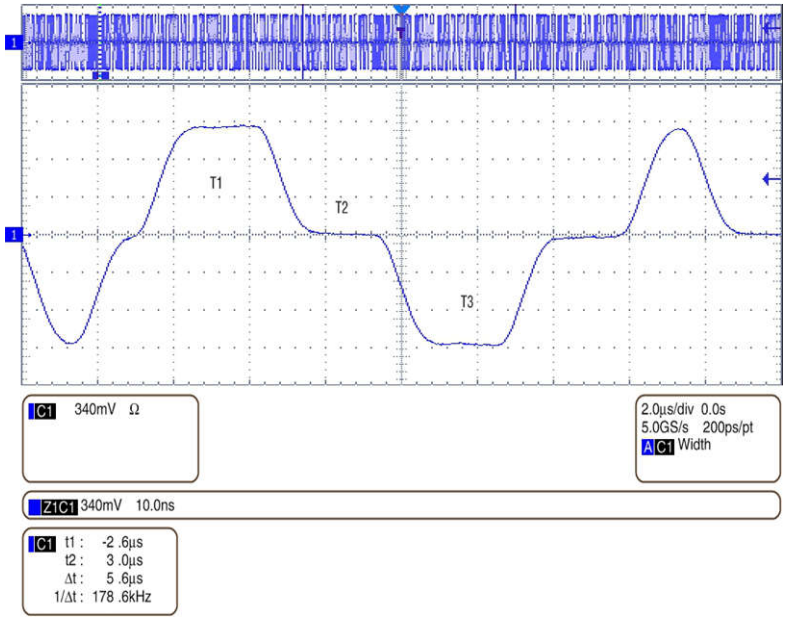

Figure 3-8. 100BASE-TX Duty Cycle Distortion Example Waveform

3.2.7 Return Loss

Purpose: To verify that the return loss is above the specified attenuation.

Pass Condition: The reflection of any incident signal to the PHY must be attenuated under the following conditions:

- ≥16 dB over the frequency range of 2 MHz to 30 MHz.
- ≥10 – 20×$\log_{10}$(f/30) dB over the frequency range of 30 MHz to 60 MHz (f in MHz, where f is the frequency.)
- ≥10 dB over the frequency range of 60 MHz to 80 MHz.

Specific Test Setup: Verify that the test fixture connections are correct.

Note

A spectrum analyzer can be required depending on the Ethernet Compliance Software used in the test.

3.3 10BASE-Te Compliance Testing

Refer to Section 5 for respective 10BASE-Te test mode scripts.

3.3.1 Link Pulse

Purpose: To verify that the link pulse waveform is within the specified bounds.

Pass Condition: The link pulse must fit into the IEEE-defined template in IEEE802.3-2005 Sub Clause 14.3.1.

Specific Test Setup: Verify the test fixture connections. Set registers according to 10BASE-Te Link Pulse in Section 5.

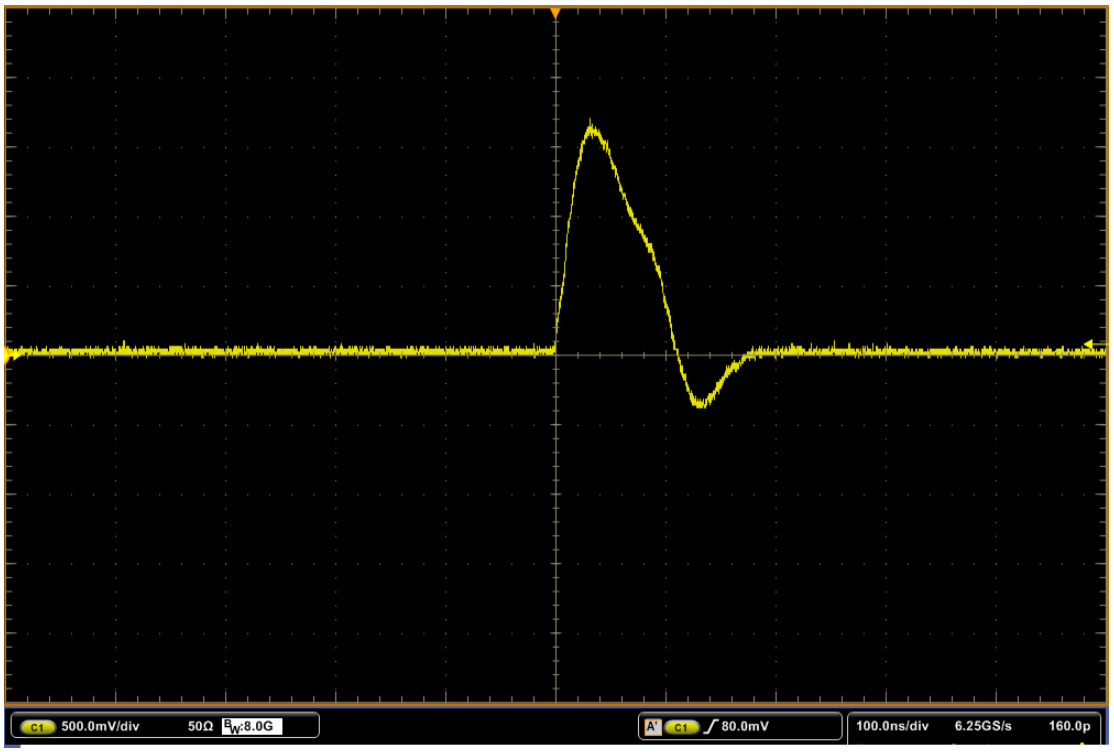

Figure 3-9. 10BASE-Te Link Pulse Example Waveform

3.3.2 10BASE-Te Standard

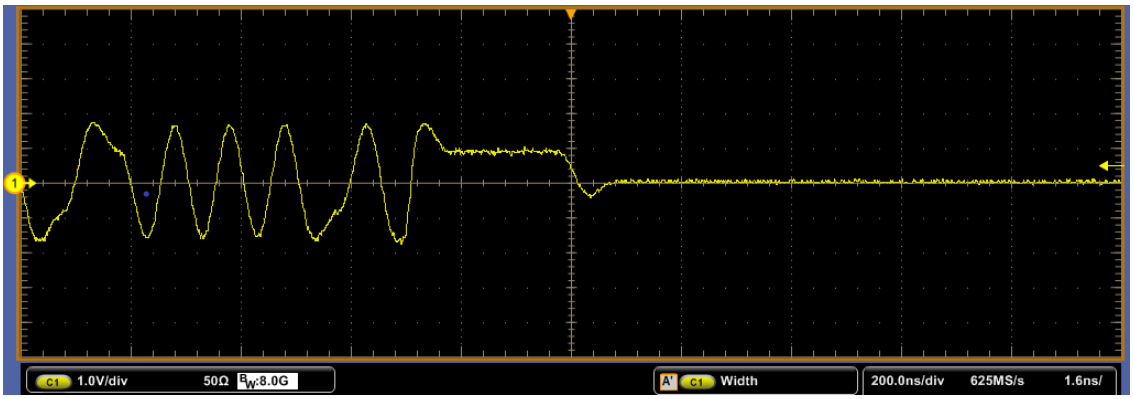

Figure 3-10. 10BASE-Te Standard Output Example Waveform

3.3.2.1 TP_IDL

Purpose: To verify that the transmitter functions properly after transitioning to an idle state.

Pass Condition: The transmitter TP_IDL pulse must fit within the template for Load 1 and Load 2 with and without the TPM. The Load 3 (100-Ω) test is an informative test and is optional.

3.3.2.2 MAU, Internal

Purpose: To verify that the transmitter output equalization is within the bounds specified in IEEE802.3-2005 Sub Clause 14.3.1.

Pass Condition: The transmitter waveform must fit within the IEEE-defined template for all data sequences when terminated with a 100-Ω resistor.

3.3.2.3 Jitter With TPM

Purpose: Purpose: To verify that the jitter is within the specified bounds.

Pass Condition: The transmitter output jitter must be less than ±5.5 ns. Note that failure with TPM does not necessarily mean noncompliance.

3.3.2.4 Jitter Without TPM

Purpose: To verify that the jitter is within the specified bounds.

Pass Condition: The transmitter output jitter must be less than ±8.0 ns.

3.3.2.5 Differential Voltage

Purpose: To verify that the differential voltage is within the specified bounds.

Pass Condition: The peak differential voltage must be between 1.54 V and 1.96 V when terminated with 100-Ω resistor.

3.3.2.6 Common-Mode Voltage

Purpose: To verify the common-mode voltage is within the specified bounds.

Pass Condition: The magnitude of the common-mode voltage must be less than the 50-mV peak.

3.3.2.7 Return Loss

Purpose: To verify that the return loss is above the specified attenuation.

Pass Condition: The reflection of any incident signal to the PHY must be attenuated ≥15 dB over the frequency range of 5 MHz to 10 MHz

Specific Test Setup: Two waveform inputs can be necessary depending on testing setup. Verify the test fixture connections.

3.3.2.8 Harmonic Content

Purpose: To verify that the harmonic content of the PHY is within the specified bounds.

Pass Condition: The Data Out circuit must drive all 1s on the MDI lines. The frequency content is analyzed of the test waveform, and all subsequent harmonics must be 27-dB below the fundamental.

Specific Test Setup: Refer to the 10BASE-Te Harmonic Content script included in Section 5. Be sure the compliance software used is looking for a test waveform of repetitive ones.

4 How to Tune DP83825 VoD Swing

DP83825 has additional control to tune VoD swing. This control can be used to verify that the device is within compliance levels set by IEEE 802.3.The standard defines a ±5% variation of VoD. This parameter is heavily influenced by magnetics, connector, test fixture, layout, and all of the aforementioned listed tolerances.

Note

For best practices, layout guidelines in *Ethernet PHY PCB Design Layout Checklist* application note must be followed, and transformer specification requirements located in the *DP83825I Low Power 10/100 Mbps Ethernet Physical Layer Transceiver* data sheet must also be met, before register tuning.

To tune the PHY for the appropriate signal level, measuring the signal level is advised to understand how much (if applicable) the signal needs to be adjusted. Once measured, the following table can be used to determine the register configurations needed. Please note that this process needs to be redone for each individual unit. In addition, the following registers are classified as extended registers and must be written to as outlined in the *DP83825I Low Power 10/100 Mbps Ethernet Physical Layer Transceiver* data sheet.

Table 4-1. VoD Tuning Register Configurations

VoD Change	0x30B	0x30C	0x30E
-12.5%	0xC80	0xE	Offset_0
-11.25%			Offset_1
-10%			Offset_2
-8.75%	0xC40	0xF	Offset_-2
-8%			Offset_-1
-6.25%			Offset_0
-5%			Offset_1
-3.75%			Offset_2
-2.5%	0xC00	0x10	Offset_-2
-1.25%			Offset_-1
0% (Default)			Offset_0
+1.25%			Offset_1
+2.5%			Offset_2
+3.75%	0xBC0	0x11	Offset_-2
+5%			Offset_-1
+6.25%			Offset_0
+7.5%			Offset_1
+8.75%			Offset_2
+10%	0xB80	0x12	Offset_-2
+11.25%			Offset_-1
+12.5%			Offset_0

To calculate Offset_X:

1. Read Reg 0x333. Note this value varies between units
2. A = 0x333[15:11] converted to decimal
3. B = 0x333[10:6] converted to decimal
4. C = 8 - A + B. This variable is bounded between 0 and 15. If C is calculated to be outside the bounds, the variable C must be rounded back to the nearest bound. If C is calculated to be -2, set C to equal 0
5. D(x) = C + x, where x is determined using Reg 0x30E column in Table 4-1
6. Offset_x = $[2D(x) + 1] \times 2048$; converted to hexadecimal

A starting point is change RBIAS to 6.34 kΩ and setting VoD to -8% to further improve margins.

4.1 Example of Tuning DP83825 VoD Swing

This section provides an example of how to tune VoD Swing in the DP83825. Figure 4-1 shows the DP83825 before VoD Swing tuning. In this example, a device with a nominal RBIAS is measuring a positive and negative VoD at 100Mbps of 1.068 V and -1.116 V, respectively. As the bounds for this speed is having [0.95 V, 1.05 V] and [-1.05 V, -0.95 V], a -8% tune is desired. This tuning brings the VoD to a theoretical 0.98 V and -1.0272 V.

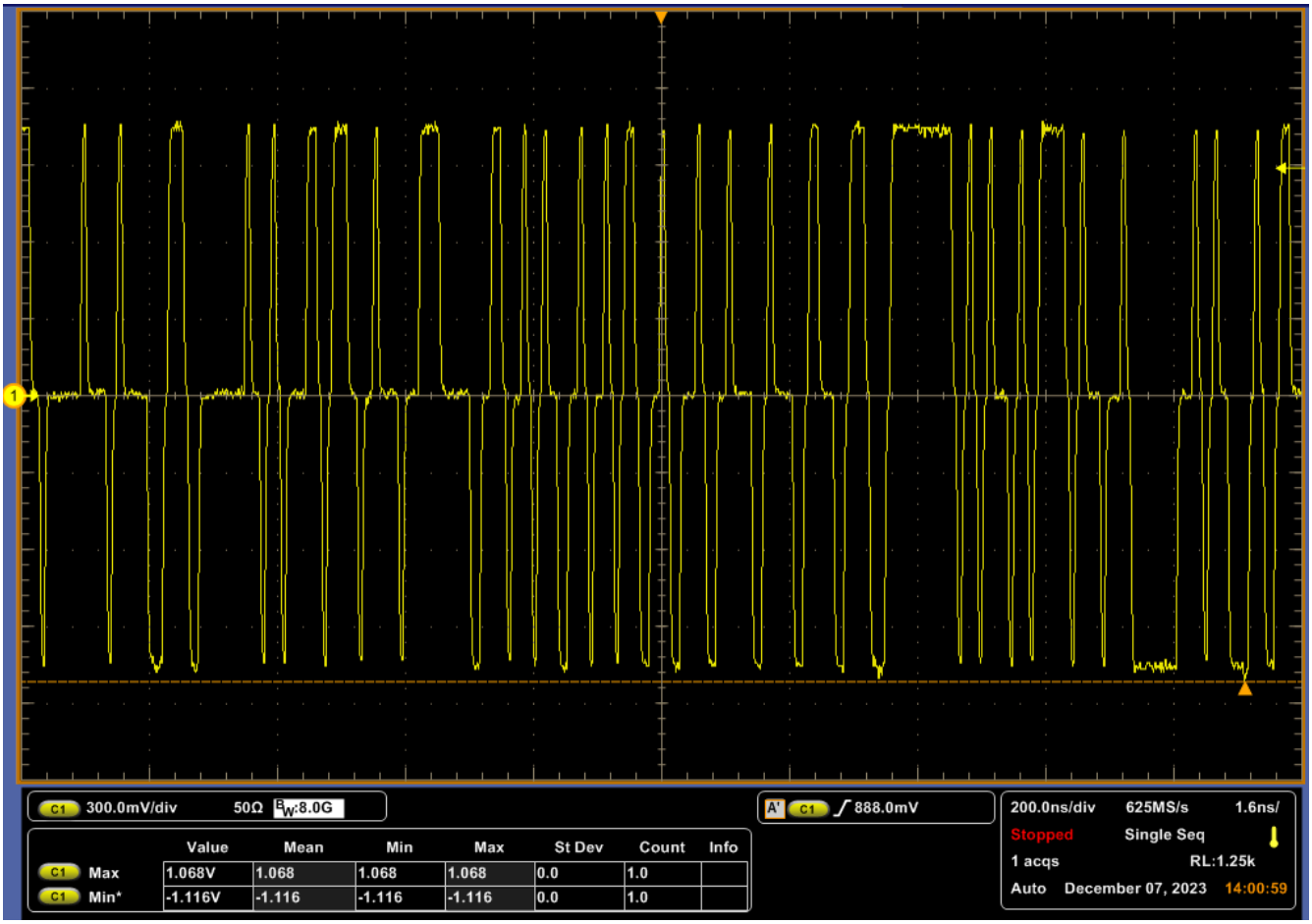

Figure 4-1. Untuned DP83825 100Mbps VoD

To tune the device for -8% swing use the following procedure.

1. Set register 0x30B = 0xC40
2. Set register 0x30C = 0xF
3. Set register 0x30E = Offset_-1.
   a. Read Reg 0x333 = 0x520B. This means that:
      i. A = 10
      ii. B = 8
   b. C = 6
   c. D = 5
   d. Offset_-1 = $2048 \times (2 \times 5 + 1)$ = 22528 = 0x5800

After programming each register, the measured VoD on the scope is 0.996 V and -1.008 V. Figure 4-2 shows the output after tuning -8%.

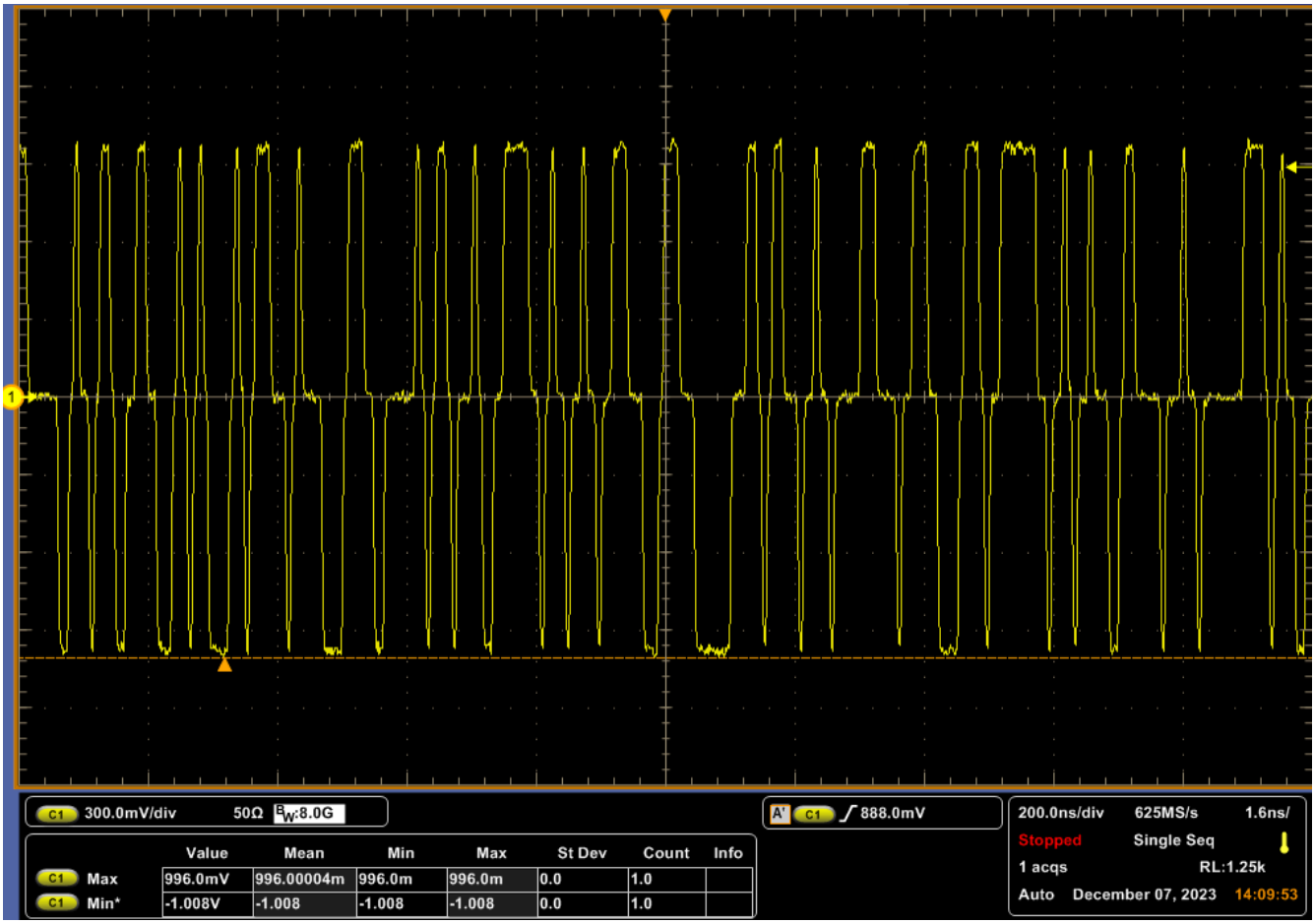

Figure 4-2. Tuned DP83825 100Mbps VoD

5 IEEE802.3u Compliance Testing Scripts for the DP8382x

The 100BASE-Tx Standard script is shown in the following code block.

Table 5-1. 100BASE-Tx Standard

Reg 0x1F = 0x8000	//Reset PHY
Reg 0x0 = 0x2100	//Program DUT to force speed 100BASE-TX mode
Reg 0x19 = 0x21	//Program DUT to Forced MDI mode. Set to 4021 for MDIX mode
Reg 0x1F = 0x4000	//Restart PHY

Table 5-2. 10BASE-Te Link Pulse

Reg 0x1F = 0x8000	//Reset PHY
Reg 0x0 = 0x100	//Program DUT to force speed 10BASE-Te mode
Reg 0x19 = 0x21	//Program DUT to Forced MDI mode. Set to 4021 for MDIX mode
Reg 0x1F =0x4000	//Restart PHY

Table 5-3. 10BASE-Te Standard (DP83822)

Reg 0x1F = 0x8000	//Reset PHY
Reg 0x0 = 0x100	//Program DUT to force speed 10BASE-Te mode
Reg 0x19 = 0x21	//Program DUT to Forced MDI mode. Set to 4021 for MDIX mode
Reg 0x16 = 0x7108	//Programs DUT to generate data and enables analog loopback mode for termination purposes
Reg 0x1F = 0x4000	//Restart PHY

Table 5-4. 10BASE-Te Standard (DP83825/6)

Reg 0x1F = 0x8000	//Reset PHY
Reg 0x0 = 0x100	//Program DUT to force speed 10BASE-Te mode
Reg 0x19 = 0x21	//Program DUT to Forced MDI mode. Set to 4021 for MDIX mode
Reg 0x16 = 0x7101	//Programs DUT to generate data and enables PCS loopback mode
Reg 0x1F = 0x4000	//Restart PHY

Table 5-5. 10BASE-Te Harmonic Content

Reg 0x1F = 0x8000	//Reset PHY
Reg 0x0 = 0x100	//Program DUT to force speed 10BASE-Te mode
Reg 0x27 = 0x0013	//Test mode enable with repetitive 1's

6 References

Refer to the following Texas Instruments literature for more information related to the DP3832x.

- Texas Instruments, *DP83822 Robust, Low Power 10/100 Mbps Ethernet Physical Layer Transceiver*, data sheet.
- Texas Instruments, *DP83825I Low Power 10/100 Mbps Ethernet Physical Layer Transceiver*, data sheet.
- Texas Instruments, *DP83826 Deterministic, Low-Latency, Low-Power, 10/100 Mbps, Industrial Ethernet PHY*, data sheet.
- Texas Instruments, *DP83822 Troubleshooting Guide*, application note.
- Texas Instruments, *DP83826 Troubleshooting Guide*, application note.

For more information related to the standards discussed in this application note, see also the following documents.

- IEEE Computer Society, *IEEE 802.3-2018 - IEEE Standard for Internet*, standard.
- ANSI X3.263-1995.

See also, the following document for information related to the tests conducted in this document.

- Tektronix®, *TDSET3 Ethernet Test Compliance Software*, user manual.

7 Revision History

Changes from Revision A (December 2023) to Revision B (April 2025)	Page
• Added harmonic content	9
• Added harmonic content script	13

Changes from Revision * (August 2016) to Revision A (December 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated throughout to add support for entire DP8382x family	1
• Updated *Ethernet Physical Layer Compliance Testing* section to provide clarity on expected test waveforms and theory behind tests	3
• Added *How to Tune DP83825 VoD Swing* section for tuning DP83825 VoD Swing with an example	10
• Updated the register configurations in the *IEEE802.3u Compliance Testing Scripts for the DP8382x* section	13
• Added references to DP8382x data sheets	14

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